

# The credit-card sized, general purpose controls platform: HadCon2

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## Introduction

The HadCon2 (<http://wiki.gsi.de/EE/HadCon2>) is a low-cost, credit-card sized, general purpose I/O module for detector and experiment controls as well as for small data acquisition systems.

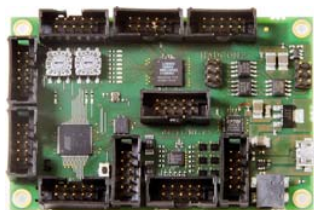


Figure 1: HadCon2

It is the successor of the discontinued first version HadCon a.k.a. HadShoPoMo.

The module has an ATMEL AT90CAN128 microcontroller providing a multitude of connectivity:

- I<sup>2</sup>C (8-fold multiplexer, 4 internally used)
- 6 channel 1-wire master, slew-controlled 1-Wire Edges
- 8 channel 8bit DAC, galvanically isolated CAN-high speed transceiver
- 8 channel 10 bit SAR ADC, single ended, or up to 4 differential
- byte oriented SPI interface
- in total up to 53 programmable I/O lines

and

- a Lattice MachX02 FPGA for fast data processing tasks.

In contrast to its precursor HadCon, in favor of a more open access and long term maintenance, it doesn't have any CPU on board, but a USB connector to directly allow communication with any type and size of computer (e.g. standard PC, Raspberry Pi, DreamPlug, ...) having an USB port on one side and at the other end the microcontroller and the FPGA.

The communication is based on an ASCII based protocol API in view of easy implementation in detector control systems like e.g. EPICS[4] and LabVIEW[5] and easy control via the command line and scripts with human readable

commands to communicate with all the interfaces available.

## Use Cases

Originally developed for a power monitor board (HadShoPoMo) for HADES[1] the HadCon family serves/will serve many different applications and collaborations:

- **HADES MDC/RPC detector controls** - EPICS controlled 1-wire devices: temperature sensors, switches, ADCs.
- **HADES RPC detector** - EPICS controlled CAN-based gas system
- **HADES RICH detector** - EPICS monitored (10Hz) current via internal ADC, in progress
- **PANDA APFEL ASIC[2]** - EPICS controlled, bit-banged interface to the SPI-like APFEL ASIC, in progress
- **NeuLand, R3B[3]** - Windows LabVIEW or EPICS controlled I<sup>2</sup>C interface for TRIPLEX[6] front end control, in progress
- **FPGA projects**
  - **Waveform Generator** - FPGA based Waveform Generator, controlled by the HadCon2's API
  - **FPGA based 1-wire ADC** - 6 channel, max. 12bit ADC to be accessed by 1-Wire protocol, in progress.

## References

- [1] HadShoPoMo, <http://tinyurl.com/kvcbw5t>
- [2] P. Wiczorek and H. Flemming, "Low Noise Preamplifier ASIC for the PANDA EMC", IEEE Nuclear Science Symposium 2010, Knoxville, USA, NSS-N47-74, Published in NSS/MIC, 2010 IEEE DOI: 10.1109/NSSMIC.2010.5873982 Page 1319 - 1322
- [3] R3B collaboration, <http://www.gsi.de/r3b>
- [4] Experimental Physics and Industrial Control System, <http://www.aps.anl.gov/epics>
- [5] LabVIEW, National Instruments, <http://www.ni.com/labview/>
- [6] "TRIPLEX, an Upgrade for the TACQUILA System", K. Koch et al, GSI Sci. Rep. 2010, PHN-IS-EE-07, p. 235.