White Rabbit Applications for FAIR Experiments

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Introduction

A White Rabbit (WR) based timing system will be used at FAIR as a field bus for accelerator controls. In addition WR Timing Receivers (WRTR) are required by FAIR experiments for the synchronizaton of independent detector sub-systems. For this purpose hardware latching of time stamps on WRTR has been implemented. A test bed has been set up to check this functionality. Furthermore it has been investigated if a WR synchronized 200 MHz clock can be used as reference for high precision time-of-flight measurements (TOF) with electronics resolution in the order of 10 ps RMS between independently operated and possibly far distant detector systems.

White Rabbit Timing Receivers (WRTR)

The development of the WRTR is a joint effort of the CSEE and CSCO departments of GSI. CSEE designed and produced the WRTR, CSCO developed and implemented the WR timing protocols on the FPGAs of the WRTR, including Linux kernel modules and libraries for user applications. Finally the adoption of the WRTR for the MBS data acquisition system and an additional VME driver development was made by CSEE.

Three types of WRTR boards have been investigated: The PCI Express based PEXARIA5, The VME board VETAR2 and the standalone module EXPLODER2. All boards can be accessed through Etherbone via USB and the WR network. In addition the PEXARIA5 can be accessed for high speed DAQ applications via PCI Express - and the VETAR2 via the VME protocol. It is important to note, that all WRTR types provide identical functionality.

All WRTR are connected to the WR network and their time base is syntonized and synchronized using the White Rabbit Precision Time Protocol (WR-PTP) implemented in the WRTR.

Global - versus Local Triggers

Basically two types of detector systems at FAIR have to be synchronized with the WRTR. The first and traditional type is readout at the occurrance of a single (global) trigger signal, producing a so called (sub)event. In the second type, often stated as triggerless, each channel is readout if a certain individually threshold is exceeded. Thus, these kind of systems produce a stream of data, whereas the entity of an event is a priori not present any more.

Synchronization of globally triggered, but independent sub-systems can be facilitated by latching time stamps in all sub-systems at the occurrance of the global triggers. By requiring time stamp differences to be inside an adjustable interval, data from different sub-systems can be connected in the data analysis. Synchronizing triggerless and/or globally triggered sub-systems works according the the same principle, but time stamp comparisons must be made for each individual channel or possibly groups of channels.

All these requirements can be provided with the WRTR. Synchronization of triggerless systems with WRTR is prepared and needs to be tested. It is not covered in this report.

Synchronizing Globally Triggered Systems

For this purpose a specified input channel on each WRTR is connected to a FIFO in its FPGA, where time stamps are stored and can be read out. Dead time protected and accepted global trigger signals are used to latch time stamps. The time stamps itself are 64 bit counters, currently with a granularity of 8 ns, referring to the 125 MHZ WR clock

A test system consisting of 4 independent MBS subsystems and all types of WRTR described above has been set up. Comparing time stamps differences of all 4 subsystems, a precicon of 5-8 ns (RMS) could be achieved in long term measurements over weeks.

High Precision TOF with WRTR

The WR-PTP protocol allows the adjustment of the 125 MHz WR clock of the WRTR in the sub nano second regime. Therefore it has been anticipated as reference clock for TOF measurements in the ps range. Since the VME TDC VFTX developed at CSEE requires a 200 MHz clock, a 200 MHz clock was derived from the native 125 MHZ in the FPGA of all types of WRTR and fed out. Another MBS test systems with up to 4 WRTR connected in various topologies to the WR network has been set up. The 200 MHz clock was fed into individual VFTX modules. A common reference signal was fed to all VFTX and their measured time differences estimated with a rate of 25 KHz. An intrinsic precision of 15-20 ps RMS between pairs of WRTR clocks have been observed. Long term tests revealed drifts in a band of 40-50 ps RMS for the differences of the reference signals. These results do not meet the requirements yet, but amongst others, possible improvements for the clock generation hardware have been identified.

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