# Paving the Way for the FAIR General Machine Timing System

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## *Abstract*

The task of the General Machine Timing system (GMT) is the hard real-time control of the GSI and FAIR accelerator complex with sub-ns precision. This is achieved by a distributed event generation system based on the notion of time in the facility. The prime features are time-synchronization of 2000 nodes using White Rabbit Precision-Time-Protocol (WR-PTP), distribution of International Atomic Time (TAI) time stamps, generation of trigger events for synchronization of equipment and providing infrastructure for common services of the accelerator control system. During the past two years, the foundations of the GMT have been specified, designed and implemented.

## Introduction

The GMT is based on a common notion of time of all connected nodes, provided by WR-PTP [1]. A dedicated network based on Ethernet and dedicated WR switches distributes the commands broadcasted by a data master to all Timing Receivers (TR). Relevant commands are decoded and enqueued for timely execution. On time, none, one or more specific actions depending on the local configuration of the TR are executed. A central clock master serves as grand-master clock to which all nodes in the WR network synchronize their clock, phase and time. As the GMT is a time based system, the precision for synchronizing actions depends only on the quality of clock and phase synchronization via WR-PTP and not on the propagation time of commands distributed by the data master.

## Hardware

More than 2000 TRs will be connected to the timing network. About 1200 Scalable Control Units (SCU) with integrated TR functionality will be the prime Front-End Computers (FEC) for equipment control and have been developed by the hardware group CSCOHW of the control system department [2]. About 500-1000 dedicated TRs of different form factors are required by beam instrumentation and Data AcQuisition (DAQ). So far, TRs in the three form factors PCIe, VME and stand-alone have been developed in a cooperation between the departments of Controls and Experiment-Electronics. As all TRs are derived from the embedded TR in the SCU, they are based on Field Programmable Gate Arrays (FPGA) from the Altera Arria® families and share many identical electronic components. The fundamental design principle is to maximize re-usability and similarity only adapting the host-bus bridge and I/O for each form factor.

## Gateware

Code for FPGAs is called gateware. Although GSI's and CERN's TRs are based on FPGAs from different manufacturers, the gateware is manufacturer independent to a large extent. The concept is to separate functionality into different Intellectual Property (IP) cores which all have an interface to the System-on-Chip (SoC) Wishbone bus. All IP cores represent Wishbone devices that are interconnected via Wishbone crossbars. The crossbars do not only provide clock domain crossings but also allow to connect form factor specific Wishbone devices to a standard architecture common to all TRs. Each form factor needs to implement its own host-bus to Wishbone bus master bridge. The connection to the WR network providing a network interface and a WR link is always encapsulated in IP cores behind a dedicated Wishbone crossbar. All Wishbone devices provide Self-Describing Bus (SDB) records, that allow querying bus-addresses, vendor and product information. Every gateware includes at least one Lattice Micro 32 CPU (LM32) softcore [3] that allows to implement application specific firmware. Gateware and firmware is developed in collaboration with CERN in the framework of the Open Hardware Repository [5].

## Driver

The main idea is to extend to SoC Wishbone bus outside the FPGA using the EtherBone protocol [4]. As EtherBone can run over any serial protocol, it only requires a form factor specific driver in the kernel implementing an interface to the Wishbone bus master interface on the TR's FPGA. This allows EtherBone to connect to the Wishbone devices of the TR over any host-bus to Wishbone bus master bridge and even network protocols such as UDP and TCP/IP.

## Status

### *White Rabbit Network*

15 production quality WR switches [6] have been obtained in 2013. All of them are in operation and work reliably with respect to their hardware. However, gateware and software are still missing some features. A clock master switch is already installed in the final position in the existing building BG at GSI. From here, already five locations

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at the existing facility are connected via optical fiber links. A part of the links will serve to connect equipment of the existing facility to the new timing system. Another part is used for testing equipment or to gain experience with long term operation of switches and equipment. Via appropriate patches, some dedicated links of up to five kilometer length have been set-up. Moreover, several kilometers of fiber have been exposed to environmental conditions on a building roof. Results of long term tests on WR clock and phase synchronization including multiple layers of switches are very promising and presented elsewhere [8].

### *Data Master*

The data master schedules actions by broadcasting commands to the TRs via the WR network [9]. A first data master has been set-up based on a SCU and includes dedicated firmware in a LM32 softcore. The firmware generates the commands that are broadcasted to the nodes. It can be configured and controlled via a dedicated API which is used by a Front End System Architecture (FESA) class. Since May 2013 the data master is in operation successfully with very little downtime. This data master serves as a proof of principle and will be replaced by a parallel multicore version in 2014.

### *Timing Receivers*

The focus of the past two years has been the development of the TRs in a joint effort of different groups. With respect to hardware, work has been carried out by CSCOHW (SCU) [2] and CSCOEE (VME, PCIe, standalone). CSCOTG has concentrated on gateware and software. The driver concept allows to access the TR from Linux user space via the EtherBone protocol in a transparent way independent of the host bus bridge - the same front-end software for equipment control can be used on different FECs independently of the form factor of the TR. As a proof-of-principle, functionality dedicated to the timing system has been integrated with FESA. This allows a FESA class subscribing to a so-called event-source within FESA and receiving a notification upon an event.

For the GMT, a main component of the gateware is the Event-Condition-Action (ECA) unit. It is a complex filter, comparing the *event* of a command received from the data master against *conditions* pre-configured by the TR's user. In case of a match, a pre-configured *action* will be scheduled for timely execution in a so-called action channel. On-time, the action channel triggers a receiving component. Here, the action such as IRQ generation, digital output or equipment action such as ramping a magnet is executed. The precision for triggering is 8 ns due to the 125 MHz system clock. If supported by the receiving component, an additional fine-delay feature allows more precise timing. All supported form factors allow fine-delay of 1 ns already in the FPGA. As a perspective, further refinement by PLL-phase-shifting (125 ps) or delay chains in transceivers of differential output pins (25 ps) might be possible inside the FPGA without the need of external fine-delay electronics.

Next to timely execution of actions, the ability for precise time stamping of triggers received by a TR is another key requirement to the GMT. As all TRs share a common notion of time, a timestamp latch unit is common to the gateware of all TRs. This feature has already been integrated by the Multi Branch DAQ System [7] and successfully tested with the form factors PCIe, VME and standalone over many weeks [8].

## Conclusion and Outlook

Significant progress has been made on the hardware, gateware and software of the TRs. A timing network spanning the existing facility has been set up with about 15 WR switches. A first timing system has been set up in May 2013. Key components like the ECA unit, the Wishbone SoC architecture, the driver concept and the communication library EtherBone have been developed and implemented.

The next step is to set up the GMT for the recommissioning of CRYRING at GSI. Here, about 50 TRs are required for synchronization of equipment of the control system and beam instrumentation. At the beginning the GMT will only provide basic features. CRYRING serves as a test ground for the control system as a whole. This is important for validating the concepts, gaining experience of operation under on-line conditions and assures the quality of the components developed.

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