SCU system goes productive

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INTRODUCTION

The SCU (Scalable Control Unit), the future standard controller and timing receiver of the FAIR control system, is composed of a base board, equipped with a COM express CPU extension and a bus system for a variety of slave boards. A powerful FPGA (Field Programmable Gate Array) on the SCU base board and the module concept makes the platform highly flexible and scalable. A broad range of digital and analog IO functions will be provided by a set of slave boards. The SCU also implements the timing receiver for the GMT (General Machine Timing) in FAIR. The SCU is now used for the first time at CRYRING.

SCALABLE CONTROL UNIT (SCU)

The SCU (Figure 1) is mechanically a stack of up to three separated boards. There is the carrier board with an Arria II FPGA, two Small Form-factor Pluggable (SFP) slots, DDR3 RAM, parallel flash and a parallel bus (SCU bus) for controlling up to 12 slave devices. In addition the carrier board is equipped with White Rabbit [1] circuitry to realize the functionality required of the timing receiver for the GMT. A COM Express™ module with an Intel Atom CPU is mounted to the carrier board. It has Ethernet, USB and PCIe interfaces.

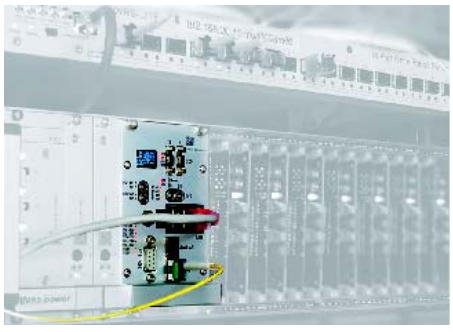

Figure 1: SCU with MIL-STD-1553 Extension

An optional extension board can be connected to the carrier board for dedicated hardware solutions especially for fast digital IO or for backwards compatibility that runs for example a MIL-STD-1553 based field bus interface. The SCU works as a front-end controller. On one side it is connected to the control system via Ethernet, on the other side it controls slave devices over the SCU bus.

THE SCU AS TIMING RECEIVER FOR THE GMT

As timing receiver it receives sub ns accurate timing information over a White Rabbit link, connected to an WR Switch. The White Rabbit receiver in the FPGA runs the Precision Time Protocol (PTP) in software on a LatticeMico32 (LM32) soft-core CPU. It is able, to do time stamping and generate pulses with a precision of 8 ns. With extra io hardware, a precision in the low ps range is possible.

SCU BUS SLAVES

The SCU communicates with devices via slave cards on SCU bus. On CRYRING different devices with variety of interfaces have to be served. For this reason a modular concept for slave cards were developed (Figure 2). This concept enables the provision of a wide range of cost-effective analog and digital interfaces. The required functionality is provided by a common base module with a powerful FPGA. The different physical interfaces are connected via interface modules. All interface modules use the same base module. A unique hardware identifier allows the auto-configuration of the firmware.

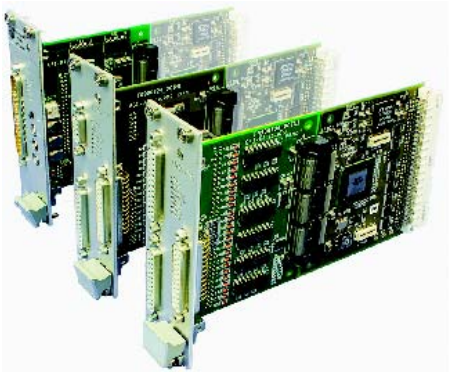

Figure 2: Modular concept for slave cards

References

[1] Moreira, P.; Serrano, J.; Wlostowski, T.; Loschmidt, P.; Gaderer, G.; , “White rabbit: Sub-nanosecond timing distribution over ethernet” Precision Clock Synchronization for Measurement, Control and Communication, 2009. ISPCS 2009. International Symposium on , vol., no., pp.1-5, 12-16 Oct. 2009