

## FPGA Hit Finder and Energy Filter for the FEBEX Pipelining ADC

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The FEBEX board was developed in CSEE Department of GSI. It features 16 differential analog inputs, 16 differential LVDS I/Os (max. 8 outputs) and a serial multi-gigabit connections to the backplane over a PCI Express [1]. The 16 differential analog signals go through 12-bit or 14-bit multi-channel pipeline ADCs with 50 MHz sampling rate.

The FEBEX boards are designed to work with globally triggered DAQ systems by accepting user defined trigger windows. The complete control and readout logic is implemented in a Lattice FPGA. Due to the FPGA's large memory size the trigger window can be set to a maximum of 8000 ADC's samples (20 ns per sample). The trigger window is divided to pre- (up to 2000 ADC's samples) and post- trigger windows, both of them are programmable. The length of the FEBEX data packed depends on the number of hits found and user defined settings. After the trigger's processing the data is moved out in block transfer mode with a rate of up to 2 Gbits per second over copper connections (back plane) and then via optical links to the PEXOR in the DAQ computer.

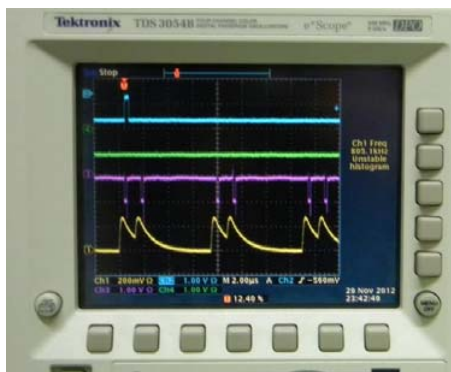


Figure 1: Self-triggering with double pulse detection.

For each channel in the core of the FPGA two methods for “self-triggering” are implemented: 3-steps comparator and Fast Trapezoidal Filter (FTF) for a leading edge selection and double pulse detection. The parameters of the FTF (both average windows and gap between them) are programmable (8 bit with maximal length of 255 ADC's samples). For both methods 12-bit thresholds are implemented for each channel individually. The generated “self-trigger” is sent out to the module for trigger selection and dead-time protection (EXPLODER [1]). This signal can be used as trigger system input.

The implemented FTF gives the system possibility to work in very “noisy” environment and to detect hits with

very low amplitude.

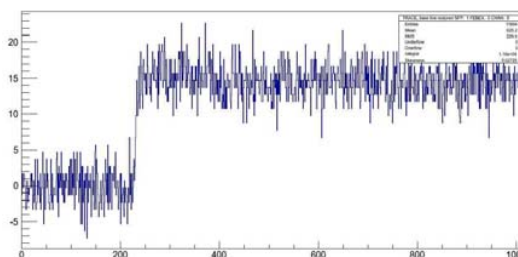


Figure 2: FEBEX signal trace with amplitude of 2 mV.

A new feature of the FEBEX board is the possibility to measure the energy of the differential input pulses. The FPGA's core includes a programmable Energy Trapezoidal Filter (ETF) for each channel (10 bit for each parameters of the ETF). The maximal length of the filter is 1023 ADC's samples.

Each FEBEX board can send out data packets in various formats: only ADCs traces with or without ETF data; summary data packets (measured energy and hit times) and ADCs traces with or without ETF data; only summary data packet and ADCs traces with or without ETF data, in case more than one hit was found in a single channel.

The FEBEX board can be programmed to operate with negative or positive input signals. Its core includes also slow control functionality over the optical link. The implemented SPI interface to the FPGA's flash memory gives the possibility to check and reload the FPGA programming file.

The interface, implemented in the FEBEX board, is designed to work with Multi Branch System (MBS) data acquisition system [2]. Through the MBS system, via the optical interface, the user has full control over all components of FEBEX: configuration, testing, start/stop of data acquisition, data readout and data logging. The MBS runs under the operating system Linux and LynxOS and supports various hardware setups. Therefore, for each user defined hardware setup, the MBS data acquisition software requires user input data, describing the hardware setup and configuration parameters.

### References

- [1] [www.gsi.de/fileadmin/EE/Module](http://www.gsi.de/fileadmin/EE/Module)
- [2] BS N.Kurz, The general purpose data acquisition system MBS, IEEE Trans. Nucl. Sci., vol. 47, no. 2, p. 336, Apr. 2000.