TRLO II — friendly FPGA trigger control *

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An easy-to-use command-line tool has been developed to simplify configuration of the TRLO II trigger logics. The system has also been enhanced with a serial trigger distribution protocol, to allow for greater flexibility in connecting multi-branch systems. The flexible FPGA trigger control TRLO II [1] for VULOM and TRIDI modules [2] has been used in over a dozen experiments with a number of different experimental setups. The system incorporates the functionality of most logic NIM modules. It also has features for advanced monitoring, e.g. recording of trigger alignment as well as plenty of general and specialised scalers and timer latches.

`trloctrl` — friendly setup utility

With around 60 types of 500+ setup registers, and 200 source and sink signals of comparably many variations, using the TRLO II could easily become a non-trivial task. The firmware now comes with a companion command-line interface for control, monitoring and read-out. This removes the need to set registers by compiled code. Complex configurations can be loaded from setup files, while one-off commands for testing can be issued quickly from a shell:

```
trloctrl "period(1)=2us" "ECL_OUT(3)=PULSER(1)"
trloctrl --print-config
```

Most functionality is provided via a library so that it can be used by other programs, e.g. in DAQ readout functions.

Serial time distribution revisited

A unidirectional serial time distribution protocol has already provided time-stamps for event synchronisation in a TITRIS-compatible manner [3] for a few experiments. The protocol has been redesigned to allow the transmitter and receivers to run at different nominal clock frequencies.

The precision is about 2 receiver clock cycles (20 ns in a VOLUM), and is thus suitable for event-synchronisation. The advantage compared to more precise solutions is the small resource usage and no need for special control of the FPGA clock. The sender and receiver require about 100 and 600 LUTs of general logic in a Virtex-4, respectively.

TRIMI — trigger distribution

To enable modules running the TRLO II to act as TRIVA replacements when operated with the MBS, a register-compatible mimic has been developed. This (TRIMI) component includes a serial protocol for trigger distribution and synchronisation between multi-crate systems. With the TRIMI essentially having its own register space, connections are controlled by a separate program: `trimictrl`. The peer-to-peer-like serial protocol makes it easy to configure inter-system connections via remote control.

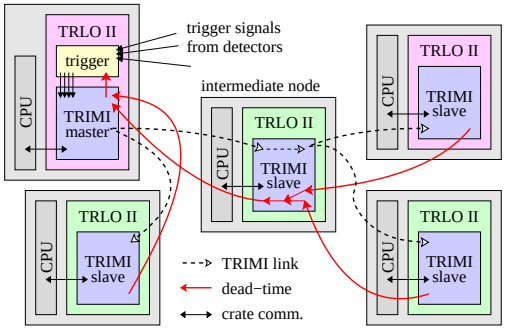

Figure 1: The TRIMI links and dead-time returns can be arranged in a tree structure with intermediate nodes doing fan-out/in and monitoring. The network topology for data flow is independent and can be treated as flat.

The master TRIMI transmits the trigger number and event count for each read-out trigger as a serial message, which is received by connected slave modules. In return, the slaves send their dead-time signals, which can be fanned-in on the way or collected individually by the master. In the latter case, the collecting module (master or intermediate, see Figure 1) also has the ability to record the duration of dead-time for individual slaves, allowing event-by-event performance investigations.

The FPGA footprint in a VULOM4 is about 1350 LUTs (7%), of which 1050 are related to the multi-system link capability. About half of those can be attributed to the full flexibility in which module in- and outputs are used.

After extensive synthetic tests, it is now being set up and verified for use in a detector test run in Cave C in 2014.

References

[1] H.T. Johansson *et al*, "TRLO II – flexible FPGA trigger control", GSI Scientific Report 2010 (2011) 231

[2] Developed at GSI-EE by J. Hoffmann *et al.* `https://www.gsi.de/fileadmin/EE/Module/VULOM/`

[3] J. Hoffmann and N. Kurz, "RISING Data-Acquisition with MBS Event Synchronization with Time Stamp Modules", GSI Scientific Report 2002 (2003), 224

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