# FPGA Based Tunable Digital Filtering for Closed Loop RF Control in Synchrotrons*

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## Introduction

The longitudinal feedback system for the FAIR accelerator SIS100 will rely on digital filters for damping longitudinal bunch oscillations. Filters with a minimum time delay are needed, thus an implementation on a field programmable gate array (FPGA) is necessary. In addition, the filter implementation has to be flexible enough for a real-time adaptation of the filter coefficients during the acceleration ramp. This will enable the tuning of the longitudinal feedback with respect to the synchrotron frequency and other relevant parameters. The filter length will be considerably longer than the currently used three-tap filter of the beam phase feedback [1], offering more degrees of freedom.

## Filter

In order to achieve a constant group delay an finite impulse response (FIR) filter was chosen. The fundamental operation of an $N$-tap FIR filter is the inner product of a vector containing $N$ time shifted scalars of the filter input $x$ with a vector $c$ consisting of the filter coefficients. In a tunable filter design $c$ has to be adapted to the current RF frequency. The adaption of the filter coefficients can be achieved by using a look-up table (LUT) based multiplication scheme on the FPGA. Here, a general purpose multiplier is replaced by a constant coefficient multiplier consisting of LUTs containing partial products followed by bit shifts and adders to calculate the final result. This concept, introduced in [2] was customized with reconfigurable LUTs (content can be changed during run-time) on recent FPGAs [3]. A reconfiguration can be performed in 16 clock cycles which corresponds to 160 ns in the current implementation. This is fast enough to tune the filter characteristics between the calculation of two filter outputs and thus leading to glitch-free switching.

The block diagram of the resulting dynamically reconfigurable FIR filtering is shown in Figure 1. Our implementation realizes a filter with up to $N = 64$ non-zero-taps. Between these taps a tunable number $L$ of virtual zero-taps are inserted to tune the bandpass characteristics of the filter. In addition to this tuning possibility, a larger range of input samples is considered which allows filtering of lower frequency components as well.

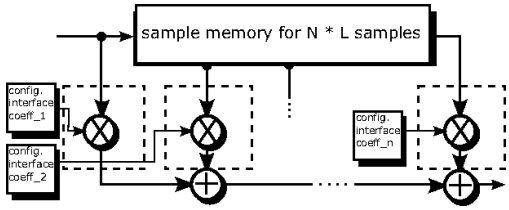


Figure 1: Dynamically reconfigurable FIR filter using reconfigurable LUT multiplication (in dashed lines)

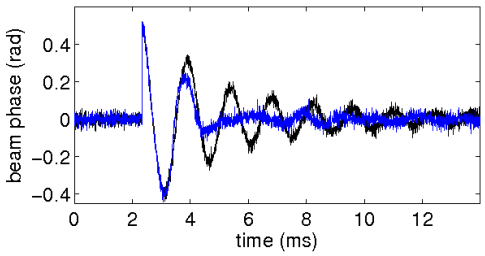


Figure 2: Simulation: open loop (black), closed loop (blue)

## Simulation and Outlook

As an example, the closed-loop performance of an FIR filter used in a longitudinal beam phase feedback loop for SIS18 is shown in Fig. 2. In this nonlinear tracking simulation, $Ar^{18+}$ with a kinetic energy of $11.4\,\mathrm{MeV/u}$ is assumed as ion species. At $t = 2.32\,\mathrm{ms}$, dipole oscillations are intentionally induced by an RF phase shift. The amplitude of the gap voltage is $1\,\mathrm{kV}$, resulting in a synchrotron frequency of $740\,\mathrm{Hz}$. In this case, the filter was designed as a highpass filter with $N = 15$ and $L = 30$.

In future several new filter designs will be possible due to the large number of taps. Further studies will also deal with the optimization of the filter design.

## References

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