Status of the CBMnet based FEE DAQ readout[*]

F. Lemke[1], S. Schatral[1,2], and U. Bruening[1]

[1]University of Heidelberg, Mannheim, Germany; [2]GSI, Darmstadt, Germany

Front-end read-out status

In the past year, the CBM read-out data acquisition (DAQ) network capabilities based on the CBMnet protocol [1] have been extended. Currently, there are two FEE ASIC implementations which include the CBMnet module blocks. The first is the SPADIC V 1.0 [2] with functioning communication, which is currently in the process of commissioning. The second ASIC is the STS-XYTER [3] which provides twice the data bandwidth in backend direction compared to the SPADIC. Therefore, the CBMnet has been extended to a four-lane core and a lot of improvements were implemented. The functional verification of the digital part has been done with two Spartan6 FPGAs in a long term test running more than 7 days. Hence, the FEE LVDS interconnect [4] has been proven as stable under laboratory conditions. To get more information about the status and error behaviour of the LVDS link in the STS-XYTER, a CBMnet diagnostics core has been developed. With that, it is possible to get information about the link quality, read the status of the link initialization and collect statistics about bit-error rates and retransmissions of the active interconnect. The test setup of the STS-XYTER connected to a SysCore3 with HDMI cables is shown in figure 1. The Syscore3 firmware has been extended and now provides a full deterministic optical link.

Figure 1: STSXYTER read-out setup

HUB ASIC prototype design

Further research has been done concerning the HUB ASIC to provide a hierachical synchronized DAQ network [5]. In addition to controlling the FEEs, the focus was to achieve a high density and enable early multilayered data aggregation capability. Thus, flexible build-up scenarios are possible, which are required due to varying amounts

of data for different detector parts. The HUB will support up to 40 FEE links (500 Mb/s) and up to 4 back-end links (5 Gb/s). Besides high density, special difficulties include handling and deadlock avoidance for the traffic, radiation tolerance, and the design of a serializer/deserializer (SERDES) capable of 5Gb/s. A collaboration with the Indian Institue of Technology Kharagpur (IITKGP) was initiated to build this SERDES in partly full-custom design. A SERDES structure diagram is presented in figure 2. It depicts handling of the receive and transmit streams, including features such as clock data recovery (CDR) and eye measurement. Currently, a prototype ASIC is being designed with the focus on testing the SERDES and critical HUB functionality. Therefore, a miniASIC submission will be prepared in 2014 with the TSMC 65nm Europractice process.
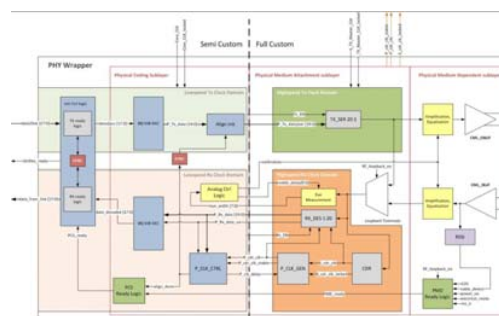

Figure 2: SERDES blockdiagram for HUB ASIC

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