CBM First-level Event Selector Data Management Developments*

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The First-level Event Selector (FLES) is the central event selection system in the CBM experiment. Its task is to select data for storage based on online analyses including a complete event reconstruction. To do so, the FLES timeslice building has to combine data from all input links to time intervals and distribute them via a high-performance network to the compute nodes. Data rates at this point are expected to exceed 1 TByte/s.

The FLES system consists of a scalable supercomputer with custom FPGA-based input interface cards and a fast event-building network (Fig. 1). Constructed largely from standard components, it will be situated at the new FAIR data center.

Timeslice Building

A *timeslice* is the fundamental data structure that manages access to all detector raw data of a given time interval. It provides random access to *microslices*, each containing data from a small amount of time and a single input detector link (Fig. 2). By duplicating a small number of microslices at the border of a timeslice (*overlap region*), differences in detector readout timing performance can be accomodated, and it is ensured that every timeslice can be processed independently.

These data structures and a timeslice-based API for the following online data processing have been developed and optimized such that computer memory access (e. g., required by additional copy operations) can be minimized.

For data transfer between the FLES nodes, it has proven practical to use an InfiniBand network. A prototype software for efficient timeslice building based on InfiniBand Verbs has been developed, especially addressing questions regarding data structures and buffer management. It implements the full data structures as intended for the final setup. The feasibility of employing a more high-level interface to the network hardware, like MPI, is currently under investigation.

Efficient Timeslice building over a state-of-the-art InfiniBand FDR network has been successfully demonstrated on a small scale on the Micro-FLES cluster installed at GSI.

FLES Interface Board (FLIB)

The CBM detector data enters the FLES system through custom add-on cards in the FLES PCs. These FLES Interface Boards (FLIBs) require high-speed optical inputs to receive the data from the CBM readout electronics, a high-performance interface to the host PC, and a large buffer memory. A specially developed FPGA-based card with a PCIe interface at the maximum achievable rate will be employed here.

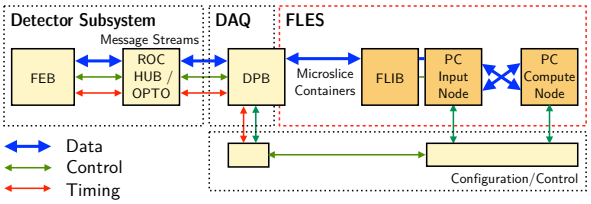

Figure 1: The First-level event selector (FLES) in the CBM read-out data path.

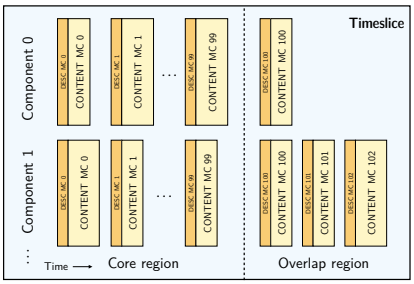

Figure 2: The FLES timeslice data structure provides indexed access to detector raw data packaged in microslices.

The FPGA design implements the DAQ protocol for receiving the data, manages the buffer memory, and controls the PCIe transfer. In contrast to the final system, early prototype setups lack the DPB layer (cf. Fig. 1) and do not support the creation of microslices. The current prototype firmware therefore includes a mockup of the foreseen DPB design and is capable of directly receiving CBM-Net messages as delivered by the CBM front-end electronics.

The FPGA design has been ported to the Xilinx Kintex-7 family of FPGAs, as the current standard readout chain for CBM detector development employs a prototype board with this device. The prototype firmware, implemented in a total of 9700 lines of VHDL code, has been completed and successfully tested in a readout setup. In the future, further optimization of the DMA architecture including the software device driver will have to be performed to minimize memory access operations on the host PC.

Both aspects, input interface and timeslice building over Infiniband, have been intergrated in a common data management software project. This allowed to set up and successfully demonstrate the FLES data chain from data generating boards connected to the FLIB optical inputs to substitute analysis code on a FLES compute node after complete timeslice building.

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