A front-end electronics board to test the assembly procedure of modules for the CBM Silicon Tracking System*

V. Kleipa[1], *C.J. Schmidt*[1], *C. Simon*[1], *and D. Soyk*[1]
[1]GSI, Darmstadt, Germany

The STS front-end electronics board

For the Silicon Tracking System (STS) of the CBM experiment, about 2000 read out electronic boards (FEBs) have to be produced. They comprise eight readout ASICs of 128 amplifier channels each which will read the 1024 sensor channels on either side of a STS detector module [1]. So there is a need to prepare tools and assembly instructions for their serial production. In order to develop and verify the assembly procedures, a test board has been designed.

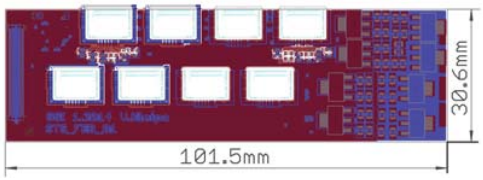

Figure 1: STS FEB8 test layout.

Module assembly chain

The assembly chain will start with the tab-bonding of the read-out micro-cables on the ASICs. Then the ASICs must be glued in spares of the FEB's printed circuit board. In a next step the ASICs will be connected to the supply, control and read-out lines with wire bond. The challenge is how to adjust the ASICs with the sensitive tab-bonded sensor-cables on the PCB and how to connect the ASÌCs further with bond wires to the main PCB.

In all these cases the hight of additional components on the PCB have to be respected. I.e. SMD capacitors and resistors or the globtop - which is protecting the bond-wires, cause barriers for the second row of ASIC chips. It needs also to be verified, if embedded passive devices are required to be reduced in height.

Two ASIC footprints are prepared on the PCB for the different test purposes. One footprint needs to be generated with laser cavity technology. Here the bond wires can be connected directly to the inner layers of the PCB. The other footprint consists only of bond pads on the top layer. Some additional routing space will be required here too. Additional thermal cycling tests are planned to proof the safety of the tab and wire bond connetions.

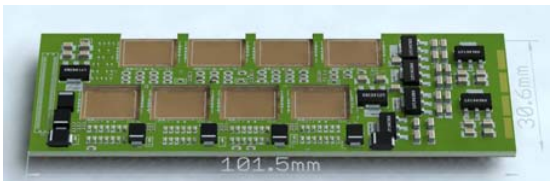

Figure 2: 3D View of equipped STS FEB Board.

Test board and assembled object

The front-end board designed to test the assembly procedure and the functionality of the pairs of ASICs and tab-bonded micro cables is shown in Figures 1 to 3:

- Figure 1 depicts the FEB layout for the assembly test.
- Figure 2 is a 3D rendering of a possible FEB PCB.
- Figure 3 depicts an assemby with FEB, ASICs and micro cables.

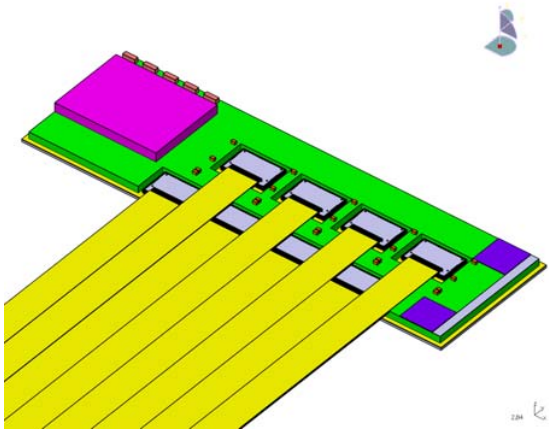

Figure 3: Assembly of sensor cables and FEB.

References

[1] J. Heuser et al., Technical Design Report for the CBM Silicon Tracking System, GSI Report 2013-4, Chapter 5.3 Modules, p. 79-83, http://repository.gsi.de/record/54798

* supported by EU-FP7 HadronPhysics3

 doi:10.15120/GR-2014-1-NQM-CBM-18