Integration of nanowires onto 100 mm wafers by the growth in-place method*

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The synthesis of submicron wires and nanowires based on ion-track-etched polymer templates and subsequent electrodeposition is an important expertise [1] this work relies on. Our approach [2] describes the growth in-place of metallic micro and nano-wires onto rigid and planar wafers of 100 mm diameter. These wafers are designed to be used for high-resolution UV lithography for batch fabrication of microstructures. Thereby, the approach paves the way to the integration of free standing submicron wires and nanowires in micro-electro-mechanical systems (MEMS) with manifold opportunities of application.

The process starts with the physical vapor deposition (PVD) of a 150 nm thick Ni film followed by microstructuring by lithography and wet etching (fig. 1 a). After stripping the photoresist, these circuit paths are gold plated by immersion. Then another photoresist layer is applied onto the wafer surface lithographically in such a way that specific areas remain open for later wire growth (fig. 1 b). In parallel, ion-irradiated polycarbonate membranes are etched to produce parallel-oriented cylindrical channels vertically perforating the membranes (fig. 1 c and d) [3]. Subsequently, the track-etched membrane is laminated onto the wafer (fig. 1 e). By applying heat and pressure, the photoresist becomes adhesive and reliably fixes the membrane on the wafer surface.

In the following, the channels are filled with a metal by electrodeposition. The control of the process parameters allows us to taylor the shape of the wire array. The wire growth can be stopped before reaching the membrane surface (fig. 1 f). Alternatively, the growth can be continued to obtain a closed top layer on the wire array (fig. 1 g). Another option is to apply PVD, thick film lithography, and electrodeposition on top of this structure and to grow another metallic microstructure on the upper layer of the wire array (fig. 1 h). By means of plasma etching, all polymer material can finally be removed releasing the wires with clean functional surfaces and without sticking of adjacent wires.

Currently, three system configurations with integrated vertical wires are investigated.

Gold submicron wires without overgrowth are studied to minimize the electrical resistance of contact systems in MEMS (fig. 1 i). The wires are very flexible and are supposed to need minimal forces to build up small resistance micro contacts (a-spots).

Wire arrays made of vertical submicron wires with a closed overgrown top layer are investigated for gas flow analyzing MEMS (fig. 1 j). The large surface-to-volume ratio is expected to accelerate the system response.

A similar configuration applies a larger microstructure on top of the flexible wire array for an acceleration detection MEMS (fig. 1 k).

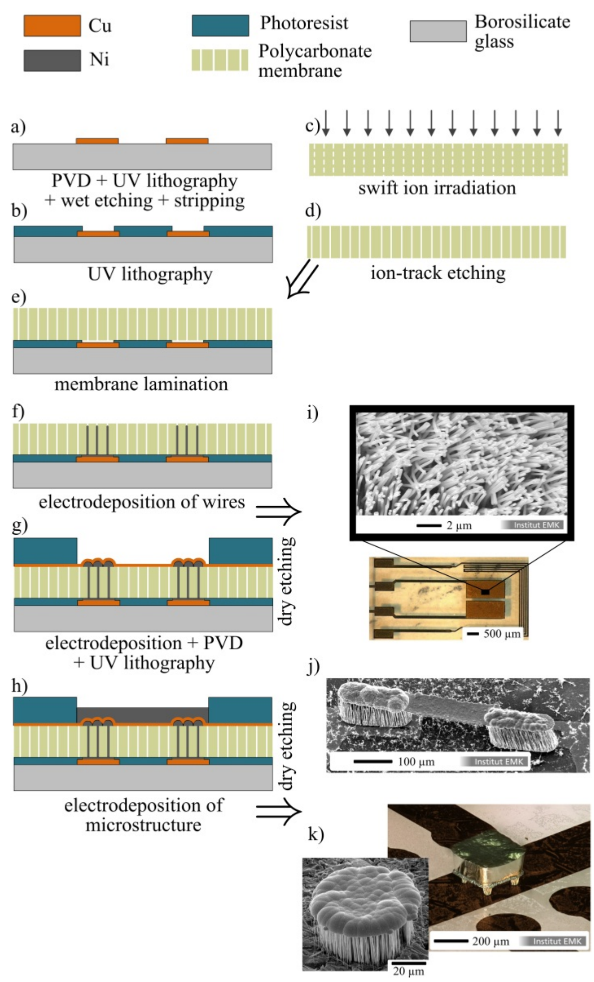

Figure 1: (a-h): Process flow of micro- and nano-wire integration by the growth in-place method; (i-k) Scanning electron and optical microscopy images of MEMS with grown in-place wire arrays.

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