VFTX (VME-FPGA-TDC 10ps)

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For high accuracy timing measurements the VME-Module VFTX (Figure 1) has been developed at GSI Experiment Electronic Department. It has an FPGA based TDC design using the tapped delay line method [1].

Figure 1: VFTX Module

The VFTX can handle up to 32 LVDS input signals or with a different add-on pcb 16 NIM signals. Available programs are:

- 16 Channel ~7ps (leading edge)
- 32 Channel ~10ps (leading edge)
- 28 Channel ~10ps with time over threshold information (leading edge and trailing edge)

An external clock input allows having more than one module running on the same clock. An external reset Input and a reset command via VME command assures that the modules clock counter are reset at the same time. Due to that there is no need of a reference signal in each TDC and no loss of √2 in resolution. The readout of this module is trigger based and the used data acquisition is MBS (Multi Branch System).

Laboratory Test Setup

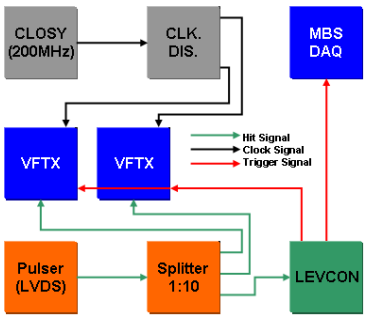

Figure 2: Block diagram Pulser Test

Figure 2 shows a simplified block diagram of the test setup in the laboratory. In grey the clock generator CLOSY [2] with the clock distribution can be seen. In orange the signal generator with the signals splitter, to have 10 times the same input pulse available. The blue blocks are the VME modules VFTX and the necessary modules for MBS readout. The LEVCON (Level-Converter) is used for sending out the trigger in different levels.

Results

The result of this measurment are despicted in Figure 3. On the left side of the picture the time resolution for a 28 channel (TOT) design with 9.5ps and on the right hand side the time resolution for a 16 channel design with 6.6ps time resolution are shown. These two results are measured both on the same VFTX module.

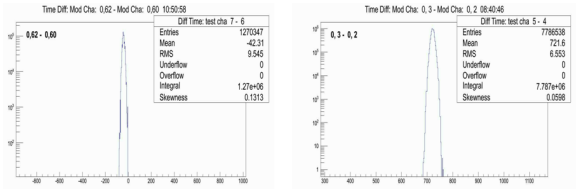

Figure 3: Time resolution between two channels.

Measurements between two VFTX modules have a resolution of ~12ps for a 10ps design and ~9ps for a 7ps design between two channels. This loss of 2ps is due to the clock splitter, which provides the master 200MHz clock for the different modules.

Conclusion & Outlook

The VFTX Module shows nice result in the laboratory tests and was already used successfully in beam by the SOFIA Collaboration for PMT readout and by the CBM–TOF Group for RPC readout.

The second iteration with small bug fixes will be available beginning March 2013.

References

[1] E. Bayer, M. Traxler: Development of a High-Resolution (< 10 ps RMS) 32-channel TDC in a Field-Programmable-Gate-Array, GSI Scientific Report 2009, p.325

[2] K. Koch: CLOSY: A very Precise Clock Generation for Timing Measurements and Synchronization of the CBM ToF Wall, GSI Scientific Report 2009, p.82