Field-Programmable-Gate-Array Based Signal Discrimination and Time Digitisation*

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The research about FPGA based Time-to-Digital Converter described in [1] is pushed further and tested with different boards using different FPGAs. As the results generated with Lattice FPGAs were promising, new boards with Lattice FPGAs have also been developed for experimental applications.

The TDC design is implemented with 16 channels on the EXPLODER1 and FEBEX 2 boards with ECP2M FPGAs. The precision of the TDC is improved to 11 ps in the single clock cycle measurement range by using the Wave-Union method [2]. For excess data suppression trigger window functionality is implemented.

For FPGA based time digitisation applications a new board, TRB3, has been developed. The board has 5 large and cost effective Lattice ECP3-150EA FPGAs with 150K LUTs, 4 of which are used for the TDC applications and the central one is used for the connectivity. The central FPGA can be configured to deliver the data through direct GbE-links or optical links running the mature TrbNet protocol also used in the HADES experiment. The TDC design is adapted to the ECP3 family architecture and each TDC-FPGA is equipped with 64 TDC channels for the time measurements and 1 reference channel for the synchronisation of the whole system with a total of 260 channels. The achieved time precision is similar with the ECP2M architecture ($\sim$11 ps) for single clock cycle time intervals. The board can cope with a hit rate of 50 MHz (in a burst) and a data readout trigger rate of 300 KHz. With the included epoch counter the measurement range of the TDC is increased to $\sim$45 minutes. The board is designed to be used in large systems using the TrbNet as well as a stand alone system with only a 48 V power supply and the GbE implementation in the central FPGA in order to send data out to a PC. The TRB3 is suitable for Time-of-Flight (ToF) and Time-over-Threshold (ToT) measurements, where the time information is encoded in the discriminated detector signals.

One of the applications for the TRB3 is the time digitisation and the readout of the photo-multiplier tubes (PMTs) and the micro-channel plate detectors (MCPs). The analogue signal from the detector is first amplified and then discriminated with the front-end electronics developed at the University of Mainz. The rising edge of the discriminated pulse carries the timing information, whereas the pulse width carries the time-over threshold (ToT) information. The discriminated pulse is then converted to a fast LVDS signal and delivered to the TRB3 for the time measurements. With this setup the readout of the PANDA Barrel-DIRC prototype was successfully carried out in the July 2012 beam time at MAMI.

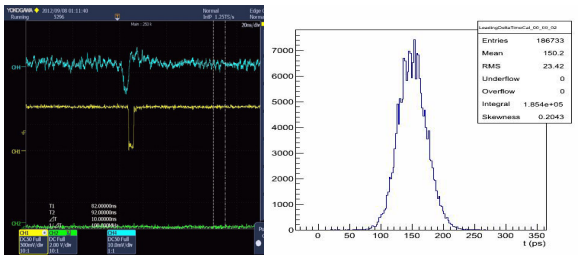

Figure 1: (a) The analogue signal is discriminated at the LVDS receivers of the FPGA and sent out for time measurements as a digital LVDS signal. (b) The precision of the whole system - discriminator board and TRB3 - is measured as $\sim$23 ps.

Another development is the discrimination of the detector signals using the LVDS buffers of an FPGA. The developed FEE board has MMICs at the amplification stage. The amplified signal is discriminated against the reference voltage at an LVDS input buffer. The time information of the leading edge and the ToT of the detector signal are encoded in the digital pulse in the FPGA. This digital pulse is sent out to the TRB3 as a differential signal via an LVDS output buffer for time measurements (Figure 1(a)). In order to set the threshold at the LVDS receiver the FPGA is used as a DAC via a Pulse Width Modulator (PWM) and low pass filter. The discrimination board is connected directly to the detector outputs. In the laboratory the time precision is measured as $\sim$23 ps RMS (Figure 1(b)). This development has been tested successfully during the PANDA-DIRC detector test beam time (@COSY) with 2400 channels in November 2012.

Further implementation of the FPGA based TDC design is carried out with FEBEX 3 boards and a prototype with 100-200 channels is foreseen.

References

[1] C. Ugur et.al, GSI Scientific Report 2010, p.237.

[2] J. Wu and Z. Shir, *The 10-ps wave union TDC: Improving FPGA TDC resolution beyond its cell delay*, Nuclear Science Symposium Conference Record, 2008 IEEE.

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