Hardware Development for CBM ToF

J. Frühauf[1], N. Herrmann[2], M. Ciobanu[3], H. Flemming[1], H. Deppe[1], I. Deppner[2], P.-A. Loizeau[2]

[1]GSI, Darmstadt, Germany; [2]Physikalisches Institut, Universität Heidelberg, Germany; [3]ISS, Bucharest, Romania

The CBM-ToF-Readout-Chain is based on preamplifier and discriminator ASICs (PADI) [1] and event-driven TDC ASICs (GET4) [2] as front-end electronic. These ASICs are specially developed for the CBM-ToF detector.

Hardware: PADI-6 and PADI-7

For the preamplifier it is necessary to go nearby to the RPC to reach the best performance. Therefore it is decided to go even inside of the RPC-GAS-Box with the preamplifiers for the outer part of the ToF-Wall. Here we have a direct connection from the RPC to the FEE. The PCB layout was done in a way that there is one baseboard for power distribution, SPI-DAC-interface and connector for the output signals and "OR" signals from PADI. Each add-on PCB is equipped with two PADI-ASICs and the connector for the RPC.
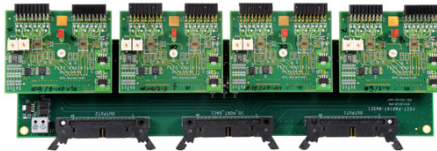

Figure 1: PADI-FEE (32 Channel)

Pulser Test: PADI-7

Two single ended pulses are injected into two input channels of PADI. The measurement was done for different signal amplitude as well as the threshold level of PADI was modified. The LVDS output signal was measured with an oscilloscope (Tektronix TDS6154C). The results of this measurement are shown in figure 2.
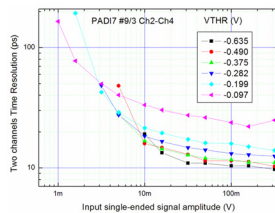

Figure 2: Resolution between two channels

The resolution between two channels for input signal amplitudes between 10mV and 100mV at different threshold values is below 20ps, which fulfils the CBM-ToF requirements.

Hardware: GET4 1.0

The test PCB for the GET4 1.0 ASIC is shown in the following picture. The main goal of this design is to test on board clock and power distribution, different supply voltages (5V; 12V and 48V) as well to test the new ASIC. One baseboard (Figure 3) can be equipped with four add-on PCBs, where each of them is equipped with four GET4 ASICs.
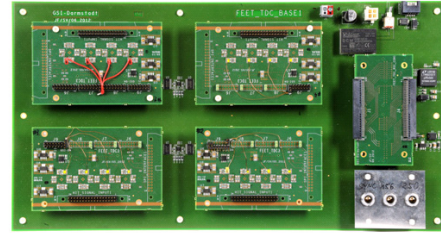

Figure 3: GET4-FEE (64 Channel)

On the left side of the picture the four add-on PCBs are seen. In the upper right corner the different power injections and in the lower right corner the two clock inputs as well as the sync signal input send out by CLOSY[3] are placed. In between, although as add-on PCB, the connector for the readout controller is placed.

Pulser Test: GET4 1.0

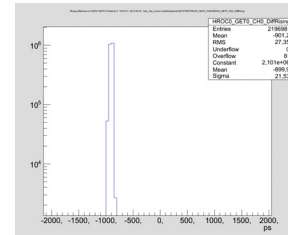The result of a pulser test in the laboratory is depicted in figure 4.

Figure 2: Resolution between two channels

The same LVDS signal is injected into two channels of two GET4 ASICs to mark each rising and falling edge with a time-stamp. The resolution between two channels is ~ 27ps.

Outlook

New frontend cards with specific layouts for each detector as well as test pcbs for the upcoming version of PADI and GET4 will be developed.

References

[1] M. Ciobanu et al., "PADI-6 and PADI-7, new prototypes for CBM ToF", this report
[2] H. Flemming et al., "GET4 1.0", this report
[3] K. Koch:"CLOSY", GSI Scientific Report 2009, p82