

## PADI-6 and PADI-7, new ASIC prototypes for CBM ToF

M.Ciobanu<sup>1</sup>, N.Herrmann<sup>2</sup>, K.D.Hildenbrand<sup>3</sup>, M.Kiš<sup>3</sup>, A.Schüttauf<sup>3</sup>, H.Flemming<sup>3</sup>, H.Deppe<sup>3</sup>, J.Frühauf<sup>3</sup>, I.Deppner<sup>2</sup>, P.A.Loizeau<sup>2</sup>, M.Traeger<sup>3</sup>

<sup>1</sup>ISS, Bucharest, Romania; <sup>2</sup>Physikalisches Institut, Universität Heidelberg, Germany; <sup>3</sup>GSI, Darmstadt, Germany

We designed a general purpose PreAmplifier-Discriminator (PADI) ASIC which can be used as a Front-End-Electronics for Resistive Plates Chambers in future CBM at FAIR. The low power PADI-chip can be used for different flavors of RPC's, with strip / pad like anode structures. These timing devices have signal rise times  $t_r < 300$  ps and primary charges in the range of 10 to 500 fC, which needs a preamplifier-discriminator stage with an intrinsic electronic resolution of  $\sigma_{IE} < 15$  ps. We developed and tested different 4 channels prototypes in CMOS 0.18  $\mu\text{m}$  technology [1,2] with the following design key parameters: fully differential using a  $50 \Omega$  input impedance at a preamplifier gain of  $G_p > 100$  with a bandwidth of  $BW_p > 300$  MHz having a peaking time for the signal of  $t_{pk} < 1$  ns and a noise related to input of  $V_{N-IN} < 25 \mu\text{V}_{RMS}$ . We use a DC feedback loop for offset and threshold stabilization; the threshold range between  $\pm 500$  mV. As auxiliary functions PADI offers an OR-out. For the last prototypes, the increase of the charge responsibility and the decrease of the DC offsets were the main tasks. The Monte Carlo simulation shows that the preamplifier schematics must be drastically changed (Fig.1).

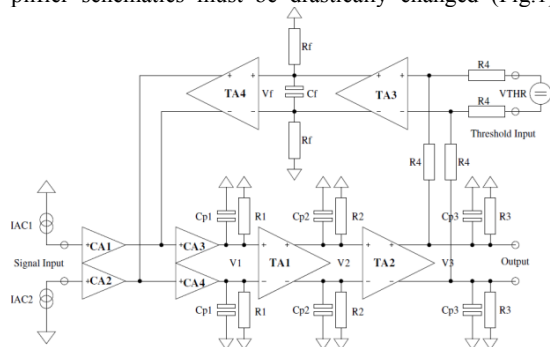


Figure 1: The simplified ac schematic of the preamplifier. The feedback path is now unique for signals and threshold voltage. The whole schematic can be evaluated like a full differential operational transconductance amplifier (OTA), having two inputs (VTHR and Signal) and one output. The resistive feedback realized with 4 identical resistors (R4) assure a linear DC transfer function. Except  $R_f$ , all resistors in schematic are physical resistors like in PADI-1. This solution achieves a maximum preamplifier bandwidth with good Monte Carlo results in matching of components or taking into account the technological dispersions. The threshold voltage is obtained from a DC bridge realized by 6 resistors R. This bridge is supplied from VDD and can be controlled internally by two 10 bits DACs (PADI-6) or externally (PADI-6 and PADI-7), by a potentiometer connected between VREF+ and VREF-pads and having the cursor at ground potential. These

pads are common for all channels and one potentiometer can control all channels. The two DACs (PADI-6) are complementary commanded and the common mode voltage is not affected by the DAC code value. We have changed the type of the interface from I2C to the very often used SPI (Serial Protocol Interface) which is more simple and robust [3]. The SPI interface is currently used in many types of microcontrollers (e.g. the PIC family) and the implementation of PADI test equipment will be easier.

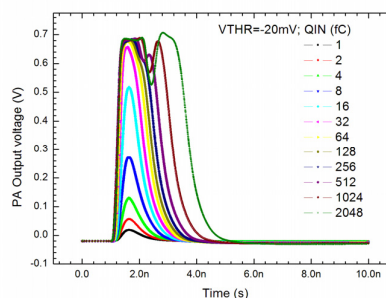


Figure 2 Simulation: PADI-6,-7 charge responsivity.

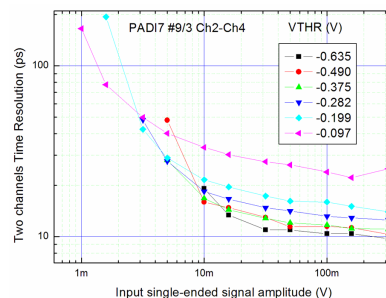


Figure 3 Measurement: Two channels time resolution versus input signal amplitude dependence to VTHR.

### References

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- [3] J. Frühauf, N. Herrmann, M. Ciobanu, H. Flemming, H. Deppe, I. Deppner, P.A. Loizeau, "Hardware Development for CBM ToF", this report.