The GSI Event driven TDC GET4 V1

H. Flemming[1] *and H. Deppe*[1]
[1]GSI, Darmstadt, Germany

Introduction

In 2009 results of a first test design of the GET4 TDC ASIC have been obtained[1]. In the meantime additional analysis of the behavior of this ASIC in beamtimes as well as the submission of two test chips to improve the linearity of the TDC core have been done. Based on these activities in march 2012 the first fully equipped GET4 V1 was submitted to the IC foundry.

The GET4 ASIC

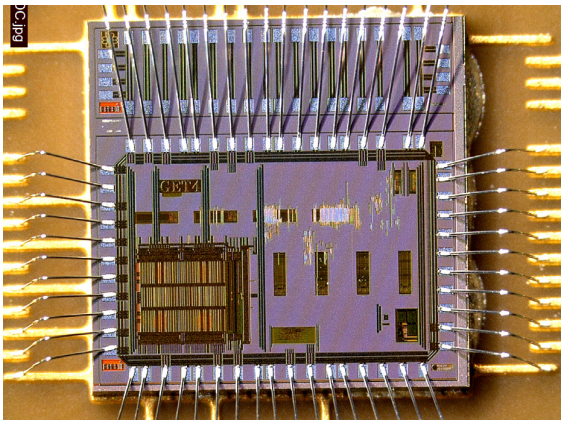

Figure 1: Die Picture of the GET4 ASIC.

The full custom designed TDC core of the GET4 V1 is based on the same architecture as the one of the first GET4 ASIC but is improved in many details. The TDC core is visible on the lower left side of the die picture in figure 1. The readout logic of the GET4V1 is completely new developed and automatically synthesised from a vhdl code. It contains a 24 bit readout mode that is compatible to the old GET4 ASIC and a new 32 bit mode that can cope with higher event rates. The 32 bit mode provides an internal time over threshold calculation and more slow control information. More information about internal structure, programming and data format can be found in the ASIC documentation[2].

Results

The tests and measurements of the GET4 V1 could confirm the good results of previous test chips. Figure 2 shows a pulse width spectrum and a time difference spectrum of a test signal generated with an internal test pattern generator. The width of the time difference peak is 27.9 ps rms. After division by $\sqrt{2}$ one gets an uncorrelated time resolution

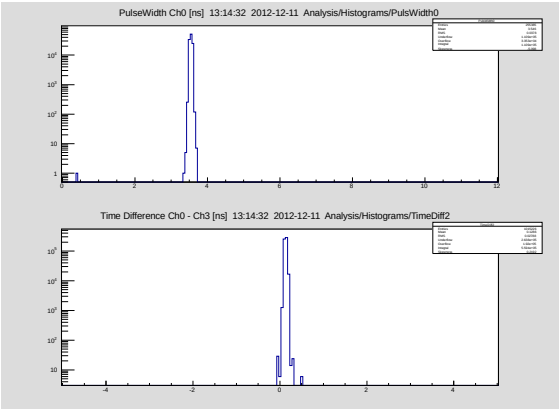

Figure 2: Pulse width and time resolution spectra.

of 19.7 ps for time differences. As the pulse width measurement contains the jitter of the internal ring oscillator as additional error contribution the result is slightly worse than the resolution for the time difference.

Outlook

Beside the very good TDC performance during tests also a few bugs have been found[3]. These bugs have been corrected in the design and on February 11th, 2013 a second iteration of this ASIC has been submitted to the foundry. This chip is expected to be produced in May. So for a new beam test campaign end of 2013 a bug fixed GET4 V1.2 will be available. In parallel the development of a programmable readout controller[4] will be continued with the second prototype that now fits to the 32 bit readout mode of the GET4 V1, delivered in February 2013. Tests will start in spring 2013.

References

[1] H. Deppe, H. Flemming, “A Wide Applicable TDC with Event-Driven Readout”, GSI Scientific report 2009

[2] H. Deppe, H. Flemming, “The GSI Event driven TDC with 4 Channels GET4 Version 1.20”, http://wiki.gsi.de/pub/EE/GeT4/get4.pdf

[3] H. Flemming, “Results of GET4 Tests, Known Bugs and Performance”,Talk in EE-meeting, http://wiki.gsi.de/pub/EE/EEMeetVortragArch/GET4V1.10Bugs.pdf

[4] H. Flemming, J. Frühauf, “A CPU Controlled SEU Hardened Readout Controller for the GET4 TDC Readout”, GSI Scientific report 2011, PHN-IS-EE-04