n-XYTER 2.0 Operative and Tested

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n-XYTER is a self-triggered multi-channel charge sensitive detector readout chip, originally developed for the signal readout of thermal neutron detectors [1] and similar to FSSR2 [2]. It is being employed in many detector prototyping activities for the FAIR experiments and others [3], [4], as it is the only front-end chip available which realizes a self-triggered architecture, is applicable for both polarity signals and finally has sufficiently high gain for the detection of MIP size signals in Silicon.

The first prototype version 1.0 has been extensively tested and turned out to show a severe temperature coefficient in the DC-signal levels of about 4%/K, which made its employment very tedious and difficult, as the slightest temperature variations resulted in enormous pedestal drifts.

With the aim to repair the temperature coefficient, the chip underwent a redesign, which primarily focussed upon the supply of several biasing potentials from outside the chip, the correction of various layout deficiencies and finally the introduction of a switch that would change the gain by about a factor of 4 and thus extend the dynamic range by the same factor.

The submission of n-XYTER 2.0 was realized as an engineering run, which served to supply a sufficient number of dies for the use in FAIR detector prototyping activities as well as thermal neutron detector developments targeted at the Physikalisches Institut Heidelberg. The design was submitted in the AMS 0.35µm process, twelve wafers were produced in total. For risk mitigation purposes one out of four locations on the reticle was filled with the original design of n-XYTER 1.0, the other three locations realized n-XYTER 2.0.

Chip Testing

The chip was taken into operation on a pcb previously employed for n-XYTER 1.0 through the use of a little fudge board, which carried the four adjustable external bias sources that need to be supplied with this version of the chip.

The strategy for setting these biases turned out comparatively simple: the bias for the pre-amp is to be set such that the DC output of the pre-amp is identical to the input potential. Further, the three dc-bias voltages for the fast shaper circuit as well as the two successive slow shaper circuits can easily be set with the target of setting the output DC levels to adequate values.

The temperature coefficient was measured for every channel on a chip and found at a level of 0.12 mV/K or ~ 2 10^{-4}/K, an improvement by a factor of 200 as compared to n-XYTER 1.0.

Then the internal charge injection circuit was tested and calibrated for two individual chips by comparison to the response of a very well calibrated external charge injection circuit. Variations were found on the level of +- 5%, which may be attributed to variations of the effective input coupling capacitance of the internal test circuits.

Likewise the gain of every channel was individually determined. Fig. 2 shows the histograms of the channel gain of one chip for pos. and neg. signal polarities.

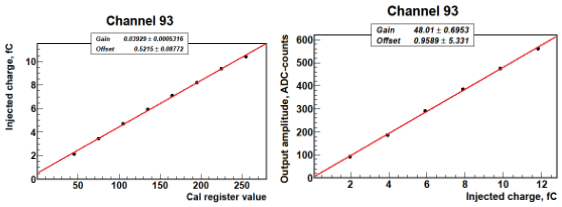

Figure 1: Calibration of the test pulse circuit, using a highly accurate external injection circuit (right) and comparing the signal response to the signals generated by the internal circuit (left)

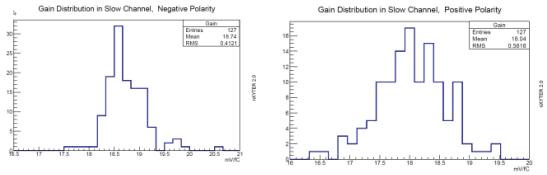

Figure 2: Histograms of measured gain for positive (right) and negative (left) input signals.

The newly introduced feature, the swichable dynamic range through swichable gain did result disappointing. Gain may indeed be changed by about a factor of 2.5. The dynamic range however resulted to remain the same, as the analogue output operating window is in effect reduced by the same factor. In conclusion, this feature may only be realized with much more sophisticated changes in the circuitry, which for this submission was omitted to minimize risk of failure.

Conclusion

n-XYTER 2.0 is functional. The temperature coefficient has been abolished. By now, the full set of tools for an automated serial test has been set up and may now be employed for a wafer-scale test campaign to characterize this batch of chips.

References

[1] A. Brogna et al., Nucl. Instr. Meth. Phys. Res. A568 (2006) 301-308

[2] Re et al, 2005 IEEE Nucl Sci Symp Conf Rec, N16-1

[3] GSI Scientific Report 2008, FAIR-Experiments 10

[4] GSI Scientific Report 2009 71