ALICE C-RORC as CBM FLES Interface Board Prototype*

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The ALICE Common ReadOut Receiver Card (C-RORC) is an FPGA-based PCIe readout card with high density parallel optical connectivity addressing the needs for the upcoming ALICE upgrade. This card is also considered as a prototype for the CBM First Level Event Selector Interface Board (FLIB) and CBM related requirements have already been integrated during development. First prototypes of this board have been produced and could be tested successfully.

FLES Interface Board

The FLES Interface Board serves as an interface between Data Processing Boards and the First Level Event Selector in the CBM readout chain. It is planned to be implemented as an FPGA-based PCI-Express plug-in card with optical interfaces at the FLES input nodes. Streaming data received on the optical interface from the front-end electronics via Read-Out Controllers and Data Processing Boards is received by the FLIB and provided the host machine using Direct Memory Access (DMA). Prototype boards are required as a test platform for FLES hardware and software development as well as for testbeam and lab setup readout. A more detailed description of the FLES developments can be found in [1].

The C-RORC is a Xilinx Virtex-6 based FPGA board developed by ALICE to replace existing readout boards and enable upgrades of the current readout architecture. The board comes with an eight lane PCI Express Gen2 interface to the host machine and 12 serial optical links up to 6.6 Gbps using three QSFP modules. The highly parallel optical connectivity, the DDR3 RAM and its interface to the host machine makes this board a suitable prototype for first FLIB firmware developments. Requirements for the usage as FLIB prototype have already been considered during the development of the card. The layout of this board was completed in 2012 and first prototypes have been produced. A picture of the board is shown in figure 1.

C-RORC Hardware Test Status

Several hardware tests have been performed to confirm the correct operation of the board and have been compared to previous firmware tests with commercially available evaluation boards. The throughput of the PCIe interface has been directly compared with a reference implementation on the HitechGlobal board and could be confirmed to be identical. All DMA tests have been performed with a custom device driver and DMA engine. A generic device driver, DMA library and software architecture is currently being developed. More details on this can be found in [2]. The onboard flash memories are accessible with both the PCIe interface and the programming cable. The FPGA gets automatically configured from these memories on power-on and the device is correctly detected on all tested host machines. The serial optical links have been tested with electrical and optical loopback adapters, optical QSFPs and active optical cables. A long term test of a full setup with two boards interconnected with QSFP transceivers and parallel fibers did not show any bit errors. First DDR3 tests with SO-DIMM modules operating with 800Mbps and 1066Mbps could also be concluded successfully. The onboard microcontroller for configuration monitoring and control could also be verified. The board is accessible from the I2C chain of the host machine, the configuration status and the board voltages can be read out with I2C and a reconfiguration of the FPGA from a selected flash partition can be triggered. There are no major PCB changes required for the next series of boards.

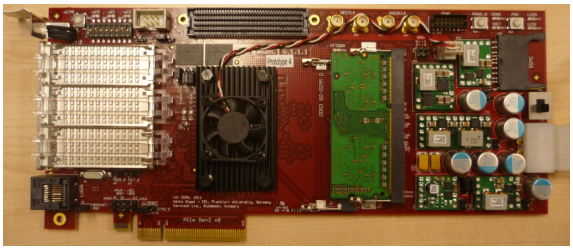

Figure 1: Photo of a C-RORC prototype with one DDR3 module.

Conclusion

All hardware tests that have been performed by now could be concluded successfully. All major interfaces have proved reliable behavior and there are only a few untested aspects of the board remaining. A larger number of boards is going to be produced in 2013 and will be provided to several working groups to investigate the hardware more deeply and continue the development of firmware and software.

References

[1] J. de Cuveland et al., “Status of CBM FLES Prototype Developments” , This report

[2] D. Eschweiler, V. Lindenstruth, “Microdrivers in High-Throughput and Real-Time Environments”, FIAS Scientific Report 2012 (to appear)

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