ToF-ROC FPGA Irradiation Tests 2012*

S. Manz[1], *J. Gebelein*[1], *A. Oancea*[1], *H. Engel*[1], *and U. Kebschull*[1]

[1]Infrastruktur und Rechnersysteme in der Informationsverarbeitung (IRI), Frankfurt University, Frankfurt, Germany

Introduction

Ionizing radiation can severely disturb the operation of electronic devices, especially SRAM based electronics like *Field Programmable Gate Arrays* (FPGAs). The theory of radiation induced failures is well known and radiation mitigation techniques have been developed [1, 2]. However, when using commercial of-the-shelf electronics the internal details of electronic circuits are generally not known and the efficiency of the mitigation techniques need to be tested in experiments before the usage of those electronics can be approved. Here we show the result of a test carried out at the accelerator facility at the *FZ Jülich*, Germany, in August 2012. Contrary to previous tests, our intention was not to characterize the chip's internal logic cells using an academic test design. We evaluate the efficiency of the radiation mitigation technique *scrubbing* on logic of an actual firmware that is currently used for readout of the GET4 TDC [3]. For characterizing the efficiency we do not use the particle flux as reference but directly count the induced upset rate in the configuration memory of a second identical device in the beam. The firmware itself was running on a Xilinx Virtex-4 FPGA operating directly in a $2\,GeV$ proton beam at a particle rate in the order of $10^7 s^{-1} cm^{-2}$.

Results

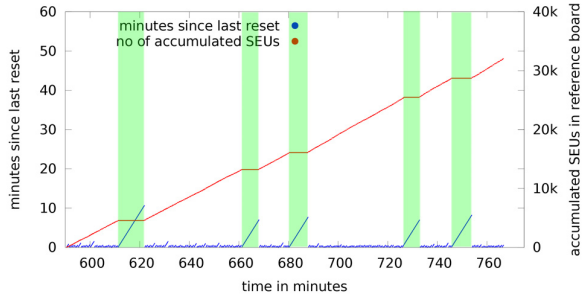
Figure 1 shows a direct impression of the values recorded during the beam time. Both diagrams show the results of a three hours run, where scrubbing is disabled (figure 1(a)) and enabled (figure 1(b)). The in-beam tests showed very promising results when using the *scrubbing* technique on an operational detector read-out firmware. The dead time of the device could be reduced by almost a factor of 50 and corrupted data could be reduced by a factor of 200 while ressource utilization increased by less than a factor of two.

Outlook

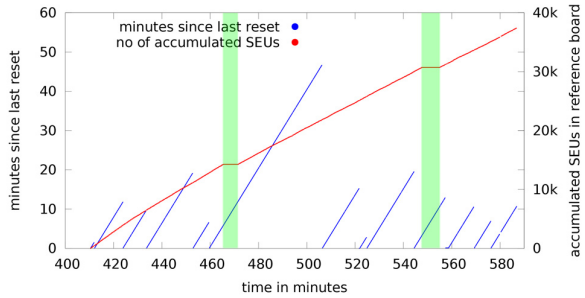
With the great efficiency of the configuration scrubber, an FPGA based read-out controller for the CBM-ToF front-end electronics is absolutely feasible.

For the real CBM experiment the occurance of an SEU needs to be logged directly in the data stream for data analysis. A concept for doing so needs to be developed and experimentally approved, also considering new possibilities that emerge with the Xilinx series 7 FPGAs [4].

* Work supported by BMBF No. 06HD9123I.



(a) Scrubbing is disabled. Full reset of the setup required in less than a minute. The setup is only stable when beam turned off.



(b) Scrubbing is enabled. The setup runs stable for several minutes.

Figure 1: The red plot refers to the number of SEUs collected in the reference board while the blue plot shows the time since the last full reset of the setup, every return-to-zero of the blue plot refers to an unrecoverable failure of the setup caused by radiation. During the highlighted time slots the beam was shut down for technical reasons.

References

[1] H. Quinn *et al.*, "An Introduction to Radiation-Induced Failure Modes and Related Mitigation Methods For Xilinx SRAM FPGAs," *Proc. Engineering of Reconfigurable Systems and Algorithms*, 2008

[2] Mike Wirthlin, "FPGAs Operating in a Radiation Environment: Lessons Learned from FPGAs in Space," TWEPP 2012 Conf., 2012

[3] H. Flemming and H. Deppe, "The GSI event-driven TDC with 4 channels GET4," *Proc. IEEE Nucl. Sci. Symp. Conf. Rec.*, 2009

[4] *7 Series FPGAs Configuration User Guide, UG470 (v1.5)*, Xilinx Inc, 2012