STS-XYTER a prototype silicon strip detector readout chip for the STS

P. Grybos[1], *K. Kasinski*[1], *R. Kleczek*[1], *P. Otfinowski*[1], *and R. Szczygiel*[*1]
[1]AGH-UST, Krakow, Poland

The STS-XYTER prototype readout ASIC for the CBM STS detector was designed in 2012. It is a full size prototype dedicated for signal detection from the double-sided microstrip sensors in the CBM environment. The self-triggering ASIC provides both timing and energy information for each incoming signal in its channels.

The chip includes 128 channels. The input current pulse from the detector is processed by the charge sensitive amplifier (CSA). The signal path is then split into a fast and a slow one (Fig. 1). The fast path includes a fast shaper with a typical shaping time of 30 ns, a discriminator and a timestamp latch. It is optimized to provide good timing resolution (<10 ns). The slow path consists of a slow shaper with the typical shaping time of 80 ns, a 5-bit flash ADC and a digital peak detecting logic. It is optimized for energy measurement and noise performance.

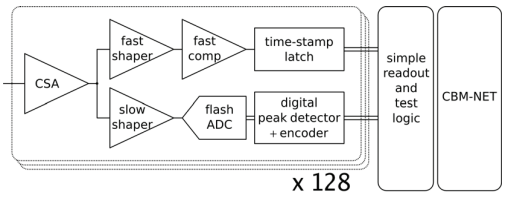

Figure 1: Block scheme of the STS-XYTER chip.

For a particle hit, each channel provides the timestamp and the ADC value corresponding to the deposited charge. Data from the channels are read out using a token-ring structure, controlled by a readout controller. The gathered data are sent out via up to four 500 Mbit/s LVDS serial data links. The data transfer to and from the chip is implemented according to the CBMnet protocol description. The HDL code of the CBMnet-related digital part was provided by ZITI, UNI-Heidelberg [1]. A simplified I2C interface allows to configure the chip without protocol overhead for test purposes. A summary of the most important parameters can be found in table 1.

The essential new feature compared to the n-XYTER architecture is an effective two level discriminator scheme. The discriminator in the fast signal lane triggers the latch of the timestamp at high timing resolution. Because of the higher bandwidth of the fast lane, the noise level and thus the noise related trigger rate is comparatively high in such a self-triggered system if the discriminator level is kept low. The noise-related trigger rate is determined by the Rice formula. If the discrimination level is kept below 3σ, noise-related hits would swamp data channels and create dead time, while if kept too high, the essential low level hits would remain undetected. The two level trigger scheme employed in the STS-XYTER adds a veto to the transmission of data in case the flash ADC has generated "zero". The discrimination level of the LSB is controlled by an internal register and effectively serves as a secondary discriminator that is exposed to the low bandwidth, low noise energy signal. This strategy makes the Rice formula applicable to the signal of the energy channel while keeping the high time resolution achieved from triggering on the fast timing channel.

Table 1: Design parameters of ASIC.

Number of channels	128 + 2 test
Pad / channel pitch	58 μm
Input signal polarity	Positive and negative
Accepted input leakage current	10 nA
ENC @ 30 pF det. capacitance	900 e-
Voltage gain in slow path	25 mV/fC
Voltage gain in fast path	71 mV/fC
ADC range	16 fC
Input clock frequency	250 MHz
Timestamp resolution	<10ns
Power consumption	<10 mV/channel
Operating temperature range	0°C < T < 40°C
Digital interface standard	4x 500 Mbit/s LVDS

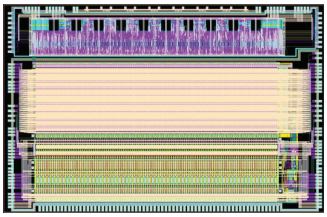

Figure 2: STS-XYTER ASIC layout.

The ASIC was designed using the UMC 180 nm process and was sent for manufacturing in October 2012. The die size is 6.5 mm x 10 mm (Fig. 2). A detector is to be connected via a Kapton cable attached to the ASIC using tab bonding. The power supply, biasing and digital interface pads are designed for wire-bonding. Particularly sensitive elements of the chip were made radiation hard.

References

[1] F. Lemke, D. Slogsnat, N. Burkhardt, U. Bruening, "A Unified DAQ Interconnection Network with Precise Time Synchronization", IEEE Transactions on Nuclear Science (TNS), Vol. 57, No. 2, 2010.

* robert.szczygiel@agh.edu.pl