RESEARCH ARTICLE

DOI: 10.34256/ijcci2123

International Journal of Computer Communication and Informatics

Design of Low Power and Area Efficient 8 Bit USR Using mGDI Technology

K.G. Dharani [a, *]

[a] Department of Electronics and Communication Engineering, Karpagam Academy of Higher Education, Coimbatore-641021, Tamil Nadu, India.

* Corresponding Author: dharani.k.g@kahedu.edu.in

Received: 19-08-2021, Revised: 04-10-2021, Accepted: 09-10-2021, Published: 30-10-2021

Abstract: Technology is growing at a faster rate after the evolution of VLSI, which mainly focuses on three major criteria-speed, area and power. All these criteria determine the compactness of a product in order to produce an efficient output at a higher rate by consuming less power. To achieve the above-mentioned factors, an efficient 8-bit Universal Shift Register (USR) has been designed using modified Gate Diffusion Input (mGDI) technique. The results have been simulated using the TANNER EDA tool and found to contribute for low power and area.

Keywords: Universal Shift Register (USR), Modified Gate Diffusion Input (mGDI) Technique, Complementary Metal Oxide Semiconductor (CMOS), Low Power and Area, Tanner Eda Tool

Introduction

In the recent days, portable electronic devices have changed the world due to its low power design. A good VLSI system should dissipate less power. Hence, the objective of VLSI is to focus on reducing the power of a device to make it even more compact. MOS devices form the major building block of most of the electronic components. Currently CMOS (Complementary Metal Oxide Semiconductor) transistor takes the advantages of low static power consumption and reduced noise immunity. In addition to these advantages, it has the lesser complexity Compared to other shift registers, USR has been recognized as the most efficient shift register due to its multi-purpose operation.

Considering the three major goals of VLSI, which is to provide a high speed, compact device with a less power consumption, an 8-bit USR has been designed which promises to give all these features. The low power technology, modified Gate Diffusion Input (mGDI) technique which is used in this paper provides guarantee to achieve the goals of VLSI. 8-bit USR has been designed and simulated based on the mGDI technique using TANNER EDA v 16.01 tool. In addition to this, the results have been compared with the conventional 8-bit USR.

The formulation of our research work is as follows: section II enhances the fundamentals of Gate Diffusion Input Technique. Section III studies the modified GDI technique. Section IV gives the overview of Universal Shift Register (USR). The simulation outcomes are examined in section V and section VI serves the conclusion

Gdi Technique

GDI stands for Gate Diffusion Input Technique. The basic GDI cell will be similar to the dual well CMOS process as shown in the Figure 1.

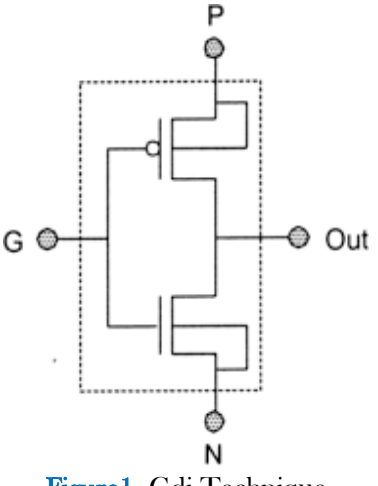

Figure1. Gdi Technique

It has three input terminals

- G- common gate input of NMOS and PMOS
- P- input to the source/drain of PMOS
- N- input to the source/drain of NMOS

The bulk terminal of PMOS and NMOS are connected to the P and N terminals respectively. Comparing to CMOS, it consumes only less power. Since the circuit design is low complex, it requires only less area. Though GDI technique is more advantageous compared to CMOS, it has its own drawbacks.

GDI faces difficulty in obtaining strong 0 and strong 1 at the output for certain combinations of input. It is difficult to manufacture in macro scale. The output voltage drop will get degraded and causes overuse of power consumption. The bulks of NMOS and PMOS are constantly connected to VDD and GND respectively which also results in high power consumption.

mGdi Technique

mGDI stands for modified Gate Diffusion Input technique. Figure 2 formation of mGDI cell from GDI cell.

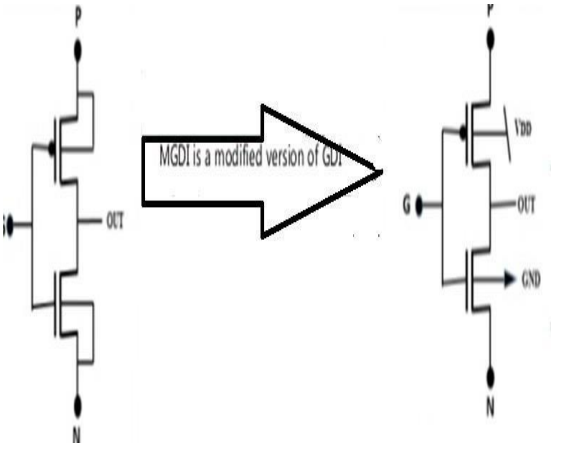

Figure 2. Formation of mGdi Cell from Gdi Cell

The PMOS transistor bulk node is connected to the VDD which is referred as the high constant voltage. The NMOS transistor bulk node is connected to the GND which is referred as the low constant voltage. The complete structure of mGDI cell in the Figure 3.

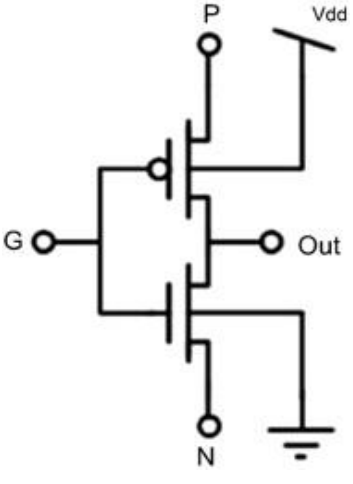

Figure 3. mGdi Technique

Compared to static CMOS gate, mGDI cell provides considerable reduction of both sub-threshold and gate leakage. They can be implemented with all current CMOS process. This technique promises to provide improved swing degradation. Since the silicon area is very much reduced compared to other conventional methods, the top down design approach is very simple and easy. The leakage power and the switching power have been lowered. Due to these properties, it consumes less power and delivers high speed.

USR

USR stands for Universal Shift Register. The major types of shift registers are Serial Input Serial Output (SISO) shift register, Parallel input Parallel Output (PIPO) shift register, Serial Input Parallel Output (SIPO) shift register and Parallel input Serial Output (PISO) shift register. USR alone will perform all these operations based on the select inputs. These operations are shift left, shift right and parallel load operations as shown in the Table 1.

Table 1. Register Operation of Usr

S1	S0	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

The block diagram of USR is shown in the Figure 4. The major blocks are multiplexer and D flip flop.

Multiplexer is used to select the register operation. D flip flop assists in storing the value.

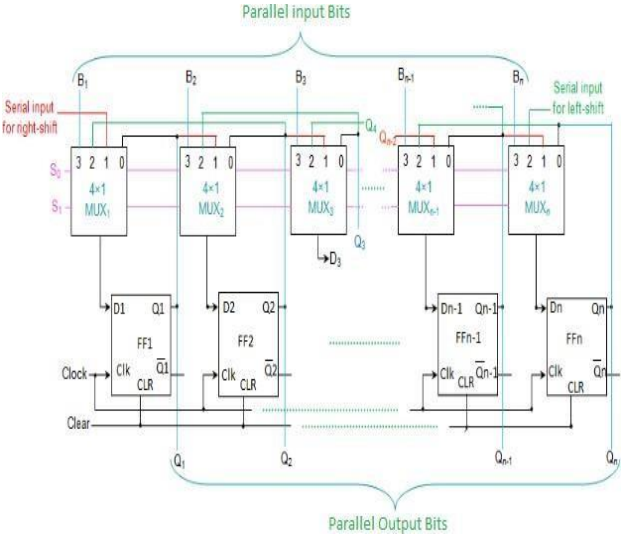

Figure 4. Universal Shift Register (Usr)

The CMOS design of conventional multiplexer is shown in Figure 5.

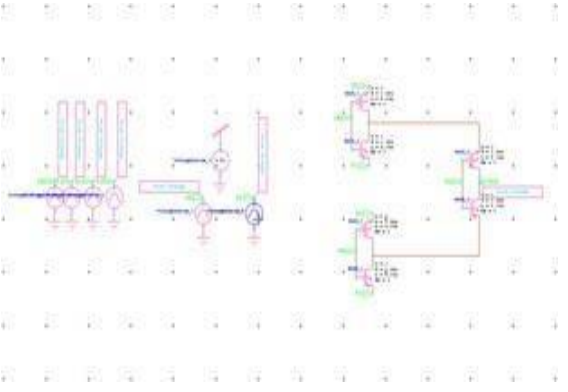

Figure 5. Schematic of Conventional Multiplexer

The CMOS design of mGDI based multiplexer is shown in Figure 6.

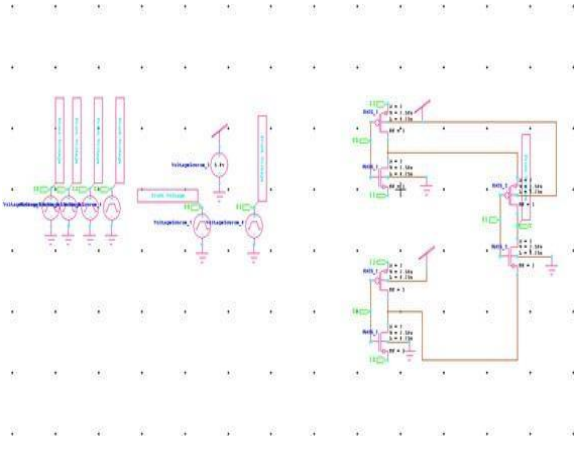

Figure 6. Schematic of mGdi Based Multiplexer

The CMOS design of conventional D flip flop using NAND gate is shown in Figure 7.

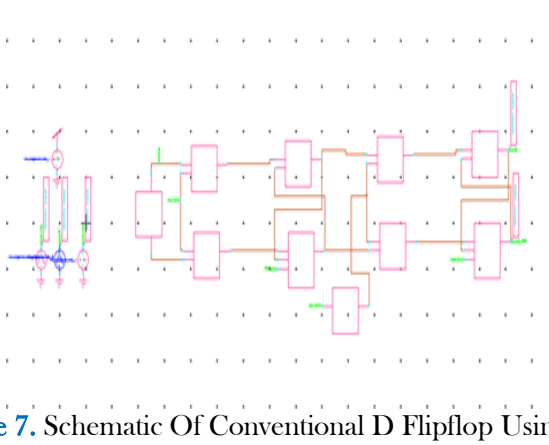

Figure 7. Schematic Of Conventional D Flipflop Using Nand Gate

The CMOS design of mGDI based D flip flop using NAND gate is shown in Figure 8.

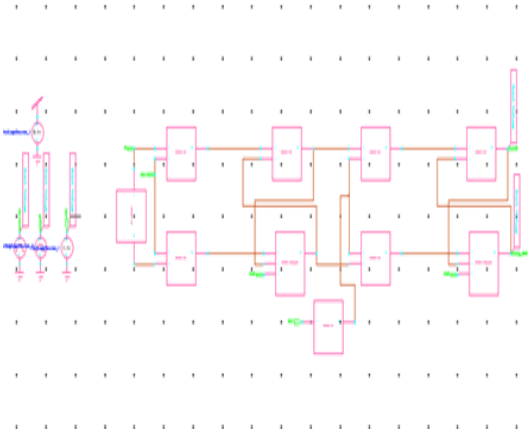

Figure 8. Schematic of mGdi Based D Flipflop Using Nand Gate

The CMOS design of conventional 8 bit USR is shown in Figure 9.

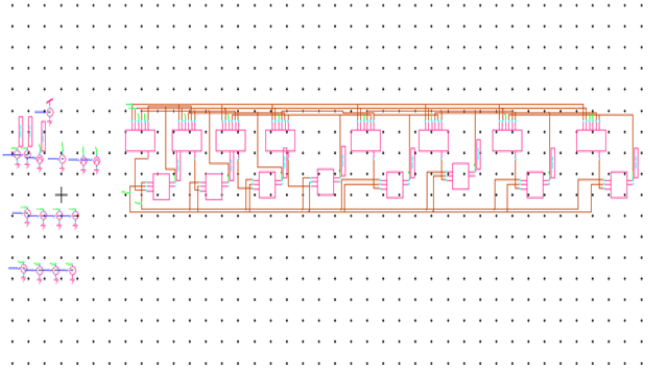

Figure 9. Schematic of Conventional 8 Bit Usr

The CMOS design of mGDI based 8 bit USR is shown in Figure 10.

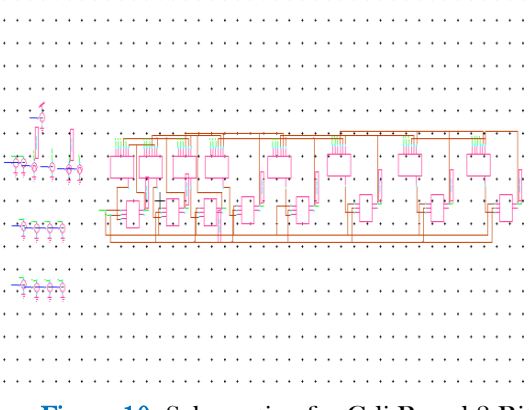

Figure 10. Schematic of mGdi Based 8 Bit Usr

Results

The simulation result of conventional multiplexer is shown in Figure 11.

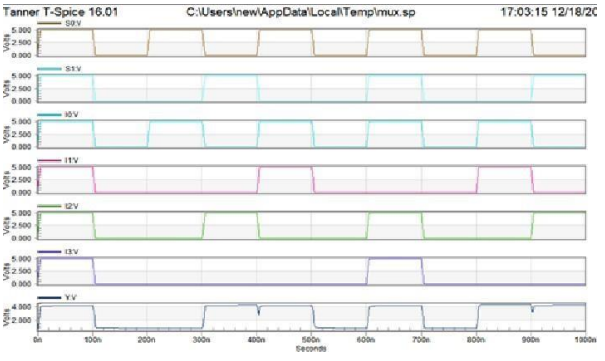

Figure 11. Outwave Of Conventional Multiplexer

The simulation result of mGDI based multiplexer is shown in Figure 12.

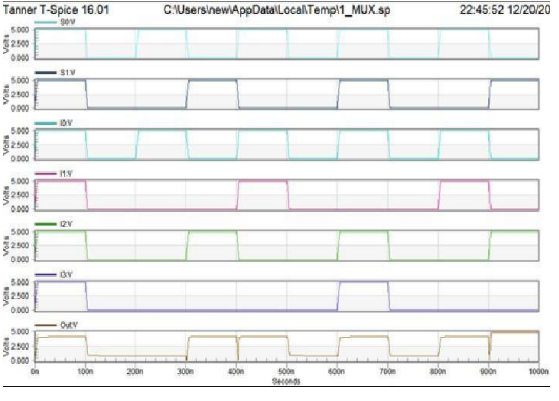

Figure 2. Output Wave of mGdi Based Multiplexer

The simulation result of conventional D flip flop using NAND gate is shown in Figure 13.

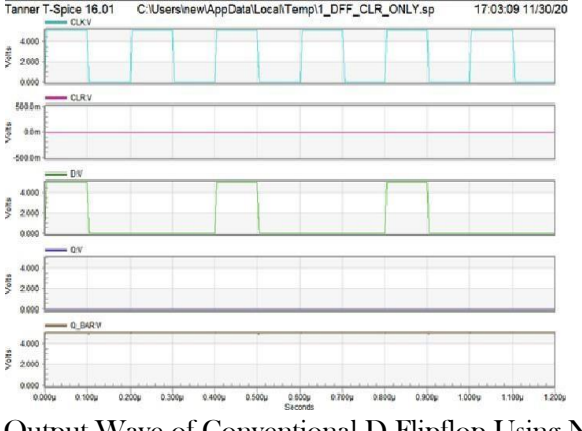

Figure 13. Output Wave of Conventional D Flipflop Using Nand Gate

The simulation result of mGDI based D flip flop using NAND gate is shown in Figure 14.

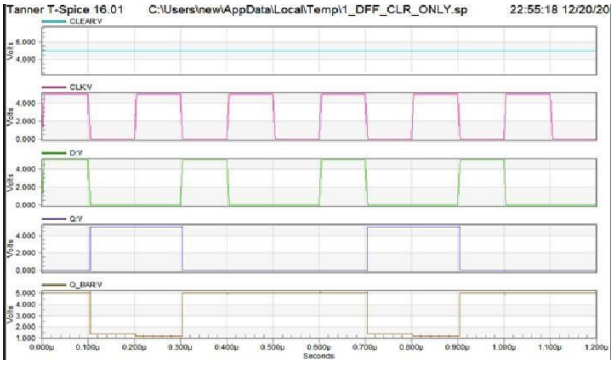

Figure14. Output Wave of Mgdi Based D Flipflop Using Nand Gate

The simulation result of conventional 8 bit USR when S1S0=10 (SHIFT LEFT) is shown in Figure 15.

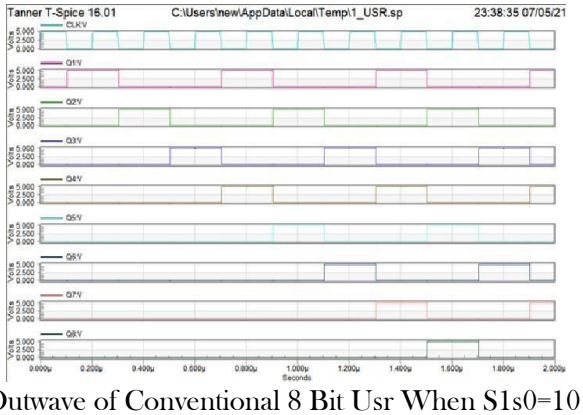

Figure 15. Outwave of Conventional 8 Bit Usr When S1s0=10 (Shift Left)

The simulation result of mGDI based 8 bit USR when S1S0=10 (SHIFT LEFT) is shown in Figure 16.

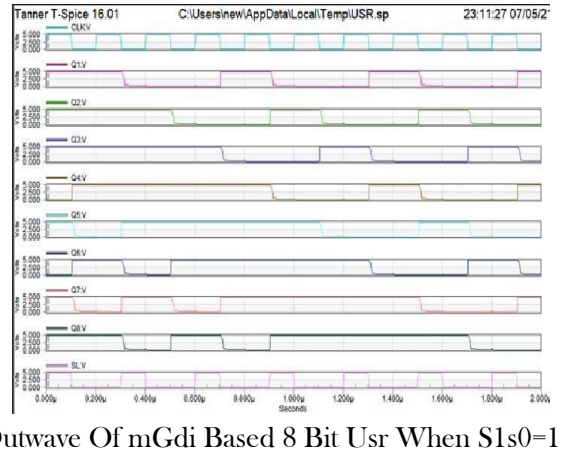

Figure 16. Outwave Of mGdi Based 8 Bit Usr When S1s0=10 (Shift Left)

Table 2. shows comparison of various logic circuit design using conventional and mGDI technique.

Table 2. Comparision Of Conventional And Mgdi Technique

No.of. Transistors		Power		Time		
Normal		MGDI	Norm Al	MGDI	Norm Al	MGDI
Multi Plexe R	67	6	29.01mw	27.52mw	1.73s	1.30s
D Flip Flop	40	40	843.6mw	390.7mw	1.44s	1.86s
4 Bit Usr	428	184	115.8 Mw	107.3 Mw	4.64s	2.48s
8 Bit Usr	560	368	664.4mw	663.2mw	13.76s	12.92s

Conclusion

In this paper, USR has been designed using conventional and modified GDI techniques. They are simulated in TANNER v16.0 EDA tool and the results have compared. From the result, it is clear that the mGDI technique helps in reduction of number of transistors used (Area), reduction of power dissipation and increases the speed. These three are the important parameters to be considered in the VLSI design. Thus the above stated mGDI technique prove to be efficient in all of its ways.

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Funding

No funding was received for conducting this study.

Conflict of interest

The Author has no conflicts of interest to declare that they are relevant to the content of this article.

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