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High-Temperature Annealing and Patterned AlN/Sapphire Interfaces

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Using the example of epitaxial lateral overgrowth of AlN on trench-patterned AlN/sapphire templates, the impact of introducing a high-temperature annealing step into the process chain is investigated. Covering the open surfaces of sapphire trench sidewalls with a thin layer of AlN is found to be necessary to preserve the trench shape during annealing. Both the influence of annealing temperature and annealing duration are investigated. To avoid the deformation of the AlN/sapphire interface during annealing, the annealing duration or annealing temperature must be low enough. Annealing for 1 h at 1730 °C is found to allow for the lowest threading dislocation density of $3.5 \times 10^8\,cm^{-2}$ in the subsequently grown AlN, while maintaining an uncracked smooth surface over the entire 2 in. wafer. Transmission electron microscopy study confirms the defect reduction by high-temperature annealing and reveals an additional strain relaxation mechanism by accumulation of horizontal dislocation lines at the interface between annealed and nonannealed AlN. By applying a second annealing step, the dislocation density can be further reduced to $2.5 \times 10^8\,cm^{-2}$.

1. Introduction

AlN of high crystalline quality is used as substrate material for many AlGaN-based electronic and optoelectronic devices. In particular, ultraviolet C (UVC) light-emitting diodes (LEDs) emitting in the spectral region between 200 and 280 nm with their wide range of applications such as disinfection of surfaces, water purification, and gas sensing are usually grown by metalorganic vapor-phase epitaxy (MOVPE) on AlN/sapphire templates to avoid expensive AlN bulk substrates.[1–4] The UVC LED devices require a low threading dislocation density (TDD) and smooth surface morphology of the underlying AlN to realize a narrow emission peak, high internal efficiency, and long lifetime.[5–10]

A low TDD can be achieved by epitaxial lateral overgrowth (ELO) of AlN on trench-patterned AlN/sapphire templates. This process allows a TDD reduction down to $5 \times 10^8\,cm^{-2}$.[10,11] For such ELO AlN, it was found that on one hand with decreasing sapphire surface off-cut angle, macro steps on the ELO AlN surface can be avoided but on the other hand the TDD increases with decreasing off-cut angle.[12] Another way to achieve low TDD down to $4.7 \times 10^8\,cm^{-2}$ in MOVPE grown AlN with layer thickness $< 1\,\mu m$ on planar sapphire is to apply high-temperature annealing (HTA) after layer growth.[13] Hence, ELO of AlN and growth of thick AlN layers to realize a low TDD are not absolutely necessary. However, for devices such as UV LEDs, it is advantageous to have a patterned interface between AlN and sapphire to improve the light extraction.[14–16] Therefore, the combination of HTA and a patterned AlN/sapphire interface is desirable. Only a few publications so far deal with the combination of both techniques showing that crack-free, smooth AlN surfaces with TDD down to $6.4 \times 10^8\,cm^{-2}$ can be realized.[17,18]

Our group has years of experience with ELO of AlN on trench-patterned AlN/sapphire templates. Furthermore, we have already shown the improvement of the light output power and lifetime of UVC LEDs by introducing an HTA step into the ELO AlN template fabrication.[7,19] As recently mentioned in our review article, combining ELO growth and HTA in a certain way can reduce the TDD down to $3.5 \times 10^8\,cm^{-2}$.[20] In this study, we therefore give a deeper insight into the combination of HTA and MOVPE ELO growth on trench-patterned AlN/sapphire.

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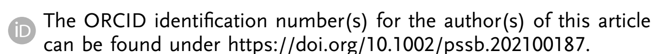
The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/pssb.202100187.

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DOI: 10.1002/pssb.202100187

2. Experimental Section

2.1. AlN Growth and High-Temperature Annealing

As substrate material 2-in. diameter sapphire substrates with a nominal offcut of 0.1° toward an m-plane were used. AlN was grown in an AIX2400G3HT production scale planetary MOVPE reactor using trimethylaluminum and ammonia as precursors. All layers were grown at a total pressure of 50 mbar with

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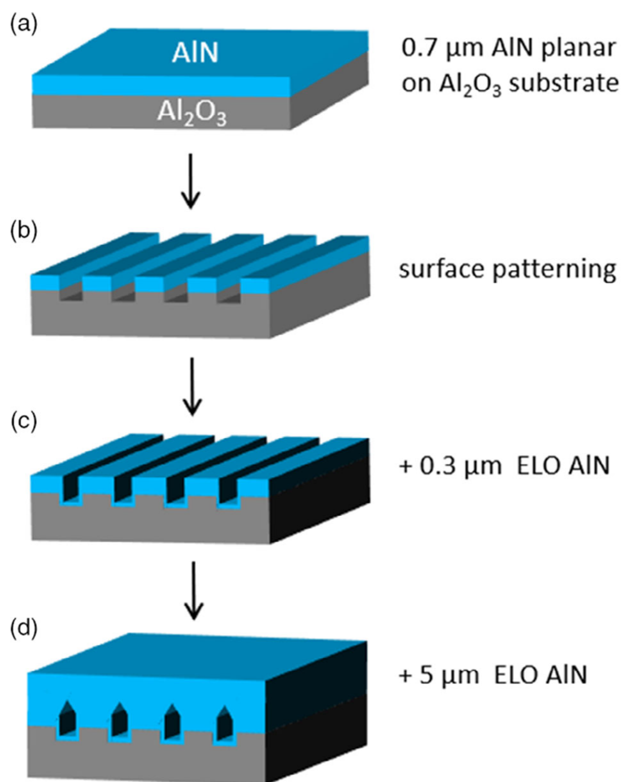

Figure 1. Schematic representation of the three steps to produce an ELO template. Panels (a–d) indicate the different stages at which the impact of an HTA step was investigated: a) Introducing HTA to the planar AlN layer before surface patterning, b) after surface patterning, c) as an intermediate step during ELO after 0.3 µm MOVPE growth (surface not planar), and d) after completed growth of the planarized ELO AlN layer.

hydrogen as the only carrier gas. For realizing an ELO template, first, planar AlN was grown with a layer thickness of 0.7 µm on sapphire (**Figure 1**).[21] Second, the AlN/sapphire layer stack was patterned by photolithography and dry etching to create trenches and ridges running along the AlN [10–10] direction ([11–20] direction in sapphire) with a pitch of 3.5 µm. Then, 5.3 µm ELO AlN was grown to achieve coalescence over the trenches. Hereby, the first 1.7 µm were grown at a group V/III ratio of 250 at 1250 °C while the residual part was grown at a group V/III ratio of 30 at 1180 °C.

To investigate the most effective way of combining ELO and HTA processes the HTA step was applied at different stages of the ELO process (shown in Figure 1). For HTA, the samples were covered with a planar AlN/sapphire template and heated in a LORA HTMReetz furnace up to 1730 °C at a pressure of 1000 mbar in N_2 environment. **Figure 2**a shows schematically how the samples were placed in the furnace based on the face-to-face configuration published by Miyake et al.[22] Fragments of a 100 µm thick sapphire wafer were used as spacers at the wafer edges. By these spacers, bonding of the sample to the cover wafer during annealing can be avoided. Figure 2b shows the furnace temperature T_{HTA} plotted against time as an example for annealing at $T_{HTA} = 1690$ °C and a heating duration T_{HTA} of 3 h. Different annealing temperatures and annealing durations were applied for the most efficient ELO–HTA combination.

2.2. Characterization Methods

To investigate the structural and morphological material properties, X-ray diffraction (XRD), transmission electron microscopy (TEM), scanning electron microscopy (SEM), atomic force microscopy (AFM), and defect selective etching (DSE) have been applied. For measuring ω-rocking curves, a Philips X'Pert MRD Pro X-ray diffractometer with 1° acceptance angle on the detector side was used. High resolution XRD (HRXRD) measurements to determine lattice constants were carried out using a Malvern Panalytical X'Pert^3 system with a triple axis configuration on the detector side. Both X-ray diffractometers are equipped with a fourfold 220 Ge monochromator and a 0.5 mm × 5 mm aperture on the source side. To image the AlN/sapphire interface, SEM was used in conjunction with energy-dispersive X-ray spectroscopy (EDX). Scanning transmission electron microscopy (STEM) under annular dark field (ADF) conditions was applied to visualize material defects in AlN. An alkaline metal hydroxide melt was used for DSE of the AlN surfaces to determine the TDD by counting the etch pits on a 10 µm × 10 µm surface area. In the following, properties of the investigated samples are repeatedly compared in the center and at the edge of 2 in. diameter wafers. The specification "edge" refers in each case to a measuring position at a distance of 5 mm from the wafer edge.

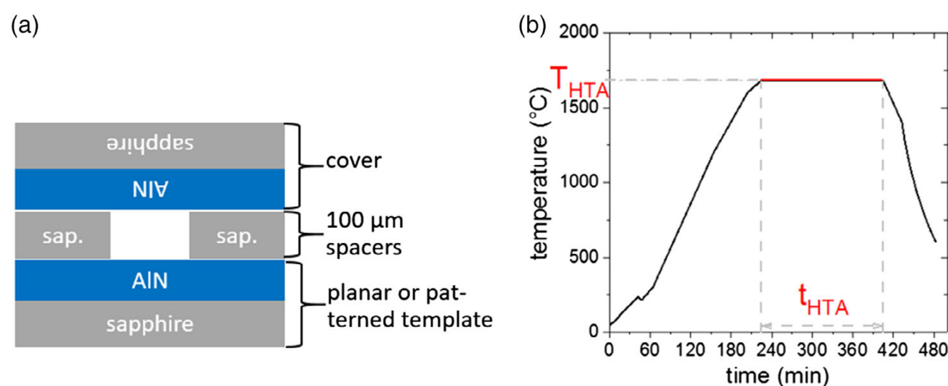

Figure 2. a) Schematic cross section of the sample arrangement during HTA. b) Temperature curve during typical heating in the HTA furnace.

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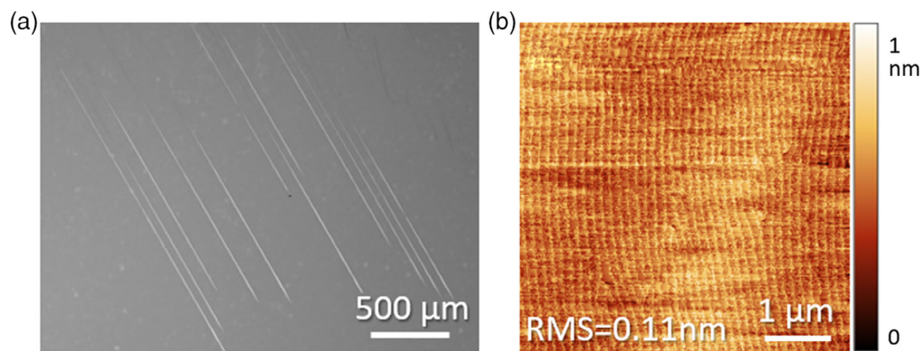

Figure 3. a) Light microscopy surface image of a 0.7 µm thick AlN layer after HTA. b) AFM surface topogram of the fully grown 6 µm thick ELO AlN based on an annealed HTA AlN/sapphire template.

3. Results and Discussion

3.1. Introduction of HTA at Different Stages of the ELO AlN Template Process

The different stages in which HTA was conducted to examine its impact on ELO AlN templates are shown in Figure 1a–d. In the first approach (a), HTA was applied after deposition of a smooth, crack-free 0.7 µm MOVPE–AlN layer. For such a planar AlN layer annealing at 1680 °C for 3 h decreases the XRC–FWHM of the 102 reflection from 960 to 400 arcsec while the XRC–FWHM of the 002 reflection is decreased from 80 to 60 arcsec. This shows the improvement in material quality, which is typical for the HTA process, by reducing the degree of twist and tilt of crystal regions against each other.[13] During MOVPE growth, the AlN layer is grown under tensile in-plane strain.[21] Furthermore, the in-plane thermal expansion coefficient of sapphire is about a factor of 2 higher than for AlN.[23] Hence, by heating up the AlN layer to temperatures higher than the growth temperature, the sapphire substrate is inducing additional tensile strain on the AlN layer. As a result, the AlN layer tends to crack during HTA starting from the substrate edges **(Figure 3a)**. However, after substrate patterning and AlN ELO, the resulting 6 µm thick layer exhibits a smooth surface with a root mean square (RMS) roughness value of 0.11 nm in the regions which were not affected by the initial cracking of the planar layer (Figure 3b). XRC–FWHM of 150 arcsec for the 002 and 370 arcsec for the 302 reflection were determined in the wafer center. Such templates have already been demonstrated as basis for UVC LEDs with 20% higher output power than on conventional ELO templates without any HTA step. This is attributed to the improved material quality. However, the cracking drastically lowers the yield and makes device processing difficult.[19]

To master the challenge of unwanted layer cracking, it seems useful to pattern the surface before HTA to decrease the tensile stress in the AlN at high temperature (shown in Figure 1b). An already patterned AlN/sapphire template was therefore annealed at 1685 °C for 1 h. A shorter time of 1 h was chosen, since the patterned AlN/sapphire with the open sapphire sidewalls is expected to be less thermally stable. After completed overgrowth, the sample shows a smooth AlN surface in the center with an RMS roughness of 0.19 nm (**Figure 4**a), but a rough surface covered with hexagonal plateaus and macro steps in the edge region of the 2-inch wafer (Figure 4b). The underlying AlN/sapphire interface was investigated in more detail by SEM on the cross-section of the sample. Compared with the wafer center (Figure 4c), the wafer edge (Figure 4d) shows a flattening of the trench walls resulting in a triangular rather than rectangular cross-section of the trench. Furthermore, the MOVPE–AlN growth after annealing is disturbed, as evidenced by the clearly visible interface, for which the contact to the further grown AlN layer is partially missing (shown by the white arrow in Figure 4d). Probably, during annealing oxygen is emitted from the etched sapphire sidewalls which leads to partial oxidation of the AlN ridges. A reduced stabilization of the wafer surface accompanied by Al(O,N) formation in the edge region of 2 in. wafers has already been observed for the high-temperature annealing of sputtered AlN/sapphire templates.[24] The formed Al(O,N) areas then act as mask and disturb the subsequent AlN growth. This effect of surface roughening and interface degradation was found to occur at the wafer edge for ELO AlN even if a lower HTA temperature of only 1560 °C was used.

Deposition of an AlN layer thick enough to protect the sapphire sidewalls but thin enough not to coalesce the AlN above the trenches seems to be necessary. AlN (0.3 µm) have already been successfully used by our group for HTA of AlN on nano-patterned sapphire.[18] Therefore, this approach was also introduced for the trench pattern studied here (shown in Figure 1c). After deposition of the additional 0.3 µm thick AlN layer on the patterned template and subsequent HTA at 1690 °C for 1 h the patterned template with now protected sidewalls was further overgrown until the total layer thickness of 6 µm was reached. The AlN surface of this layer is atomically smooth over the entire 2 in. wafer with RMS values of 0.16 nm, as shown by the AFM topograms in **Figure 5**a (wafer center) and b (wafer edge). Unlike growth without covering the sapphire trench walls (Figure 4d), for this sample the pattern of the AlN/sapphire interface is not affected by the HTA step (Figure 5c,d). The XRC–FWHM of the 002 and 302 reflection in the wafer center were 140 and 370 arcsec, respectively.

The fourth approach, shown in in Figure 1d, is to anneal after the 6 µm ELO AlN layer is fully grown. For this purpose, the corresponding sample was annealed at 1690 °C for 1 h. As result, the relatively thick, coalesced AlN cracks completely

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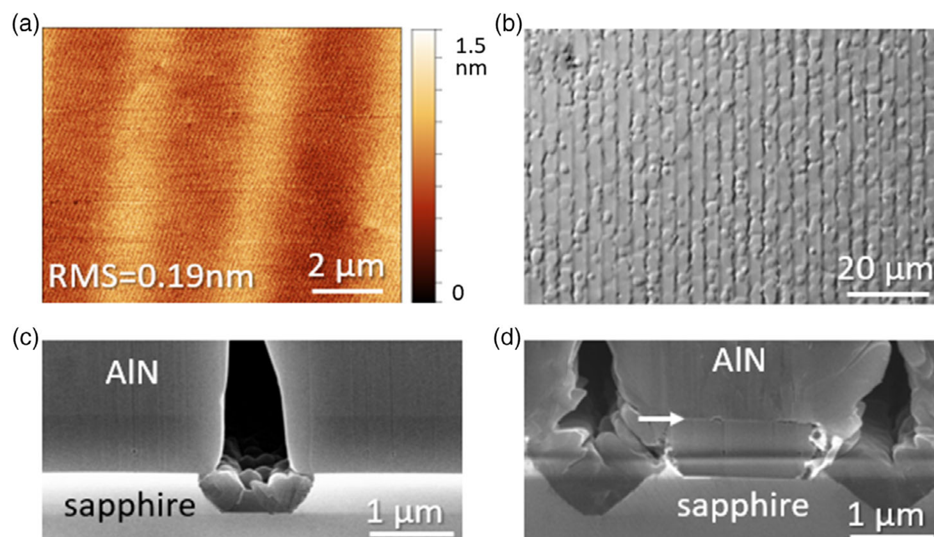

Figure 4. a) AFM surface topogram of 6 μm ELO AlN grown on a high-temperature annealed trench pattern taken in the 2-in. wafer center and b) Nomarski light microscopy surface image taken in the edge region. c,d) Cross-section SEM images showing the AlN/sapphire interface in the c) center and d) edge region. Arrow in (d) marks the interface between seed layer after HTA and MOVPE ELO layer with voids due to local growth inhibition.

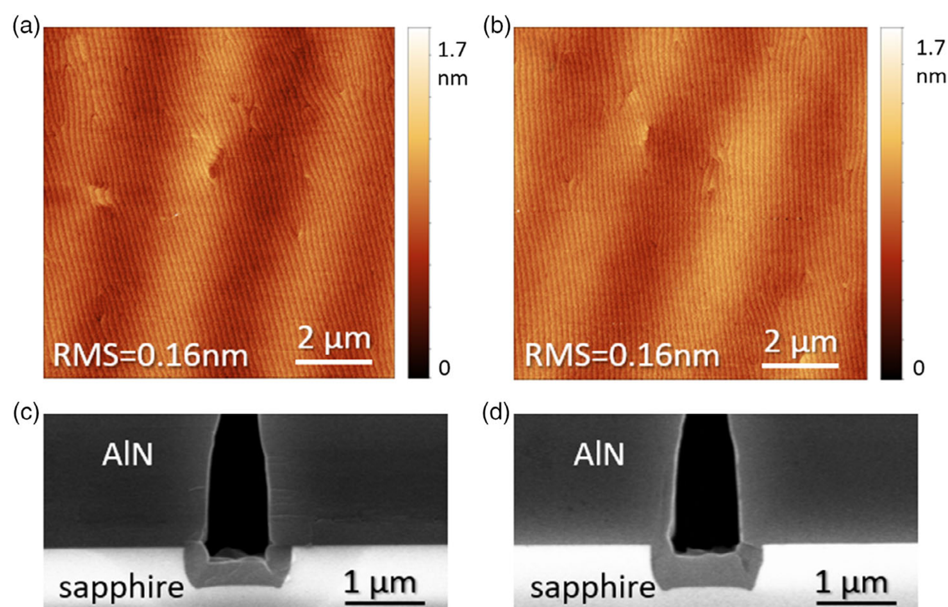

Figure 5. AFM surface topograms taken in a) the center and b) edge region of 6 μm ELO AlN grown on trench patterned AlN/sapphire with intermediate HTA after covering the sapphire sidewalls of the trenches with AlN. Cross-sectional SEM images showing c) the center and d) edge region.

due to the thermal stress during the HTA step. The approach is therefore not suitable to combine HTA and patterned interfaces.

Table 1 shows the results of the different HTA and ELO combinations presented in this section. The TDD estimated from the XRC-FWHM in the wafer center for approach (a), (b), and (c) were in the range of 8–9 × 10^8 cm^{-2} and thus up to a factor of 2 lower compared with ELO AlN templates without HTA.[19,25] Regarding the surface morphology of the completed 6 μm ELO AlN layer over the entire 2-in. substrate, only the procedure (c) was successful. Therefore, this approach was investigated in more detail with respect to the influence of annealing temperature and annealing duration as described in the following.

3.2. Annealing Temperature and Annealing Duration Impact on AlN ELO Templates

In the case of planar AlN layers, increasing the annealing temperature leads to a decrease in TDD.[13] To investigate the influence of the annealing temperature on AlN ELO, HTA was carried

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Table 1. Overview of XRC–FWHM, TDD_{XRC} and surface morphology of 6 μm thick AlN ELO layers with HTA introduced at different steps as shown in Figure 1a–d.

HTA at step...	XRC-FWHM 002[a)] [arcsec]	XRC-FWHM 302[a)] [arcsec]	TDD_{XRC} [cm^{-2}]	Surface morphology on 2 in. wafer
Figure 1(a)	150	370	9×10^8	Center smooth, cracked edge region
Figure 1(b)	150	350	8×10^8	Center smooth, rough edge region
Figure 1(c)	140	370	9×10^8	Atomically smooth, crack-free
Figure 1(d)	–	–	–	Completely cracked
Without HTA (Conventional)[19]	140	470	15×10^8	Atomically smooth, crack-free

a)Measured in wafer center.

out at temperatures between 1650 and 1730 °C for 1 h at step (c) of the ELO process chain (Figure 1). For comparison, a sample was treated in the same way but without HTA after growth of the first 0.3 μm AlN on the patterned template. The resulting 6 μm thick films all show an atomically smooth surface in the center and edge regions of the 2 in. wafers, comparable to the sample annealed at 1690 °C (Figure 5a,b). RMS roughness values determined from $10 \times 10\,\mu m^2$ AFM surface topograms are in the range of 0.12–0.20 nm (Figure S1, Supporting Information). Especially for layers with low TDD wing tilt can become one of the main broadening mechanisms for XRC.[26–28] Hence, the TDD value calculated from the XRC–FWHM usually overestimates the actual one. DSE was therefore applied to determine the TDD more precisely. In this process, the sample surface is etched to form etch pits at the penetration points of dislocations as shown in the SEM image in **Figure 6**a for the sample with HTA at 1730 °C. The etch pit density (EPD) is equivalent to the TDD (hereafter referred to as TDD_{DSE}). Small pits correspond to pure edge type dislocations while for the larger ones the pit diameter increases with increasing screw component of the underlying threading dislocation.[29] Since very large etch pits can overlap smaller ones, when large etch pits occurred, the corresponding area was excluded from the etch pit density determination. The orientation of the overgrown trenches can still be seen due to lining up of dislocations along the trench direction (indicated by the white arrow in Figure 6a). At lower annealing temperatures of 1650 and 1670 °C the TDD is about 11×10^8 cm^{-2} and hence, as high as for the ELO template without HTA step (Figure 6b). For HTA temperatures of 1690 °C and higher, a decrease in the TDD with increasing temperature down to $3.5 \times 10^8\,cm^{-2}$ can be observed. Higher annealing temperatures than 1730 °C were not tested to protect the furnace equipment. To obtain an estimate of how accurate it is to count the dislocations after DSE on a $10 \times 10\,\mu m^2$ area, five different $10 \times 10\,\mu m^2$ areas were counted for the HTA ELO sample annealed at 1715 °C. This gave a mean etch pit density of 4.7 cm^{-2} with a sample variance of 6%. From this it can be deduced that a relatively accurate value of the dislocation density can be determined by counting on a surface area of $10 \times 10\ \mu m^2$.

Hence, to reach a lower TDD, the previously described experiment was also performed at 1690, 1710 and 1730 °C for 3 h. For all three temperatures, TDD_{DSE} of about $4 \times 10^8\,cm^{-2}$ is achieved (Figure 6b). Consequently, a high annealing temperature is not absolutely necessary to reach the low TDD. This experiment also shows that for an annealing temperature of 1730 °C the TDD cannot be further decreased by increasing the annealing duration from 1 to 3 h. In addition, the sample annealed at 1730 °C for 3 h exhibits an increased surface roughness in the edge region (inset of Figure 6b) with up to 50 nm high steps

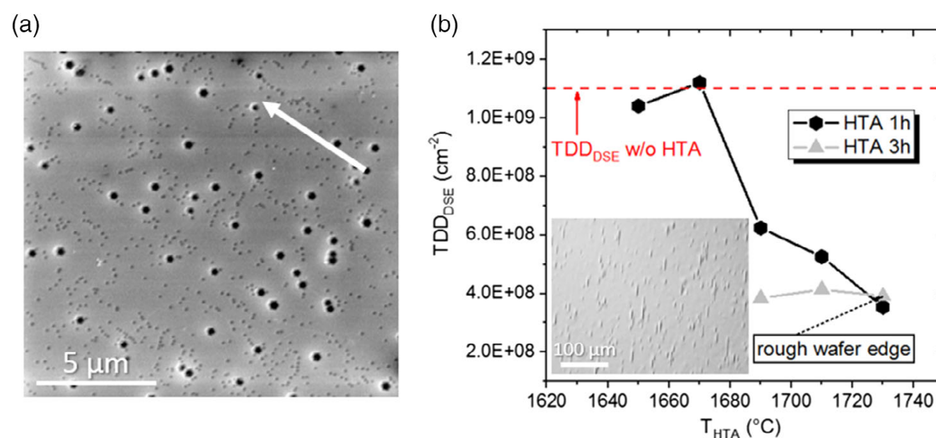

Figure 6. TDD determined by defect selective etching (TDD_{DSE}) of the AlN surface. a) Exemplary SEM image of the etched surface of the sample annealed at 1730 °C. The white arrow indicates the direction of the buried trench. b) TDD_{DSE} plotted against annealing temperature (T_{HTA}) with dashed line indicating TDD_{DSE} for the sample without HTA. Inset in (b) shows a Nomarski light microscopy image indicating surface disturbance at the wafer edge of the sample treated by HTA at 1730 °C for 3 h. Reproduced with permission.[20] Copyright 2020, Wiley-VCH.

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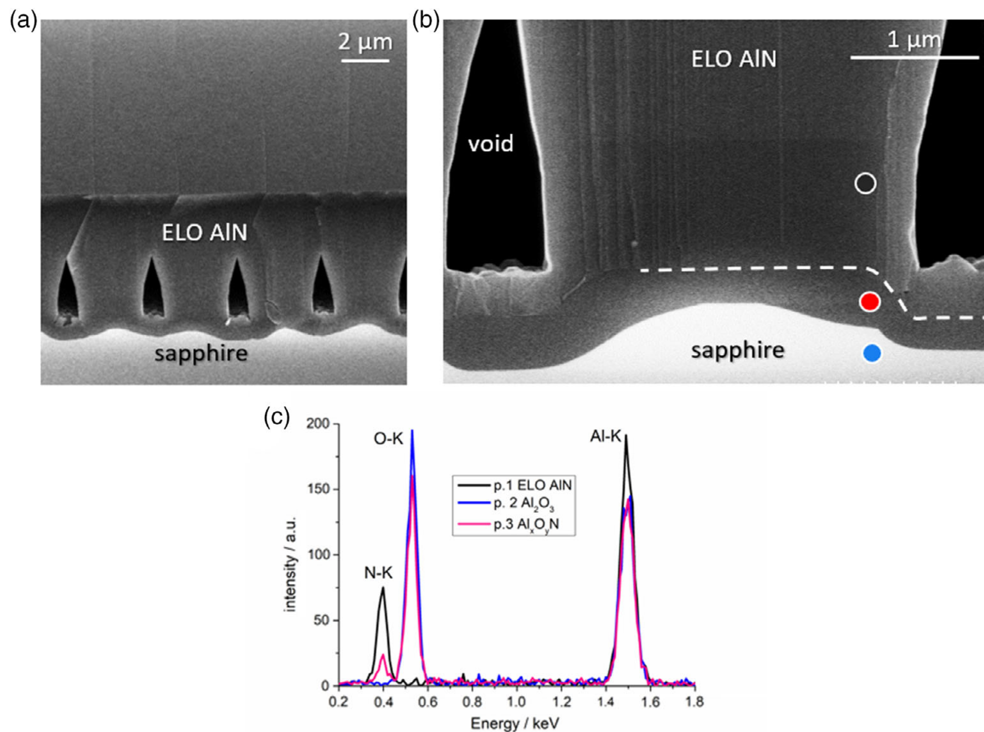

Figure 7. a) Bird's eye view on the cross section and surface of an ELO template with intermediate HTA at 1730 °C for 3 h. The shape of the AlN/sapphire interface is wavy. b) At higher magnification, a layer showing contrast to AlN can be found covering the sapphire (partly indicated by the dashed line). Circles in (b) indicate positions from where c) EDX spectra were taken.

running parallel to the underlying trench direction. The disturbed surface morphology suggests that despite the 0.3 µm AlN cover, the surface pattern was damaged during HTA. The corresponding SEM cross sections in **Figure 7**a and b clearly show that the interface between AlN and sapphire is strongly rounded and irregular in the edge region. An up to 500 nm thick layer can be seen directly on the sapphire (Figure 7b). A closer investigation by EDX measurements (Figure 7c) shows the presence of aluminum, oxygen, and nitrogen in this layer. Accordingly, Al_xO_yN is formed at the interface between sapphire and AlN by the solid phase reaction of AlN and sapphire at high temperature.[24] Most likely the deformation of the AlN/sapphire interface leads to slightly tilted ridges and therefore to step formation during coalescence of the ELO AlN.

It is known that both planar AlN on sapphire and AlN on patterned sapphire take on a smaller a-lattice constant through HTA than before annealing.[18,30,31] This is caused by the relaxation of the AlN at high temperatures and the compressive stress arising during cooling to room temperature.[32] Consequently, assuming biaxially strained AlN, the higher the annealing temperature, the larger the c-lattice constant. To investigate the impact of the annealing temperature on the in-plane strain ε_{xx} of HTA AlN ELO templates, the samples with intermediate HTA for 1 h were examined by HRXRD. The 004 *2θ* peak position was measured to access the c lattice constant from Bragg's law. From the c lattice constant, the out-of-plane strain can be calculated.

$$\varepsilon_{zz} = \frac{c_0 - c}{c} \quad (1)$$

with $c_0 = 0.4982\,\text{nm}$ being the natural c lattice constant of unstrained AlN.[33] Under the assumption of a biaxially strained lattice the in-plane lattice strain can be determined.

$$\varepsilon_{xx} = \frac{\frac{E}{2\nu} + C_{13}}{C_{11} + C_{12}} \varepsilon_{zz} \quad (2)$$

with Young's modulus $E = 308\,\text{GPa}$, Poisson's ratio $\nu = 0.179$[34] and the elasticity constants $C_{11} = 396\,\text{GPa}$, $C_{12} = 137\,\text{GPa}$, $C_{13} = 108\,\text{GPa}$.[35] The c lattice constants and the calculated in-plane strain are plotted in **Figure 8** against T_{HTA}. The higher the annealing temperature, the higher the compressive strain in the fully grown AlN ELO layer. This shows that despite the ELO at least a part of the compressive strain introduced during HTA is retained during subsequent MOVPE AlN growth.[22,32]

To gain insight into the propagation of threading defects in the ELO AlN layers cross-sectional ADF-STEM measurements were performed. It should be noted that an STEM lamella for cross-section investigation is only about 200–250 nm thick, which restricts the use of this technique for quantitative analysis of defect densities at least for the TDDs in the order of magnitude of $10^8\,\text{cm}^{-2}$. From the etch pit distribution in Figure 6a, it can be seen that the number of dislocations in such thin STEM cross-section images will strongly depend on the observation position. However, cross-sectional STEM analysis can reveal the mechanisms responsible for the defect formation as well as for their annihilation. **Figure 9** shows ADF-STEM images in which all kinds of dislocations are visible simultaneously. Dislocations that run to the AlN surface originate largely from the initial AlN

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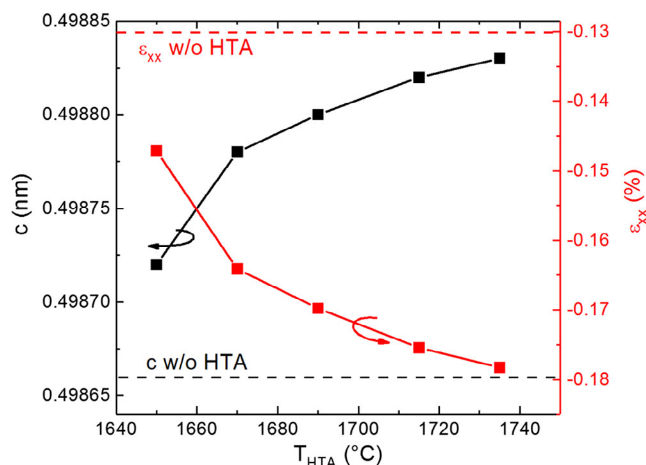

Figure 8. *c* lattice constant and the corresponding in-plane lattice strain for 6 µm thick ELO AlN plotted against temperature of the intermediate HTA step.

nucleation on the ridges. However, threading dislocations can be also formed above the trenches during coalescence when adjacent twisted and tilted ELO wing crystal regions coalesce (black arrow on the left, Figure 9a). In addition, there is a high number of nearly horizontal defects, especially in the plane of coalescence (white arrow in Figure 9a), but also within the bulk material (area circled by dashed line). The formation of these defects is attributed to relaxation of strain accumulated during the growth of the 6 µm thick AlN layers.

A closer investigation of the region above a ridge (Figure 9b) clearly shows that only a few threading dislocations can be found in the 1 µm thick, annealed material on top of the ridges. Many dislocation lines are bent toward voids inside the AlN due to the attractive image forces that become significant in the presence of the open surface of the voids (Figure 9b(I)). These voids are formed during the high-temperature annealing. Due to the open surface of the voids, dislocations become pinned to them. Thus, their vertical propagation direction can change, but the climbing through the AlN ridge during HTA becomes hindered. Above the ridge in Figure 9b the interface between HTA AlN and subsequently grown AlN is clearly visible as indicated by (II). Here several dislocation lines are bent out of their original vertical direction due to the compressive AlN growth on HTA AlN.[18,36] Some of the dislocations which change direction at the HTA/ELO–AlN interface annihilate during further growth (Figure 9b(III)).

Furthermore, many horizontal dislocation segments are visible at this interface, similar to the plane of the coalescence (see the white arrow in Figure 9a). The reason for this dislocation accumulation effect is unclear. From our numerous studies of differently strained planar AlN layers, it can be assumed that compressive growth might create dislocation half-loops that migrate through the material down until they reach the interface between HTA AlN and non-HTA AlN. This is an interesting relaxation process which requires a further systematic study.

3.3. Second Annealing to Further Improve the Material Quality

The more compressively strained AlN due to the introduction of HTA in step (C) in Figure 1 also opens the possibility to apply HTA to the fully grown 6 µm thick ELO–AlN template without layer cracking. For this purpose, samples were prepared as described in the previous section using $T_{HTA} = 1730\,°C$ for 1 h after covering the patterned AlN/sapphire template by a 0.3 µm thick AlN layer. After the completed overgrowth these samples then underwent HTA a second time, one sample at 1730 °C for 1 h and the other one for 5 h. The resulting AlN surfaces are crack-free and smooth with RMS values of about 0.2 nm (**Figure 10**a,b). The TDD_{DSE} (Figure 10c,d) is further reduced from $3.5 \times 10^8\,cm^{-2}$ without second HTA to $2.7 \times 10^8\,cm^{-2}$ and $2.5 \times 10^8\,cm^{-2}$ with second HTA for 1 h and 5 h, respectively. The dislocation density after 5 h is similar to that after 1 h. The sample surfaces after DSE in Figure 10c,d show lining up of dislocations as exemplarily indicated by dashed lines. Probably this is caused by pinning of dislocations to surface steps, which restricts dislocation movement and therefore annihilation in AlN.

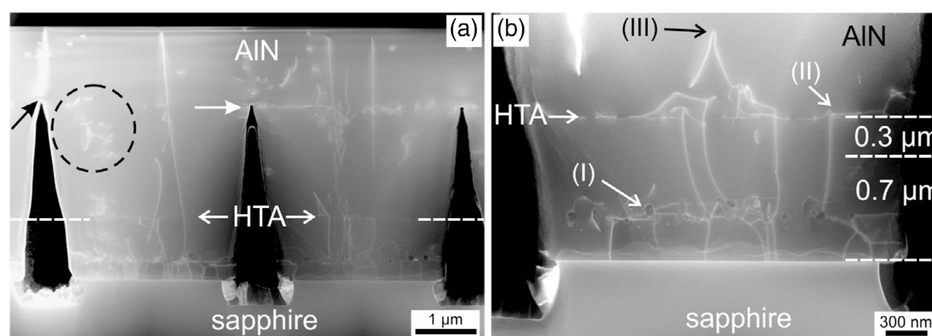

Figure 9. Cross-sectional ADF-STEM images showing all types of threading dislocations in ELO AlN with an intermediate HTA step at 1730 °C for 1 h. a) Defects are generated at coalescence points (arrows) and during bulk growth (exemplarily circled by dashed line). b) High magnification above a ridge shows voids (I), horizontal dislocation accumulation at homoepitaxial HTA/non-HTA AlN interface (II) and annihilation of threading dislocations (III) in ELO AlN.

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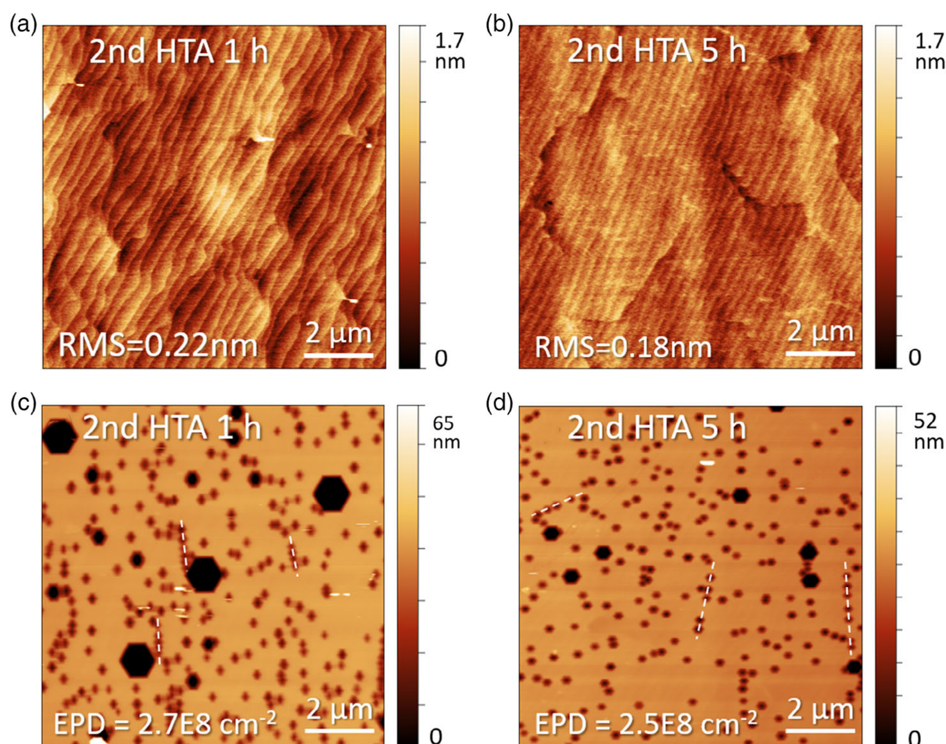

Figure 10. AFM surface topograms of 6 µm thick ELO AlN with second HTA at 1730 °C for a) 1 h, b) 5 h. Surface after DSE of the sample annealed for c) 1 h and d) 5 h with white dashed lines exemplarily indicating lining up of dislocations.

4. Conclusion

The impact of introducing a high-temperature annealing step into the ELO process flow on AlN/sapphire templates was investigated. It was found that covering the open sapphire surfaces of the patterned AlN/sapphire template by a thin AlN layer (0.3 µm) is necessary to preserve the trench shape during annealing. With such intermediate annealing at 1730 °C for 1 h, a crack-free, smooth surface with RMS = 0.16 nm and a dislocation density of $3.5 \times 10^8\ cm^{-2}$ over the entire 2 in. wafer could be achieved for the subsequently grown 6 µm thick ELO AlN. ADF-STEM analysis reveals an effective dislocation reduction in HTA treated AlN as well as a rearrangement of vertical defect lines at the HTA/non-HTA interface, In addition, an accumulation of horizontal dislocation segments at the HTA/non-HTA interface was observed, which can be a result of strain relaxation taking place during the growth of thick layers with a relatively low TDD. Despite the favorable effect of HTA on the TDD, coalescence of the wing regions in ELO AlN can act as an additional source for the formation of threading dislocations. With increased annealing duration from 1 to 3 h a TDD of $4 \times 10^8\ cm^{-2}$ was realized even for lower HTA temperatures of 1690 and 1710 °C. For 1730 °C and an annealing duration of 3 h, the patterned AlN/sapphire interface starts to degrade most likely by formation of AlON. The compressive strain introduced into the AlN layer during HTA is at least partially maintained during ELO. This enables a second HTA step of the fully grown, coalesced ELO AlN template at 1730 °C. By this a TDD of $2.5 \times 10^8\ cm^{-2}$ was reached while a smooth surface was maintained.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors thank T. Petzke for technical support in epitaxial growth. This work was partially supported by the German Federal Ministry of Education and Research (BMBF) through the consortium "Advanced UV for Life" under the project contracts 03ZZ0130A, and 03ZZ0134B.

Open access funding enabled and organized by Projekt DEAL.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

AlN, epitaxial lateral overgrowth, high-temperature annealing, MOCVD, patterned sapphire

Received: April 30, 2021
Revised: June 17, 2021
Published online: July 27, 2021

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