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On the Conduction Properties of Vertical GaN *n*-Channel Trench MISFETs

ELDAD BAHAT TREIDEL [1], OLIVER HILT [1], VEIT HOFFMANN [1], FRANK BRUNNER [1], NICOLE BICKEL [1], ANDREAS THIES [1], KORNELIUS TETZNER [1], HASSAN GARGOURI [2,3], CHRISTIAN HUBER [4], KONSTANTY DONIMIRSKI [5], AND JOACHIM WÜRFL [1], (Member, IEEE)

1 Ferdinand-Braun-Institut gGmbH, Leibniz-Institut für Höchstfrequenztechnik, 12489 Berlin, Germany
2 Plasma Process Technology Department, SENTECH Instruments GmbH, 12489 Berlin, Germany
3 Konica Minolta Group, Instrument Systems GmbH, 81677 München, Germany
4 Corporate Research Division, Advanced Technologies and Micro Systems Department, Robert Bosch GmbH, 71272 Renningen, Germany
5 SEEN Semiconductors Ltd., 02-672 Warsaw, Poland

CORRESPONDING AUTHOR: E. BAHAT TREIDEL (e-mail: eldad.bahat-treidel@fbh-berlin.de)

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ABSTRACT ON-state conductance properties of vertical GaN *n*-channel trench MISFETs manufactured on different GaN substrates and having different gate trench orientations are studied up to 200 °C ambient temperature. The best performing devices, with a maximum output current above 4 kA/cm^2 and an area specific ON-state resistance of 1.1 mΩ·cm^2, are manufactured on ammonothermal GaN substrate with the gate channel parallel to the *a*-plane of the GaN crystal. The scalability of the devices up to 40 mm gate periphery is investigated and demonstrated. It is found that, in addition to oxide interface traps, the semiconductor border traps in the *p*-GaN layer limit the available mobile channel electrons and that the channel surface roughness scattering limits the channel mobility. Both strongly depend on the gate trench orientation and on the GaN substrate defect density.

INDEX TERMS Vertical GaN trench MISFETs, HVPE, ammonothermal, conductivity, mobility, mobile charge carriers' density, gate insulator, atomic layer deposition (ALD).

I. INTRODUCTION

Vertical GaN-based MISFETs for high voltage power switching applications have the potential to outperform Si and SiC based competitors in terms of power density and switching speed [1], [2], [3], [4], [5]. As compared to lateral GaN HFETs, vertical GaN FETs for power switching applications are expected to provide significant merits: lower area specific ON-state resistance down to ~1.0 mΩ·cm^2 [2], [4], [5], [6], [7], reduced dispersion (R_{on_dyn}) and switching losses [1], [2], [3], [5], [8], and enhanced thermal dissipation using bulk GaN. Progress in the development of low defect density GaN substrates and the possibility of strain free homoepitaxy allows growing thick *n*-GaN drift layers for an OFF-state blocking capability larger than 1 kV [2], [4], [5], [6]. Several prominent concepts for vertical GaN transistors are considered worldwide: Current Aperture Vertical Electron Transistors (CAVETs) [4], regrown semi-polar channel and *p*-type gate structure [2], vertical junction field-effect transistor (VJFET) [5], trench gate MISFET [1] and vertical FinFETs [7], [9]. A particular challenge of the first three concepts is the epitaxial regrowth. The GaN-based Trench-MISFET owns the advantage of one epitaxial growth step, intrinsic normally-off nature and low gate currents. On the other hand, it requires a robust gate insulating layer to allow for channel inversion and for good transport properties close to the semiconductor insulator interface [10], [11]. Unlike Si- or SiC- based MOSFETs, GaN does not have a native oxide that can serve as gate insulator. Thus, a foreign insulating layer must be deposited between the gate metal and the channel for field effect modulation. In addition, the lateral epitaxial *n-p-n* FET junction requires deep etching through these layers. A gate oxide deposited on such "etch-damaged" surfaces can lead to distortion of the space charge region preventing channel inversion.

Among the GaN substrate production methods hydride vapor-phase epitaxy, HVPE, and ammonothermal are the most promising technologies for large scale commercial production [12], [13]. The HVPE production method has the advantages of good growth condition control at high growth rate ∼100 μm/h, large wafer diameter > 150 mm, relatively high material purity and relatively low cost per area ∼200 USD/cm^2. However, HVPE grown wafers are challenged by growth on foreign substrates which still renders defect density to be higher than 5 × 10^6 cm^{-3}, builds in mechanical stress which is turned into wafer bow and crystal-axis angle variation. The ammonothermal production method has the advantages of low defect density ∼5 × 10^4 cm^{-3}, low impurity concentrations, low building strain and therefore it produces very flat wafers. However, the wafer diameter size, ≤ 50 mm, and the low growth rates ∼2 μm/h using this method are among its limitations resulting in very high cost per area ∼1000 USD/cm^2. Unlike for the HVPE method, long crystals can be achieved by extremely long growth time. Therefore, a significant cost reduction down to ∼10 USD/cm^2 is predicted for large scale production. Recently, fully vertical GaN-on-Si power MOSFETs [14], [15] and quasi-vertical FinFETs on engineered substrates [16] were demonstrated as a solution for low cost large wafer size but these solutions need additional sophisticated substrate removal or back etching technologies.

This study was motivated by the development of vertical GaN trench MISFET technology for direct GaN chip on laser chip pulsed laser driving applications with maximum voltages < 100 V [17]. Drivers for pulsed lasers are required to deliver very high currents up to 250 A in very short pulse lengths between 3 ns and 10 ns [18]. Vertical GaN *n*-channel trench MISFETs are particularly suited for realizing the required steep current slopes due to their low output capacitance and gate charge figure of merits, $C_{OSS} \times R_{on}$ and $Q_g \times R_{on}$ [1], [3]. Additionally, this device technology allows aggressive device scaling and enables a high current density per unit area [19].

In this work we present for the first time a systematic and comprehensive study with very large devices' population, including many geometrical designs variations and multiple GaN substrate variations from different sources and production technologies. We further discuss the impacts of GaN substrate quality and gate trench orientation on the formation of the electron inversion layer in the transistor channel, which is situated in the *p*-GaN layer close to the gate oxide interface. For this, we first measure the devices pulsed output characteristics and compare the ON-state resistance correlation to gate periphery for the different substrates and gate trench orientations. Afterwards, the gate channel capacitance is measured to determine the channel inversion mobile charge carrier density. There, we discover large differences between devices on different substrates and for different gate orientations. The temperature dependent output properties are measured up to 200 °C and the temperature dependent effective mobility and interface trap density are evaluated. Then, we discuss the channel inversion properties and the scattering mechanisms dominating the channel mobility focusing on the different substrates and the two gate trench orientations. Finally, we conclude on the mechanisms that impede the conductance of the vertical GaN trench *n*-channel MISFETs.

TABLE 1. GaN substrates datasheet[a].

Wafer	Resistivity (Ga-face) [Ω·cm]	N_D [cm^{-3}]	EPD [cm^{-2}]	FWHM (102) [arcsec]
HVPE "A"	1.50 × 10^{-2}	2 × 10^{18}	(-)	∼124
HVPE "B"	1.34 × 10^{-2}	(-)	1.6 × 10^6	∼69
HVPE "C"	(-)	1.5 × 10^{18}	< 5 × 10^6	∼40
Ammono "A"	3.23 × 10^{-3}	1 × 10^{19}	< 5 × 10^4	∼20
Ammono "B"	3.18 × 10^{-3}	1 × 10^{19}	< 5 × 10^4	∼20

[a]The parameters are provided by the substrate vendors.

II. GAN SUBSTRATES, EPITAXIAL GROWTH AND DEVICE MANUFACTURING

For conduction properties comparison of the *n*-channel trench MISFETs, five 2 inch highly conductive GaN substrates are selected; three commercial hydride vapor phase epitaxy (HVPE) approaches from different vendors, HVPE "A," HVPE "B" and HVPE "C" and two nominally identical ammonothermal GaN substrates from a fourth vendor, Ammono "A" and Ammono "B." For all wafers the top side *c*-plane (0001) is an epi-ready polished Ga-face surface. The main flat is *m*-plane ($1\bar{1}00$) and the secondary flat, which is 90 ° to the left, is *a*-plane ($\bar{1}\bar{1}20$). To avoid any confusion, the crystal orientation of the etched planes were confirmed by a sidewall wet etch process with the highly selective anisotropic etch solution tetramethylammonium hydroxide (TMAH), [8], [14], [20], [21], [22], [23], [24]. The conductivity and quality parameters provided by the different substrate vendors' datasheets and the XRD measurements of the GaN rocking curve FWHM of the (102) diffraction plane are given in Table 1.

A. EPITAXIAL DESIGN AND GROWTH

On top of the different GaN substrates nominally the same epitaxial GaN layers are subsequently grown by metalorganic vapor phase epitaxy (MOVPE). The epitaxial layer stack starts with a highly conductive 3.2 μm thick n^+-GaN:Si (N_D = 3.5 × 10^{18} cm^{-3}) seeding and drain contact layer. The typical sheet resistance of this drain layer measured by transmission line model (TLM) is 1.72 ± 0.05 Ω/□. Next, a 5.3 μm thick n^--GaN:Si (N_D = 1.4 × 10^{17}cm^{-3}) drift layer is grown followed by a *p*-GaN:Mg (N_A = 1.5 × 10^{17} cm^{-3}) blocking layer with a thickness of 300 nm. The blocking layer thickness is also considered as the gate length, L_g. For well-defined *p-n* junctions the Mg segregation during the *n*-GaN overgrowth is reduced by more than one order of magnitude using a low temperature *n*-GaN:Si 100 nm (N_D = 3.5 × 10^{18} cm^{-3}) interlayer on top of the blocking layer. In-situ activation of the *p*-GaN:Mg is accomplished by

annealing before and after the *n*-GaN:Si interlayer growth. Finally, a 500 nm thick *n*-GaN:Si ($N_D = 1 \times 10^{18}$ cm^{-3}) source layer is followed by 20 nm highly doped n^+-GaN:Si ($N_D = 1.1 \times 10^{19}$ cm^{-3}) cap layer. The typical sheet resistance of the source top layer on the complete epitaxial stack measured by TLM is 281.8 ± 1.4 Ω/□. Here the sheet resistance is much higher than for the drain layer since it is partially depleted by the *p*-type blocking layer beneath. The XRD FWHM for all wafers did not change with the epitaxial growth.

B. DEVICE MANUFACTURING

The device manufacturing starts with the formation of the back side drain ohmic contact. A Ti/Al/Mo/Au metal stack is e-beam evaporated and annealed at 830 °C in N_2 ambient. To achieve high resolution and alignment accuracy for highly dense structural features on the wafers, *i*-line stepper lithography is used for all process steps. Next, the gate channel trench is defined and etched using a Cl_2 based inductive coupled plasma (ICP) dry-etch process. The gate trench is 1 μm deep and the etch process is stopped in the upper part of the drift layer. Then, the device process sequence follows the "ohmic contacts first" concept. The selection of this processing sequence is due to the thermal budget of the gate insulator oxide layer. Source ohmic contacts are defined and a Ti/Al/Mo/Au metal stack is e-beam evaporated. An additional top side drain ohmic contact is formed on the wafer front side. This requires additional deep trench etching through the drift layer down to the highly doped n^+-GaN layer. After evaporation of the topside drain ohmic contact metal-stack the contacts are annealed again at 830 °C in N_2 ambient. Afterwards, in order to remove dry-etch surface damages, a Buffered Oxide Etchant (BOE) dip and a 25% TMAH solution dip at 40 °C for 5 min followed by an in-situ remote NH_3-plasma pre-treatment at 400 °C. Then, a 25 nm thick Al_2O_3 gate insulator layer is deposited by plasma enhanced ALD at 250 °C [25]. For vertical trench sidewall conformal coverage of the gate electrode, a TiW film is sputtered and reinforced with 1 μm electroplated Au. All top-side contacts are then reinforced using a 2 μm Au electroplated layer which also forms the top-side contact pads for automated on-wafer electrical characterization in quasi-vertical configuration of the true vertical devices. Source and gate interconnects are insulated by 500 nm SiN_x. A schematic cross section of the manufactured vertical GaN *n*-channel trench MISFET is illustrated in Fig. 1 (a). For electrical properties evaluation, four device types with different gate width [19], W_g, and gate density per unit area were prepared; 10.2 mm, 20.4 mm and 40.8 mm gate width "finger" type devices with a gate density of ~113 mm/mm^2 and a half cell pitch of 9 μm, and 32.0 mm gate width hexagonal-cell design devices with ~305 mm/mm^2 gate density and a half cell pitch of 6 μm. Single hexagon cell devices with $W_g = 0.63$ mm are used for temperature dependent conduction properties analysis. The gate width, W_g, is defined by the perimeter of the trench structure etched through the GaN top layer and the unit area is the whole device active area excluding the coplanar contact pads. To investigate the influence of the trench channel orientation with respect to the GaN crystal planes, identical finger-devices and hexagonal-cell devices with gate trench channel oriented parallel and perpendicular to the wafer main flat are formed (shown in Fig. 1 (b) and (c)). Devices with channel gate trench parallel to the main wafer flat are designated as "*m*-plane" and devices perpendicular to the main flat are designated as "*a*-plane."

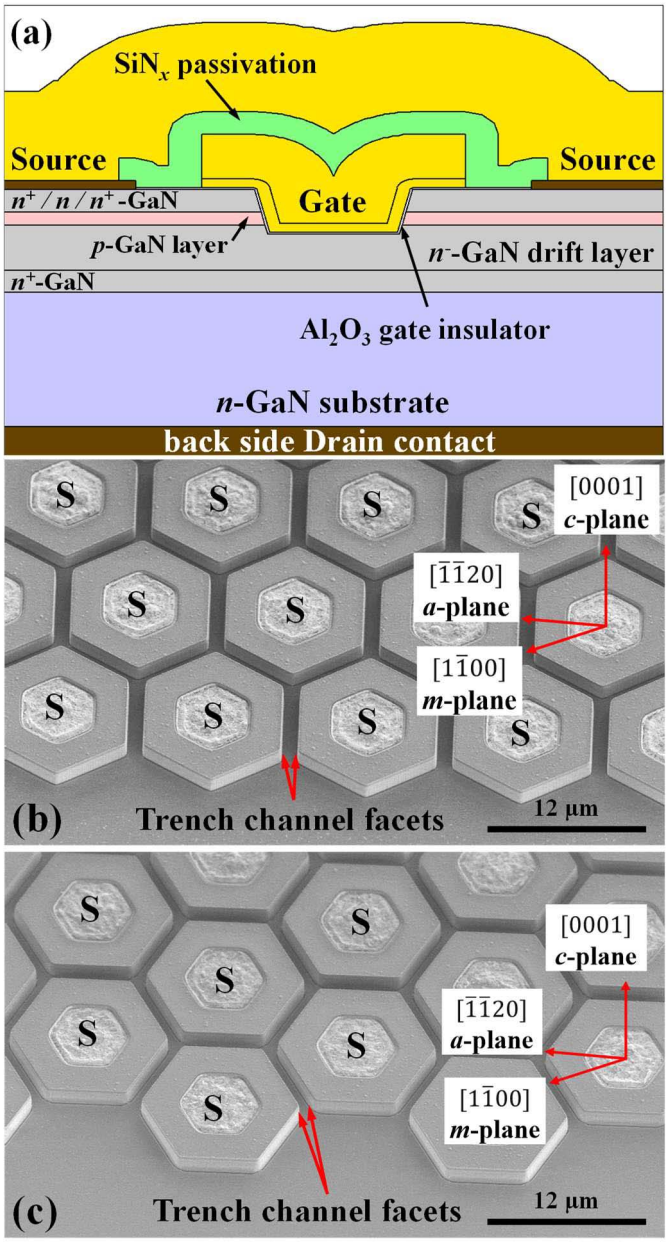

FIGURE 1. (a) Schematic cross section illustration of a vertical GaN trench MISFET. A scanning electron microscope micrograph of a $W_g = 32$ mm (b) *a*-plane and (c) *m*-plane hexagonal cell transistor with the respect GaN crystal planes indication. The images are captured during their process prior to the gate insulator deposition.

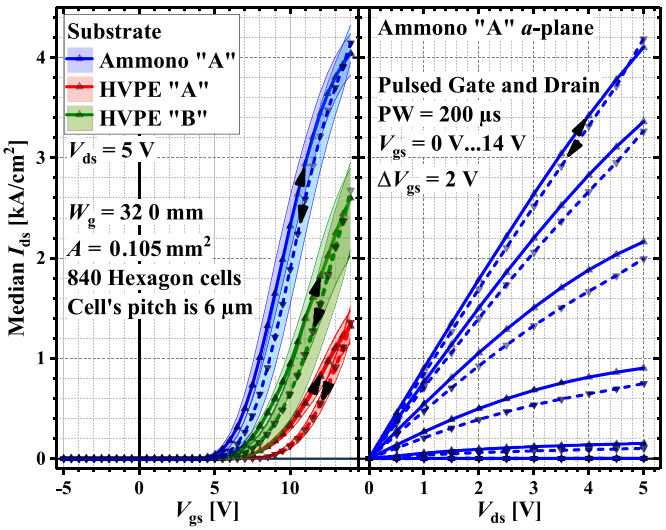

FIGURE 2. (Left) Wafer level median bidirectional pulsed transfer characteristics measured for some of the different GaN substrates. (right) Wafer level median bidirectional pulsed output characteristics measured for wafer Ammono "A." For this comparison cellular hexagon *a*-plane transistors with W_g = 32.0 mm are measured with pulsed gate and drain PW = 200 μs. The arrows indicate the measurement sweep direction and the error bands are 25 % and 75 % quantiles.

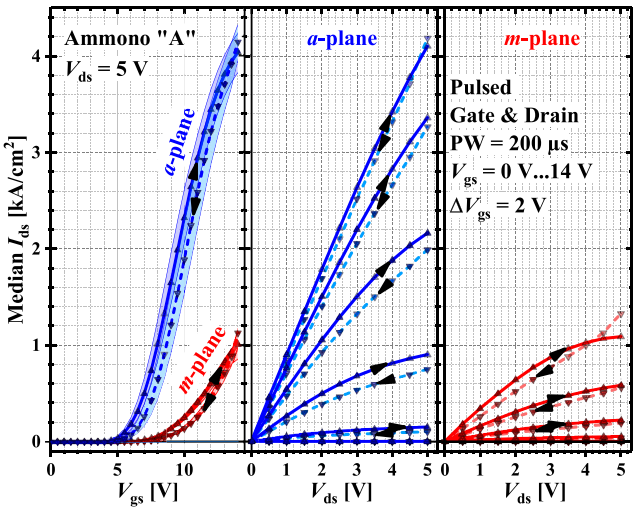

FIGURE 3. Ammono "A" Wafer level median bidirectional pulsed transfer characteristics measured for the different gate trench orientation devices (left). Wafer level median bidirectional pulsed output characteristics measured for *a*-plane (center) and (right) *m*-plane gate trench orientation devices. For this comparison cellular hexagon transistors with W_g = 32.0 mm are measured with pulsed gate and drain PW = 200 μs. The arrows indicate the measurement sweep direction and the error bands are 25 % and 75 % quantiles.

III. EXPERIMENTAL RESULTS

After process completion, the devices are electrically characterized using Keysight B2902A precision source/measure unit. The devices are electrically characterized using simultaneous 200 μs gate and drain pulses with repetition rate of 20 ms. The devices are characterized on-wafer in quasi-vertical configuration by using the top-side drain contacts to simplify the wafer-level measurements. A Hewlett-Packard HP4275A multi-frequency LRC meter with small signal frequency of 1 MHz and amplitude of 100 mV is used for the capacitance measurements.

It should be noted that the blocking voltage for all tested devices exceeds 100 V to fulfill the laser driver requirement.

A. PULSED CONDUCTANCE OUTPUT CHARACTERISTICS

Fig. 2 (left) depicts the forward and backward median transfer characteristics of 840 hexagon-cell 32.0 mm *a*-plane transistors of three selected wafers. Transistors on the ammonothermal substrate have higher current density in comparison to devices on the HVPE substrates. In addition, a large conductance difference is observed between the two HVPE substrates as well. Besides, significant differences in the threshold voltage, V_{th} are obtained. Fig. 2 (right) shows the Ammono "A" wafer level median pulsed output characteristics, with output current density exceeding 4 kA/cm^2 and an area specific ON-state resistance, $R_{ds\_ON} \times A$, of 1.1 mΩ·cm^2. Clockwise hysteresis effects are identified which indicate trapping of charge carriers in dielectric/semiconductor interface defect states [26]. Fig. 3 shows a wafer-level comparison between devices with gate trench oriented parallel to the *a*- and *m*- crystal planes, respectively, measured on Ammono "A" wafer.

TABLE 2. Wafer level median electrical output parameters evaluation for the different gate trench orientation at 25 °C [a].

Wafer Gate trench orientation	I_{ds_max} [mA / mm]	R_{ds_ON} [Ω·mm]	V_{th} [V]	g_{m_max} [mS / mm]
HVPE "A"				
a-plane	40.3 ± 0.8	46.3 ± 1.3	5.6 ± 0.0	6.8 ± 0.1
m-plane	3.4 ± 0.2	422.2 ± 15.2	9.8 ± 0.1	0.7 ± 0.0
HVPE "B"				
a-plane	88.6 ± 4.1	32.0 ± 6.9	4.3 ± 0.1	17.6 ± 0.5
m-plane	1.5 ± 0.1	958.6 ± 65.6	10.9 ± 0.1	0.4 ± 0.0
HVPE "C"				
a-plane	41.6 ± 1.1	50.7 ± 1.9	6.1 ± 0.0	7.2 ± 0.2
m-plane	23.1 ± 0.8	69.8 ± 8.9	6.7 ± 0.0	3.8± 0.1
Ammono "A"				
a-plane	181.5 ± 4.6	23.3 ± 0.7	3.8 ± 0.1	27.2 ± 0.7
m-plane	35.7 ± 1.6	82.9 ± 7.7	6.2 ± 0.1	6.9 ± 0.3
Ammono "B"				
a-plane	154.6 ± 2.0	26.2 ± 0.6	4.2 ± 0.1	23.2 ± 0.4
m-plane	12.6 ± 0.5	283.1 ± 17.4	8.1 ± 0.0	2.6 ± 0.1

[a] The parameters evaluated from a W_g = 10.2 mm five fingers devices. I_{ds_max} and R_{ds_ON} are determined for V_{gs} = 14 V and V_{ds} = 5 V

A superior conductance of the *a*-plane over the *m*-plane type devices with a four-times higher maximum current density is clearly seen. Table 2 summarizes the conductance output parameters evaluated on 10.2 mm "finger" devices for all processed wafers and for both gate trench orientations. The superior conduction properties of devices with gate trench parallel to the *a*-plane are systematically observed for all wafers. However, large differences in the degree of change are observed; a factor of 1.8 to 60 in maximum current, I_{ds_max}, a factor up to 30 in ON-state resistance, R_{ds_ON}, and a factor of 2 to 45 in maximum transconductance, g_{m_max}, between devices on both substrate types. A significant difference in the device threshold voltage, V_{th}, is apparent as

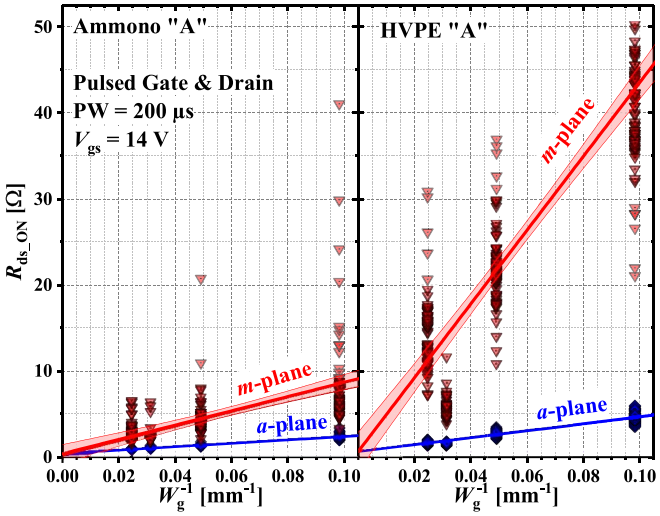

FIGURE 4. Wafer level absolute R_{ds_ON} as function of the reciprocal scaling of transistor gate width, W_g^{-1}, measured for *a*-plane and *m*-plane devices on Ammono "A" and HVPE "A" wafers in quasi vertical co-planar configuration. The error bands are the upper and the lower 95% fitting confidence level.

well. A straight correlation between the output parameters and threshold voltage is observed. The more positive the threshold voltage the lower is the output current and the transconductance and the higher is the ON-state resistance. For example, devices manufactured on HVPE substrates have a more positive V_{th} than devices on ammonothermal substrates and *m*-plane devices on all substrate types have more positive values than *a*-plane devices. This may indicate substantial differences in the mobile charge carrier concentration during channel inversion and possible differences in the carriers' mobility. A thorough analysis of the mobile charge carrier concentration is presented in Section III-C.

B. GATE WIDTH AND AREAL SCALING ANALYSIS

For power-switching applications large periphery transistors with low ON-state resistance are required. Due to their relatively low current density per gate width, in comparison to lateral HFETs, vertical GaN *n*-channel trench MISFETs need larger gate periphery for similar area-specific ON-state resistance. The geometrical nature of trench MISFETs allows for a very dense gate scaling [1]. Thus, we have realized devices with 142 mm gate width and 305 mΩ (2.75 mΩ·cm^2) ON-state resistance and operated them as laser diode drivers [17].

Fig. 4 shows the absolute R_{ds_ON} of scaled devices with different gate widths as a function of the reciprocal gate width, W_g^{-1}. The ON-state resistance may be represented by two linear terms [19]:

$$R_{ds\_ON} = \overline{R}_{sh\_ON} \cdot W_g^{-1} + \sum \overline{R}_{ext} \quad (1)$$

$\overline{R}_{sh\_ON}$ [Ω·mm] is the sum of sheet resistances that scale with the gate width, namely, the source and channel sheet resistances. $\sum \overline{R}_{ext}$ [Ω] represents the sum of extrinsic (parasitic) resistances, which are almost independent of gate width, specifically, the topside drain contact resistance and the drift region resistivity. In this experiment the discrete devices are not insulated by a mesa, therefore, the drift region dimensions are constant and independent of the gate width and the active area. The average ON-state sheet resistance, $\overline{R}_{sh\_ON}$ [Ω·mm] is deduced from linearly fitting the slope, and the $\sum \overline{R}_{ext}$ [Ω], is taken from the intercept of the curve with the R_{ds_ON} axis, namely, when the gate width is infinite. The extraction of $\overline{R}_{sh\_ON}$ is important for the later determination of the channel mobilities, as presented in Section III-F.

TABLE 3. On-state resistance analysis [a].

Wafer Gate trench orientation		$\overline{R}_{sh\_ON}$ [Ω·mm]	$\sum \overline{R}_{ext.}$ [Ω]
HVPE "A"			
	a-plane	40.0 ± 0.8	0.66 ± 0.05
	m-plane	429.1 ± 18.1	0.64 ± 1.13
HVPE "B"			
	a-plane	24.0 ± 0.8	0.62 ± 0.05
	m-plane	920.5 ± 60.1	0.76 ± 3.71
HVPE "C"			
	a-plane	49.0 ± 2.2	0.67 ± 0.14
	m-plane	64.4 ± 2.0	0.72 ± 0.13
Ammono "A"			
	a-plane	18.6 ± 0.9	0.43 ± 0.06
	m-plane	82.9 ± 8.5	0.38 ± 0.53
Ammono "B"			
	a-plane	22.6 ± 0.6	0.47 ± 0.04
	m-plane	334.4 ± 22.8	0.43 ± 1.45

[a] Evaluated at V_{gs} = 14 V.

In Fig. 4 two representative substrates, Ammono "A" and HVPE "A," and the two gate-trench orientations, *a*-plane and *m*-plane are compared. It is observed that for all device types the absolute ON-state resistance is linearly correlated to the inverse gate width which is demonstrated by the low tolerance values of the linear fits. Especially the *a*-plane devices are scaling very well with inverse gate width, W_g^{-1}. The ON-state sheet resistance, $\overline{R}_{sh\_ON}$ of each type of the devices is significantly different. Distinct is the difference between the two gate orientations, *m*- and *a*-plane, with a factor of 4 and 10 times for the Ammono "A" and the HVPE "A," respectively. It is clearly observed that for each wafer the linear correlation curves intercept the R_{ds_ON} axis at a similar $\sum \overline{R}_{ext}$ resistances value significantly lower than the total R_{ds_ON} of the studied devices. This indicates that the R_{ds_ON} is limited only by resistances which scale with the gate width, most probably the channel resistance. It should be noted that the ON-state resistance is calculated as the reciprocal of the maximum conduction, $R_{ds\_ON} = 1/g_{d\_max}$, at V_G = 14 V. Therefore, an arithmetic small variation in a small conduction value will turn into a large variation in a large resistance value.

The linearly fitted ON-state sheet resistance and the extrinsic (parasitic) serial resistance for all measured devices are summarized in Table 3. Devices manufactured on ammonothermal substrates have smaller average ON-state

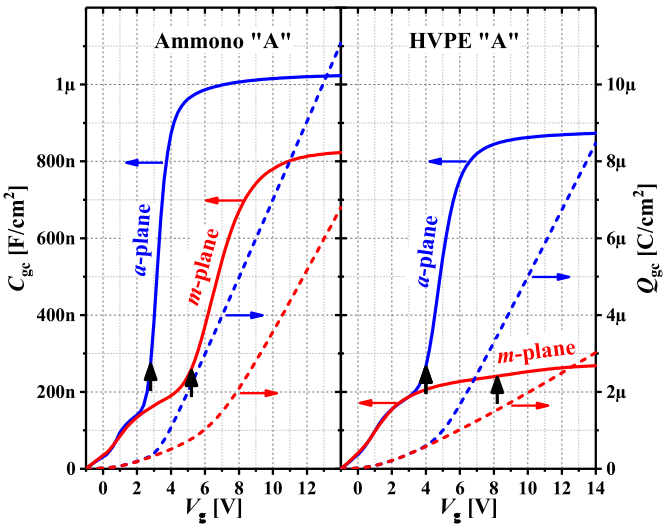

FIGURE 5. Gate channel capacitance, C_{gc}, and gate channel charge density, Q_{gc} , measured for *a*-plane and *m*-plane devices on Ammono "A" and HVPE "A" wafers with the gate dimensions of $W_g = 10.2$ mm and $L_g = 3 \times 10^{-4}$ mm. The small signal frequency is 1 MHz with amplitude of 100 mV. The threshold voltage is indicated by the black vertical arrows.

TABLE 4. Mobile channel charge analysis.

Wafer Gate trench orientation	$\overline{Q}_{sh\_ON}$ [pC / mm]	$\sum \overline{Q}_{ext}$ [pC]	V_{th} estimated from CV [V]
HVPE "A"			
a-plane	5.48 ± 0.52	79.9 ± 13.5	4.4 ± 0.6
m-plane	0.46 ± 0.07	-1.8 ±1.7	8.2 ± 0.4
HVPE "B"			
a-plane	6.21 ± 0.47	98.5 ± 12.8	3.7 ± 0.6
m-plane	0.11 ± 0.06	0.4 ± 1.6	9.0 ± 0.9
HVPE "C"			
a-plane	11.30 ± 0.48	33.8 ± 13.1	3.7 ± 0.3
m-plane	10.74 ± 0.54	83.8 ± 14.5	3.4 ± 0.4
Ammono "A"			
a-plane	11.32 ± 0.85	89.5 ± 23.0	2.6 ± 0.4
m-plane	5.51 ± 1.05	43.6 ± 28.2	5.1 ± 1.1
Ammono "B"			
a-plane	13.71 ± 0.58	81.3 ± 15.6	2.6 ± 0.3
m-plane	1.23 ± 0.53	-8.5 ± 14.3	8.0 ± 0.4

[a] Evaluated at $V_{gs} = 14$ V.

sheet resistance, $\overline{R}_{sh\_ON}$ [Ω·mm], for both channel orientations over HVPE devices. In addition the sum of extrinsic (parasitic) resistances, $\sum \overline{R}_{ext}$ is lower which is probably due to the lower defect density that results in lower drift region layer sheet resistivity (Table 1). It is observed that for all wafers the $\overline{R}_{sh\_ON}$ is larger for the *m*-plane by a factor of up to 40 times than for the *a*-plane devices. On the other hand for each wafer, independent on the gate channel orientation, the sum of extrinsic (parasitic) resistances, $\sum \overline{R}_{ext}$ is comparable for both orientations. For wafer HVPE "C" the $\overline{R}_{sh\_ON}$ ratio between the two gate trench orientations is relatively low, a factor of 1.3, which may indicate that for this substrate the intrinsic resistivity is dominated by a more powerful component rather than the inversion channel properties along the two GaN crystal planes.

C. MOBILE CHANNEL CHARGE ANALYSIS

For more comprehensively understanding the conduction properties of the vertical GaN MISFET, an accurate estimation of the mobile channel charge density, $Q_n(V_g)$, is crucial. The gate capacitance with respect to the short-circuited source and drain was measured as a function of gate bias to obtain the gate-to-channel capacitance, $C_{gc}(V_g)$. Integration over $C_{gc}(V_g)$ is used for accurate quantification of $Q_n(V_g)$ [27]. Fig. 5 shows a representative example of $C_{gc}(V_g)$ measurement of 10.2 mm finger type devices manufactured on Ammono "A" and HVPE "A" and the two gate-trench orientations, *a*-plane and *m*-plane. When comparing *a*-plane devices from the two wafer types it is seen that the HVPE "A" wafer has lower $C_{gc}(V_g)$, its threshold voltage is positively shifted and it has larger capacitance at the lower bias below the threshold. At the same time, when comparing *a*-plane and *m*-plane devices from the same wafer it is seen that the *m*-plane devices have lower $C_{gc}(V_g)$, the threshold voltage is positively shifted and it has the same capacitance at the lower bias below the threshold. Most of the capacitance at the lower bias below the threshold is a result of the presence of oxide interface traps [27]. Furthermore, for the *m*-plane device on the HVPE "A" wafer the gate-channel capacitance above the threshold voltage is extremely low. This indicates that the channel is only in low accumulation condition rather than inversion. This effect is similarly observed for *m*-plane devices on Ammono "B" and HVPE "B" substrates. Integration of $C_{gc}(V_g)$ over the applied bias is the total gate channel charge $Q_{gc}(V_g)$, shown in Fig. 5 right axis, which includes the mobile inversion charge and the non-mobile charges filling the oxide interface traps and the depleted acceptors in the *p*-GaN region. The mobile channel charge $Q_n(V_g)$ values are obtained by integrating $C_{gc}(V_g)$ from the threshold voltage to the applied gate voltage. More accurate threshold voltage value is obtained from the maximum value in the second derivative of the CV measurements (shown in Table 4). Similar to the ON-state resistance, the mobile channel charge, $Q_n(V_g)$, can be understood as the sum of channel charges scaling linearly with the device dimensions (e.g., gate width, W_g,) and of constant inversion added charges. Here again, devices on the same wafer share the dimensions and properties of the epitaxial layers, gate oxide properties and process parameters, their scaling is dominated by the gate width, see Fig. 6. The mobile channel charge may be then represented by two linear terms:

$$\overline{Q}_n(V_g) = \overline{Q}_{sh\_ON} \cdot W_g + \sum \overline{Q}_{ext} \tag{2}$$

$\overline{Q}_{sh\_ON}$ [C/mm] is the average ON-state mobile sheet charge that scales with the gate width. $\sum \overline{Q}_{ext}$ [C] represents parasitic device charges, accumulated above the threshold voltage, contributing to a parallel capacitance [28], [29], [30]. The average ON-state sheet mobile charge, $\overline{Q}_{sh\_ON}$ [C/mm] is deduced from linearly fitting the slope of $\overline{Q}_n(W_g)$. $\sum \overline{Q}_{ext}$ [C] is taken from the intercept of $\overline{Q}_n(W_g)$ with the Q_n axis. For all wafers and all gate orientations the linearly

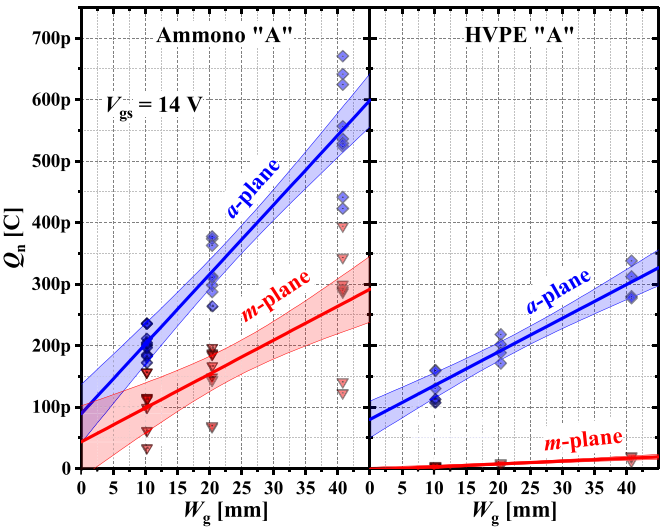

FIGURE 6. Mobile channel charge, Q_n as function of the scaling of transistor gate width, W_g, measured for *a*-plane and *m*-plane devices on Ammono "A" and HVPE "A."

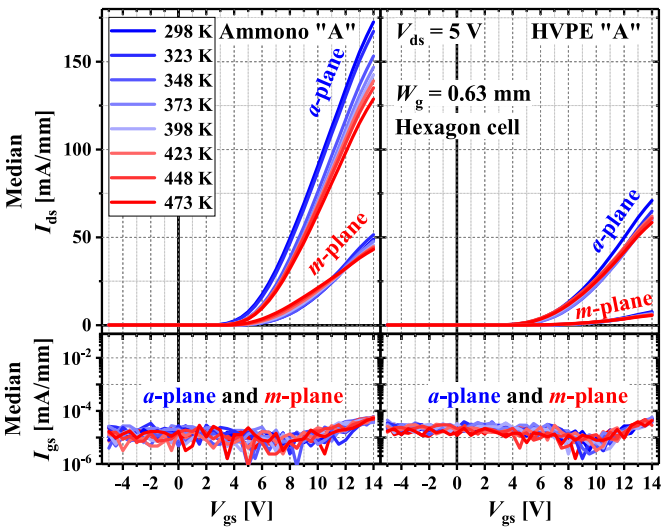

FIGURE 7. Wafer level median transfer characteristics as function of the base plate temperature measured for *a*-plane and *m*-plane hexagon cell devices on Ammono "A" and HVPE "A" wafers where W_g = 0.63 mm.

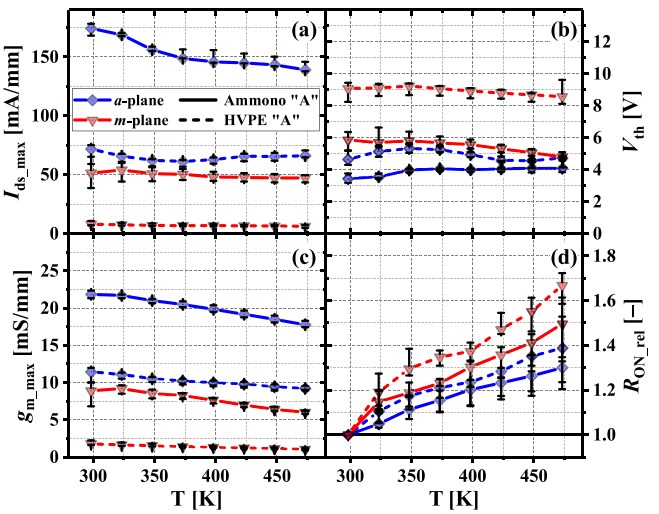

FIGURE 8. Wafer level median output conductance parameters extracted from the measurements in Fig. 7, (a) maximum output current I_{ds_max}, (b) Threshold voltage V_{th}, (c) maximum transconductance g_{m_max}, and (d) relative ON-state resistance R_{on_rel}, as function of the base plate temperature measured for *a*-plane and *m*-plane hexagon cell devices on Ammono "A" and HVPE "A" wafers where W_g = 0.63 mm.

fitted ON-state sheet mobile charges, $\overline{Q}_{sh\_ON}$, and the added inversion layer charges $\sum \overline{Q}_{ext}$ are summarized in Table 4.

Devices manufactured with gate trench along the *a*-plane show more ON-state mobile sheet charges, $\overline{Q}_{sh\_ON}$, than for *m*-plane devices, irrespective from the type of substrate. $\overline{Q}_{sh\_ON}$ is larger for the *a*-plane by a factor of 2 to 60 times than for the *m*-plane devices. For *m*-plane devices manufactured on Ammono "B," HVPE "A" and HVPE "B" the estimated $\overline{Q}_{sh\_ON}$ value is extremely low, confirming the channel is only in low accumulation condition rather than inversion. For these devices the $\sum \overline{Q}_{ext}$ is approximately zero [30]. Devices manufactured on ammonothermal substrates along the crystal *a*-plane, in principle, have more ON-state mobile sheet charges, $\overline{Q}_{sh\_ON}$ [C/mm], over HVPE devices by up to a factor of 2.5 times. Here again, devices from HVPE "C" wafer are exceptionally different from the other HVPE and ammonothermal wafers. The large $\overline{Q}_{sh\_ON}$ values for both gate trench orientations indicate a strong inversion in HVPE "C" devices similar to the ammonothermal wafers *a*-plane devices. The ratio between the two gate trench orientations is relatively low with a factor of only 1.05. Nonetheless for devices manufactured on this substrate the high ON-state mobile sheet channel charge is not translated into high ON-state conductivity. This is in agreement with our earlier assumption that for this substrate the intrinsic resistivity is dominated by a larger contribution that is not dependent on the channel orientation rather than the transport properties along the two GaN crystal planes.

D. TEMPERATURE DEPENDENT CONDUCTANCE PROPERTIES

The temperature dependent output and transfer characteristics are used to evaluate the mobility and interface states trap density. For the temperature dependent characteristics on the different wafers 0.63 mm single hexagon cell transistors in both crystal orientations are measured in a true vertical configuration using the substrate back side as drain contact. The temperature dependent wafer level median pulsed transfer characteristics are depicted in Fig. 7. Here we compare two representative wafer substrate types, Ammono "A" and HVPE "A," and the two gate-trench orientations, *a*-plane and *m*-plane. It is observed that for devices on both substrate types in both channel orientation the drain currents do not degrade strongly in the temperature range between 298 K and 473 K. It is also shown that the gate current is not increasing with temperature and remains below the lower detection limit of 10^{-4} mA/mm for all measured devices. Fig. 8 reviews the

TABLE 5. Electron mobility evaluation at 25 °C.

Wafer Gate trench orientation	μ_{eff_max}	$\bar{\mu}_{sh\_ON}$ (V_{gs} = 14 V)
HVPE "A"		
a-plane	6.14 ± 0.08	4.17 ± 0.43
m-plane	2.50 ± 0.06	4.58 ± 0.72
HVPE "B"		
a-plane	5.66 ± 0.33	4.93 ± 0.79
m-plane	2.56 ± 0.30	9.60 ± 5.55
HVPE "C"		
a-plane	4.51 ± 0.12	1.65 ± 0.10
m-plane	3.93 ± 0.31	1.31 ± 0.08
Ammono "A"		
a-plane	6.45±0.32	4.53 ± 0.37
m-plane	3.82±0.70	2.04 ± 0.43
Ammono "B"		
a-plane	6.62±0.07	3.00 ± 0.16
	2.64±0.20	1.96 ± 0.87

[a] Electron mobility units are [cm^2 / (V·s)].

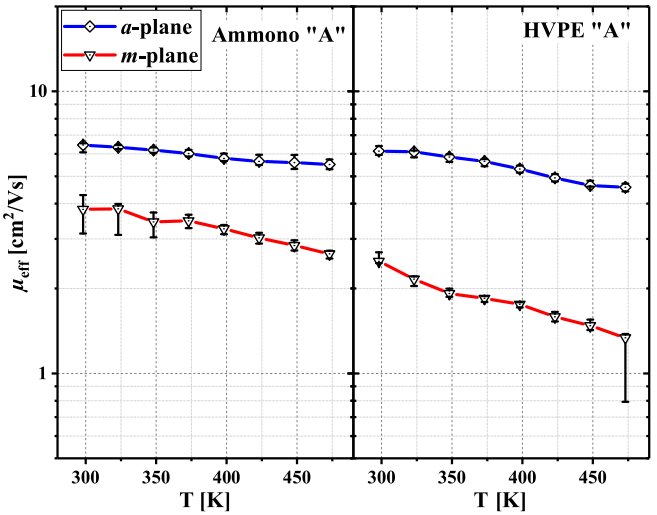

FIGURE 9. Wafer level median electron effective mobility, μ_{eff}, estimations as function of the base plate temperature measured for *a*-plane and *m*-plane hexagon cell devices on Ammono "A" and HVPE "A" wafers where W_g = 0.63 mm.

main median parameters as a function of the base plate temperature for both wafers and the two gate-trench orientations; I_{ds_max}(T), V_{th}(T), g_{m_max}(T) and the relative increase of the ON-state resistance, $R_{ON\_rel}(T) = R_{ds\_ON}(T)/R_{ds\_ON}(298K)$.

Observed drifts of electrical parameters for Ammono "A" *a*-plane device between 298 K and 473 K are < 20% for I_{ds_max}, < 19% for g_m, < 0.65 V for V_{th} and only a factor 1.3 increase in the R_{ds_ON}. For comparison, for the same temperature range lateral GaN MISFETs may suffer from reduction of more than ~60% in output current, reduction by 55% in g_{m_max}, V_{th} shifts by ~3.5 V and a factor 3 increase in the R_{ds_ON} [31].

For better understanding the temperature dependent conduction properties and the limiting scattering mechanisms in the device, the temperature dependent mobility is extracted. From the temperature dependent output characteristics, the effective mobility, μ_{eff}, is estimated [27]:

$$\mu_{eff} = \frac{g_d(V_{gs})L_g}{W_g Q_n} \tag{3}$$

g_d is the drain conductance calculated from the output characteristics branches between V_{gs} = 0 V to +14 V. The measured test devices gate width, W_g, is 0.63 mm and for all mobility evaluation the gate length $L_g = 3 \times 10^{-4}$ mm is used. It is assumed that the inverted channel mobility dominates, according to Mathiessen's rule, since it is much lower than other mobilities in the device and the drain conductance is limited by the channel resistance which is much larger than the source contact resistance and the drift region resistance. For the temperature dependent effective mobility assessment more approximations are considered; the mobile channel charge density is given by the rectangular gate-oxide capacitance, $C_{OX}(V_{gs})$, contour approximation $Q_n \approx C_{ox}(V_{gs} - V_{th})$, This approximation does not take into consideration any parasitic capacitances and other losses associated with charge trapping effect like oxide interface and semiconductor traps. The gate oxide capacitance is estimated from room temperature CV measurement of on-wafer MIS circular planar capacitors manufactured on top of an n^+-GaN drain layer [25]. (The estimated C_{ox} values for each wafer are shown in Table 6). Nevertheless, since the temperature dependent threshold voltage, V_{th}(T), is not certainly well known and C_{ox} is only estimated from external lateral MIS capacitor, the true value of $Q_n(V_{gs})$ is also not precisely known (as discussed earlier).

Table 5 summarizes the estimated maximum mobilities according to Eq. 3 at 25 °C. A significant and consistent correlation on the gate trench orientation is observed for all types of wafers. The effective mobility ratio between the two orientations varies between a factor of 1.2 to 2.4. On the other hand, even though devices manufactured on ammonothermal wafers show some higher effective mobility the difference between the different wafers types is not as large as the difference in the output parameters. A representative comparison of the temperature dependent mobility, μ_{eff}(T), between devices manufactured on Ammono "A" and HVPE "A" and the two gate-trench orientations, *a*-plane and *m*-plane is shown in Fig. 9. Here a relatively weak dependence of the mobility is witnessed between 10% and 20% per 100 K for *a*-plane and *m*-plane, respectively. This is also reflected in the weak dependency of the output parameters on the temperature (Fig. 8).

E. INTERFACE TRAP DENSITY ANALYSIS

From the subthreshold swing, S_{sub}, we can infer the interface trapped charge density, D_{it}, between the semiconductor and the gate dielectric [27], [32]:

$$S_{sub} = (\ln 10)\left(\frac{k_B T}{q}\right)\left(\frac{C_{ox} + C_D + C_{it}}{C_{ox}}\right) \tag{4}$$

where the interface-traps associated capacitance is given by C_{it} [F·cm^{-2}] = qD_{it} [$C^2 \cdot eV^{-1}cm^{-2}$], k_B is Boltzmann constant, q is the elementary charge and with temperature T in

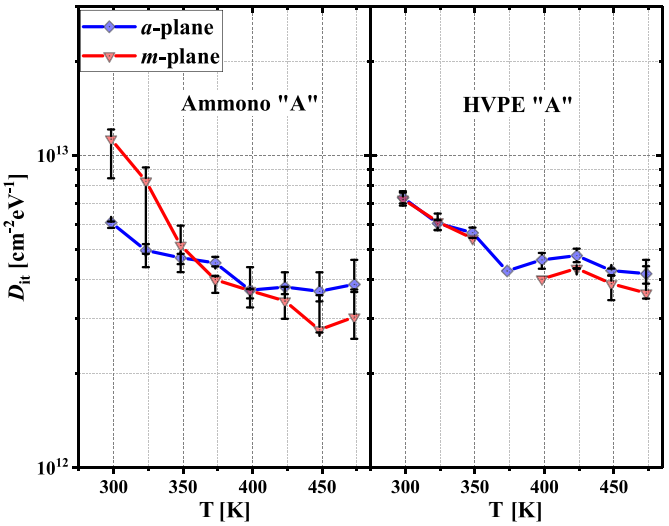

FIGURE 10. Wafer level median interface trapped charge density, D_{it}, between the semiconductor and the gate dielectric, estimated from the transfer characteristics sub-threshold slope as function of the base plate temperature measured for *a*-plane and *m*-plane hexagon cell devices on Ammono "A" and HVPE "A" wafers where $W_g = 0.63$ mm.

Kelvin. The subthreshold swing, S_{sub}, is measured between 10^{-8} A and 10^{-7} A and $V_{ds} = 0.1$ V. In this range the device is under weak inversion condition where the channel depletion capacitance, C_D, is much smaller than the sum of C_{it} and C_{ox}, since the *p*-GaN channel layer is to a large extent depleted from top and bottom by the source and drift layers. Table 6 summarizes the interface trapped charge density, D_{it}, at 25 °C. Comparable interface trap density values are calculated for the devices on the examined substrates in the range of 5 to 11 $\times$ 10^{12} eV^{-1}cm^{-2}. These values are slightly larger than reported values for lateral MIS capacitors on non-polar GaN [33]. One reason that may explain the larger interface trap density is that unlike epitaxial non-polar lateral structures, in the vertical MISFET devices the non-polar faces are damaged by the dry etch process. It should be noted that for the HVPE wafers the difference between the two gate orientations is relatively small. In contrast, the ammonothermal devices have distinct differences between the two device orientations. A representative comparison of the temperature dependent interface trapped charge density, $D_{it}(T)$, between devices manufactured on Ammono "A" and HVPE "A" and the two gate-trench orientations, *a*-plane and *m*-plane is shown in Fig. 10. It is observed that the interface trap density for both types of wafers and in the two gate orientations is not significantly different. Although the same reduction of the D_{it} is observed with the increased temperature, it is a relatively weak dependency.

F. ON-STATE CHANNEL MOBILITY ANALYSIS

The ON-state sheet resistance, $\overline{R}_{sh\_ON}$, (data for $V_{gs} = 14$ V in Table 3) and the ON-state sheet mobile charge, $\overline{Q}_{sh\_ON}$, (data for $V_{gs} = 14$ V in Table 4) are now evaluated as a function of the applied gate overdrive voltage, $\overline{V}_{over} = V_{gs} - \overline{V}_{th}$, between the threshold voltage, estimated from CV, and the maximum of $V_{gs} = 14$ V and presented in Fig. 11 (top). Here, it is clearly observed that for the same overdrive voltage, more mobile sheet charges, $\overline{Q}_{sh\_ON}(V_{over})$, are present for the *a*-plane devices than for the *m*-plane devices.

TABLE 6. Interface trapped charge density of states at 25 °C.

Wafer Gate trench orientation	D_{it} [cm^{-2}·eV^{-1}] × 10^{12}	C_{ox} [nF / cm^2]
HVPE "A"		224
a-plane	7.3 ± 0.4	
m-plane	7.2 ± 0.4	
HVPE "B"		222
a-plane	9.7 ± 0.6	
m-plane	8.0 ± 0.7	
HVPE "C"		233
a-plane	6.1 ± 0.5	
m-plane	5.2 ± 0.5	
Ammono "A"		214
a-plane	6.1 ± 0.6	
m-plane	11.3 ± 1.0	
Ammono "B"		216
a-plane	4.8 ± 0.5	
m-plane	9.9 ± 0.5	

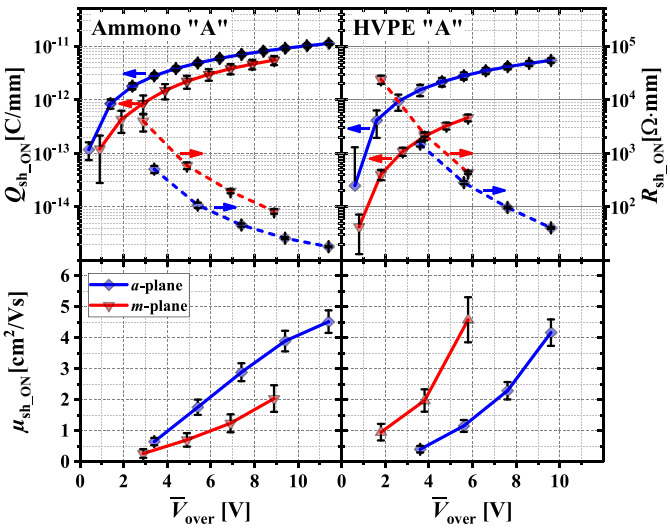

FIGURE 11. Wafer level median sheet resistivity $\overline{R}_{sh\_ON}$ and the sheet ON-state mobile charge $\overline{Q}_{sh\_ON}$ (top) and ON-state channel mobility $\overline{\mu}_{sh\_ON}$ (bottom) as function of the gate over voltage for *a*-plane and *m*-plane devices on Ammono "A" and HVPE "A" wafers.

The behavior of the $\overline{R}_{sh\_ON}(V_{over})$ is quite similar with respect to $\overline{V}_{over}$. When comparing the *a*-plane devices on the Ammono "A" and HVPE "A" substrates, the larger mobile sheet charge and lower $\overline{R}_{sh\_ON}(V_{over})$ on Ammono "A" substrate for similar over voltage is observed.

After estimation of both, $\overline{R}_{sh\_ON}(V_{over})$ and $\overline{Q}_{sh\_ON}(V_{over})$, we may use these values to estimate the ON-state conduction mobility:

$$\overline{\mu}_{sh\_ON}(V_{over}) = \frac{L_g^2}{\overline{R}_{sh\_ON}(V_{over}) \cdot \overline{Q}_{sh\_ON}(V_{over})} \quad (5)$$

Fig. 11 (bottom) displays the dependency of the median ON-state conduction mobility as a function of the applied gate overdrive voltage for representative devices on Ammono "A" and HVPE "A" and for both gate trench orientations. The median ON-state conduction mobilities, $\overline{\mu}_{\mathrm{sh\_ON}}$ at $V_{\mathrm{gs}} = 14$ V for all measured devices are summarized in Table 5. A similar $\overline{\mu}_{\mathrm{sh\_ON}}$ for *a*-plane devices on the different substrates is fundamentally observed. For the *m*-plane devices on wafers Ammono "B," HVPE "A" and HVPE "B" where the channel inversion is uncertain the dominator in Eq. 5 is ruled by the low $\overline{R}_{\mathrm{sh\_ON}}$ value and the calculated mobility is higher and accompanied by a larger error.

G. MOBILE CHARGE INVERSION EFFICIENCY

The total gate charge during switching from OFF-state, $V_{\mathrm{gs}} = 0$ V, to ON-state, $V_{\mathrm{gs}}+14$ V with source and drain terminals grounded, is estimated by measuring the gate current transient flowing across a $R_{\mathrm{L}} = 10$ MΩ load resistor connected in series to the gate electrode as a response to the gate voltage step function from OFF- to ON-state. Integration of the measured current over 20 ms (20 ms >> $5{\cdot}R_{\mathrm{L}}C_{\mathrm{g}}$) gives the total gate charge, see Fig. 12. The measured total gate charge may be Q_{g}, since other gate capacitances towards source and drain are of much lower magnitude. These measurements revealed that the gate oxide charge is independent on both, the substrates and the device gate orientation. This is easy to understand since the gate oxide and the capacitor metal plate is manufactured at the same time using identical process steps for all devices. Then again, the measured gate oxide charge is strongly dependent on the devices gate width, W_{g}. From the linear fit of the gate oxide charge to the gate width we obtain the sheet gate oxide charge $\overline{Q}_{\mathrm{sh\_g}} = 49.34 \pm 0.34$ [pC/mm]. The mobile charge inversion efficiency may be now estimated with the ratio between the mobile channel sheet charges to gate oxide sheet charges:

$$\overline{\theta}_{\mathrm{sh\_ON}} = \frac{\overline{Q}_{\mathrm{sh\_ON}}}{\overline{Q}_{\mathrm{sh\_g}}} \cdot 100\% \tag{6}$$

Fig. 13 summarize the mobile charge inversion efficiency, $\overline{\theta}_{\mathrm{sh\_ON}}$, measured at $V_{\mathrm{gs}} = 14$ V for the examined devices on the different substrates. Once more the advantage of the *a*-plane device on the ammonothermal substrates is clearly seen. However, the mobile charge inversion efficiency in any of the devices does not exceed a value of 30% and most of the switching energy is translated into non-mobile charges.

IV. DISCUSSION

This study on the ON-state conduction properties of vertical GaN trench MISFETs on different free standing GaN substrates shows that although the devices are manufactured in the same process batch with identical process parameters considerably different electrical parameters are measured. When approaching this systematic study, it could be seen that there are some pronounced challenges to achieve statistical significance: 1) The small number of different substrates

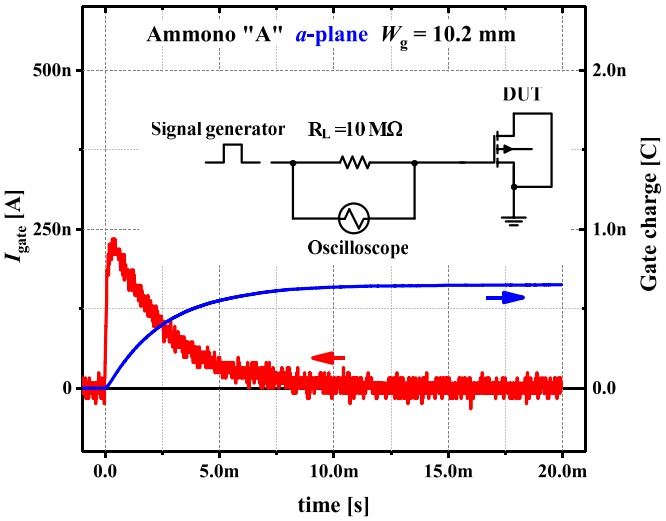

FIGURE 12. Representative measurement example of gate current during switching and the calculated gate charge. The device under test is an Ammono "A" *a*-plane with $W_{\mathrm{g}} = 10.2$ mm. The measured (inset) schematic drawing of the gate charge measurement setup.

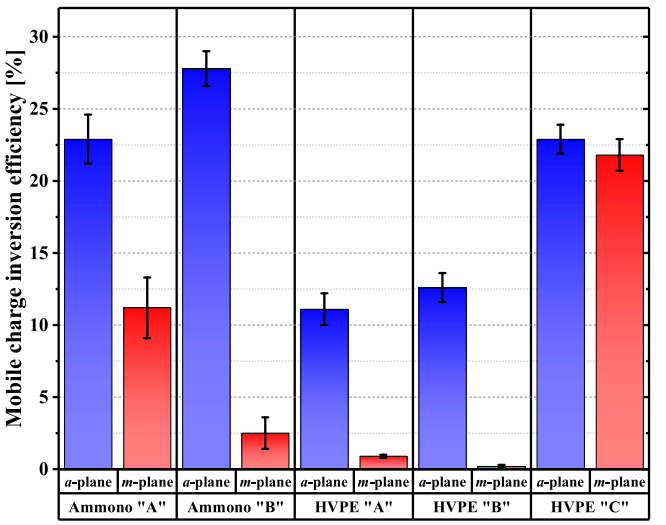

FIGURE 13. Wafer level median mobile charge inversion efficiency, $\overline{\theta}_{\mathrm{sh\_ON}}$, estimated from the sheet gate mobile charge, $\overline{Q}_{\mathrm{sh\_ON}}$, at the gate bias of $V_{\mathrm{GS}} = 14$ V for *a*-plane and *m*-plane devices on all wafers.

due to the fact that GaN substrates are still rare and costly for development purposes, only one wafer from each HVPE substrate and two ammonothermal wafers due to the reason. 2) For epitaxial growth a single wafer reactor has been used, this of course increases the wafer to wafer ambiguity. 3) Other single wafer process steps and low volume manufacturing in the process-line. Instead, large device populations and types on the same two inch GaN substrate may give us valuable first order information to assess how suitable the substrates are for vertical MISFET switching devices.

A substantial observation is that, for all substrate types, devices with a gate trench etched parallel to the non-polar *a*-plane exhibits more drain current and a higher electron

concentration in the inversion channel than devices with perpendicular layout design with gate trench etched parallel to the non-polar *m*-plane. This observation stands in contradiction to recent reports on crystal-orientation dependent device characteristics [8], [9], [14], [21], [33], [34].

An analysis of the ON-state IV curves together with gate CV characterization revealed a correlation between the estimated channel inversion charge, $\overline{Q}_{sh\_ON}$, and the differences in device parameters like I_{ds_max}, R_{ds_ON}, V_{th} and g_{m_max}, for the different examined devices. The observed capacitance-increase of the $C_{gc}(V_g)$ measurements below the threshold voltage (designated in Fig. 5) is a result of the presence of oxide interface traps where $D_{it} \neq 0$ [27]. Their interface trap capacitance C_{it}, contributes noticeably to C_{gc} near the threshold voltage. The threshold voltage is then shifted positively by Q_{it}/C_{ox} where donor traps occupied by electrons are neutral and acceptors traps occupied by electrons are negatively charged. It is clear from the $C_{gc}(V_g)$ measurements for all types of wafers and for both gate trench orientations, that a similar amount of non-mobile charge, in terms of oxide interface trap charges, is accumulated in the gate stack prior to creation of mobile image charges in the channel. It is shown in Fig. 10 and in Table 6 that the oxide interface trap densities for the different devices on the different substrates do not differ to a large extent from each other and show a low dependency on temperature. This can be understood by assuming the presence of deep level oxide interface traps in all examined devices.

Comparing the CV curves of the *a*- and *m*-plane devices on the Ammono "A" substrate (see Fig. 5 (left)) illustrates this situation. The oxide layer, the process steps and the semiconductor epitaxial layers for both devices are identical. Both devices thus should contain the similar oxide interface traps and should feature a similar D_{it}. This is demonstrated in Fig. 10, where D_{it} was determined from the sub-threshold slopes of the transfer characteristics. As a result, both devices should have a similar C_{it} contribution, which is reflected in the corresponding CV curves for $V < 2.5$ V (Fig. 5). From this, a similar threshold voltage would be expected. However, with respect to the *a*-plane devices, the *m*-plane devices have a +1.2 V shifted threshold voltage and a lower C_{gc} above the threshold voltage.

It is known from Si-based MOSFETs that – for an ideal gate oxide – the inversion channel capacitance, C_{ch}, and the oxide capacitance are in series [26], [27], [30].

$$C_{gc} = \frac{C_{ox} \cdot C_{ch}}{C_{ox} + C_{ch}} \tag{7}$$

Which for strong inversion conditions the channel capacitance is much larger than the oxide capacitance $C_{ox} << C_{ch}$, results in a gate channel capacitance approximately equal to the C_{ox}. And, in a very poor inversion where the oxide capacitance is much larger than the inversion capacitance $C_{ox} >> C_{ch}$, therefore the gate channel capacitance is approximately C_{ch} and the mobile channel charge density is very low. The interface capacitance C_{it} is in parallel to C_{ch} in this model [27], yielding

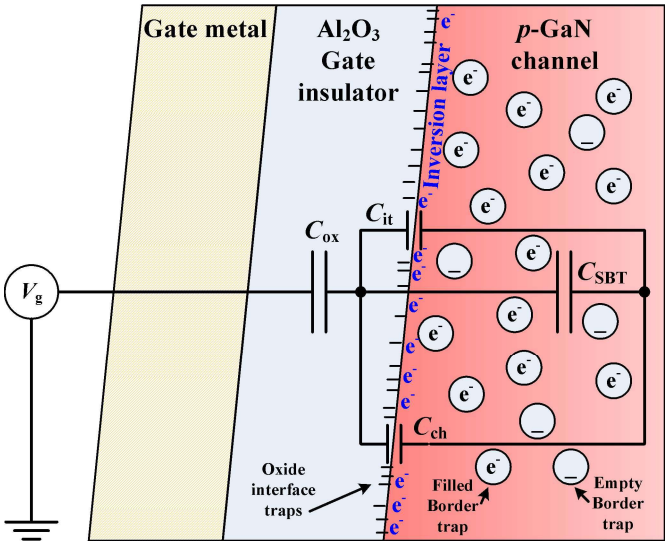

FIGURE 14. Illustration of the transistors gate during ON-state with the different natures of charges have to be considered and their respective capacitances equivalent circuit.

$$C_{gc} = \frac{C_{ox} \cdot (C_{ch} + C_{it})}{C_{ox} + C_{ch} + C_{it}} \tag{8}$$

C_{it} contribution to overall C_{gc} is only significant close to the threshold voltage where the channel inversion is weak. It is now better understood that for the Ammono "A" *a*-plane devices with the occurrence of strong channel inversion (large C_{ch}) the measured C_{gc} is approximately the oxide capacitance.

As compared to the *a*-plane devices, capacitance increase due to generation of the inversion layer is delayed in *m*-plane devices. It is assumed that under these bias conditions, additional charges get trapped in semiconductor border traps inside the *p*-GaN layer for the *m*-plane devices rather than contributing to the inversion channel. Note that charges inside the border traps, Q_{SBT} are immobile [8] and do not contribute to the inversion channel conductivity. The location of Q_{SBT} is distributed from the semiconductor-oxide interface into the *p*-GaN layer, which is why their associated capacitance C_{SBT} is less than C_{ch} for the same amount of induced charges. Eq. 8 then extends to

$$C_{gc} = \frac{C_{ox} \cdot (C_{ch} + C_{it} + C_{SBT})}{C_{ox} + C_{ch} + C_{it} + C_{SBT}} \tag{9}$$

In total, three different natures of charges have to be considered and their respective capacitances are illustrated in Fig. 14. The sketched situation can be found for the Ammono "A" *m*-plane devices in Fig. 5 for gate voltages between 2.5 and 4.5 V. Less charges get induced by the gate voltage step from 2.5 to 4.5 V for the *m*-plane device than for the *a*-plane device, because they contribute to the (smaller) C_{SBT} rather than for (the larger) C_{ch}, as it is the case for the *a*-plane devices. For V > 4.5 V, the inversion charges get also induced in the *m*-plane devices and – according

to C_{ch}–the capacitance slope is then (almost) similar to the *a*-plane devices. As consequence, the threshold voltage of the *m*-plane devices is shifted positively, because semiconductor border traps have to be charged first before the mobile inversion channel gets formed.

We can now distinguish between two types of parasitic trapping; gate oxide interface traps (which are similar for both orientations) and added sidewall semiconductor "border" traps [8] with non-mobile border charge Q_{SBT}. These semiconductor "border" charges have anisotropic nature and have significantly larger charge density towards the *m*-crystal face.

An analogous comparison can be made between the *a*-plane devices on the Ammono "A" and HVPE "A" substrates. Although in this comparison the gate oxide is deposited in the same process batch on both wafers the interface is not identical and so the epitaxial layers, still their properties are very similar. Here, oxide interface traps add similar amount of C_{it}, which is observed below the threshold voltage therefore both should have the same resulting positive threshold shift. However, the *a*-plane devices on the HVPE "A" substrate have a larger positive threshold shift and lower C_{gc} which means that here again C_{ch} is smaller and there are additional nnmobile negative charges stored in C_{SBT} in the semiconductor side of the interface. By comparing *a*- and *m*-plane devices on the HVPE "A" substrate the situation is extreme since the generation of the conductive inversion layer – associated to C_{ch} – can be hardly detected. Maximum C_{gc} for the *m*-plane devices is only 30% of C_{gc} of the *a*-plane devices since a significant amount of inversion charges fill the semiconductor border traps and the associated $C_{SBT} << C_{ch}$ reduces overall C_{gc} according to Eq. 9.

The observation that the sidewall "border" traps density is strongly linked to the substrate type and the crystal anisotropy may suggest the following hypothesis: As reported by the wafer manufacturers the different substrate crystals have significantly different defect and dislocation densities as reflected in the broadening of the XRD measurements rocking curve presented in Table 1. Along the epitaxial growth some of the crystal defects and dislocations coalesce but most of them propagate to the upper epitaxial layers. Shi *et al.* [35] calculated the piezoelectric polarization and its associated charge density for edge, screw, and mixed dislocations oriented parallel to the *c*-axis in wurtzite GaN which is the conventional growth direction. They showed that the edge dislocations produce polarization fields which have non-zero divergence at interfaces generating electric fields that will induce free charges in the material [35]. Gmeinwieser and Schwarz [36] show that stress-induced dipole-like states are detected around the dislocation core of edge- or mixed-type dislocations, with an angular orientation coinciding with the high-symmetry crystal directions. They show that a single strain-induced dipole field of unperturbed edge dislocations is oriented according to the six possible orientations of the Burgers vector given by the hexagonal crystal symmetry. The stress-related dipoles induced by edge dislocations have a preference in the $\langle 1\bar{1}00 \rangle$-directions, i.e., perpendicular to the *m*-plane [36]. Furthermore, Cherns *et al.* [37] showed that edge dislocations in *n*-doped GaN are highly negatively charged, whereas those in *p*-doped GaN are positively charged. They assume that the dislocations have one or more deep states in the band gap that pin the Fermi level. For *p*-GaN, electrons would flow out of a dislocation state and would cause band bending towards the valence band. A positively charged dislocation then creates polarization-induced acceptor-like traps [37]. Hence, it is suggested that an epitaxial *p*-GaN channel layer grown on a dislocation-rich GaN substrate has a higher density of polarization-induced acceptor-like traps than a similar layer grown on a substrate with low dislocation density. Further, an *m*-plane surface in a gate trench is much more prone to the same acceptor like traps than an *a*-plane surface. Therefore, *a*-plane devices on (high-quality) ammonothermal substrates have less defect-related negatively charged "border" traps than *a*-plane devices on HVPE substrates. And, *a*-plane devices on any of the substrates have less negatively charged polarization-induced acceptor-like traps than *m*-plane devices on the same substrate.

Fig. 8 (b) shows that the threshold voltage for devices, manufactured on all substrate types in both orientations remains almost unchanged with temperature up to 200 °C. This observation also holds for the devices that are significantly affected by a high amount of Q_{SBT}. The associated semiconductor border trap states can thus be considered as deep level acceptors in the upper level of the bandgap occupied by electrons. A temperature-dependent Q_{SBT} would lead to a threshold voltage shift.

Device characteristics on HVPE "C" are exceptionally different from the other substrates. Here, in comparison to the other substrates, low drain currents and high ON-state resistances are initially measured. In addition only small differences between the *a*- and *m*- plane devices are found. On the other hand, the charge carrier analysis (Section III) yields a large number of inverted mobile sheet charges for this wafer in both gate trench orientations, see Fig. 13. This implies a low semiconductor border trap density in the trench which is in good agreement with the reasonably high substrate quality, as indicated by the narrow reflection peak in HRXRD characterization (Table 1). One way to explain the discrepancy between the high amount of mobile channel charges and the small device current densities is by considering a large resistance component serial to the channel which scales linearly with the gate periphery dimensions. Since the measured source and drain layers TLM sheet resistances are identical for all wafers other epitaxial layers such as the drift region layer resistivity may be suspected as the root cause.

The obtained channel mobilities < 10 cm^2/V s for all measured devices are significantly smaller than channel mobilities reported for lateral GaN MIS-HFETs. For comparison, a channel mobility of 165 cm^2/V s was obtained for a lateral GaN true MOS device with gate oxide deposited on the *c*-plane etched GaN surface [38]. In vertical GaN

MISFET technology, oxide interface traps provide scattering sites that reduce the mobility. Additionally, a high concentration of positive interface charges in close contact with the *n*-channel will increase Coulomb scattering due to ionized impurities [39]. Since ionized impurities are also known to reduce electron mobility in lateral GaN MOSFETs [11], [40], the root cause for the very low trench MOSFET channel mobility must be different. Carriers under inversion conditions generally have reduced channel mobilities [29]. Coulomb scattering is limiting the mobility up to $V_{over} = 3$ V. Above this limit other mechanisms such as optical phonons and surface roughness-limited scattering start to have a larger effect in Si MOSFETs as well as in lateral GaN MISFETs [40]. For lateral GaN MOSFET Pérez-Tomás *et al.* [10] showed significant current and field-effect mobility increases with higher temperature. They showed that for low applied gate bias and low temperature the interface traps reduce mobility by Coulomb scattering, μ_C thus limits the conduction. The Coulomb scattering limited mobility increases significantly with temperature resulting in an increase of the MOSFET's ON-state conductance. The gate oxide in lateral GaN MOSFETs is deposited on an epitaxial *c*-plane layer which has a relatively low surface roughness. Therefore the surface-roughness limited mobility, μ_{sr}, is much higher than the μ_C in lateral GaN MOSFETs. In addition it is shown that μ_{sr} has a very weak temperature dependency in comparison to μ_C, μ_{sr} is only dropping slightly up to 500 K.

We have shown for all vertical GaN channel MISFETs on the different substrates and with the different gate orientations studied here that the mobility is decreasing slightly with temperature (Fig. 9). Such temperature dependence is in accordance the surface-roughness mobility but not the Coulomb mobility. Here, unlike the lateral MOSFET, the vertical channel surface is aggressively etched leaving a rough and damaged vertical surface. Even though some surface treatment process steps, i.e., BOE and TMAH wet etch, are introduced it is more than likely that the surface remains severely damaged which leads to a substantial reduction of the surface roughness-limited mobility, μ_{sr}, which then limits the overall mobility.

As shown in Fig. 9, *a*-plane devices still have a higher mobility than *m*-plane devices which may be explained by a lower surface roughness on the *a*-plane side wall. The observation that the presented devices' conduction parameters I_{ds_max}, $R^{-1}_{on\_rel}$, and g_{m_max}, similar to the effective mobility, weakly decrease with temperature (Fig. 9) points out that they are strongly limited by the surface roughness limited low mobility. It is previously reported, that anisotropic selective TMAH wet etching for long etch times (60 min) and at high temperatures (80 °C to 85 °C) leaves a smoother surface on the *m*-plane than on the *a*-plane and improves device output characteristics [14], [20], [21], [24]. At the same time it was shown that the *a*-plane surfaces are aggressively attacked by the wet etch leaving an extremely rough surface. Therefore, the surface roughness-limited mobility is expected much higher for *m*-plane devices than for *a*-plane devices. As consequence it appears that TMAH-etched *m*-plane devices own superior conductivity over the *a*-plane. However, in this work a very delicate low surface-damage ICP etch process prior to gate oxide deposition was developed. Such soft surface treatment leaves a surface with less roughness on the *a*-plane side wall resulting in higher surface-roughness-limited mobility, μ_{sr}. As a result the *m*-plane devices output characteristics are similar to previously reported devices but the *a*-plane devices own superior conductive properties.

V. CONCLUSION

In this systematic study we have investigated the ON-state conduction properties of the vertical GaN trench MISFET. They are limited by the coincidence of two main factors; the channel mobility and the mobile channel charge carrier density. The mobility for all types of devices is, in comparison to the bulk mobility, very low and limited by channel-trench side-wall roughness scattering. A large fraction of the gate-bias induced inversion charges in the channel is nnmobile due to trapping in semiconductor border traps that are most likely polarization-induced acceptor traps in nature, triggered by crystal defects. As a consequence, fewer electrons are available to serve as conductive inversion layer. For the devices presented in this article, less than 30% of all channel charges contribute to the transistor conduction and more than 70% of the energy transferred from the gate driver to the gate module is dissipated and does not contribute to drain current modulation.

Devices manufactured on ammonothermal GaN substrates with the gate trench etched along the *a*-plane crystal axis have demonstrated superior conduction properties. These are the result of a higher mobile charge carrier density in the channel, due to improved substrate crystal quality and reduced damage on the *a*-plane improved gate-trench surface, as compared to the other studied devices. Careful processing of the trench sidewall is required to prevent channel conductivity degradation.

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