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Wafer-Scale High-Quality Microtubular Devices Fabricated via Dry-Etching for Optical and Microelectronic Applications

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Mechanical strain formed at the interfaces of thin films has been widely applied to self-assemble 3D microarchitectures. Among them, rolled-up microtubes possess a unique 3D geometry beneficial for working as photonic, electromagnetic, energy storage, and sensing devices. However, the yield and quality of microtubular architectures are often limited by the wet-release of lithographically patterned stacks of thin-film structures. To address the drawbacks of conventionally used wet-etching methods in self-assembly techniques, here a dry-release approach is developed to roll-up both metallic and dielectric, as well as metallic/dielectric hybrid thin films for the fabrication of electronic and optical devices. A silicon thin film sacrificial layer on insulator is etched by dry fluorine chemistry, triggering self-assembly of prestrained nanomembranes in a well-controlled wafer scale fashion. More than 6000 integrated microcapacitors as well as hundreds of active microtubular optical cavities are obtained in a simultaneous self-assembly process. The fabrication of wafer-scale self-assembled microdevices results in high yield, reproducibility, uniformity, and performance, which promise broad applications in microelectronics, photonics, and opto-electronics.

Self-assembly as a common phenomenon to build hierarchically ordered structures widely exists in nature, ranging from nanoscale sizes such as protein folding up to microscale origami-like architectures. In contrast to the nanoscale where the self-assembly is driven by chemical functional group interactions, on the microscale strain engineering forms an elegant way to create 3D microstructures from lithographically patterned 2D thin films. Notorious examples are microcylinders,[1,2] cubes,[3] and other polyhedrons,[4] which have already found applications, for instance, in electronics,[5–7] photonics,[8,9] and biology.[10–12] Self-assembly by the roll-up of structured thin-film stacks into tubular "Swiss rolls" has been particularly successful in creating micromachined devices such as inductors,[13,14] capacitors,[15,16] microrobots,[17–19] and optical resonators[20–22] to only name a few. However, wet-release techniques that are used in the fabrication of these microtubular architectures often suffer from serious stiction and damage problems due to the presence of capillary forces and aggressive reagents, resulting in limited yield, reproducibility, uniformity, and an overall deterioration of the device performance. Although dry release methods have been explored by spontaneous delamination of layer stacks upon thermal annealing[23,24] or selective underetching in gaseous atmosphere,[25] well-controllable fabrication with high yield and quality on wafer-scale has not been reported so far. To address this issue, we present wafer-scale fabrication of high-quality microtubular devices via dry rolling of prestrained metal, dielectric, and/or metallic/dielectric hybrid nanomembranes from a silicon sacrificial layer, indicating broad applications in photonic and electronic applications compatible to complementary metal oxide semiconductor (CMOS) integration.

The fabrication procedure is schematically shown in **Figure 1**. The overall process is split into two main steps, namely patterning of thin films in a planar wafer scale fashion (Figure 1a) and dry release of strained thin films in plasma or gas phase atmosphere (Figure 1b). Owing to the high quality of the fabricated microtubular devices both, electronic applications, that is, rolled-up microcapacitors, and optical applications, that is, whispering gallery mode resonators, are demonstrated as examples (Figure 1c).

For the self-rolling of thin films, a strained film is deposited onto a sacrificial layer, where the strain can be created by varying the deposition rate during film growth. The strained bilayer possesses a compressive strain in the bottom layer (**Figure 2**a red) whereas a tensile strain in the top layer (Figure 2a green).

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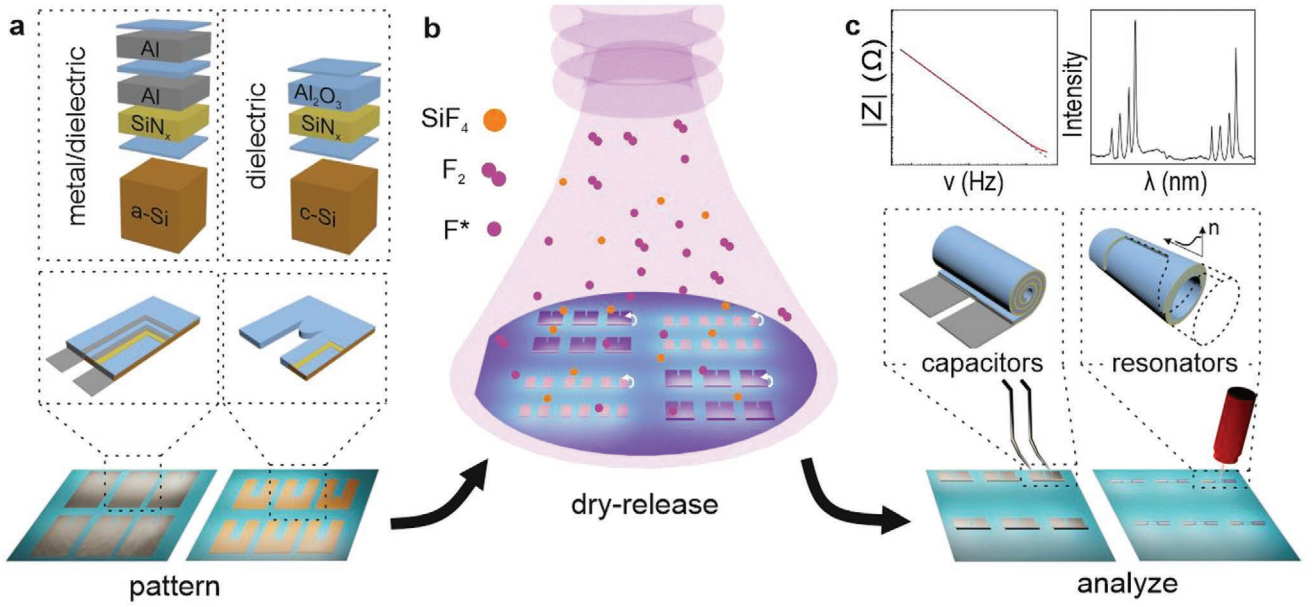

Figure 1. Schematic illustration of the fabrication of 3D microtubular devices via dry release at wafer scale. a,b) Different materials can be flexibly used to fabricate devices by the deposition and patterning of strained layer stacks (a), followed by the dry release in an isotropic plasma or gas phase etch (b). c) 3D microcapacitors and optical microresonators are demonstrated via the dry roll-up of metallic/dielectric and dielectric nanomembranes, respectively.

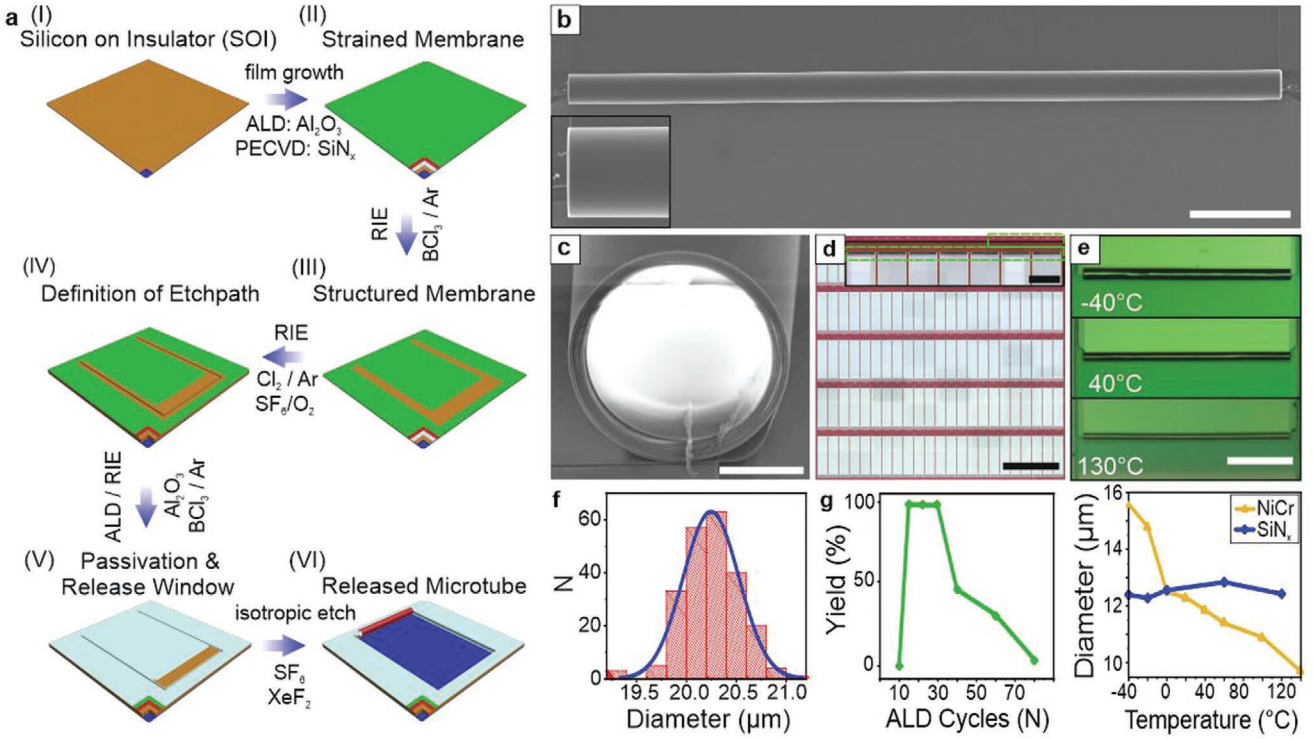

Figure 2. a) Schematic diagram showing the fabrication process with the cutout illustrating the layer stack (blue: SiO_2, brown: Si, white: Al_2O_3, red: compressive strained, green: tensile strained). b) SEM image of a rolled-up $Al_2O_3/SiN_x/Al_2O_3$ stack (scale bar 50 μm; inset 10 μm). c) SEM image from the side of a rolled-up microtube (scale bar 5 μm). d) Optical microscopy image of a chip with 115 SiN_x microtubes rolled over 2 mm length (scale bar 2 mm). Inset showing a magnification of a tube array (scale bar 400 μm). e) Top: optical images of NiCr tubes released at different etching temperatures (scale bar 100 μm). Bottom: diameter of SiN_x and NiCr microtubes as a function of etching temperature. f) Typical diameter distribution of fabricated tubes on a single chip. g) Yield dependence on the amount of ALD cycles for the passivation layer.

As such, the strained film will roll up to release the strain when the sacrificial layer is etched away. The fabrication starts with selecting and depositing a suitable sacrificial layer (e.g., Si, Ge, SiGe, Mo)[26–28] on an etch stop layer (Figure 2a-I). In this work, we use c-Si and a-Si as sacrificial layers which possess excellent properties such as chemical and mechanical stability, high temperature resistance, and high release rates compared to other dry methods like polymeric sacrificial layer etching by an O_2 plasma.[29] Silicon on insulator (SOI) commercial wafers provide a c-Si layer that can naturally act as the sacrificial layer and can be utilized simultaneously for on-chip integration. A strained bilayer, as illustrated in Figure 1, is deposited onto the sacrificial layer (Figure 2a-II) and patterned by standard lithography techniques (Figure 2a-III). In the following step, trenches are etched into the sacrificial layer (Figure 2a-IV) and the whole sample is passivated by atomic layer deposition (ALD) with sub-3 nm Al_2O_3. The starting rolling edge is defined by opening a release window via reactive ion etching (RIE) (Figure 2a-V). The sample is then subjected to an isotropic silicon etching process to release the strained nanomembranes, performing simultaneous self-assembly of microtubular structures (Figure 2a-VI) on the whole wafer. In this step, the fluorine radicals or XeF_2 molecules react with silicon atoms to form gaseous SiF_4. As a result, the strained nanomembranes are released to form microtubular structures in a dry environment. Scanning electron microscopy (SEM) images for the main steps can be found in Supporting Information. High yield and high quality self-assembly of the rolled-up structures crucially depend on a proper starting edge (Figure 2a-V) as well as a very thin guiding Al_2O_3 passivation layer (Figure 2g). A sub-3 nm thick Al_2O_3 layer allows for easy and continuous ripping while preventing undesirable etching from the pattern sides. This design leads to a deterministic, directional, and long-distance roll-up process,[16] reducing rocking and tilting motions, thus suppressing the formation of voids and slidings between different windings. SiN_x was shown previously as a material with a well controllable strain gradient enabling the self-assembly of rolled-up structures.[30,31] Figure 2b shows an SEM image of a typical self-assembled SiN_x microtube with excellent alignment, as well as dense and almost void-free windings (Figure 2c). Twelve SiN_x microtube samples fabricated on 10 × 10 mm dies and arranged in 23 × 13 arrays showed a yield of 98.4 %. Figure 2d shows an optical image of SiN_x microtubes with a yield of 99.1% for structures with a 2 mm rolling length. We also obtained high-quality microtubular structures with a narrow diameter distribution of around 20.25 µm ± 0.28 µm (Figure 2f). For metal nanomembranes, we observe a strong dependence of the tube diameter on substrate temperature during the layer release. As shown in Figure 2e, the tube diameter decreases by more than 37% when the temperature is changed from −40 to 130 °C. This phenomenon can be explained by the different temperature expansion coefficients of Ni ($\alpha = 13.4 \times 10^6\ K^{-1}$) an Cr ($\alpha = 4.9 \times 10^6\ K^{-1}$),[32] which introduces an additional thermal stress into the strained bilayer. For SiN_x microtubes, the diameter stays almost constant over the whole analyzed temperature region. In this case, there is no significant thermal expansion mismatch in the nanomembrane, therefore leading to only a weak temperature dependence of the tube diameter. In the following, we fabricate and characterize 3D microcapacitors and optical microresonators by rolling up metallic/dielectric and dielectric hybrid nanomembranes, respectively. In these devices, a SiN_x layer provides the necessary strain gradient due to its strong compressive stress in the GPa range in comparison to dielectric ALD films and sputtered metal layers, which only show moderate tensile strain in the MPa range.

3D microcapacitors were fabricated onto a 4" wafer (**Figure 3**a) with a-Si as the sacrificial layer. The devices consist of a strained 100 nm layer stack of $Al_2O_3^{4nm}/SiN_x^{30nm}/Al^{30nm}/Al_2O_3^{8nm}/Al^{30nm}/Al_2O_3^{3nm}$ with a >94% rolling yield. For the preparation of metal plates and contact pads, aluminum was selected due to its excellent processability, CMOS compatibility, as well as electrical performance, which improved the frequency response of the rolled-up capacitors compared to previous reports.[16] Alumina was chosen as a dielectric as well as protection layer owing to its stability in fluorine chemistry and high dielectric constant. A patterned wafer with thousands of rolled-up devices organized in arrays is shown in Figure 3a. Figure 3b shows a map of a 4" wafer with arrays of microcapacitors. Electrical characterization of all devices by an automated probe station at 1 kHz documents a yield of working devices exceeding 91 %, among which 99.9 % fall within the E12 (C = 2.7 ± 10 % nF), 91.3% within the E24 (C = 2.9 ± 5 % nF), 81,9 % within the E48 (C = 2.87 ± 2% nF), and 49,6 % within the E96 (C = 2.87 ± 1 % nF) industrial standard according to IEC/EN 60062 (Figure 3d–g). Individual capacitors shown in Figure 3c were characterized by four probe measurements from 40 Hz up to 110 MHz showing close to ideal performance up to 350 kHz (Figure 3h–j).

The capacitors have a capacitance of around 2.85 nF (47.8 µF cm^{-2}) (Figure 3h) and are stable up to 3 V. The complex impedance plot is shown in Figure 3j. In its double logarithmic coordinate, a linear behavior is observed for the complex impedance in the range of 40 Hz to 10 kHz, which is caused by the rolled-up spiral structure and the high sheet resistance of the thin metal plates. At higher frequencies between 10 kHz and 10 MHz, just a small area of the rolled-up structure contributes to the capacitance until the total transversal sheet resistance of 16 Ω is reached. Another distributed capacitance region is observed between 10 and 100 MHz, which is likely due to a small capacitor formed between the contact pads, the oxide layer, and the silicon substrate. At 110 MHz, the contact resistance is around 1.3 Ω.

Optical microtube resonators further confirm the high quality of the structures fabricated by the dry self-assembly method. The devices were fabricated on an SOI wafer with a 10-µm-thick c-Si layer as the sacrificially layer. The layer stack consists of $Al_2O_3^{4nm}/SiN_x^{30nm}/Al_2O_3^{30nm}/Al_2O_3^{3nm}$ with an average refractive index of 1.8, where $Al_2O_3^{3nm}$ acts as a guiding layer for rolling up the strained membrane. The average refractive index was calculated based on the refractive index of every layer and the corresponding layer thickness. For the rolled-up optical whispering gallery mode resonators, the silicon nitride layer acts not only as a compressively strained layer, but also provides a broad photoluminescence (PL) spectrum due to luminescent nitrogen edge states.[33] The microresonators were rolled up from U-type membrane patterns, resulting in a free-standing segment at the tube center (see **Figure 4**b). Moreover, a lobe structure was designed at

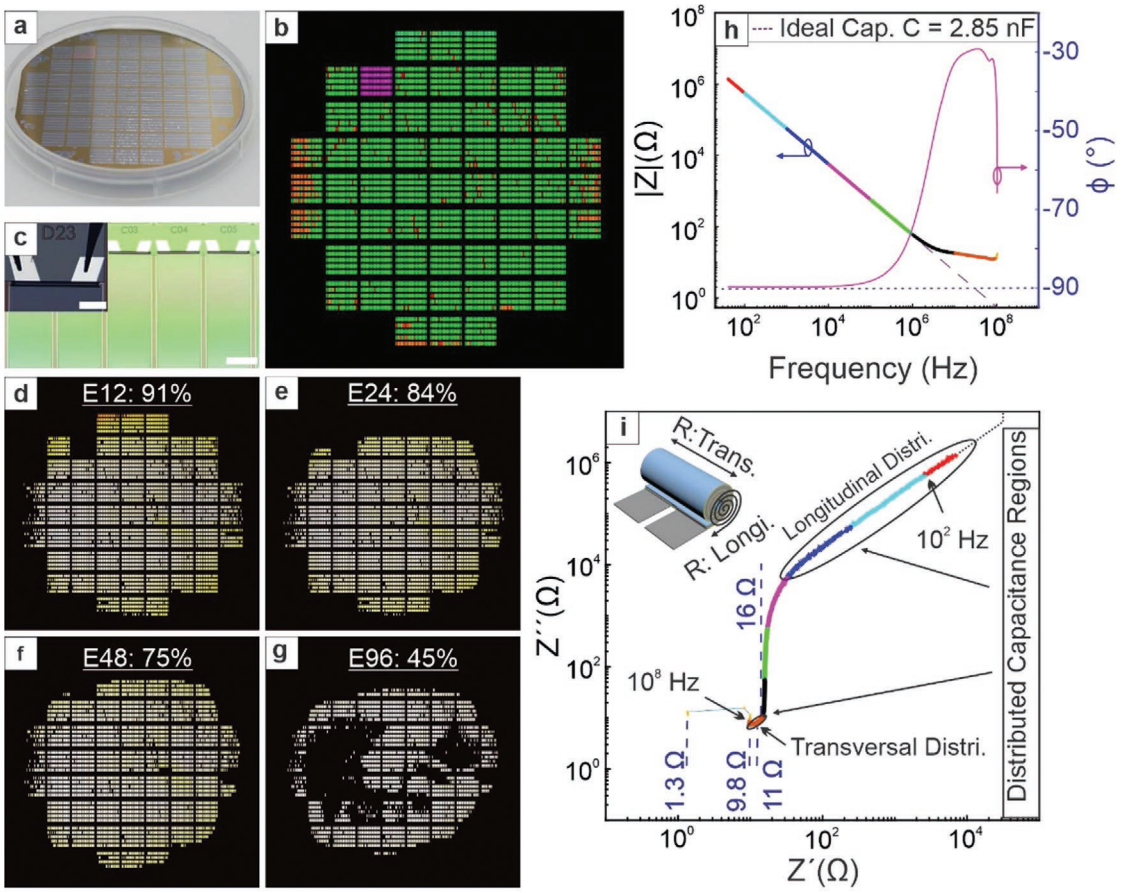

Figure 3. Microcapacitor. a) Image of a wafer consisting of 6495 rolled-up capacitors on 60 chips. b) Wafer map of electrically characterized devices with red indicating faulty devices ($-85° < \phi < 0°$), green marking functional devices ($-90° < \phi < -85°$), orange representing $\phi > 0$, and pink labeling chip open circuit calibration. c) Optical image of rolled-up capacitors (scale bar 200 µm). Inset shows electrical characterization of an individual microcapacitor (scale bar: 100 µm). d–g) Maps showing the yield within different quality standards E12–E96 according to IEC/EN 60062. h) Bode plot of a typical device and its corresponding complex impedance plot. j) Each color change represents a change of frequency by one order of magnitude. The transversal sheet resistance is located at 16 Ω and the contact resistance at 1.3 Ω.

the center of the tube, which provides a refractive index gradient along the axis to generate an axial confinement for the resonant modes.[21] Atomic force microscopy (AFM) measurements reveal wafer quality surface roughnesses of 0.18 nm on the outer tube surface and 0.27 nm on the inner surface (Figure 4b bottom). An SEM image of a typical sample is shown in Figure 4a with a magnification of the central lobe region shown in Figure 4b. The central free-standing segment with approximately 2.7 windings and an average thickness of 190 nm is used to support optical resonances. The optical cavities are characterized by a standard laser confocal setup, where the silicon-rich nitride layer is excited by a solid-state laser emitting at 457 nm. The resonant transverse electric (TE) modes are shown in Figure 4c. The resonant modes show a Q-factor up to 7800 at ≈955 nm, which is the highest value ever reported for active rolled-up resonators.[34] The Q-factors slightly decrease toward shorter wavelengths, which is attributed to an increased absorption in the SiN_x as well as increased scattering at higher frequencies.

In summary, a deterministic well-controlled CMOS compatible process for the preparation of rolled-up microdevices is demonstrated on wafer scale. The process flow is easily realized with standard tools used in commercial production lines for electronic and photonic chip integration. The dry release from a silicon sacrificial layer is controlled by the deposition of an ultra-thin selective guiding layer that helps to guide the roll-up. A customized design of trenches and opening windows enables the simultaneous self-assembly of thousands of devices on a single wafer. We demonstrate that this novel release scheme yields excellent uniformity and reproducibility for fabricating high quality rolled-up microcapacitors. An 84% yield of microcapacitors are well within the E24, and 91% are within the E12 industrial standard of IEC/EN 60062. For photonic components, we show that active optical microtube resonators exhibit optical resonances in a broad spectral range with record high Q-factors >7800. The process quality can be further enhanced in an industrial fabrication line due to superior cleanness and optimized deposition processes aiming for an even higher yield of micro-capacitors within the most demanding E96 standard. This approach can be applied to other materials such as III–V and II–VI compounds for the fabrication of microelectronic and optical device via dry release. Our work represents a

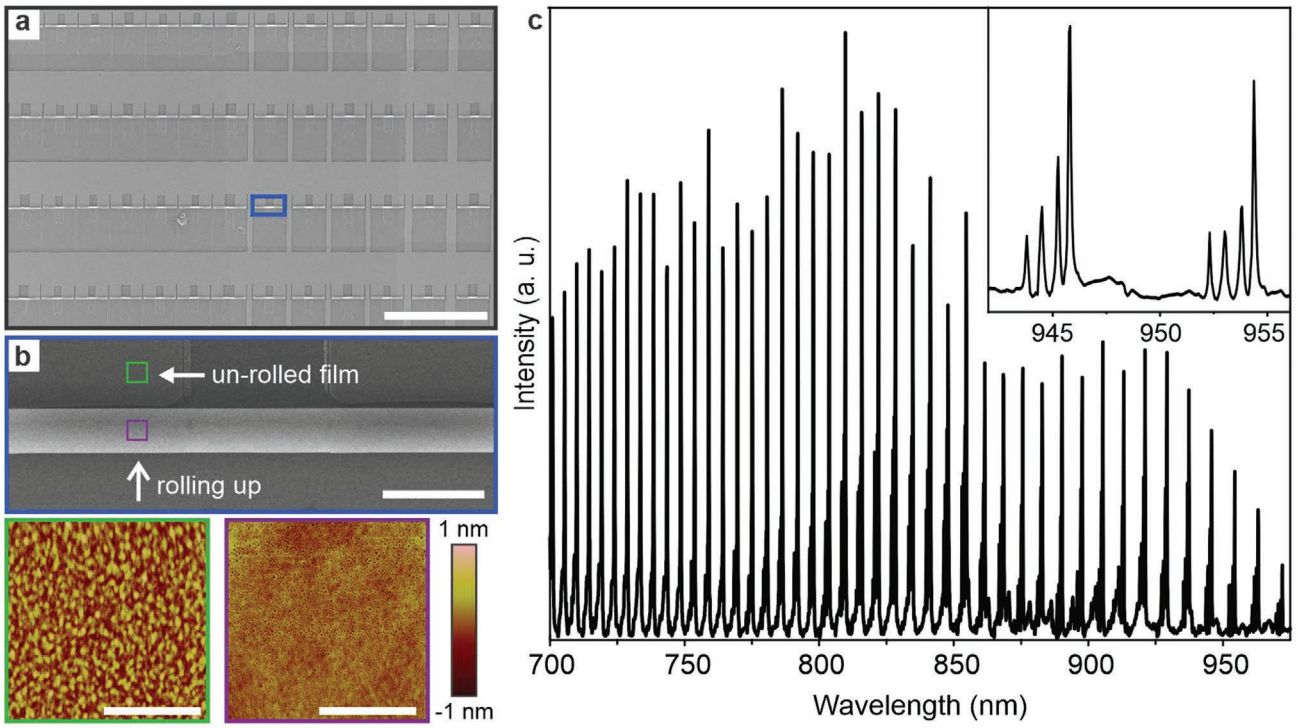

Figure 4. Optical resonators. a) SEM image of optical microtube resonator array (scale bar: 1000 µm). A single microtube resonator marked in blue frame is shown in (b) with a scale bar of 60 µm. AFM measurements of the upper film surface (green frame), which represents the inner microtube surface, and out microtube surface (purple frame) show a roughness of *R*q = 0.27 nm and *R*q = 0.18 nm, respectively. The scale bar in AFM images is 1 µm. c) Photoluminescence spectrum of a series of resonant modes emitted from a rolled-up microtube resonator. Inset shows two groups of resonant modes together with higher order axial modes. The peaks have a width down to 0.126 nm at the full with half maximum, which corresponds to a Q-factor of up to 7800.

major step toward on-chip mass integration of 3D electronic, photonic, optoelectronic, and micro/nanoelectromechanical systems relying on guided self-assembly of multifunctional nanomembranes.

Experimental Section

Substrates: Silicon on insulator wafer (SOI), handling layer: 600 µm, buried thermal oxide (BOX): 1 µm, device layer of 10 µm <100> N/Ph, $R < 5\ \Omega$, (ULTRASIL cooperation, Hayward, CA, USA); silicon wafer 4'', silicon wafer: 525 µm < 100> P/B, $R = 10–20\ \Omega$, wet oxide 1.5 µm, (SIEGERT WAFER GmbH, Aachen, Germany).

Lithography: Samples were cleaned by immersion in DMSO, acetone, and isopropyl alcohol (VWR, Darmstadt, Germany); degassed on a hotplate (130 °C); and cleaned in O_2–plasma (Pico, Diener electronic GmbH, Ebhausen, Germany). Photoresist (1.4 µm) was spun onto individual dies at 4500 U min^{-1}. Pattering was performed by a maskless aligner (MLA 100, Heidelberg Instruments Mikrotechnik GmbH, Heidelberg, Germany). After pattering, the resist was inverted by a 3 min post baking at 120 °C and flood illumination.

Capacitors: A 550 nm a-Si sacrificial layer was deposited onto a 4'' wafer; following the sacrificial layer deposition, groves and markers were etched by RIE into the sacrificial layer utilizing chlorine chemistry, to place the contact pads directly onto the oxide. The whole wafer was than coated by 4 nm PEALD Al_2O_3 followed by SiN_x 30 nm and 30 nm aluminum (2.14 Å s^{-1}) metal plates were deposited by lift-off and sputter deposition onto the strained membrane, (HZM-4P, IvA, Dresden, Germany). The dielectric between the first and second metal plate consisted of 8 nm Al_2O_3 (74 cyc., 280 °C, TMA, O_2) and was deposited by PEALD. After the deposition of the second metal plate, the strained device was structured by RIE and passivated by ALD. A starting edge was defined by RIE and the devices were released utilizing the SF_6 process for about 2 h. The release progress was monitored with a standard microscope by removing the sample every 30 min from the chamber.

SiN_x Microtubes: A 4 nm thick Al_2O_3 was deposited onto an a-Si sacrificial layer by PE-ALD (FlexAL, Oxford Instruments PLC, Abingdon, UK) to act as a passivation for the SiN_x during roll-up. SiN_x was deposited by ICPECVD SI 500 D (Sentech Instruments GmbH, Berlin, Germany). By changing the ICP power and the bias, the diameter could be easily adjusted. The membranes were structured by RIE (Plasma Lab 100; Oxford Instruments PLC, Abingdon, UK) utilizing chlorine and fluorine chemistry and released by an Isotropic SF6 etch, (Plasma Lab 100; Oxford Instruments PLC, Abingdon, UK) or a gas phase etch (Xactix e2; Orbotech LTD., Yavne, Israel).

Devices: Optical resonators were fabricated onto the top of an SOI wafer due to the better surface finish of the polished substrate. Onto the cleaned Si surface, a 4 nm PEALD Al_2O_3 was deposited followed by 30 nm SIN_X and 30 nm ALD Al_2O_3. The membrane was structured by RIE, and grooves etched into the Si layer until the buried oxide was reached by DRIE. Following DRIE, the sample was passivated by 2.5 nm Al_2O_3. The resonators were released utilizing the SF_6 process.

Sample Characterization: Atomic force microscopy was taken with an ICON AFM (Bruker, Billerica, MA, USA). Scanning electron microscopy images were taken on a DSM982 GEMINI at 5 kV (Carl Zeiss Microscopy GmbH, Jena, Germany). Optical characterization was performed with a confocal photoluminescence setup at an excitation wavelength of 405 nm (LabRAM HR Evolution, Horiba Ltd., Kyoto, Japan). Two-probe characterizations were performed in a probe station (Summit 12000; Cascade Microtech Inc., Beaverton, OR, USA) using a precision LCR Meter

(E4980A Agilent Technologies Inc., Santa Clara, CA, USA) at a constant voltage of 500 mV. Four-probe characterizations were performed in a probestation (PSM 6 Süss MicroTec Garching, Germany) at 500 mV with a bias from 0–3 V utilizing a Precision impedance analyzer (4294A Agilent Technologies Inc., Santa Clara, CA, USA).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

dry release, microcapacitors, roll-up, self-assembly, whispering gallery mode resonators

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