X-ray Nanodiffraction on a Single SiGe Quantum Dot inside a Functioning Field-Effect Transistor

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ABSTRACT: For advanced electronic, optoelectronic, or mechanical nanoscale devices a detailed understanding of their structural properties and in particular the strain state within their active region is of utmost importance. We demonstrate that X-ray nanodiffraction represents an excellent tool to investigate the internal structure of such devices in a nondestructive way by using a focused synchotron X-ray beam with a diameter of 400 nm. We show results on the strain fields in and around a *single* SiGe island, which serves as stressor for the Si-channel in a fully functioning Si—metal—oxide semiconductor field-effect transistor.
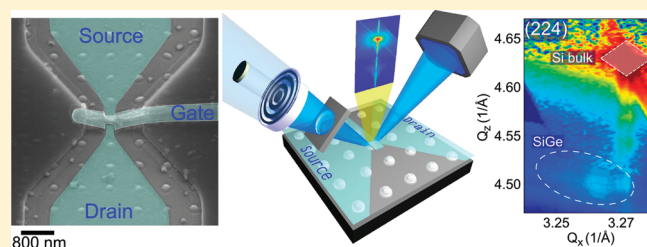
KEYWORDS: X-ray nanodiffraction, semiconductor nanostructures, structural investigations, finite element simulations, ordered island growth, silicon germanium

The design of advanced electronic and optoelectronic devices is increasingly based on nanostructures. To tune device characteristics at the frontiers of scaling, strain engineering is a versatile tool to overcome restrictions or tailor material properties.[1,2] Despite the fact that the understanding and application of strain are vital to several research fields,[3−9] it is still quite challenging to precisely assess strain and its influence on device characteristics. Transmission electron microscopy (TEM) is often considered the only available technique providing at the same time the required spatial and strain resolution to map strains at the nanoscale, within single devices or single nanostructures.[10,11] Especially in the case of fully processed devices, the drawback of these methods is the necessity of a specific sample preparation (use of grids, lamellaes) and the impossibility of accessing nanostructures in their functional environment, with a nondestructive approach. X-ray diffraction (XRD) techniques are nondestructive and compatible with thick heterogeneous samples and offer elemental sensitivity, large penetration depth, and high strain resolution. For devices, where structures are buried below insulating and contacting layers, the fact that X-rays easily penetrate such layers makes them an ideal tool to investigate buried nanostructures. However, analysis so far has required large ensembles of identical structures due to the typical size of X-ray beams being so large that many nanostructures contribute to the scattered X-ray intensities, leading to ensemble-averaged data. Often, the

interesting part of the device is built around a *single* nanostructure and represents only a very small portion of the area. In this case the scattering signal contributed by the object of interest is averaged out or hidden by the scattering from the rest of the area. With focused X-rays this usually insufficient spatial resolution of XRD can be overcome. Recent development of X-ray sources, focusing of hard X-rays,[12] and experimental setups for nanopositioning enable the exclusive probing of very small areas in the submicrometer range, while maintaining the advantages of XRD: in particular these methods are nondestructive with high strain resolution below 0.1%.[13−15] Focused beams with sizes ranging from a few micrometers down to below 100 nm are currently available on several beamlines at third generation synchotron sources and are used to gain valuable information on single nanostructures[16−21] or small ensembles, e.g., SiGe quantum dot molecules,[22] or to map strain and composition within a single nanostructure[23] or device (in this case with a spatial resolution in the range of 2 μm).[24]

Here, we apply this advanced characterization method to explore the structural properties and the strain field in a fully processed strained Si n-channel metal—oxide—semiconductor
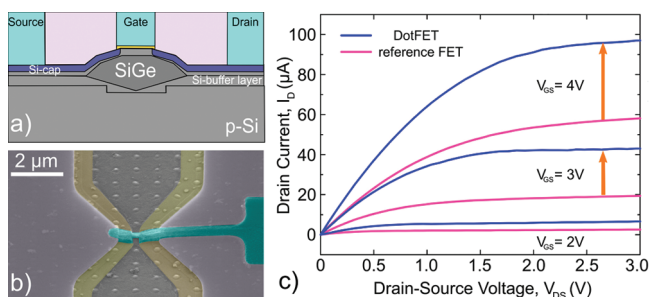
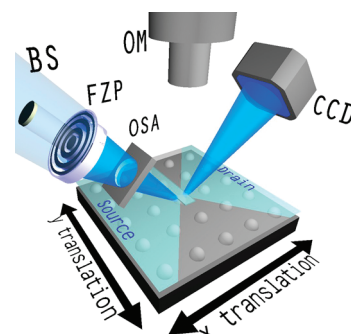**Figure 1.** Sketch of the transistor layout. (a) The blue area within the Si cap layer represents the conducting, As-implanted areas. (b) A SEM image of the central part of the transistor junction. The image was taken after the etching of the gate finger (light blue) which is aligned precisely to one of the islands. The As-implanted silicon cap layer corresponding to the source and drain area (gray) is yet free without contacts attached, so the pattern of the buried quantum dot array is still visible. The violet marked area is the SiO_2 isolation layer, the region marked yellow the remaining SiO_xN_y dielectric. (c) Output characteristics at three different source−gate voltages for such a device with a gate length of 150 nm and a gate width of 300 nm are shown (blue) in comparison to a reference FET without SiGe dot as stressor for the channel (magenta).


Figure 2. Schematics of the focusing setup and the sample as it was mounted on the sample stage with respect to the beam direction. On the primary beam side, a setup consisting of a beamstop (BS), a Fresnel zone plate (FZP), and an order sorting aperture (OSA) was applied to focus the beam and eliminate higher diffraction orders of the zone plate. An optical microscope (OM) was mounted for a rough alignment of the sample. The sample itself is mounted on a piezo stage for precise positioning with respect to the incident X-ray beam for both lateral directions (x and y translation) as well as in vertical direction.

field-effect transistor (MOSFET). To speed up Si transistors, depending on the geometry of the device either tensile (for n-type) or compressive strain (for p-type) can be applied to the silicon channel of MOSFETs.[4,6] Tensile strain values are typically of the order of 0.3% for transistors utilizing $Si_{1-x}Ge_x$ stressors[6,7] and even higher for devices with both $Si_{1-x}Ge_x$ underneath the Si channel and $Si_{1-y}C_y$ in the source drain regions.[8] To enhance the tensile strain, a concept has been proposed which relies on a SiGe dot ("dot", derived from the term quantum dot, although due to the size of those structures, no 3D carrier confinement effects occur) positioned below the channel of a Si transistor as illustrated in Figure 1a. The 3D geometry of the dot enables a higher degree of elastic relaxation for the $Si_{1-x}Ge_x$ alloy and therefore provides much larger tensile strain to the Si lattice on top of it without introducing dislocations. This enhanced tensile strain significantly affects the conduction band structure and enhances the mobility of electrons in the channel, giving this type of MOSFET, the so-called dotFET a better speed performance.[25,26] The electrical evaluation of this transistor was performed by comparing it to nonstrained reference devices processed on the same wafers but without dots: the dotFET showed an increase of drain current between 20 and 60% (see Figure 1c).[27] The quantum dots required for this device have to be grown on a regularly patterned Si substrate, as following processing steps have to be tuned precisely to the position of one specific island. Therefore, unlike previous investigations by XRD, it becomes mandatory to perform the diffraction experiment only on one *single* island. Additionally it is required that specifically the island below the transistor gate must be aligned into the X-ray beam. Beside this precise alignment, a further challenge for the success of this experiment is the small scattering volume provided by a single SiGe island with a diameter of 250 nm and a height of 52 nm. We show that we were able to find the desired single island by means of scanning X-ray diffraction (SXD)[16] techniques and record the reciprocal space maps (RSM) needed to base strain calculations on. We also gain insight on how device fabrication affects the structural properties of the Si channel between source and drain.

For the fabrication of the devices, 4 in. Si(001) wafers were used with a sample layout fitting the requirements for both island growth and subsequent transistor processing:[27]

- Patterning of the Si substrate: within square-shaped fields of 300 μm sidelength 2D arrays of pits with a period of 800 nm were defined by electron beam lithography (EBL) and reactive ion etching (RIE). On one such field, one transistor device is situated.
- Epitaxial growth by MBE: the successive growth of a 36 nm Si buffer layer (at a temperature increasing from 450 to 550 °C) and 6 ML of Ge at 720 °C resulted in the formation of dome-shaped SiGe islands with a diameter of 250 nm and a height of 52 nm (aspect ratio 0.2) with one island per pit.[28] The capping with 30 nm Si was performed at a lower temperature (360 °C) to avoid intermixing with the buried SiGe island.[29−31]
- Deposition of a SiO_2 isolation layer by plasma-enhanced chemical vapor deposition (PECVD) at 400 °C, removal of the isolation by RIE in the source, gate, and drain areas.
- Gatestack: the gate consists of a 15 nm thick SiO_xN_y gate dielectric (deposited by inductive coupled plasma enhanced chemical vapor deposition at 250 °C) and the 150 nm Al(1% Si) gate layer deposited by physical vapor deposition (PVD) at 50 °C.
- To activate the source/drain areas, they were implanted with As^+ ions at a dose of 10^{15} cm^{-2}. A single shot from a XeCl excimer laser (λ = 308 nm) was applied to melt and recrystallize the damaged Si volume.
- After the removal of excessive gate material, a second 800 nm thick SiO_2 isolation layer was deposited by PECVD at 400 °C. The source and drain area were then opened again and contacted by depositing a 905 nm thick Al(1% Si) layer at 350 °C. To connect the device to the metal pads, Al(1% Si) metal tracks with a thickness of 1.4 μm were fabricated as seen in the SEM image shown in Figure 3a.
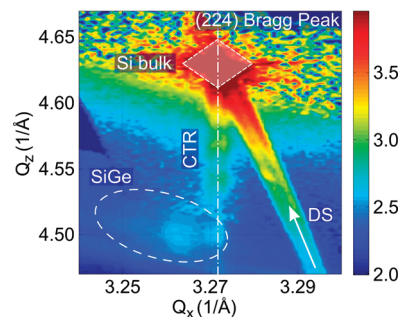
A sketch of the transistor is shown in Figure 1a. The whole device setup is precisely centered around a single island, the alignment of the gate finger with respect to that island can be seen in the scanning electron microscopy (SEM) image in Figure 1b.
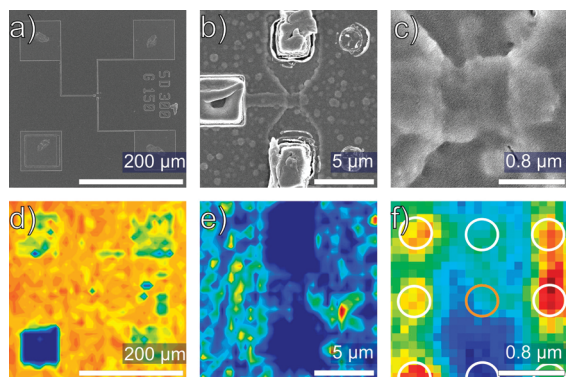
Figure 3. (a−c) SEM images of the investigated dotFET device at different magnifications. The irregular spotty surface is due to a thin Au layer deposited prior to SEM measurements to avoid charging. Panels d−f show according images obtained in scanning X-ray diffraction (SXD) mode at the same scale. For the first map shown in (d) the diffractometer was tuned to the diffuse Si signal around (004) to find the transistor junction with the focused beam. The fine-tuning was done using the SiGe (224) dot signal as shown in (e) and (f) to locate the island positions. Image (e) shows a further alignment map to find the center of the transistor junction. The source and drain patches are visible as dark areas where the signal from the dots is attenuated. In image (f) the individual island positions are visible as well-defined spots of higher intensity (marked by circles). The position of the center dot (orange circle) can be clearly determined, it is weaker due to absorption by the gate stack on top of the dot.


Figure 4. Reciprocal space map around the vicinity of the (224) Bragg peak measured on the SiGe dot beneath the transistor gate. The map includes the Si (224) bulk peak (labeled Si) as well as the SiGe dot signal (SiGe) in the lower left section of the map. The feature along the vertical direction marked by the dashed-dotted line represents the crystal truncation rod (CTR). The detector streak (DS) marked by an arrow indicates frames with higher intensity due to enhanced air scattering when the goniometer passes the position of the intense Si Bragg peak during the scan. The color bar shows the decadic logarithm of the intensity in counts per second. Q_z and Q_x denote reciprocal space coordinates along the [001] and [110] directions, respectively.

X-ray experiments were carried out at beamline ID01 at the ESRF in Grenoble at an energy of 8 keV. The setup is sketched in Figure 2: A gold Fresnel zone plate (FZP) of 200 μm diameter and 100 nm outmost zone width is used as focusing element.[32] The individual zones of the FZP introduce a phase shift of π for the part of radiation traversing through the Au rings, thus acting as a phase grating. A 60 μm diameter beamstop is placed before the FZP to eliminate the transmitted beam. A 50 μm order sorting aperture (OSA) is placed close to the sample position to block higher diffraction orders from the FZP.[23] The resulting effective focus diameter, which is also influenced by beamline instabilities such as mutual vibrations of FZP and sample stage, was 400 nm FWHM. At an incidence angle of 34.7° for the Si(004) or 79.6° for the (224) Bragg peak, the footprint of the beam on the sample is smaller than the period of the patterned SiGe dot array, which was 800 nm. This is true for the intense central part of the focused beam, but especially at lower incidence angles a very small contribution to the scattered intensities may arise due to neighboring islands illuminated by the beam tails. For the alignment of the setup and recording reciprocal space maps a Maxipix CCD camera was employed.

Several challenges are inherent to the diffraction experiment on a single island: first of all, the diffracted intensity is rather at the limit of detection due to the small island volume.[33] Another crucial part of the experiment is the identification of the island beneath the transistor gate as the alignment has to be done using the focused X-ray beam itself. Thus a characteristic signal of the structure of interest has to be identified and the sample position scanned to determine the position of the X-ray focus on the sample. In this case it is straightforward to directly use the Bragg peak of the Si and SiGe alloy, respectively.[16] In order to locate the transistor, the diffractometer angles are first tuned to the diffuse scattering signal around the Si (004)/(224) bulk peak. With the

goniometer thus tuned to the Si peak, the sample is then translated laterally (denoted as x and y translation in Figure 2) while recording the peak intensity. Panels a−c of Figure 3 show SEM images of scanned areas with the according SXD maps underneath them. As the Si signal is attenuated when metal lines of the transistor are moved into the incident beam, such a scan results in a real-space map of the sample surface as seen in Figure 3d. The four square-shaped metal patches used as contacts for the device are clearly visible as darker green/blue areas of low intensity, and hence the center of the transistor can be located. In a second step, the goniometer was tuned to the expected position of the scattering signal originating from the SiGe islands, and by again mapping the intensity distribution in real space, the location of the islands was detected (Figure 3e,f). Note that along the vertical axis of the SDX image (Figure 3f) the dot signals appear weaker in SXD, due to absorption by the thicker metalization layers on top of them.
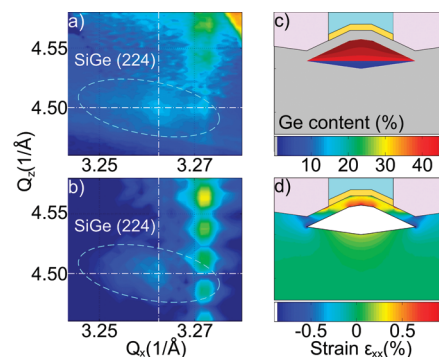
With the center dot located, the sample position was kept fixed to record a reciprocal space map as shown in Figure 4. The map includes the Si (224) bulk peak (labeled Si) which is used as internal standard for data correction. The rather diffuse signal (SiGe) in the lower left section of the RSM originates from the SiGe island. From the position of this signal in reciprocal space an average Ge content of 45% was derived. The oscillations of the crystal truncation rod (CTR) indicate a thickness of about 24 nm for the Si-capping layer. The streak (DS) marked by an arrow indicates the position of the CCD detector in reciprocal space, those specific frames with higher intensity are a result of enhanced air scattering when the goniometer passes the position of the intense silicon Bragg peak during the scan. Due to the hollow-cone-like property of the focused incident beam, well-defined features such as the CTR, the Si bulk peak, or the detector streak (DS) appear to be split in lateral direction.

To quantify the strain in the Si channel above the island in the transistor, we used the COMSOL Multiphysics[34] package for finite element method (FEM) calculations. To verify the strain data, simulations of the X-ray intensity distribution using kinematical diffraction theory[35] were performed based on the displacement fields obtained by the FEM calculations for comparison with
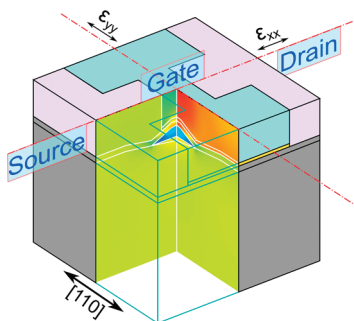
Figure 5. Sketch of the model geometry used for FEM calculations with a faceted island in a pit, covered by a 24 nm Si cap layer. The model as well includes the 15 nm thin gate dielectric layer (yellow), the Al gate finger (light blue), and the SiO$_2$ isolation layer (violet). In the cut-open sections strain fields are displayed as an example, the map for ε_{xx} is oriented along the middle of the channel between source and drain which corresponds to the crystallographic [110] direction, the one for ε_{yy} perpendicular to the source–drain direction.

Figure 6. Comparison of experimental (a) and simulated data (b) based on the FEM model presented in this paper. In the maps only the region around the diffuse SiGe (224) signal is shown. (c, d) 2D maps of the Ge concentration and the in-plane strain ε_{xx} as results of the FEM calculations. For clarity, the strain field is shown only for the Si cap and substrate. Both maps are oriented along the middle of the channel between source and drain which corresponds to the crystallographic [110] direction.

the experimental data on the single island. Such a comparison of an experimental and the according simulated RSM are shown in panels a and b of Figure 6, respectively. The FEM model contains the epitaxially grown components of the transistor structure, namely, the SiGe island and the Si cap, as well as the SiO$_x$N$_y$ layer representing the gate dielectric, the Al(1%)Si-gatefinger, and the SiO$_2$ isolation, which directly contribute to the strain state of the buried SiGe island (see Figure 5). Further elements of the transistor setup such as source and drain contact patches or metalization lines were not taken into account since their contributions to the strain in the island and the channel are negligible. The classical dome-shaped geometry containing {105}, {113}, and {15 3 23} facets[36] for the buried quantum dot and the shape of the Si capping layer were derived from an AFM analysis of uncapped and capped samples grown under the same conditions[28] and are in excellent agreement with TEM images shown by Jovanović et al.[27] Resonant Raman spectroscopy experiments on buried SiGe islands grown on *flat* Si substrates revealed a considerable interdependence of the strain within the Si capping layer and its thickness.[37] To check whether the transistor processing had an influence on the channel material, the thickness of the Si-capping layer was determined directly from features seen in the RSM recorded on the finished transistor. The period of the X-ray intensity oscillation along the crystal truncation rod yields the thickness of the buried Si capping layer, which was found to be only about 24 nm, instead of the nominal value of 30 nm. This thickness was used for the FEM model geometry. As the final structure contains not only epitaxially grown components (Si buffer layer, SiGe quantum dot and Si cap layer), but additional layers as described above, the process of calculating the strain state is divided into several steps as well.[38] The first step contains the crystalline sections grown by MBE: the Si substrate, a dome-shaped SiGe island and the Si capping layer. In the successive three steps the SiO$_x$N$_y$-gate dielectric, the Al-gatefinger, and the SiO$_2$ isolation filling up the empty volume are added separately as they have no epitaxial relation to the Si/SiGe sections of the transistor. For those nonepitaxial components individual initial strain values resulting from differences in the thermal expansion coefficient were applied to take into account mutual straining during annealing and cooling steps within the fabrication process. For the island a SiGe alloy with a Ge content varying from

0 to 5% along the z direction was used in the pit area and a realistic onion-skin-like Ge distribution with a Ge content of 43% at the bottom and 48% at the top was applied for the upper dome-shaped part of the island (see Figure 6c), resulting an average Ge content of about 40% for the whole SiGe structure including pit and island.

As it turns out, both the gate stack and the SiO$_2$ isolation layer do have some influence on the strain distribution in the Si cap. With the gatefinger and the SiO$_2$ isolation layer, two components are directly connected which behave quite differently when heated during the process flow. For a fully processed device, maximum tensile strain values (ε_{xx}) of 1% are achieved in the source–drain direction within the active region of the Si cap. Due to the geometry of the Al-gatefinger and its interaction with the SiO$_2$ layer, it applies compressive strain to the Si cap directly underneath the gate, which leads to a local decrease of the strain in the Si cap layer down to about 0.3% and a reduction of the effective channel thickness (see strain map shown in Figure 6d). The shape of the Al gatefinger actually leads to higher strains in the direction perpendicular to source–drain but slightly reduces the strain in the source–drain direction. If in the same model the gate stack is omitted, the strain values in the active region of the Si cap vary between 0.8 and 1.25% and are distributed more homogeneously. This result shows that in order to further improve transistor characteristic, optimizing the shape and material combinations of the whole gate stack is essential. In general, scattered X-ray intensity distributions are very sensitive to slight deviations in the Ge distribution or to externally applied stress that can also be reproduced in X-ray calculations based on FEM models. Considering the divergence of the X-ray beam due to the focusing setup, the experimental resolution is about 0.0025 Å^{-1}, corresponding to an error bar of approximately 2% for the Ge content. This renders X-ray diffraction a technique which is able to detect even small changes in the strain distributions.

In conclusion, we have successfully applied X-ray diffraction with a beam focused to 400 nm diameter to determine the strain state and structural properties of the Si n-channel above a single buried SiGe island in a fully functioning field-effect transistor. The experimental data were obtained without need for any sample preparation, leaving the investigated device in its operational state.

Tensile strain values up to 1% along the source—drain direction were determined in the Si channel using reciprocal space mapping and finite element calculations. With the method presented in this paper valuable insight is gained into the interactions of nanostructures with additional components necessary for operational devices. This information can be used to optimize future device generations. The presented work opens the road for further, even more advanced studies like monitoring devices during operation or the investigation of processes in devices during breakdown at elevated current levels or temperatures. Even the modifications during particular process steps, especially high-temperature ones, can be assessed "online". Such studies will become even more powerful when using advanced analysis schemes such as model-free phase retrieval approaches by exploiting the coherence properties of nanofocused X-ray beams.[39]

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