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# Selective Lateral Germanium Growth for Local GeOI Fabrication

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High quality local Germanium-on-oxide (GeOI) wafers are fabricated using selective lateral germanium (Ge) growth technique by a single wafer reduced pressure chemical vapor deposition system. Mesa structures of 300 nm thick epitaxial silicon (Si) interposed by $SiO_2$ cap and buried oxide are prepared. HCl vapor phase etching of Si is performed prior to selective Ge growth to remove a part of the epitaxial Si to form cavity under the mesa. By following selective Ge growth, the cavity was filled. Cross section TEM shows dislocations of Ge which are located near Si / Ge interface only. By plan view TEM, it is shown that the dislocations in Ge which direct to $SiO_2$ cap or to buried-oxide (BOX) are located near the interface of Si and Ge. The dislocations which run parallel to BOX are observed only in [110] and [1–10] direction resulting Ge grown toward [010] direction contains no dislocations. This mechanism is similar to aspect-ratio-trapping but here we are using a horizontal approach, which offers the option to remove the defective areas by standard structuring techniques. A root mean square of roughness of ∼0.2 nm is obtained after the $SiO_2$ cap removal. Tensile strain in the Ge layer is observed due to higher thermal expansion coefficient of Ge compared to Si and $SiO_2$.
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Germanium (Ge) is a very attractive material for optoelectronic applications and for future CMOS technologies, because of direct bandgap of Γ valley at 0.8 eV. However lattice constant mismatch between Ge and silicon (Si) leads to high density of misfit dislocations and threading dislocations, which degenerate electrical properties (e.g. increase of dark current for optoelectronics applications).[1] Therefore the creation of Ge on Si with low defect density is of great interest. Several techniques to grow high quality Ge on Si are reported e. g. in combination with thermal cycling,[2,3] cyclic annealing and etching,[4,5] aspect ratio trapping[6] and nano hetero epitaxy.[7] On the other hand, for optoelectronic devices, Ge-on-insulator (GeOI) substrate is widely used. Wafer bonding technique[8] and Ge condensation method[9] are applied for GeOI wafer fabrication. However, in order to integrate Ge lasers / photodiodes into CMOS technology, local GeOI in Si-on-insulator (SOI) substrate is preferred because both Si-based devices and Ge-based devices are required. For local GeOI fabrication, epitaxial lateral overgrowth using $GeCl_4$[10] is reported. However, chemical mechanical polishing process is required to planarize the deposited Ge.

In this study, a technique of high quality local GeOI fabrication using selective growth of Ge to lateral direction in cavity covered by $SiO_2$ is presented. The cavity was formed by selective Si sidewall etching[11] of a mesa-patterned $SiO_2$ / Si / buried oxide stack. High quality and smooth Ge surface without using chemical mechanical polishing process are demonstrated. The strain distribution in the Ge layer is also discussed.

## Experimental

Lateral Ge growth is carried out by using a single wafer reduced pressure (RP) chemical vapor deposition (CVD) system. For sample preparation, epitaxial Si is deposited on SOI wafer of (001) orientation to adjust Si on buried oxide thickness to 430 nm. Then wet oxidation is performed to produce a 300 nm thick $SiO_2$ cap on top of 300 nm thick Si on the buried oxide (BOX). After that the $SiO_2$ cap is patterned by photolithography and etched by buffered HF to form mesa structure. Checkerboard mesa structures and line and space structures with [110] and [010] oriented sidewalls are fabricated.

After that, the wafer is cleaned by standard RCA cleaning followed by HF last dip. Then the wafer is loaded into the RPCVD reactor and baked at 850°C in $H_2$ to remove residual oxide on the Si surface. Then selective HCl vapor phase etching (VPE)[9] is performed at 850°C to etch Si surface around the mesa and form a cavity under the mesa by lateral Si etching. About 1.5 μm of lateral cavity interposed by $SiO_2$ is formed by selective HCl VPE. Afterwards Ge is deposited selectively in the cavity using a $H_2$-$GeH_4$ source gas at 650°C. To ensure selectivity, small amount of HCl is also added during the selective Ge epitaxy.

Scanning electron microscope (SEM) is used for characterization of the deposited Ge. Scanning transmission electron microscope (STEM) is applied for dislocation analysis. For STEM sample preparation, focused ion beam (FIB) is used to cut out a lamella at center of the mesa structure. The FIB lamella is cut out perpendicular to the sidewall orientation for both [110] and [010] oriented mesa structures.

STEM high-angle annular dark field (STEM-HAADF) image is used for characterizing interface of Ge and Si. Nano beam diffraction (NBD) and micro Raman spectroscopy at 514 nm laser wavelength are used for strain distribution analysis in Si and Ge layers. The Raman shift of the Ge-Ge mode $\omega_{Ge\text{-}Ge}$ in the Ge layer and the Si-Si mode $\omega_{Si\text{-}Si}$ in the Si were measured with respect to the phonon mode energies $\omega^0_{Ge\text{-}Ge}$ and $\omega^0_{Si\text{-}Si}$ as measured in Ge(001) and Si(001) reference bulk crystals respectively. The equivalent in-plane biaxial strain $\varepsilon^{bi}$ was calculated using the relationships.[12,13]

$$\varepsilon^{bi}_{Ge} = \frac{\omega_{Ge-Ge} - \omega^0_{Ge-Ge}}{-390} \quad [1]$$

$$\varepsilon^{bi}_{Si} = \frac{\omega_{Si-Si} - \omega^0_{Si-Si}}{-830} \quad [2]$$

## Results and Discussion

Figure 1a and Fig. 1b show an angle view and cross section SEM image of the sample after HCl VPE, respectively. By the HCl VPE, the Si around $SiO_2$ mesa structures and Si between the BOX and the $SiO_2$ cap are removed. A ∼1.3 μm to ∼1.5 μm deep cavity is formed by the HCl VPE. The thickness loss of the BOX and the $SiO_2$ cap are not visible indicating that this HCl VPE process is highly selective to $SiO_2$. No bending is observed at the floating part of the $SiO_2$ cap layer. At the etch front of Fig. 1b, a (331) facet is observed. In the case of line and space structure with [110] sidewall, no (331) facet but only a (111) facet were observed. The different etch front formation of the mesa structure seems to be caused by various HCl VPE directions. The HCl VPE starts from four different sidewalls and corners. Because the etch rate of the corner is faster compared to straight sidewall region, the orientation of the facet becomes not only (111) but also additional non-parallel orientations to [110] sidewall. The sample of Fig. 1b is cut at the position whose sidewall is not perpendicular to the cross section surface.

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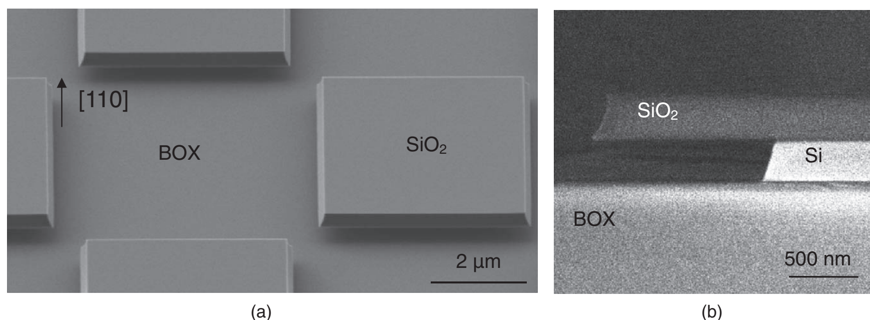


**Figure 1.** Angle view (a) and cross section (b) SEM images of sample after HCl VPE. The orientation of the sidewall is parallel to the [110] direction.

A cross section STEM image of the sample after HCl VPE and selective Ge growth is shown in Fig. 2. In Fig. 2a, the sidewalls are parallel to [110] and in Fig. 2c parallel to [010] direction. Close up images of interface between Si and Ge of Fig. 2a and Fig. 2c are shown in Fig. 2b and Fig. 2d, respectively. The Ge layers are selectively grown laterally on the Si sidewall in the cavity formed by the HCl VPE. No polygrain formation is observed in the cavity in Fig. 2a and Fig. 2c. That shows that the deposition process is highly selective. In Fig. 2c, smaller width of the epitaxial Si pillar after etching is observed compared to that of the mesa structure with [110] sidewall (Fig. 2a) indicating faster etch rate during the HCl VPE. For both samples, complex interface which contains (111), (331), (−331) and (−111) is observed between Si and Ge in Fig. 2b and Fig. 2d. The complex interface seems to be caused by HCL VPE of various etching direction in the mesa structure due to four sidewalls and corners. The sidewall of Si is not perpendicular to the TEM lamella. Dislocations are densely located in the Ge near the interface between Si and Ge for both [110] and [010] direction (Fig. 2b and Fig. 2d). The dislocations in Ge are directed to [111] or [11–1]. Aspect ratio trapping[5] works for the lateral direction, resulting in a high crystal quality Ge layer growth. The defects are located in the first ∼150 nm of the layer.

Figure 3a and 3b show plan-view STEM images of a 5 µm square mesa structure with [110] and [010] sidewall after HCl VPE and lateral Ge growth, respectively. For both cases, high density dislocation networks are located near the Si interface only. These high density dislocations are also observed in the cross section STEM images in Fig. 2a – 2d, so they are directed to $SiO_2$ cap or BOX. Long dislocations which run parallel to BOX are observed also. The long dislocations run direct to the [110] and [1–10], independently on the sidewall orientation of mesa structures. Therefore a wide Ge area without any dislocations is formed toward [010] direction.

In Figure 4, an AFM surface roughness image of the 5 µm square mesa structure with [010] sidewall direction is shown after the HCl VPE and the lateral Ge growth followed by removal of the $SiO_2$ cap by buffered HF dip. The interface between Si and Ge is visible. A step between Si and Ge surface of about ∼0.5 nm is observed. The step formation is mainly caused by the cap layer removal. The root mean square of roughness (RMS) of Si and Ge surfaces are ∼0.2 nm and ∼0.19 nm, respectively. In the case of vertical Ge growth on Si, low temperature seed Ge layer is required to realize smooth surface.[4] However, in this case, the low temperature seed Ge deposition process to form two-dimensional smooth surface[4] is not required for the selective lateral Ge growth, because the surface of the GeOI is determined by surface roughness of $SiO_2$ cap layer after the HCl VPE process. That gives additional advantage to improve throughput by operating higher growth rate condition at higher temperature.

The strain distribution plots of Si and Ge measured by micro Raman mapping are shown in Fig. 5a and Fig. 5b, respectively. In the Si pillar, ∼0.09% of tensile strain is observed (Fig. 5a). This tensile

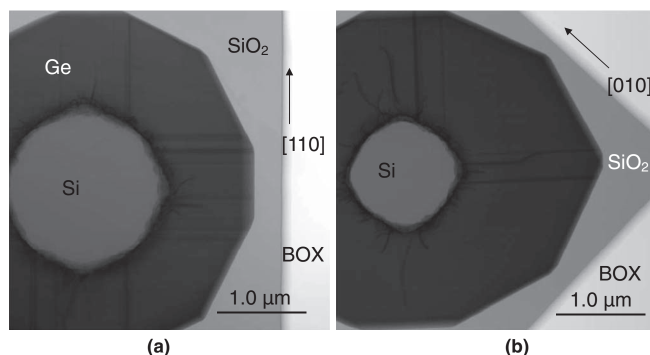


**Figure 3.** Plan-view STEM image of 5 µm square mesa structure with (a) [110] and (b) [010] sidewall direction after HCl etching and lateral Ge growth. The sidewall orientation is described with arrow.

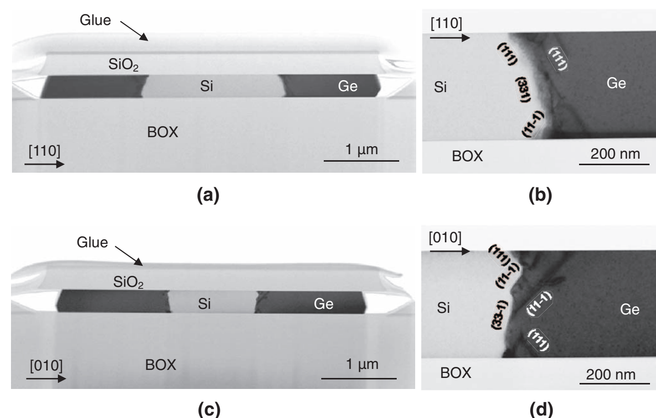


**Figure 2.** Cross section STEM images after HCl VPE followed by selective Ge deposition. Orientations of the sidewall of (a) and (b) are parallel to [110] direction and (c) and (d) are parallel to [010] direction. Higher magnification images near interface between Si and Ge are shown in (b) and (d).

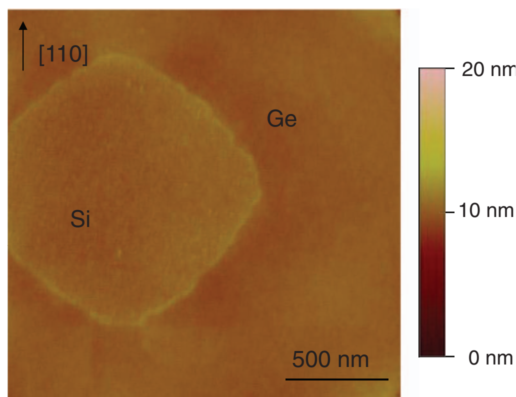


**Figure 4.** AFM surface roughness image of 5 µm square mesa structure with [010] sidewall direction after HCl VPE, lateral Ge growth and removal of the $SiO_2$ cap by buffered HF. The [110] direction is indicated by the arrow.

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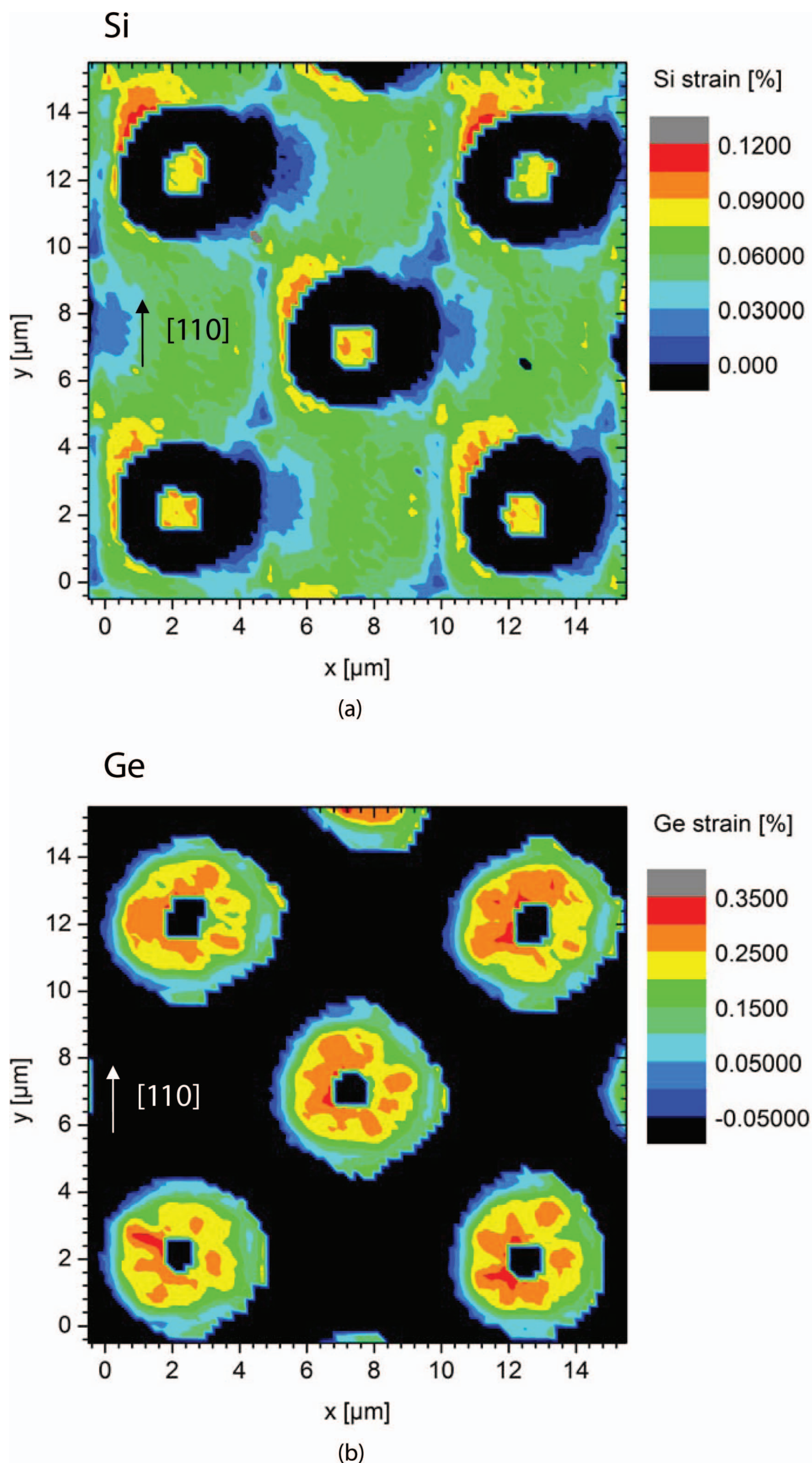


**Figure 5.** Strain distribution of (a) Si and (b) Ge of mesa structures by micro Raman spectroscopy. Mesa structures with [110] sidewall orientation are shown. [110] direction is indicated by arrow.

strain level in the Si pillar was also detected from the sample after HCl VPE (before selective growth of Ge). However, no strain in Si on BOX was evidenced in wide plain area of the same wafer, which is located outside of the checkerboard mesa array structure. These results are indicating that the Si on the BOX is not initially strained. Because the interface area between the Si pillar and $SiO_2$ is small, the Si pillar seems to be slipped during the HCl VPE at 850°C due to thermal expansion coefficient difference between Si ($\sim 4 \times 10^{-6}$ $K^{-1}$) and $SiO_2$ ($\sim 5 \times 10^{-7}$ $K^{-1}$). The tensile strain in the Si pillar could be formed during cooling period after the HCl VPE. On the other hand, the Ge around Si pillar is also tensely strained (Fig. 5b). The degree of strain is ~0.25% to ~0.3%. The strain of the Ge layer near the edge is weaker compared to that near interface to the Si pillar. Possible cause of the strain compensation could be a slight bending of $SiO_2$ cap layer,

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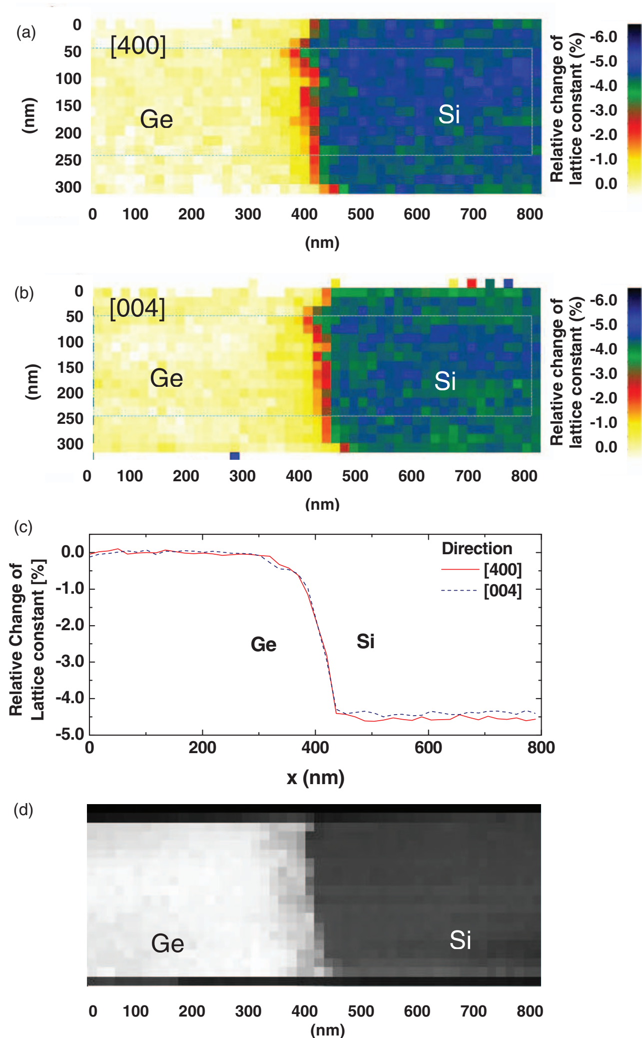


**Figure 6.** Relative change of lattice constant of (a) [400] and (b) [004] direction by NBD. Relative lattice constant of [400] and [004] obtained by NBD image is shown in (c). STEM HAADF image near Si and Ge interface is shown in (d). Ge part is used for internal reference for lattice constant calibration.

because $SiO_2$ cap layer near the edge of the mesa is floating. Even though the maximum temperature during the Ge growth is 650°C in this case, which is lower than conventional Ge growth on Si with cyclic annealing at 800°C,[3,4] the tensile strain in the Ge around the Si pillar is higher (~0.25%) compared to the conventional Ge growth on Si (~0.14%). The possible source of additional tensile strain in the Ge seems to be the tensile strain in the Si pillar.

Figure 6a and 6b present mapping of relative change of lattice constant of lateral ([400] direction) and perpendicular ([004] direction) to substrate by NBD measurement, respectively. For calibrating the lattice constant, Ge part is used for internal reference. For both Si and Ge, the distribution of the lattice constant in the vertical direction is uniform indicating an almost constant strain in z direction. The relative differences of lattice constants of the Si [400] direction and the Si [004] direction are −4.6% and −4.4%, respectively. That means the degree of strain in the Si part is shifted to compressive direction compared to the strain in the Ge. With the support of micro-Raman results (Fig. 5a, 6b), it is possible to conclude that the Si pillar is tensely strained and the degree of the tensile strain is lower compared to that in the Ge part. The curves of the relative lattice constant of [400] and [004] direction (averaged in dotted square in Fig. 6a and Fig. 6b) are almost parallel for both the Ge and the Si part (Fig. 6c). This indicates constant strain in lateral direction for both Si and Ge for 400 nm from the interface at least. These results also support the micro Raman measurement already shown in Fig. 5a and 5b. In Fig. 6c, a small reduction of lattice constant in Ge near Si / Ge interface is observed. STEM-HAADF image (Fig. 6d) shows a contrast change in Ge near the interface, indicating presence of Si in the Ge near the interface. Because process temperature is below 650°C, no or very few Si diffusion in Ge is expected. It seems that the interface between Si and Ge of the STEM lamella is not perpendicular to the lamella. In this case the lower lattice constant of Ge at the interface is caused by projection of non-straight Ge / Si interface.

## Conclusions

High quality local GeOI wafers are fabricated using selective lateral Ge growth technique by a single wafer RPCVD system. Mesa structures of 300 nm $SiO_2$ cap and Si on BOX with [110] and [010] oriented sidewall are prepared. Selective etching of Si by HCl followed by selective lateral Ge growth is performed. Lateral aspect-ratio-trapping is working in the Ge layer resulting in prevention of dislocation formation after ~150 nm from the Si interface. Dislocations along the Ge growth direction are oriented only in [110] and [1–10] directions. Therefore a wide area of Ge without dislocations is grown toward [010] direction. The deposited Ge exhibit a smooth surface. Tensile strain in the Ge layer is observed due to thermal expansion coefficient difference between Si and Ge. Higher degree of the strain is observed because of additional tensile strain in Si pillar. These results demonstrate the feasibility of the fabrication of local GeOI with high crystal quality. Defective part can be removed by an additional lithography and an etching process.

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