ECS Journal of Solid State Science and Technology, 4 (7) P195-P199 (2015)

Dislocation Generation and Propagation during Flash Lamp Annealing

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Dislocation generation and propagation during flash lamp annealing for 20 ms was investigated using wafers with sawed, ground, and etched surfaces. Due to the thermal stress resulting from the temperature profiles generated by the flash pre-existing dislocations propagate into the wafer from both surfaces during flash lamp annealing. A dislocation free zone was observed around 700 μm depth below the surface of a 900 μm thick sawed wafer. The dislocation propagation can be well described by a three-dimensional mechanical model. It was further demonstrated that in wafers being initially free of dislocations no dislocations are generated during flash lamp annealing.

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Manuscript submitted March 17, 2015; revised manuscript received April 9, 2015. Published April 24, 2015. This was Paper 1639 presented at the Cancun, Mexico, Meeting of the Society, October 5–9, 2014.

During the last years, thermal processing on the millisecond scale was developed first of all for the creation of shallow dopant profiles in high end electronic device technologies and for the thermal treatment of layers.[1,2] Flash lamp anneals (FLA) or laser anneals are able to heat the silicon wafer within a few milliseconds to temperatures up to the melting point. Depending on the irradiance of the flash, this can cause strong thermal gradients in the wafers inducing thermal stress which can generate defects.[2]

The aim of our investigations was to investigate dislocation generation and propagation during FLA. In addition, we modeled the temperature distribution and stress in a silicon wafer subjected to FLA and compared it to experimental results of dislocation propagation. The results of modeling help to understand the experimental results.

Experimental

The experimental flow can be seen in Fig. 1. The wafers used for the experiments were 150 mm in diameter and of a resistivity of about 10 Ωcm. The concentration of interstitial oxygen was in the range of $6.9–7.1 \times 10^{17}$ cm^{-3} (DIN 50438/1, new ASTM F121-83).

In order to investigate dislocation generation and propagation during FLA, wafers of different surface state were prepared. Part of the wafers, 900 μm in thickness, was just sawed, another part was also ground down to a thickness of 750 μm, and the remaining part was also etched after grinding down to a thickness of 680 μm. After subjecting these wafers to FLA for 20 ms in nitrogen, (110) cleavage planes perpendicular to the surface were etched by Secco etchant for 3 min for dislocation delineation.[3]

The FLAs were carried out for 20 ms with a normalized irradiance of 0.97 using the flash annealing tool of the Institute for Ion Beam Physics and Materials Research of the HZDR. A tool for flash annealing usually contains both, halogen lamps for pre-heating and xenon lamps for the flash. Descriptions of typical tools for flash lamp annealing can be found in Refs. 1 and 2. In our case, the wafer was pre-heated for about 2 min from the back side by halogen lamps up to a temperature of 800°C. This helps to reduce the thermal gradients, the wafer stress, and reduces the energy required by the flash to reach a certain temperature. Then, the flash was initiated by the xenon-lamps energized by discharging a capacitor unit. The wafer was placed between two quartz plates under a nitrogen gas flow during FLA. Because we used a 100 mm flash tool, squares of 100 mm diagonal length corresponding to 70.7 mm side length were cut from the 150 mm wafers and annealed in the flash tool.

It was confirmed in Ref. 2 that the flash intensity is proportional to the square of the voltage to which the capacitors are charged. We increased the voltage up to the point where the surface starts melting. In this way, we got the normalized irradiance which is the ratio between the squared voltage and the squared voltage necessary for melting a polished surface. The duration of the flash refers to the half width of the flash intensity.

Modeling

Thermal model.— This model describes the temperature T as a function of the time t and the depth from the wafer surface x. The model is based on the one dimensional heat diffusion equation

$$\rho C_p \frac{\partial T}{\partial t} = \frac{\partial}{\partial x}\left(k \frac{\partial T}{\partial x}\right) + \dot{q} \quad [1]$$

with the volumetric heat capacity ρC_p, the thermal conductivity k, and the rate of heat generation per unit volume $\dot{q}$. The volumetric

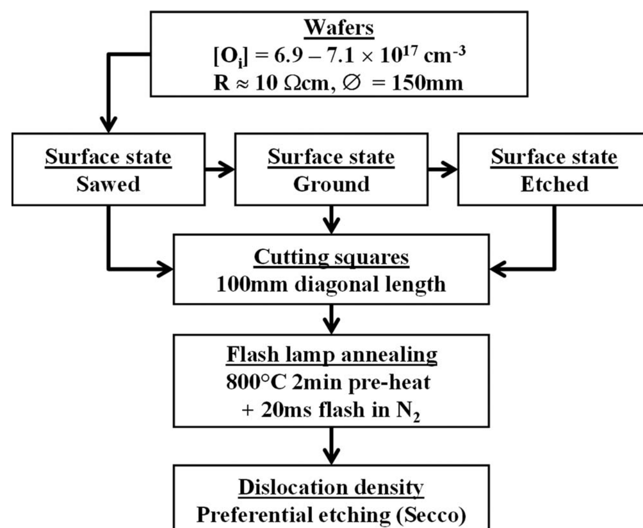

Figure 1. Experimental flow for the investigation of dislocation generation and propagation during flash lamp annealing.

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heat capacity and thermal diffusivity were inserted into the model by fitting curves to the experimental values taken from Ref. 4.

For the heat generation by the flash, a simplified approach was used. A typical intensity profile of a 20 ms flash lamp pulse can be found in Ref. 2. The intensity I is given in arbitrary units. We have adjusted the heat generation per unit volume by a factor F in the way that a certain maximum surface temperature is reached after applying the model. We further assumed that the radiation of the flash penetrates into the surface. Then we get

$$\dot{q} = I \times F \times \exp(-ax) \quad [2]$$

with a being the absorption coefficient. A typical flash lamp spectrum is shown in Ref. 2. For simplicity, we used the absorption coefficient for a wavelength of 550 nm which is the mean wavelength. Here, the absorption coefficient is 6.4×10^3 cm^{-1}.[5] There are no drastic changes in the absorption coefficient for the whole wavelength range of the flash spectrum.

Because the wafer is pre-heated for flash annealing, the simulation of the temperature profile in the wafer is started at the time $t = 0$ with a temperature which is equal to the temperature of pre-heating T_{pre} and independent of the depth. This means that the initial condition is as follows

$$T(x, 0) = T_{pre} \quad [3]$$

The boundary conditions for the front surface and the back surface of a wafer of the thickness d are defined by convection, radiation, and heat generation as follows

$$-k \left.\frac{\partial T}{\partial x}\right|_{x=0} = h\left[T_\infty - T(0,t)\right] + \varepsilon\sigma\left[T(0,t)^4 - T_\infty^4\right] - I \times F \quad [4]$$

$$-k \left.\frac{\partial T}{\partial x}\right|_{x=d} = -h\left[T_\infty - T(d,t)\right] - \varepsilon\sigma\left[T(d,t)^4 - T_\infty^4\right]. \quad [5]$$

The first term describes the heat loss by convection and the second term the heat loss by radiation. The temperature of both the surrounding and the gas flow T_∞ was assumed to be room temperature. The convection heat transfer coefficient h was assumed to be 10^{-3} W K^{-1} cm^{-2} which corresponds to a medium level of cooling by convection. The temperature dependent emissivity ε was taken from Ref. 6 and the Stephan-Boltzmann constant σ is 5.67×10^{-8} W m^{-2} K^{-4}.

Mechanical model.— The mechanical model is based on the equations of mechanical equilibrium for a volume element in classical linear elasticity theory and Cartesian coordinates *x, y, z* as follows:

$$\begin{aligned}
&\frac{\partial \sigma_x}{\partial x} + \frac{\partial \tau_{xy}}{\partial y} + \frac{\partial \tau_{xz}}{\partial z} + F_x = 0\\
&\frac{\partial \tau_{xy}}{\partial x} + \frac{\partial \sigma_y}{\partial y} + \frac{\partial \tau_{yz}}{\partial z} + F_y = 0\\
&\frac{\partial \tau_{xz}}{\partial x} + \frac{\partial \tau_{yz}}{\partial y} + \frac{\partial \sigma_z}{\partial z} + F_z = 0
\end{aligned} \quad [6]$$

with σ_i and τ_{ij} being the normal and shear stress components, respectively. The directed body forces F_i are assumed to be zero. This means that also gravitational forces are neglected here. This was done because in the experiments only small squares of 100 mm diagonal length placed on several quartz strips were used where gravitational stress is of negligible impact. The gravitational forces are important e.g. if the impact of certain wafer carriers on the stress distribution in large wafers during thermal processing is modeled.[7] The stress and strain components are related to each other via Hook's law for the isotropic case as follows:

$$\begin{Bmatrix} \sigma_x \\ \sigma_y \\ \sigma_z \end{Bmatrix} = \frac{E}{(1+\nu)(1-2\nu)} \begin{bmatrix} 1-\nu & \nu & \nu \\ \nu & 1-\nu & \nu \\ \nu & \nu & 1-\nu \end{bmatrix} \begin{Bmatrix} \varepsilon_x - \alpha\Delta T \\ \varepsilon_y - \alpha\Delta T \\ \varepsilon_z - \alpha\Delta T \end{Bmatrix} \quad [7]$$

with ν being Poisson's number and E being Young's Modulus. Equation 7 contains the elastic strain components as the difference between the total strain components and the thermal expansion with the thermal expansion coefficient α and the temperature difference ΔT. The strain components are defined via the displacements u, v, w as follows:

$$\begin{aligned}
\varepsilon_x &= \frac{\partial u}{\partial x} & \tau_{xy} &= \frac{E}{2(1+\nu)}\left(\frac{\partial v}{\partial x} + \frac{\partial u}{\partial y}\right)\\
\varepsilon_y &= \frac{\partial v}{\partial y} & \tau_{yz} &= \frac{E}{2(1+\nu)}\left(\frac{\partial w}{\partial y} + \frac{\partial v}{\partial z}\right).\\
\varepsilon_z &= \frac{\partial w}{\partial z} & \tau_{zx} &= \frac{E}{2(1+\nu)}\left(\frac{\partial u}{\partial z} + \frac{\partial w}{\partial x}\right)
\end{aligned} \quad [8]$$

At least three equations with the three unknowns u, v, w were solved together with the thermal model by the partial differential equation solver of the commercial software COMSOL Multiphysics. All surfaces were free. The temperature dependent parameters E, ν, and α were inserted into the model by fitting curves to the experimental values taken from Ref. 4.

If the thermally induced stress reaches a certain level yielding can occur resulting in plastic deformation of the material. A well-known yielding criterion is based on the von Mises stress

$$\tau_M = \sqrt{\left\{0.5\left[\left(\sigma_x - \sigma_y\right)^2 + \left(\sigma_y - \sigma_z\right)^2 + \left(\sigma_z - \sigma_x\right)^2\right] + 3\left(\tau_{xy}^2 + \tau_{yz}^2 + \tau_{zx}^2\right)\right\}} \quad [9]$$

with the yielding condition

$$S \cdot \tau_M \geq \tau_{uy} \quad [10]$$

Here, S is the Schmid factor which transforms the stress into the slip systems. In silicon with the slip systems $\{111\}$ $\langle 110 \rangle$, the Schmid factor can vary between 0 and 0.41. For our considerations, we used the maximum possible value. The upper yield stress τ_{uy} is temperature dependent and was applied as determined in Ref. 8

$$\tau_{uy} = (4.27 \pm 0.20) \times 10^{-3}\,[\mathrm{MPa}] \cdot exp\left(\frac{(0.70 \pm 0.01)\,[\mathrm{eV}]}{kT}\right) \quad [11]$$

Experimental

The sawed, ground, and etched wafers used in the flash experiments were first investigated by scanning transmission electron microscopy (STEM) in the surface near region. In the ground and sawed wafers, dislocation loops were observed which are the result of surface damage. In the surface near regions of etched wafers neither surface damage nor dislocations were observed. Figure 2 shows the surface near region of a ground wafer.

After flash lamp annealing with a normalized irradiance of 0.97, the wafers were cleaved and preferentially etched in order to reveal the dislocations generated. The etched cleavage planes can be seen in Fig. 3. In the sawed and ground wafers, dislocations propagate from the front surface into the wafer bulk. A much smaller density of dislocations also propagates from the back surface into the wafer bulk. A region which is nearly free of dislocations can be found in the lower wafer parts. The etched wafers are free of dislocations. This means that only preexisting dislocations propagate into the wafer during flash lamp annealing.

Results of Modeling and Discussion of Experimental Results

In contrast to rapid thermal annealing, which heats and cools the bulk of the silicon wafer quite homogeneously to the soak temperature, FLA generates temperature profiles in the wafers. They can lead to different stages of shrinking of the grown-in oxygen precipitate nuclei depending on the temperature reached and they can influence the profiles of the concentration of intrinsic point defects.[9]

Fig. 4 shows the temperature profile during the flash (full lines) and during cooling (dashed lines) for the flash duration used. The

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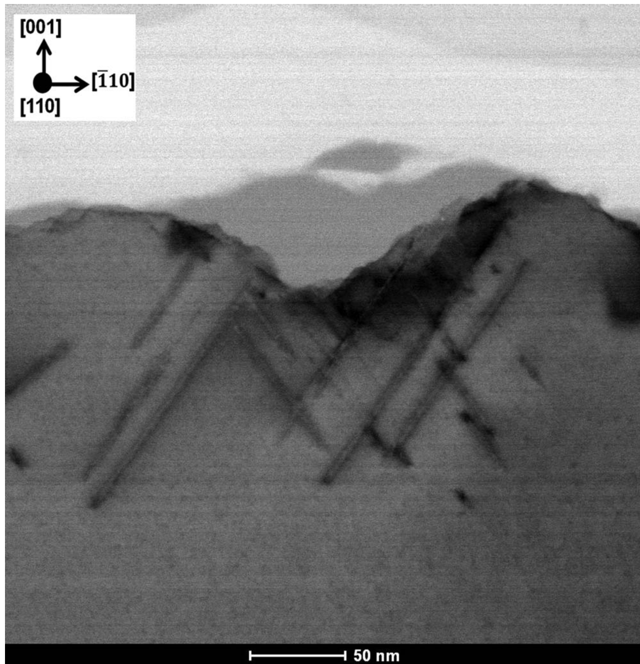

Figure 2. Dislocation loops observed by STEM in the surface near region of a ground wafer.

temperature at $t = 0$ (dotted line) is the temperature of pre-heating which amounts 800°C. It can be seen that during the 20 ms flash, about half of the wafer depth below the front surface reaches temperatures in the range of 1200 - 1400°C. The temperature profile is equalized at a temperature level of about 1210°C within about 40 ms. All these temperatures are high enough to markedly shrink the grown-in nuclei in the whole wafer depth. Therefore, BMD formation is suppressed in wafers after flash lamp annealing for 20 ms.[9]

All simulations shown here were made for 900 μm thick squared silicon wafers with 70 mm side length which represents the geometry of the sawed wafers. The displacement of such a wafer as the result of the thermal gradients during a 20 ms flash is shown in Fig. 5. For such a strong displacement, small deflection theory which assumes that the middle plane is stress free cannot be applied. The distribution of the dislocation etch pits in Fig. 3 is a further indication that the lateral deflections are accompanied by stretching of the middle surface.

Figure 6 shows the von Mises stress multiplied with S in comparison to the upper yield stress at the maximum temperature during 20 ms flash annealing. Except in a depth around 700 μm, the von

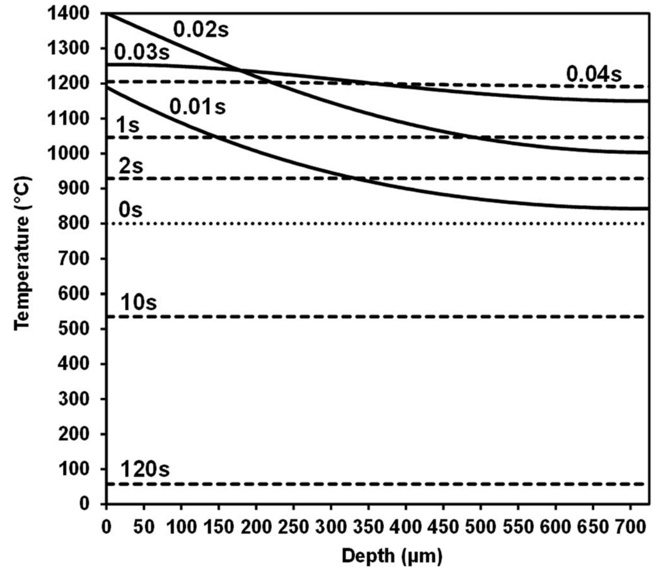

Figure 4. Temperature plotted as a function of the depth from the surface for 20 ms flash lamp annealing. The dotted, full, and dashed lines represent the temperature profiles at the end of pre-heating, during the flash, and during cooling, respectively.

Mises stress exceeds the upper yield stress and the yielding criterion is fulfilled. The etch pit density which is also plotted in Fig. 6 indicates that in the region around 700 μm depth nearly no dislocations were found which is in good agreement with the simulation. However in the region around 180 μm depth, the von Mises stress is also low but the etch pit density is high.

This can be explained by comparison with the dislocation velocity v which is determined according to Refs. 10 and 11 as follows:

$$\mathrm{v} = B\, exp\left(\frac{-Q}{kT}\right)(\langle\sqrt{J_2} - A\sqrt{N}\rangle)^m$$

$$\text{with} \quad A = \frac{Eb}{4\pi\left(1-\nu^2\right)} \quad \text{and} \; \sqrt{J_2} = \tau_M/\sqrt{3} \qquad [12]$$

Here, b is the Burgers vector and J_2 is the second invariant of the stress deviator which can be obtained from the von Mises stress. The term in the second bracket represents the effective stress which is reduced in the course of plastic deformation by dislocation generation. We calculated the initial dislocation velocity and in this case the dislocation density N is set to zero. The material parameter B was

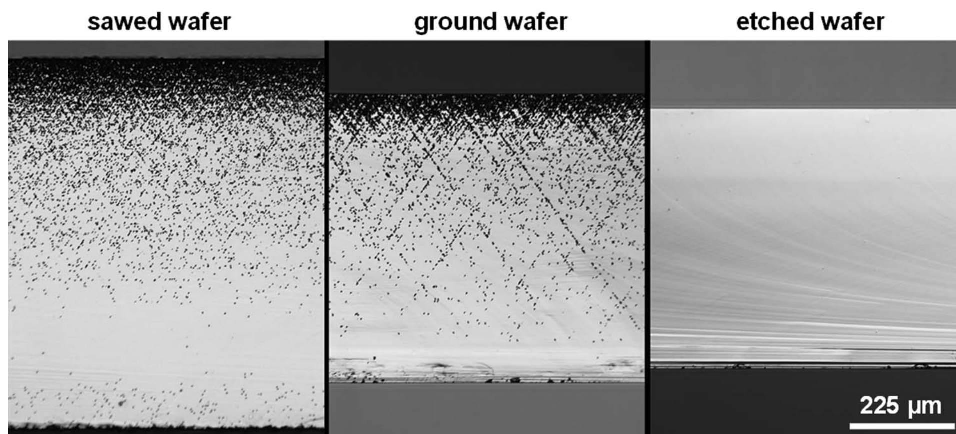

Figure 3. Cross-sectional micrographs of the etched cleavage planes of different wafer types after flash lamp annealing for 20 ms with a normalized irradiance of 0.97. The dark features represent the etched dislocations.

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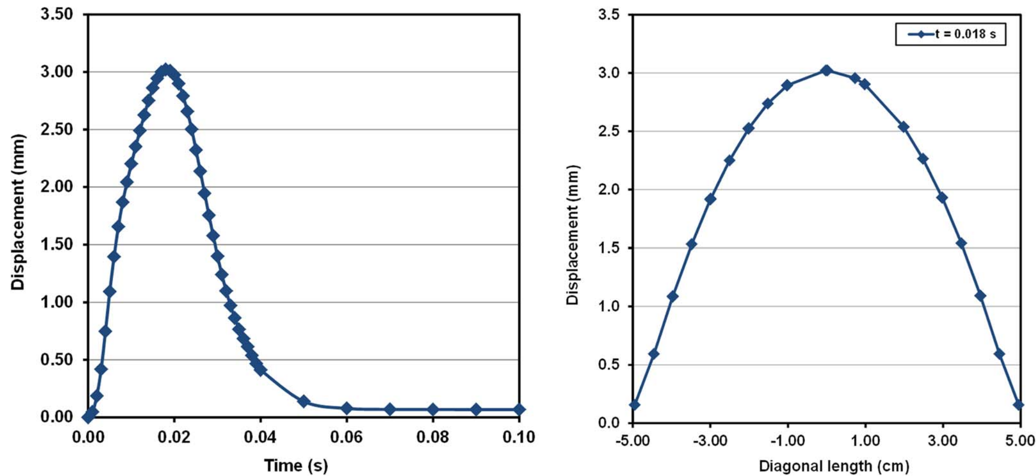

Figure 5. Left: maximum displacement of the squared silicon wafer plotted as a function of the time during flash lamp annealing for 20 ms with a maximum surface temperature of 1400°C. Right: displacement at t = 0.018 s plotted as a function of the diagonal position on the squared silicon wafer.

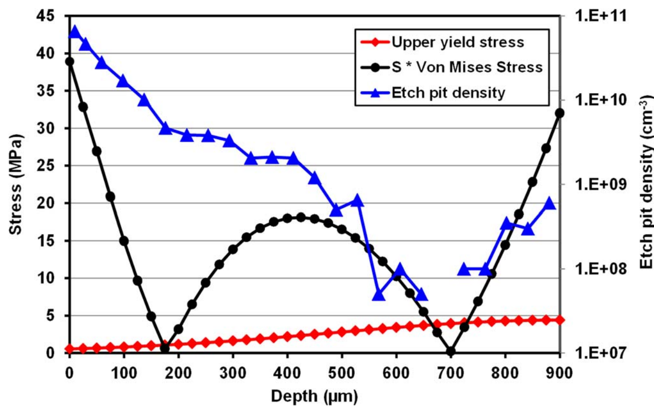

Figure 6. Von Mises stress multiplied with S compared to the upper yield stress and etch pit density of the sawed wafer after 0.018 s (at maximum surface temperature of the 20 ms flash) all plotted as a function of the wafer depth.

assumed to be $10^{-4}\ \frac{\mathrm{m}}{\mathrm{s \cdot MPa}}$, the Peierls potential Q was set to 2.2 eV, and the stress exponent m was assumed to be 1. These parameters for 60° dislocations which are the common glide dislocations in silicon were taken from Ref. 12.

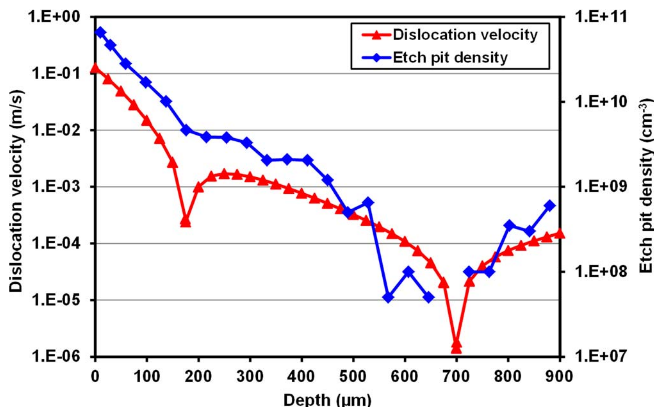

Figure 7. Initial dislocation velocity compared to the etch pit density after 0.018 s (at maximum surface temperature of the 20 ms flash) all plotted as a function of the wafer depth.

In Fig. 7, the initial dislocation velocity at maximum surface temperature of the 20 ms flash is compared to the etch pit density. It can be seen that in the region around 700 µm where the yielding condition is not fulfilled both the etch pit density and the dislocation velocity are low. In the region around 180 µm, the dislocation velocity is high although $\tau_M \cdot S$ is nearly equal to the upper yield stress. In addition, the minimum of the von Mises stress is shifting around 180 µm depth during the flash anneal as the result of the changing thermal gradient in the course of FLA. Therefore, the dislocation propagation is not hindered in this depth. The mechanical model which was applied here to the sawed wafers is in good agreement with the experimental results.

In the etched wafer without pre-existing dislocations, no dislocations were found after FLA although the yielding critera are fulfilled for these wafers as well. The reason is that the formation of dislocations would require overcoming the energy barrier of homogeneous nucleation of dislocations which is too high and would need stresses in the GPa range. Oxygen precipitates as sources for nucleation of dislocations can be excluded as well in our experiments because the grown-in oxygen precipitates are too small and just shrink during FLA.[9]

Conclusions

In summary, our investigations of dislocation generation and propagation during flash lamp annealing for 20 ms have shown that due to the thermal stress resulting from the temperature profiles generated by the flash pre-existing dislocations propagate into the wafer from both surfaces during flash lamp annealing. A dislocation free zone was observed around 700 µm depth below the surface of a 900 µm thick sawed wafer. The propagation of dislocations can be well described by a three-dimensional mechanical model. It was further demonstrated that in wafers being initially free of dislocations no dislocations are generated during FLA.

Acknowledgment

The authors thank Dr. W. Skorupa for providing them the possibility to carry out flash lamp anneals at the Institute for Ion Beam Physics and Materials Research of the HZDR. We also thank T. Schumann from HZDR for his technical assistance during the flash anneals.

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