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Enhancement-mode Ga_2O_3 wrap-gate fin field-effect transistors on native (100) β-Ga_2O_3 substrate with high breakdown voltage

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Sn-doped gallium oxide (Ga_2O_3) wrap-gate fin-array field-effect transistors (finFETs) were formed by top-down BCl_3 plasma etching on a native semi-insulating Mg-doped (100) β-Ga_2O_3 substrate. The fin channels have a triangular cross-section and are approximately 300 nm wide and 200 nm tall. FinFETs, with 20 nm Al_2O_3 gate dielectric and $\sim 2\,\mu m$ wrap-gate, demonstrate normally-off operation with a threshold voltage between 0 and +1 V during high-voltage operation. The I_{ON}/I_{OFF} ratio is greater than 10^5 and is mainly limited by high on-resistance that can be significantly improved. At $V_G = 0$, a finFET with 21 μm gate-drain spacing achieved a three-terminal breakdown voltage exceeding 600 V without a field-plate. © *2016 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).* [http://dx.doi.org/10.1063/1.4967931]

Gallium oxide (Ga_2O_3) is emerging as a potential disruptive electronic material for high-voltage electronics applications. The excitement of this material is due to its (1) ultra-wide bandgap of $\sim$4.8 eV with $\sim$8 MV/cm theoretical critical field strength,[1] (2) up to four-inch native substrate availability and capability of melt-growth synthesis,[2] and (3) a wide range of n-type doping achievable by halide vapor phase epitaxy (HVPE),[3] molecular beam epitaxy (MBE),[4] low-pressure chemical vapor deposition (LPCVD),[5] metal-organic chemical vapor deposition (MOCVD),[6] and metal-organic vapor phase epitaxy (MOVPE).[7,8] The β-phase Ga_2O_3 unit crystal has a monoclinic structure and is reported as the most thermally stable and conducive for the single-crystal homoepitaxial growth.[9,10] For heterogeneous integration, a notable cleavage plane is located along the (100) crystal plane, which has incited nanomembrane research for integration with arbitrary substrates and two-dimensional semiconductors.[11–13]

The first transistor devices by homoepitaxial Ga_2O_3 were demonstrated with a Sn-doped Ga_2O_3 channel grown by MBE on (010) semi-insulating β-Ga_2O_3 substrates.[1,14] Metal-oxide-semiconductor field-effect transistors (MOSFETs) followed later with a Si-doped channel and ohmic contacts by implantation with breakdown exceeding 750-V with a field-plate.[15,16] Most recently, Sn-doped Ga_2O_3 MOSFETs homoepitaxially grown by MOVPE on (100) semi-insulating β-Ga_2O_3 achieved a record-high 3.8 MV/cm critical field strength surpassing GaN and SiC bulk theoretical field strengths.[17]

For power electronics applications, a normally-off transistor is preferred for safe high-voltage operation and to mitigate off-state power dissipation. To achieve a high-current density, Ga_2O_3 MOSFETs require high doping concentration resulting in a negative threshold voltage (V_{TH}). To shift toward positive V_{TH}, non-planar fin-shaped channels offer enhanced electrostatic control of the channel by depleting it from the side walls without sacrificing doping. Achieving dense, parallel arrays of fin channels is most easily achieved by top-down plasma etching though reports of fin channels formed by metal-catalyzed wet-etching[18] and self-assembly[19] are promising to avoid plasma etch damage.

GaN-based fin-channel field-effect transistors (finFETs) have been reported with Si-doped GaN junctionless and high-electron mobility AlGaN/GaN heterostructure channels where the gate wraps around fins with enhanced electrostatics to nearly or fully deplete the channel.[20–22] However, the main drawbacks for GaN are cost and the availability of native substrates for low-defect density homoepitaxial growth. In this letter, we present a finFET with arrays of parallel Sn-doped Ga_2O_3 fin channels formed by top-down plasma etching to achieve normally-off operation on a native (100) semi-insulating β-Ga_2O_3 substrate. The results show the feasibility of wrap-gate architecture to shift the V_{TH} to positive values while maintaining volume current densities for consideration in future high-voltage device design.

Fin-array field-effect transistors (finFET) devices were fabricated from a 300-nm Sn-doped Ga_2O_3 channel grown homoepitaxially by MOVPE on a 100-mm^2 Mg-doped semi-insulating (100) β-Ga_2O_3 substrate.[7,8,23] First, arrays of $\sim$300-nm wide fin channels with a $\sim$900-nm pitch were formed by electron beam lithography followed by 150-nm Cr

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metal evaporation as the hard mask. A second 200-nm Cr hard mask was superimposed on the fin mask by projection lithography to create bulk mesa contacts for source and drain electrodes. Both Cr layers were etched by inductively coupled plasma (ICP) etching using BCl_3 chemistry.[24] The etch conditions were 120 W reactive ion etching (RIE) power and 300 W coil power with 20 sccm BCl_3 and 16 mTorr chamber pressure. The etch selectivity of Ga_2O_3:Cr was approximately ~2:1. To sufficiently remove the entire 300-nm channel between fins, an over-etch was required, which completely etched the fin Cr mask resulting in triangular-shaped fins. Residual Cr on the source and drain mesas was removed by commercially available Cr wet-etchant. Ohmic contacts consisted of Ti/Al/Ni/Au (20/100/50/50 nm) rapidly annealed for 1-min at 470 °C in nitrogen. A 20-nm Al_2O_3 gate dielectric was deposited by atomic layer deposition (ALD) at 250 °C and patterned by fluorine-based RIE to allow for Ni/Au (20/480 nm) interconnects and ~2 μm long optical gate metal evaporation. Finally, a second 20-nm ALD Al_2O_3 layer was deposited and patterned on the sample to passivate the etched Ga_2O_3 surfaces between interconnects. The fabrication process is illustrated in Fig. 1(a).

The finFET has a centered two-finger gate layout with each gate finger wrapping along 48 fins. The total source to drain distance (L_{SD}) is ~4-μm, and the fin-array spans approximately ~3-μm of this source-drain distance. A tilted SEM image of the fin channels with wrap-gate and bulk-like ohmic contacts is shown in Fig. 1(b). The sidewall morphology appears relatively smooth as previously observed using high-power ICP plasma etching with BCl_3.[24] A representative cross-sectional SEM image of three fins is shown in Fig. 2(a). The darker contrast observed in the fin compared to the substrate is indicative of the Sn-doped channel and adequate electrical isolation between fins. Fig. 2(b) depicts that the fins are approximately ~300 nm at the base with tapered sidewalls joining at ~200 nm thickness. The 20-nm Al_2O_3 gate dielectric and Ni/Au gate metal conform to the fin on all sides.

The mobility and doping concentration of the fins were measured from on-wafer Van der Pauw (VdP) test structures and device *C-V* measurements. It is widely reported that ionized donor concentration, N_D, can vary significantly from the chemical Sn-doping concentration.[8,17] The sheet resistance (R_{SH}) and electron mobility (μ) were measured on a VdP structure near the reported device as ~40 kΩ/sq and ~24 cm²/Vs, respectively. We observed the larger geometry of the Cr mask used for the VdP mesa etched slower compared to the Cr fin-array mask; therefore, the VdP mesa was protected during the fin-array definition process. A forward and reverse *C-V* measurement of the finFET is shown in Fig. 3 indicating ~0.8 V of hysteresis, which has been previously reported as mobile border traps in accumulation.[25] In the inset, an $N_D \sim 2.3 \times 10^{17}$ cm^{-3} was extracted from the linear region of $1/C^2$ as a function of V_{GS}. The area was estimated as $L_G W_{fin} N_{fin}$ where W_{fin} is ~200 nm after considering a ~70 nm backside depletion width and using a 3:2 width-to-height triangular fin cross-section. Finally, the flat-band capacitance, C_{FB}, can be calculated by the measured oxide capacitance ($C_{ox} \sim 225$ fF) in series with the semiconductor capacitance (C_S).[26] The corresponding forward and reverse sweep flat-band voltage, V_{FB}, is 1.3 V and 2.1 V, respectively.

In the absence of accurate models for Ga_2O_3, one-dimensional analytical expressions were used to estimate the depletion widths (W_d) on the two sides and bottom facet of the Sn-doped fins. The partial depletion width of the sides in the ungated region can be estimated by the built-in energy potential (V_{bi}) using the energy band lineup at the Al_2O_3/Ga_2O_3 interface[20]

$$E_G^{Al2O3} = E_{VBM}^{Al2O3} + \Delta E_C + \left(E_C^{Ga_20_3} - E_F\right) + V_{bi}, \qquad (1)$$

where E_G, ΔE_C, and E_{VBM} are the bandgap, conduction band offset, and valence band maximum with respect to the Ga_2O_3 Fermi level energy (E_F), respectively. $V_{bi(ug)}$ represents band-bending in the ungated Ga_2O_3 due to the presence of interface traps. Kamimura *et al*. reported on the Al_2O_3/Ga_2O_3 interface with $E_G \sim 6.8$ eV, $\Delta E_C \sim 1.5$–1.7 eV,[25,27] and $E_{VBM} \sim 3.8$ eV[25] using XPS measurements. For $N_D \sim 2.3 \times 10^{17}$ cm^{-3}, the semiconductor $E_C - E_F$ energy difference can be expressed as

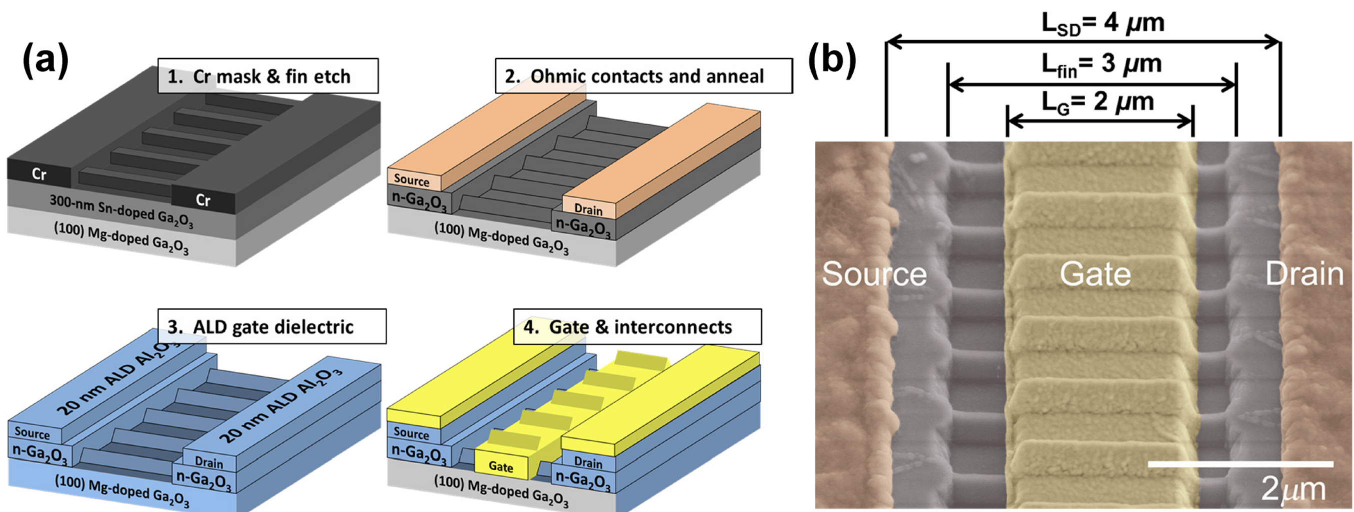

FIG. 1. (a) Fabrication process for Ga_2O_3 finFETs and (b) the tilted false-colored SEM image of a $L_{SD} = 4$ μm finFET depicting the geometry of Ga_2O_3 fin channels and contacts.

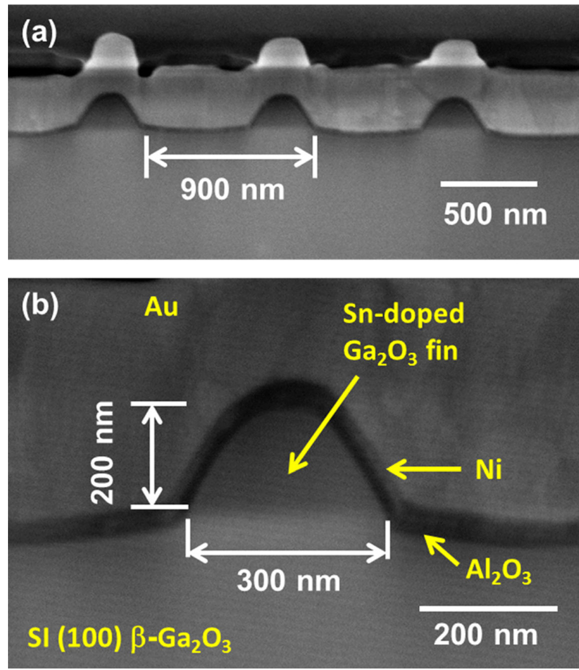

FIG. 2. (a) The cross-sectional SEM image of three Ga_2O_3 fins and (b) a high magnification SEM image of one Ga_2O_3 fin channel with associated dimensions.

$$-V_t \ln\left(\frac{N_D}{N_C}\right), \tag{2}$$

where V_t and N_C are the thermal voltage (~26 mV at 300 K) and effective conduction band density of states for Ga_2O_3.[28] This analysis shows $E_C - E_F$ is ~73 meV and leaves a non-negligible $V_{bi(ug)} \sim 1.4$ eV, which may be related to interface traps and/or pinning, which is neither well-understood nor reported.

A similar study of GaN finFETs deduced a $V_{bi} \sim 0.74$ eV in the ungated region and was explained by Al_2O_3/GaN interfacial chemistry by XPS.[20,29] Furthermore, in the gated region, the band-bending can increase an additional ~1.15 eV due to the difference in metal work functions of Ni ($\Phi_m = 5.15$ eV) and Ga_2O_3 ($\Phi_S = \chi_s + E_C - E_F$),[20]

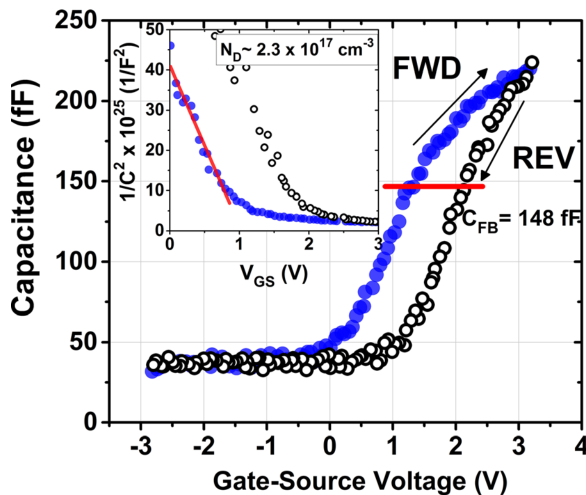

FIG. 3. Forward and reverse C-V_{GS} sweep of the finFET indicating the calculated flatband and oxide capacitance; and, (inset) C^{-2}-V_{GS} characteristics to extract carrier concentration.

where χ_s is the electron affinity of Ga_2O_3 (~3.5 to 4.0 V).[27,30] However, this does not consider trap-assisted tunneling for thin Al_2O_3 gate oxide,[27] and it remains unclear how the $V_{bi(ug)}$ compensates for the band-bending normally induced by a gate contact without thorough XPS characterization of our particular interface. For a simple case, however, where both energy barriers are combined in the gated region, the $V_{bi(g)}$ is ~2.5 V, which is reasonably close to the measured reverse sweep V_{FB}. The maximum depletion width, W_d, for each region is calculated by the following equation:

$$W_d = \sqrt{\frac{2\varepsilon_o \varepsilon_S V_{bi(ug,g)}}{qN_D}}, \tag{3}$$

where ε_o and ε_S are the permittivity of free space and Ga_2O_3 dielectric constant, respectively. This yields $W_d \sim 83$ nm and ~110 nm in the ungated and gated regions, respectively. A backside depletion width from the semi-insulating substrate is found to be ~70 nm assuming a mid-gap interface trap density of $\sim 2 \times 10^{17}$ cm^{-3}.[17,31] Therefore, we estimate an undepleted fin with approximately ~26 nm (base) × ~17 nm (height) in the ungated region contributes to the volume conduction mechanism in the finFET. In contrast, the depletion from the sides and substrate fully deplete the fin dimensions in the gated region to realize the normally-off operation. It should be noted that once $V_{GS} > V_{FB}$, the finFET is operating in accumulation similar to non-planar normally-off junctionless GaN finFETs.[20,32]

Fig. 4(a) shows the family of I_D-V_D curves from $V_{GS} = +4$ V to 0 V. At $V_{GS} = +4$ V, the on-current (I_{ON}) reaches ~3.5 μA. An upper bound on expected current in the partially depleted fin-arrays can be approximated by the open channel current density (J_n) where $V_{DS} < |V_{GS}$-$V_{TH}|$ using the drift current equation

$$J_n = q\mu N_D E_{CH}, \tag{4}$$

where $E_{CH} = V_{DS}/L_{CH}$ is the potential across the source-drain channel (L_{CH}). Using the partially depleted fin-array cross-sectional area at $V_{DS} = 2$ V and $L_{CH} = 3$ μm, $J_n = 5.9$ kA/cm^2 or $I_D \approx 1.3$ μA, which is close to the measured value in Fig. 4(a). For comparison, this simple analysis is also in agreement at $V_{DS} = 1$ V ($I_{DS} = 0.55$ mA) for the planar Sn-doped Ga_2O_3 MOSFET reported by Green *et al.* using the surface and substrate depletion widths with the reported N_D and Ti/Au gate.[17] The gate width, $W_G = W_{fin}N_{fin}$, is ~19 μm corresponding to an $I_{ON} \sim 0.18$ μA/μm. The low I_{ON} is a main limitation of the fin-array topology reported here, but can be drastically improved in the future with higher-mobility materials and on-resistance optimization. For this device, the gate swing was limited by the conduction band offset of Al_2O_3/Ga_2O_3, which can be improved with, for example, ALD SiO_2.[33] The gate leakage characteristics are shown in Fig. 4(b) and indicate ultra-low gate leakage near 10^{-12} Amps before an onset of trap-assisted tunneling at forward bias appears.[27]

Fig. 4(c) shows the I_D-V_G characteristics at $V_{DS} = 10$ V. Despite I_{ON} limitations, the finFET has $>10^5$ I_{ON}/I_{OFF} ratio. The device reaches an off-state approaching 10^{-12} Amps between 0 and +1 V_{GS} indicating enhancement-mode operation. To rule out the parasitic conduction in the substrate

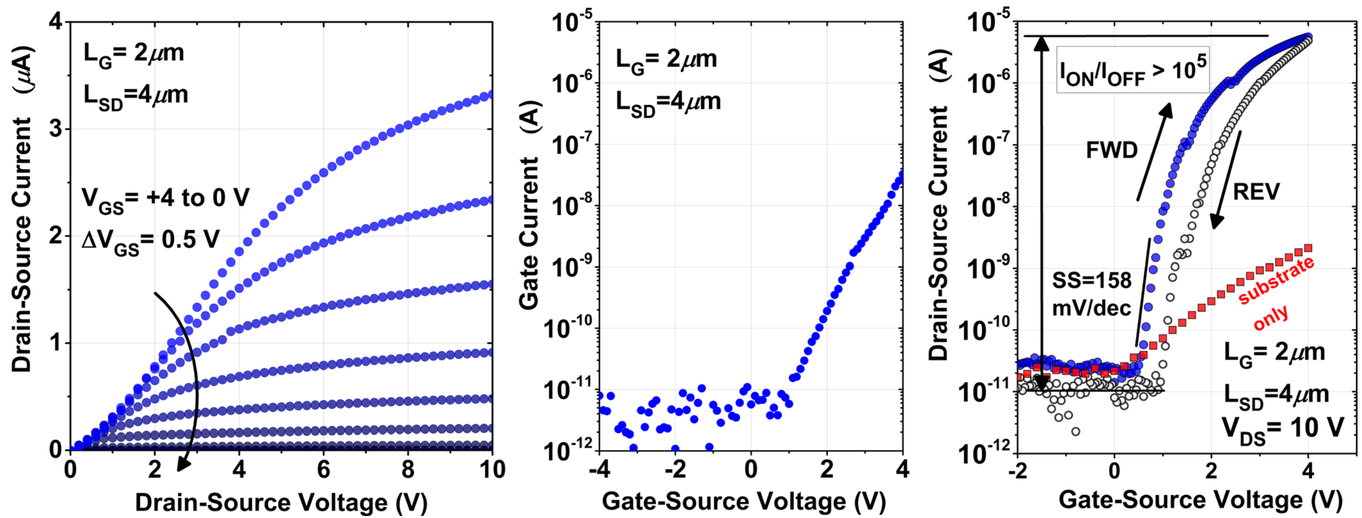

FIG. 4. (a) The I_D-V_D family of output curves from $V_{GS} = +4$ to 0 V; (b) Two-terminal log(I_G)-V_G gate leakage performances from off-to-on state; and, (c) log(I_D)-V_G forward and reverse sweeps indicating a normally-off state at $V_{GS} = 0$ V. An identical device with the entire epitaxial channel etched is included to illustrate the effect of parasitic substrate conduction.

between fins, an identical MOSFET with the epitaxial channel etched away was fabricated and shows minimal modulation of the remaining etched SI substrate. We attribute this parasitic modulation to uncompensated free carriers in the substrate being accumulated at the Al_2O_3/SI-Ga_2O_3 interface. The forward and reverse sweeps reveal trapping effects that may be a combination of the unoptimized Al_2O_3/Ga_2O_3 interface and density of interface traps (D_{it}) caused by the plasma etching of the fin side walls. Despite no surface treatment optimization, the subthreshold slope (SS) is 158 mV/dec, which is superior to previously reported Ga_2O_3 MOSFETs. The D_{it} can be estimated by the shift in forward and reverse V_{FB} from Fig. 3 using the following expression:

$$D_{it} = \frac{C_{ox}\Delta V_{FB}}{qE_G^{Ga_2O_3}}, \quad (5)$$

which is approximately $\sim 3.9 \times 10^{11}$ cm^{-2} eV^{-1} where C_{ox} ~ 3.8 fF/μm^2. The area for C_{ox} is calculated using the measured C_{ox}, 20 nm thickness and a gate dielectric constant of 8.5; though, estimating the area using the sum of the fin side facets multiplied by L_G gives nearly the same value. This D_{it} value is similar to previously reported Al_2O_3/Ga_2O_3 and SiO_2/Ga_2O_3 MOS capacitors on (-201) n^+ β-Ga_2O_3 substrates with $D_{it} < 1.0 \times 10^{12}$ cm^{-2} eV^{-1} after surface treatment optimization.[33,34] The effect of surface plane orientation of the fin facets and the dielectric-Ga_2O_3 interface quality is unclear and requires further investigation.

FinFET high-voltage operation on wider devices with $L_{GD} = 16$ μm and 21 μm was characterized with an Agilent B1505A on a Cascade Tesla probe station. At $V_{GS} = 0$ V, the I_{DS} is $<10^{-7}$ Amps until a breakdown voltage (V_{BK}) is reached. For each L_{GD}, a $V_{TH} = +0.8$ is measured at $V_{DS} = 10$ V, which is shown by the inset of Fig. 5. It should be noted that the I_{ON} for large L_{GD} devices have a very high on-resistance and do not saturate at $V_{DS} = 10$ V. At $V_{GS} = 0$ V, a V_{BK} was measured at 567 and 612 V for $L_{GD} = 16$ and 21 μm, respectively. As indicated in Fig. 5, V_{BK} is destructive and limited by peak electric fields in the gate oxide.

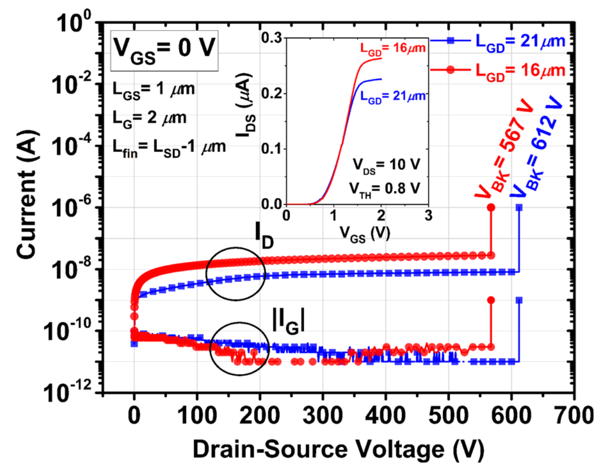

FIG. 5. The breakdown voltages of Ga_2O_3 finFETs with $L_G = 2$ μm and $L_{GD} = 16$, 21 μm while biased in the off-state at $V_{GS} = 0$ V. The inset shows the transfer characteristics of the same device indicating a $V_{TH} = +0.8$ V.

To conclude, we have fabricated an enhancement-mode Ga_2O_3 MOSFET enabled by arrays of Sn-doped fins on a semi-insulating (100) β-Ga_2O_3 substrate. A V_{BK} exceeding 600-V at $V_{GS} = 0$ V off-state was demonstrated and represents the highest breakdown voltage measured without field-plate for β-Ga_2O_3 transistors, and the highest breakdown for any transistor technology utilizing non-planar device channels.[20–22,35–37] Future work includes understanding the role of traps at the dielectric-Ga_2O_3 interface and optimizing on-resistance by reducing the fin channel length and using highly doped ohmic cap layer.

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