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Introducing pinMOS Memory: A Novel, Nonvolatile Organic Memory Device

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In recent decades, organic memory devices have been researched intensely and they can, among other application scenarios, play an important role in the vision of an internet of things. Most studies concentrate on storing charges in electronic traps or nanoparticles while memory types where the information is stored in the local charge up of an integrated capacitance and presented by capacitance received far less attention. Here, a new type of programmable organic capacitive memory called p-i-n-metal-oxide-semiconductor (pinMOS) memory is demonstrated with the possibility to store multiple states. Another attractive property is that this simple, diode-based pinMOS memory can be written as well as read electrically and optically. The pinMOS memory device shows excellent repeatability, an endurance of more than 10^4 write-read-erase-read cycles, and currently already over 24 h retention time. The working mechanism of the pinMOS memory under dynamic and steady-state operations is investigated to identify further optimization steps. The results reveal that the pinMOS memory principle is promising as a reliable capacitive memory device for future applications in electronic and photonic circuits like in neuromorphic computing or visual memory systems.

1. Introduction

Organic nonvolatile memory (ONVM) devices have been intensively investigated as the future promising data storage media due to attractive attributes, such as potentially being low-cost, high-density, high mechanical flexibility, and simple fabrication.[1,2] ONVM device technologies that are commonly encountered in literature are resistive random access memory (ReRAM), single transistor-based memory comprising a floating gate layer as charge-storage (trapping/detrapping) layer, ferroelectric memory, or electrochemical memory.[3–8] ReRAM devices have a programmable electrical bistability that usually leads to two different conductance states. They can achieve high storage densities at low costs but achieving multiple-bit storage is difficult.[9–11] Although achieving multiple-bit storage is quite possible for transistor-based memory devices, their inherent minimum channel length requirement sets a technological limit to the further downscaling of such cells.[12,13]

Most studies focus on using resistance-switching organic memory for holding information, including bipolar switching in ReRAM and charge-trapping-based switching in transistor memory. Such devices can be modeled by using memristive equations and are widely anticipated to be useful as artificial neuromorphic devices in artificial neural networks.[11,14,15] Another type of memory device, the memcapacitor, has been less researched than memristors, even though it can possess bias-history-based switchable capacitances and has prospective applications such as capacitive artificial neural networks without suffering from cross-talk currents in the steady-state and can have a lower power consumption during writing, erasing, and reading.[16,17]

In 1952, A. W. Holt first proposed the possibility of storing information with discrete elements by connecting two parallel but opposite diodes with a capacitor in series.[18] In that concept, the diodes allow the charge/discharge of the capacitor at a higher positive or negative voltage, but keep the information at lower voltages close to 0 V. This is similar to one diode-one resistor cell arrays, where a diode in series with a hybrid ONVM device are composed into an integrated memory cell for the sake of mitigating cross-talk issues.[19,20] Although the diode provides an active access function in this kind of diode-switch organic bistable memory, the whole device is still a resistive memory device based on the memory element. Here, we adopt this concept into a novel integrated memory cell where all functions of the discrete elements are achieved by a single stack of layers.

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In fact, our discovery of this memory effect came through another research direction: capacitors combined with diodes in order to produce the alternating current (AC) driven organic light-emitting (OLED) devices. These AC OLEDs incorporate one or two dielectric layers that can improve the lateral voltage uniformity, minimize electrical shorts, reduce damage from continuous overvoltage, make use of alternative charge injection mechanisms, or lead to new applications where capacitive coupling triggers the emission of light.[21–25] Both the frequency dependence and the necessity of applying another negative half-cycle in AC signal to restore light emission already indicated a capacitive switching memory nature of AC OLEDs. Therefore, a detailed investigation of capacitor-based capacitive memory devices is essential not only to pick up Holt's work in an integrated device, but also to advance the understanding of AC OLEDs.

In the device architecture discussed in this paper, an insulator layer was combined with a p-doped/intrinsic/n-doped (p-i-n) junction to yield a novel capacitive nonvolatile memory that can be programmed by either voltage application or ultraviolet light illumination as well as read out electrically or by optical-range light emission. The capability to store charge and the accompanying change in the series capacitance of the diode and metal-oxide-semiconductor (MOS)-capacitor portions are the key aspects of this new programmable p-i-n-(pin)MOS memory, also leading to the possibility of multiple-bit storage. The easy-to-fabricate, simple diode-capacitor based memory device achieves a reliable endurance over 10^4 cycles and a promising retention time over 24 h. The realization of optoelectronic control opens the application possibilities in both electronic and photonic circuits, and helps to better understand how charges and information are stored in insulator/diode based electronic devices.

2. Results and Discussion

2.1. Device Architecture

The pinMOS memory as shown in **Figure 1**a was fabricated on top of a 50 nm aluminum oxide (Al_2O_3) layer using the typical crossbar electrode architecture in conjunction with our standard red-emitting OLED stack.[26] The oxide layer, deposited by atomic layer deposition, results in very low leakage currents. The area of both doped layers was intentionally structured to be 0.3 mm smaller in all direction compared to the active area given by the electrodes (Figure 1b) in order to eliminate the leakage currents related to lateral device charge up in crossbar architectures.[27]

2.2. Memory Characteristics of the pinMOS Memory Device

In the first part of this discussion, we will introduce the electrically assessed memory effect and its characteristics while still sticking to quite generic language, e.g., "stored information/charges," before we discuss our current understanding of the complex physical working mechanism in more detail. The ITO electrode which is connected to the oxide layer is referred to as anode, while the Al electrode that is connected to the n-doped layer is called cathode hereinafter.

To verify the data storage capability of the pinMOS memory, the capacitance-voltage characteristics were investigated by impedance spectroscopy (**Figure 2**a). Unless otherwise mentioned in this paper, all capacitance measurements were performed at 100 Hz. A prebias of −15 V was applied for 5 s as "writing process" to bring the device into the defined state. When the bias is then swept from −3 to +3 V and back to −3 V, a pronounced hysteresis could be seen with excellent repeatability, as evidenced by the fact that the three consecutive runs of prebias and ± 3 V sweeps perfectly coincide. The 2.4 V voltage difference ΔV between the rising curve during the forward sweeping and the drop of the curve during the reverse sweeping is the memory window we obtain. This memory window clearly is the result of the charge "information" stored by the application of a prebias to the device which is then being erased when the voltage is swept to +3 V. During all cycles, two distinct capacitances at 3.4 and 2.9 nF become apparent, which we subsequently refer to as the states "1"(ON) and "−1"(OFF) of the pinMOS memory device, respectively.

The pinMOS memory also possesses a bias-history-dependent capacitance. If the bias sweep was done three times in a row but without repeating the prebiasing at −15 V, we obtained three different cycle shapes (Figure 2b). The full memory window is only visible in the first cycle since, as said above, an application of +3 V clearly already turns the

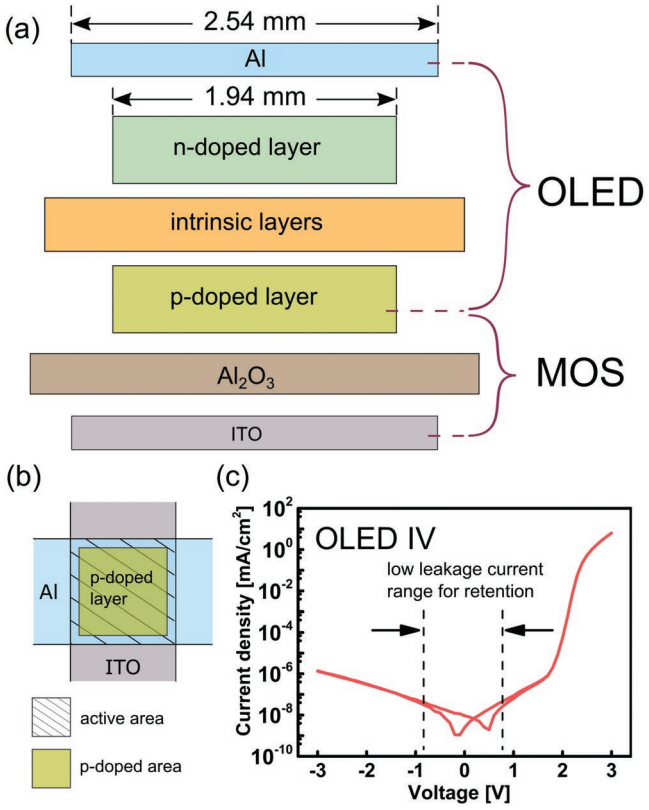

Figure 1. a) Schematic cross-section of architecture for the pinMOS memory. b) Top view of showing the relative position of the structured p-doped layer and crossbar electrodes. c) *I–V* characteristics of individual OLED element under steady state by keeping each applied voltage for 100 s before measurement.

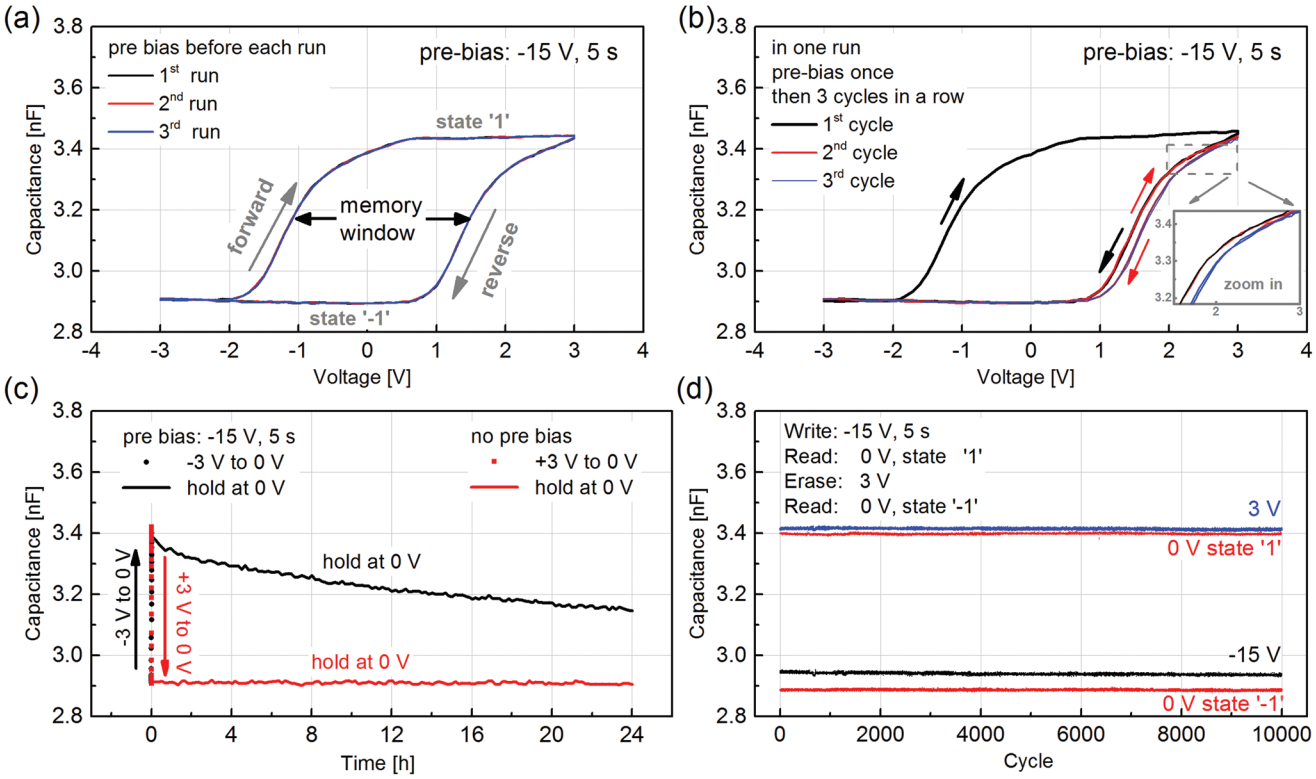

Figure 2. a) Three repeated capacitance–voltage (CV) runs and b) three continued CV cycles in one run of pinMOS memory after applying a prebias of −15 V for 5 s. Inset: Zoom in image of reverse curves. c) Retention characteristics and d) sweep endurance of a pinMOS memory device.

state from "1" to "−1." Since in this experiment there was no writing (prebias) process after the end of the first cycle, the forward curves of the subsequent cycles 2 and 3 coincide with the reverse curves of cycles 1 and 2, respectively (compare colored arrows in Figure 2b and zoomed inset). The small remaining hysteresis in the 2nd cycle stems from a still not fully completed erasure of the memory during the 1st cycle, whereas no hysteresis can be measured in the 3rd cycle. The magnitude of the threshold voltages for capacitance increase or decrease and their dependence on the measurement parameters will be further discussed below.

The memory states of the pinMOS memory devices are nonvolatile and even at this early development stage they show fairly promising retention characteristics, as shown in Figure 2c. For the retention time test, the reading voltage was chosen to be 0 V, based on the separable extracted capacitance at both "1" and "−1" states at this voltage. The pinMOS memory was first programmed to the written state through applying −15 V for 5 s. Then a single voltage sweep was applied from −3 to 0 V as before, and subsequently the capacitance at state "1" at 0 V was being recorded as a function of time in intervals of 10 min. The state "1" capacitance then shows a slow decrease from the initial 3.40 nF to 3.15 nF in over the course of 24 h. For the equivalent test for state "1," a positive voltage +3 V was supplied to the same device for several seconds to fully switch it to state "−1" before the voltage was swept back from 3 to 0 V and held there. Under this state, the capacitance at 0 V maintains well over 24 h. The capacitance of both states can be well distinguished even after 24 h, suggesting a stable charge-storing retention capability. Please note that during this measurement, the measurement equipment was electrically connected to the device at all times, basically allowing the device to discharge at any time like it would in a real circuit application. This is done in conscious deviation from retention time measurements commonly encountered in literature where memory devices in which leakage currents will also dissipate stored information, e.g., devices with a floating gate or charged-up nanoparticles, are electrically connected and probed only intermittently (pointwise) over a long time span. This latter way of assessing retention time leads to artificially increased life times of the memory states, since without electrical connection leakage currents that destroy the stored information cannot flow.

The reliability of the pinMOS memory device was also investigated via cyclic endurance testing during which many writing/erasing bias cycles were applied and after each of which the capacitance was measured (Figure 2d). The writing process was completed by applying −15 V for 5 s, while the erasing and reading voltages were +3 and 0 V, respectively. The two states of the pinMOS memory can be clearly distinguished even after 10^4 cycles without any significant changes, indicating a reliable endurance characteristic.

2.3. Multiple Tunability by Modulating Operation Parameters

Another attractive property of the pinMOS memory device is its potential to store multiple bits, i.e., the tunability of the

memory window based on changes to the operation parameters (**Figure 3**). For example, for the same "−3 to +3 to −3 V" sweep range in Figure 3a, the threshold voltage to the capacitance increase in forward sweep direction can be shifted from 0 to −2.5 V by varying the hold time of the prebias (−15 V) from 1 to 10 s. In this case, the overlap of the reverse curves indicates the effectiveness of the application of the erasing voltage of +3 V to erase the memory. Nevertheless, the expansion of memory windows according to the hold times at the prebias voltage does show a saturation. Another possibility to modulate the amount of charges stored in the devices without any change to the writing process is to vary the upper sweep voltage as shown in Figure 3b. Herein, the reverse curves horizontally shifted to more and more positive voltages while the forward curves remained the same and kept overlapped. Importantly, the high and low capacitance plateaus cases remain identical in both cases.

The information stored in the device by the application of the initial writing process can be released in fractional amounts via different sweep ranges, giving rise to what is in principle a multiple-bit storage (Figure 3c). After an initial prebias −15 V, 5 s to create a defined state "1," a cyclic sweep with lower voltage −3 to 0 V was applied to obtain the 1st cycle. Further sweeps without new prebias were performed with same lower voltage −3 V but with the upper voltage being varied stepwise from 1 to 6 V. The successive positive shift of the memory windows proves that the device information is preserved between the previous reverse cycle and the next forward cycle. By

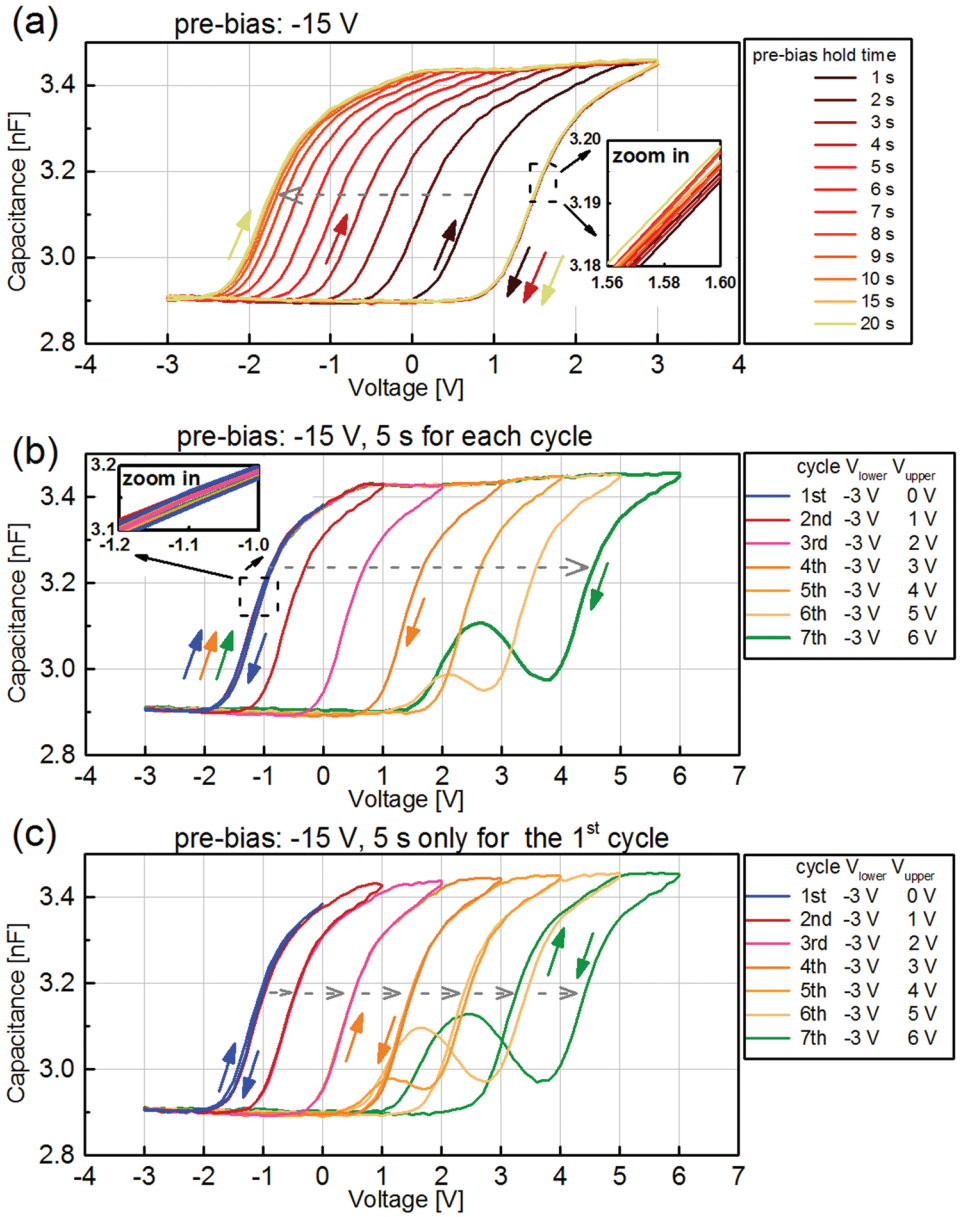

Figure 3. a) CV curves measured under same prebias −15 V but different hold times. Inset: Zoom in image of reverse curves. CV curves swept under different ranges with prebias applied b) for each cycle or c) only for the 1st cycle.

increasing the upper cycle voltage more and more of this stored information is "released," corresponding to a gradual shift of both forward and reverse curves. Overall, the amount of charge left in the device determines the forward curve behavior, while the upper voltage limits the reverse curve behavior.

2.4. Working Mechanisms of the pinMOS Memory

To better understand how information is stored by the pinMOS memory, it is helpful to not only look at the static bias-free states, but to also consider the quasi-steady states under application of negative or positive voltages (**Figure 4**). First, we have to assume that the 50 nm p-doped layer which is embedded between the insulator and the intrinsic layer will never be entirely depleted at any of the voltages applied here. A (possibly thin) region in the p-doped layer will always exist in which the original free hole carrier concentration is retained. The potential of this still undepleted region of the p-doped layer is symbolized by the potential V_p as shown in the middle circuit schematic in Figure 4 and can serve as a reference potential. The left and right sides of the p-doped layer as seen from this reference region can then be considered as decoupled parts, allowing the pinMOS memory to be understood as two series-connected individual elements: a MOS capacitor and an OLED as visualized in Figure 4 in the middle. As indicated by V_p, the Fermi level in the undepleted reference part of the p-doped layer can be used to define the voltage drops over the insulator and the p-i-n structure, respectively. Based on the above description, the working mechanism can be explained in more details. Initially, before application of any bias, the memory device is in the initial state "0," where the device is in full thermal equilibrium, i.e., the Fermi level is flat throughout the device.

2.4.1. Writing Process

First, we discuss the writing process. If we apply a negative voltage to the pinMOS memory, the Fermi energy of the anode is increased with respect to the cathode as shown in Figure 4(i). This situation will result in a new quasi-steady state in which no current can flow as the insulator is assumed to be ideal, i.e., blocking any flow of carriers between the semiconductor and the metal at all voltages. The only case in which no current

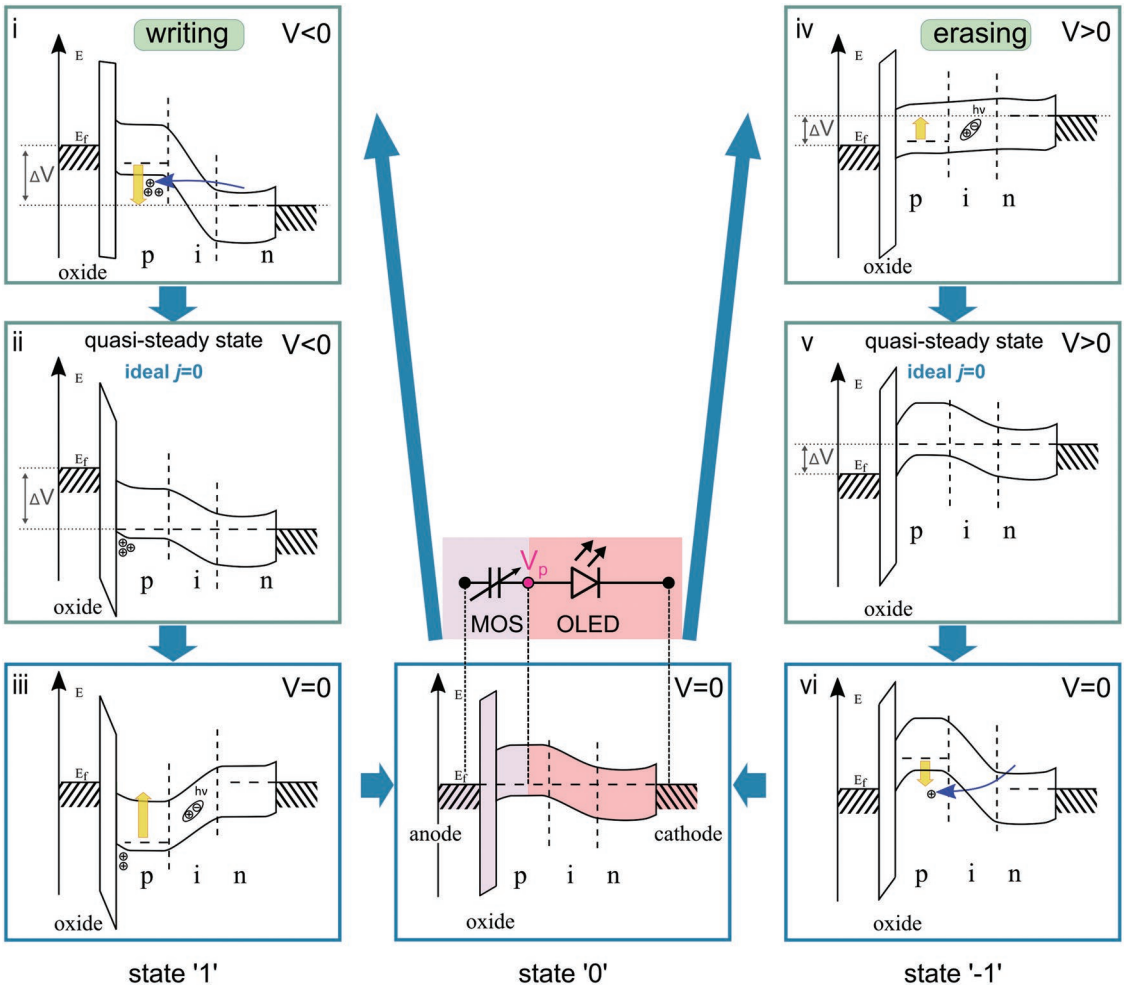

Figure 4. Overview of working mechanisms in pinMOS memory. The holes shown in the schematic are excess holes in the p-doped layer.

flows in the p-i-n structure is when there is no potential drop over it, as schematically shown in Figure 4(ii). Thus, in the idealized quasi-steady state, it is essential to realize that any applied voltage drops over the insulator entirely. This also means that V_p in Figure 4(i) has to approach to the potential of the cathode as illustrated by the yellow arrow, which can only be achieved by charge exchange between the cathode and p-doped layer via tunneling. Just after switching the pinMOS memory to a large negative voltage and before this quasi-steady state is reached, a significant potential drop across the OLED element in the reverse direction results the Zener tunneling which leads to holes tunneling into the p-doped region.[4,10,28] While the holes accumulate in the p-doped layer, the Fermi level of p-doped layer gradually lowers from case (i) to case (ii) of Figure 4, achieving the quasi-steady state.

Once the applied bias voltage is reduced back to 0 V (Figure 4(iii)), the voltage drops over the oxide will be as big and opposite to the voltage drops over the p-i-n stack. As a consequence, the OLED element of the device will be biased in the forward direction, i.e., charges will flow into the intrinsic region, recombine, and emit light. As the current density in the forward direction can be quite high (Figure 1c), the V_p will readily relax toward the potential of the external electrodes. However, this results in the forward voltage drop over the OLED element to be reduced, and the current flow will sharply decrease as well. Eventually a further discharge of pinMOS memory will be almost stopped, and only leakage currents in the forward direction remain. The time it takes for the device to return from the "stressed" state "1" to the initial state "0" is then the retention time of the pinMOS memory, and it mainly depends on the leakage current through the oxide or the p-i-n stack.

2.4.2. Erasing Process

When a small positive voltage is applied to the pinMOS memory in the state "0" (initial state), charges are injected into the OLED element, holes from the p-doped layer, and electrons from the cathode (Figure 4(iv)). The charges form excitons that radiatively recombine and produce light emission, accompanied by a current flow in the forward direction of the OLED element. However, the holes from the p-doped layer are eventually depleted due to their injection being blocked by the insulator, creating a depletion region in the p-doped layer. Similar to the writing process, the V_p in Figure 4(iv) has to change according to the potential of the cathode to reach the new quasi-steady state "−1" in Figure 4(v). During this process, the OLED element is operated under the forward direction, so that erasing can be quite fast since high current densities are achievable in the forward direction of the OLED element.

If the applied voltage is reduced back to 0 V, the internal potential drop over the p-i-n stack of OLED element will now be in the reverse direction as shown in Figure 4(vi). Considering the small current density in the reverse direction of the OLED element, the p-doped layer will on very slowly be populated with holes again. The destruction of state "−1" will be caused by any process that leads to the repopulation of the p-doped layer with holes, e.g., light absorption, Zener tunneling, or generally leakage through either the p-i-n junction or the insulator.

These assumptions are based on an idealized scenario. In reality, any leakage currents through the oxide will prevent the internal potential V_p to be fully aligned with the potential of the cathode at the quasi-steady state. Nonetheless, the qualitative description of the idealized case remains valid also for the real device.

2.4.3. Reading Process and a Short Summary

Besides the writing and the erasing processes, reading the actual device state is also highly important to the memory functionality. Reading basically means to distinguish between state "1" and state "−1" at a chosen voltage, e.g., 0 V. There are two possible readout methods: i) readout of the capacitance difference at different states, and ii) checking whether light emission occurs upon forward bias application. The first method will keep the state while the second is destructive, i.e., may switch the device state from "−1" to "1."

The working mechanism discussed above suggests that the information storing and releasing processes of the pinMOS memory rely on the internal potential V_p. Due to the presence of the insulator, all electrical currents that flow after an external bias potential is applied will be internal, i.e., flow in the p-i-n stack exclusively (apart from leakage through the insulator) . This will lead to quasi-steady states in which the applied voltage eventually drops entirely over the insulator, no matter which sign of external potential is applied. Please find the transients of the current during writing or erasing in Figure S1 of the Supporting Information. However, once the external bias is removed under any such quasi-steady states, there will be a significant built-in potential that drops over the p-i-n stack, representing a nonequilibrium state that is the precise reason for the memory effect we observe. The processes of writing and erasing this memory device are accompanied by hole accumulation and hole depletion in the p-doped layer as well as carrier recombination and Zener tunneling in the p-i-n stack. During these writing and erasing processes, the capacitance of pinMOS memory varies as the two voltage-dependent capacitances of the two abstract device elements, the MOS-capacitor and the p-i-n stack, vary. In both cases, the modulation of the capacitance results from the variable depletion zone width of the incorporated doped layers. Due to the series connection of both subdevice capacitors (MOS-capacitor, p-i-n stack), they contribute differently to the total device capacitance, i.e., the lower one will predominantly define the device capacitance that we can measure by the impedance spectroscopy.

2.5. Pulse Characteristics and Corresponding Optical Property

To verify and record the state-dependent light emission from the pinMOS device, a setup was created that consists of a photodiode and a camera and is mounted directly on top of an OLED to record the pulse-varying luminance signals and emission images. Since in this device there is no emission under DC bias application in the forward direction, voltage pulses with varying pulse parameters were applied to the pinMOS memory. We used a pulse with a repetition rate of 100 Hz and a duty cycle of

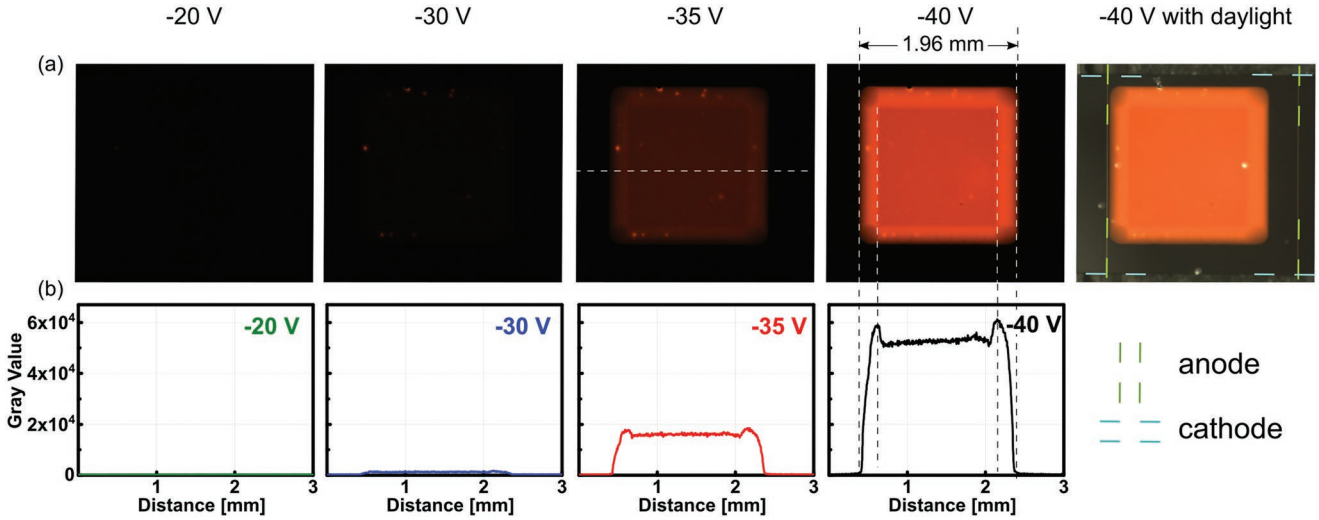

Figure 5. a) Images of a pinMOS memory device under different pluses. b) The corresponding light intensities, spatially resolved.

20%, with writing voltage pulses in the range of −20 to −40 V and 8 ms duration, and erasing voltage pulses of 3 V (constant) and 2 ms duration. The resulting emission images and the corresponding light densities were recorded after a 5 s integration time as shown in **Figure 5**. All images in Figure 5a except the last one were recorded in the dark.

The x-axes in Figure 5b correspond to the horizontal positions in the images in Figure 5a, and the light intensity values are extracted along the positions indicated by the white dashed line in the image with −35 V. The image for the −20 V writing voltage shows no emission intensity distribution. This suggests that at −20 V the Zener tunneling during the 8 ms writing pulse duration is not sufficient to repopulate the p-doped region with holes to an extend that would produce detectable emission during the reading pulse. With the increase of the writing voltage to −30, −35, and −40 V, an increase in overall light intensities is obtained due to the fact that more holes can tunnel into the p-doped layer in the presence of the stronger electric fields across the p-i-n junction.

We observe a square-like, homogeneous emission area with a side length of 1.96 mm, which is smaller than the active area given by the overlap of the electrodes (see daylight figure in Figure 5a), but is in good agreement with the size/area of the p-doped layer. The lateral distribution of emission intensity is also related to the sample rotation during device fabrication that leads to slight variations in the layer thickness which can be observed as emission nonuniformities at the edges and the corners. In general, conversion from electrical to an optical signal in the pinMOS memory is verified by the emission signal and the structuring of the doped layers efficiently dominates the emission area.

After the qualitative proof of the device emission, a more detailed study of the pulsed measurements and the corresponding optical properties was done with the same 20% duty cycle and 100 Hz repetition rate. For these tests, the erasing voltage under which light is emitted was fixed to be 3 V, while the writing voltage was again varied (**Figure 6**a). The curves in green and orange (obscured by the green) were recorded at −20 V which as shown already above is not sufficiently replenishing the p-doped layer within the 8 ms application time and thus produces no device emission. The writing voltage was stepwise increased from −30 to −40 V (red-tone curves) and decreased back to −30 V (blue-tone curves) in steps of −1 and +1 V, respectively. The corresponding device brightness values were recorded by the photodiode shown in Figure 6c with the same color groups as before. The near perfect overlap between the two groups of curves hides the forward curves (orange and red-tone) and thus confirms an excellent repeatability of the pulsed emission. Regardless of the device brightness value, the photodiode traces prove that the light emission starts immediately after changing the voltage from negative to +3 V before it is rapidly quenched due to the exhaustion of holes in the p-doped layer, leading to a series of sharp emission peaks. Moreover, such light emission only happens if a sufficiently high negative writing voltage is applied beforehand. With the increase of the writing voltage magnitude, a higher electric field across the p-i-n junction promotes stronger Zener tunneling. As a consequence, more holes are accumulated in the p-doped layer, producing higher and sharper brightness curves. It is important to recall that both the writing and erasing voltage values and their respective pulse durations are determining the number of charges that are stored. Applying −15 V for seconds is sufficient for charging the p-doped layer to a definite potential, but in order for shorter durations such as 8 ms to be sufficient, larger voltage such as −30 V are required. The voltage operation parameters are, at this early stage of device development, still beyond practical levels. However, the writing efficiency is expected to increase if the Zener tunneling is enhanced by accurate control over the doping concentration and the thickness of the intrinsic layers, both constituting our planned research direction to further improve the device.[28]

Next, we evaluated the relationship between erasing voltage and light emission. For these tests, the writing voltage remained constant at −40 V, while the erasing/light emission voltage was varied from −10 to +5 V (Figure 6b). Curves for negative erasing voltages are in blue and all other curves

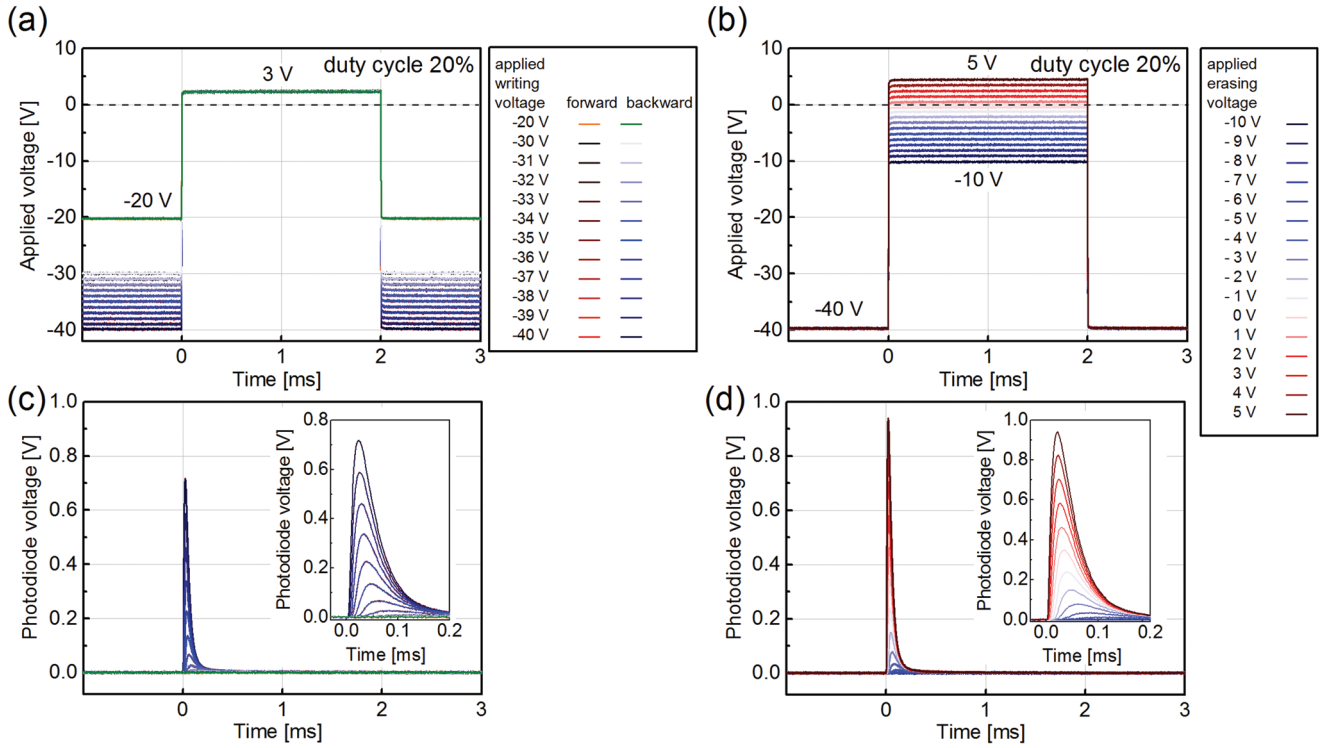

Figure 6. Time-resolved measurements of applied device voltages a,b) and corresponding device brightness c,d) for duty cycle of 20%. Inset: Zoom in images of device brightness.

are in red tones. In contrast to a typical OLED, light emission can occur already at negative erasing voltages as can be seen in Figure 6d, i.e., light emission can here surprisingly occur after application of two negative voltage biases: a large negative writing bias and a small negative erasing bias. Within our proposed working mechanism this can be understood from the fact that the large negative voltage application can accumulate excess amounts of holes in the p-doped layer (compared to the device initial state) which enables charges to flow back to the OLED element to recombine under light emission even at an applied upper voltage −4 V. Similarly, the higher the erasing voltage is, the sharper and higher the brightness curve can be, owing to the larger applied voltage in the OLED element in the forward direction.

2.6. Photoinduced Writing Process

If the pinMOS memory can be read out by light, it would be interesting and for certain applications also highly desirable to be able to write the device by light as well. To demonstrate the basic function of this concept for our pinMOS device, we used ultraviolet (UV) light with a wavelength of 375 nm, generated by a commercial LED, that is known to create free charge carriers in this kind of red OLEDs.[29] As can be seen in **Figure 7**, the illumination intensity that is controlled by both the UV LED current and the duration of the exposure, has an evident influence on the shape of the CV curve. The effect is similar to applying a negative electrical bias with the most notable difference that under the UV illumination,

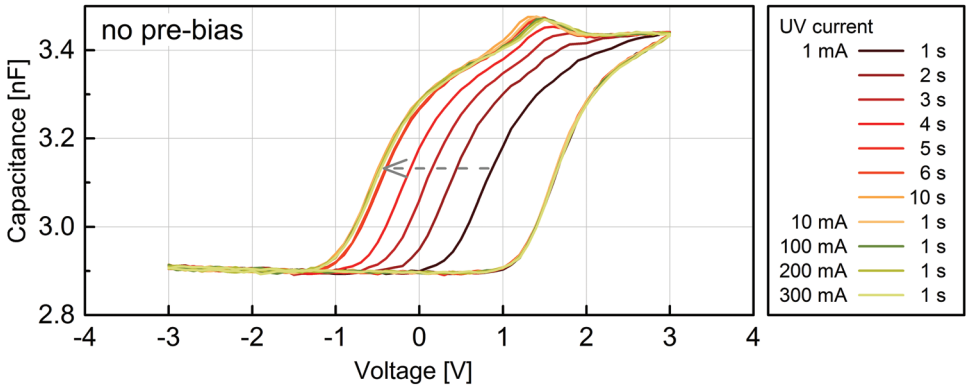

Figure 7. CV curves measured under a preillumination of UV light.

band-to-band excitation and generation of electron–hole pairs in the intrinsic layer rather than Zener tunneling controls the hole population in the p-doped layer. An exposure to the UV light from the UV LED driven at 1 mA (intensity exposed to the device is $\approx 8 \times 10^{-2}$ mW cm^{-2}) for 1 s already generated enough carriers to observe a memory window of 1 V. The pinMOS memory exhibits light-dependent characteristics based on both light intensity and illumination time. Except for the hump at the high-capacitance plateau around 1.3 V, the CV curves have similar behaviors in forward curves shifting and reverse curves stabilization as voltage stimuli curves.

The most pronounced memory window could be achieved under 1 mA UV LED illumination for 5 s. Although the maximum memory window obtained from UV illumination is smaller than the one obtained electrically, a controllable memory behavior can still be obtained through UV irradiation. The reason for the hump in the high-plateau at 1.3 V is currently unclear, but it amplifies the capacitance difference between the "1" and "–1" state at this specific voltage instead of eliminating the information. Such a hump is "removable" and will disappear when the device is measured again with voltage sweep without UV illumination. Compared to the electrically obtained CV curve hysteresis, the capacitance values of both low and high plateaus remain unchanged, although the hole regeneration mechanism in the p-doped layer is different under UV light illumination. This confirms that two series-connected and sweep-voltage dependent capacitances of the MOS-capacitor and the p-i-n junction are not generally affected by the writing method. Besides this, the pinMOS memory can be programmed by optical stimulation and output light-dosage-dependent and history-dependent capacitance states, for which holds promise for optical storage, like constructing an artificial visual memory system as an image sensor, or being used as a UV photosensor based on capacitance mapping.[30–32]

3. Conclusion

We fabricated a nonvolatile, multiple-bit storage, capacitive memory device dubbed pinMOS memory that provides optoelectronic control in both the writing and reading processes. The fairly simple, diode-capacitor based memory device shows good performance with an endurance of well over 10^4 cycles (no change within 10^4) and retention times over 24 h. The depletion-accumulation mechanism, distinguished from the conventional charge-trapping or charge tunneling based devices, enables various pathways for reading, erasing and writing. We are positive that our realization of this easily fabricated memory provides an avenue for future electronic or photonic applications. For example, paired with synapse capacitors, the pinMOS memory devices promising capacitive neuromorphic computing in which serve as memcapacitive neurons. The possibility to manipulate the memory states by light—here currently UV light to write, red light emission to read—creates new opportunities for the development of the photonic memory devices, artificial visual memory system, and photosensing systems.[30]

4. Experimental Section

Device Fabrications: After cleaning of the glass substrate with prestructured finger-like indium tin oxide (ITO, anode) electrodes, a 50 nm aluminum oxide (Al_2O_3) layer was deposited by atomic layer deposition (ALD, TFS 500, Beneq Oy). Then, p-doped/electron blocking/intrinsic/hole blocking/n-doped/top cathode layers covered onto Al_2O_3 layer by using 50 nm Spiro-TTB:F_6-TCNNQ (4 wt%), 10 nm NPB, 20 nm NPB:Ir(MDQ)$_2$(acac) (10 wt%), 10 nm BAlq$_2$, 50 nm BPhen:Cs (ratio 1:1), and 100 nm aluminum (Al) via thermal vapor deposition in high vacuum (base pressure $<10^{-8}$ mbar). F_6-TCNNQ was purchased from Novaled AG (Dresden, Germany). All samples were encapsulated in a nitrogen atmosphere and share the same crossbar architecture. Both p-doped layer and n-doped layer (1.94×1.94 mm^2) were designed to be smaller than the active area (2.54×2.54 mm^2) defined by the overlap between the top and bottom electrodes.

Device Characterizations: The capacitance versus voltage/time characteristics were done by using an HP 4284 A Precision LCR meter, under a modulation amplitude of 10 mV at a frequency of 100 Hz. For all pulsed measurements, an arbitrary waveform generator 33600A from Keysight Technologies provided a low-voltage/high-frequency (100 Hz) sine wave signal, which was fed into a 50 times voltage amplifier. The DPO7354C digital phosphor oscilloscope from Tektronix is used for recording all electrical data, while the luminance was obtained by photodetector. The APG2C1-375-E UV LED was a InGaN based 375 nm single chip LED from Roithner Lasertechnik. All characteristics were measured and controlled by SweepMe! (sweep-me.net).[33]

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

Dr. Axel Fischer is co-founder of "Axel Fischer und Felix Kaschura GbR," which provided the measurement software "SweepMe!" (sweep-me.net). The name of the program is given in the Experimental Section.

Keywords

diode-capacitor memory, metal-oxide-semiconductor, nonvolatile organic memory devices, organic light-emitting diodes, Zener tunneling

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