Normally-off GaN Transistors for Power Applications

To cite this article: O Hilt *et al* 2014 *J. Phys.: Conf. Ser.* **494** 012001

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Normally-off GaN Transistors for Power Applications

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Abstract. Normally-off high voltage GaN-HFETs for switching applications are presented. Normally-off operation with threshold voltages of 1 V and more and with 5 V gate swing has been obtained by using p-type GaN as gate. Different GaN-based buffer types using doping and backside potential barriers have been used to obtain blocking strengths up to 1000 V. The increase of the dynamic on-state resistance is analyzed for the different buffer types. The best trade-off between low dispersion and high blocking strength was obtained for a modified carbon-doped GaN-buffer that showed a 2.6x increase of the dynamic on-state resistance for 500 V switching as compared to switching from 20 V off-state drain bias. Device operation up to 200 °C ambient temperature without any threshold voltage shift is demonstrated.

1. Introduction

High voltage GaN-based power switching transistors enable efficient power converters with increased power density. High converter switching frequencies can be realized with lateral GaN-based HFETs due to the low area-specific on-state resistance for a given blocking strength and the low gate charge required for switching [1]. The GaN HFET technology is also considered as cost-efficient since devices can be manufactured on Si substrates using processing steps of a CMOS-Fab environment [2]. Major challenges for market introduction is the conversion of the natural normally-on device characteristic to normally-off and the reduction of the increased dynamic on-state resistance when switching the device from high-voltage off-state bias to the on-state.

Recent attempts to convert AlGaN/GaN high electron mobility transistors (HEMTs) into normally-off devices, using gate recess [3] or fluorine incorporation [4] showed limited applicability for power electronics due to their low threshold voltages $V_{th} < +1$ V, their low gate swing of ~ 2 V and their high on-state gate current. The introduction of a gate insulator suppresses the gate current and may extend the gate swing [2]. The used extrinsic insulator layers are often atomic layer deposited (ALD) oxides like Al_2O_3 or HfO_2 and are deposited at temperatures < 300°C. The observed trap states in the insulator bulk or at the interface to the AlGaN barrier often deteriorate the device switching performance and limit the device reliability [5]. Gate-injection GaN-HFETs using a p-type AlGaN-gate have been developed by Panasonic and give a threshold voltage of +1 V - +2 V [6].

The here presented p-GaN gate GaN-HFETs use a similar concept for normally-off operation as in [6]. While Panasonic highlights the hole-injection regime for on-state operation, this regime is avoided for the presented devices. Hole injection from the gate is paired with additional gate current and an

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increased gate charge. Both would contribute to losses during switching transistor operation and should thus get avoided.

This paper focuses on GaN-buffer variations for the lateral GaN devices to obtain an optimum combination of secure normally-off characteristic, high off-state blocking voltage and a low dynamic on-state resistance. Additionally, the high-temperature DC characteristics up to 200 °C base-plate temperature get presented.

2. P-GaN gate normally-off transistors

In the p-GaN gate transistors presented here, the gate consists of in-situ grown Mg-doped GaN with an ohmic contact for biasing [7]. P-GaN gate GaN-HFETs combine the high-mobility two-dimensional electron gas (2DEG) transistor channel known from AlGaN/GaN HEMTs with reliable normally-off operation, as required for applications in power electronics.
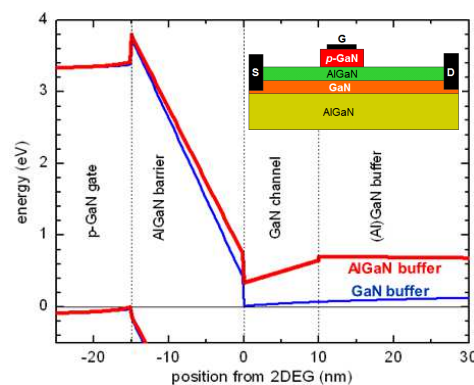

Figure 1. Simulated band diagram at the gate position of a p-GaN gate AlGaN/GaN HFET with GaN buffer (blue) and AlGaN buffer (red). The conduction band energy at the 2DEG position is significantly shifted above the Fermi level for the AlGaN buffer structure. The device structure is sketched in the inset.

The gate acceptors deplete the 2DEG of the transistor channel, when unbiased and a positive gate bias is needed to open the transistor. The simulated band diagram at the gate position (figure 1) confirms that the 2DEG channel at the heterojunction between GaN channel and AlGaN barrier does not cross the Fermi level (blue conduction band line in figure 1). Replacing the GaN buffer by AlGaN and using uid GaN for the transistor channel generates a virtual p-type doping at the AlGaN back-barrier of the channel and further increases the 2DEG depletion beneath the gate (red conduction band line in figure 1). Fabricated p-GaN gate transistors with $Al_{0.05}Ga_{0.95}N$ buffer and with iron-doped buffer (GaN:Fe) demonstrate the normally-off characteristics, see figure 2. Threshold voltages of +1 V and above have been realized for this normally-off approach.

In on-state, the gate bias can be driven to 5 V and more. The nature of the pin-type gate diode restricts the on-state gate current to 10 µA/mm for V_{GS} = 5 V. Driving the gate to V_{GS} > 7 V will lead to hole injection from the gate to the transistor channel as described in [6] for the p-AlGaN gate transistors.

In off-state, at V_{GS} = 0 V, the drain leakage current is limited to 1 µA/mm for the AlGaN-buffer device and to 30 µA/mm for the GaN:Fe-buffer device. As suggested by figure 1, a higher threshold voltage has been obtained for the AlGaN buffer devices with the incorporated back barrier.

250 V / 85 mΩ normally-off switching transistors in p-GaN gate technology have been fabricated by using the AlGaN buffer approach. The required device gate width of 113 mm has been divided into 30 sub-cells that are connected via bumps to the sub-mount (right side of figure 3).
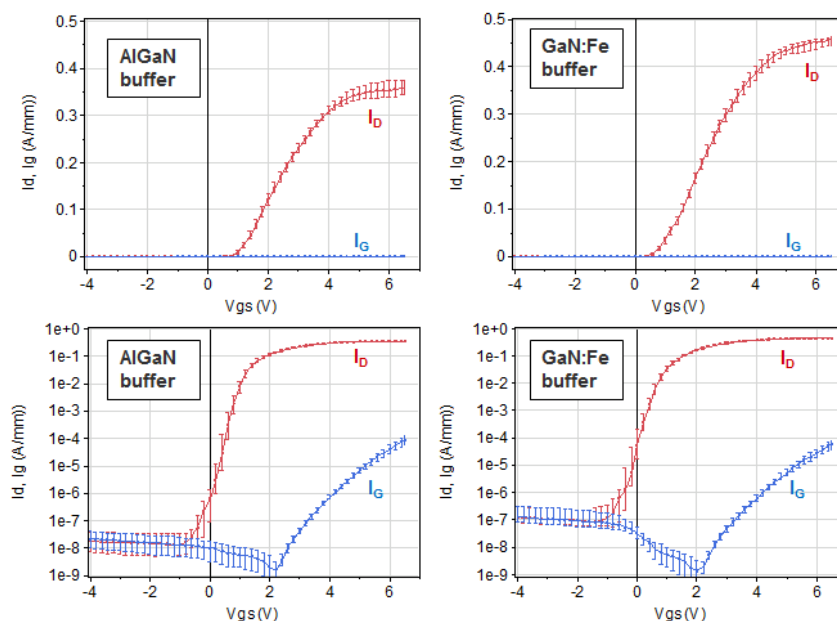
Figure 2. Transfer characteristics and gate current (linear representation on top, logarithmic representation on bottom) of p-GaN gate HFETs based on an AlGaN buffer (left) and on an iron-doped GaN buffer (right). The median currents with 25%/75%-quantiles (error bars) of 30 devices spread over a 3" wafer are shown. Device gate width is 2.1 mm, gate drain separation is 15 μm and $V_{DS} = 10$ V.

The device output characteristics demonstrate off-state condition for $V_{GS} = 1$ V and on-state condition for $V_{GS} = 5$ V (left side of figure 3). The current can be driven to more than 20 A. The 250 V blocking strength is derived from the off-state drain leakage < 1 mA/mm. The area-specific on-state resistance is $R_{ON}A = 1$ mΩcm^2 with considering the active device area as A only. This value is approx. a factor 5 lower than for Si-based MOSFETs of the same voltage class [7].
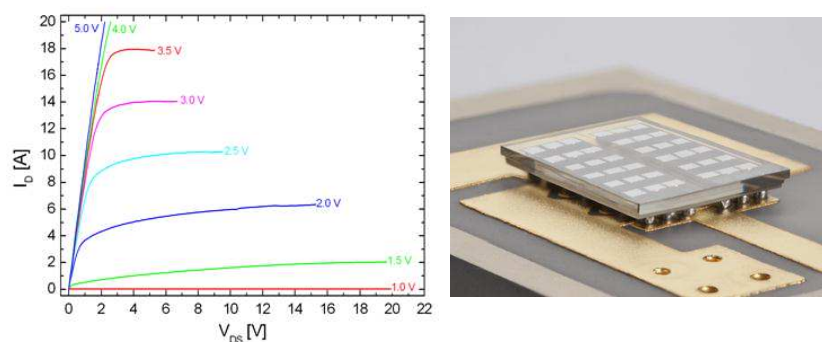

Figure 3. Output characteristics (left) and photograph (right) of a 250 V / 85 mΩ normally-off GaN HFET in p-GaN gate technology. The device has 113 mm gate width and is assembled in flip-chip technology.

3. Buffer concepts for high voltage operation

The breakdown voltage of GaN HFETs should ideally increase with the gate-drain separation d_{GD} since the electric field in off-state distributes between gate and drain. This breakdown voltage scaling is lost when electrons from the transistor channel manage to bypass the gate control region via deep

layers in the buffer. The resulting source-drain leakage current prevents higher blocking voltages, independent of d_{GD}. The major cause for this electron punch-through effect is the limited barrier height of the GaN buffer beneath the transistor channel with the two-dimensional electron gas [8]. The Fermi level in uid-doped MOCVD-grown GaN-layers is usually shifted towards the conduction band and the back-side barrier towards the buffer is in the order of 100 meV, see figure 1.

Punch-through effects and the associated source-drain leakage can get suppressed by a better electron confinement to the channel. An AlGaN buffer beneath the GaN channel creates an efficient barrier for the channel electrons (figure 1). The buffer conduction band is shifted upwards due to the polarization differences and the band energy differences between the GaN channel and the AlGaN buffer [8]. A breakdown voltage scaling of 40 V/µm gate-drain separation was measured for $Al_{0.05}Ga_{0.95}N$ back-barrier based p-GaN gate devices and 870 V breakdown voltage has been obtained [7]. GaN-buffer compensation doping with carbon (GaN:C) or iron (GaN:Fe) also shifts the buffer Fermi level towards the valence band and prevents electrons in the channel to enter the buffer. More than 1000 V breakdown strength with 100 V/µm scaling has been obtained for a GaN:C-based p-GaN gate transistor [10]. GaN:Fe buffer yield 50 V/µm blocking strength scaling [9].

4. Dynamic characteristics and high voltage switching

An increase of the dynamic on-state resistance (dyn. R_{ON}) immediately after switching from high-bias off-state condition is often observed in GaN-HFETs. Trap states in the (Al)GaN-based semiconductor stack or on the semiconductor surface are considered as root cause for this effect [11]. Electron traps inside the buffer may get filled under high bias off-state condition and deplete the transistor channel after switching the transistor to on-state.

Buffer material with very low trap densities is thus considered as straightforward for low-dispersion switching properties of the transistor. Non-compensated buffer designs, however, may be in conflict to the buffer optimization approaches as discussed above for optimum device blocking strength. Pure GaN buffer suffer from punch-through and the device blocking strength of the (non-doped) AlGaN buffer devices is only mediocre.
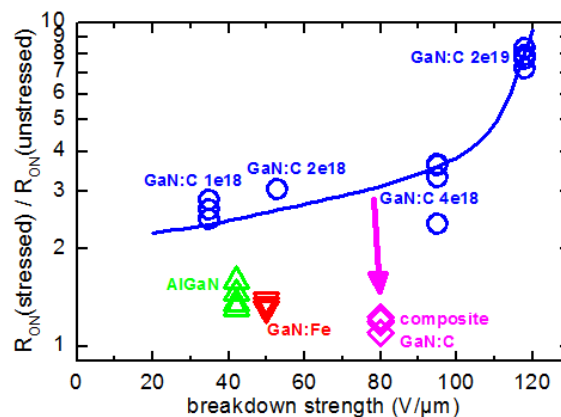

Figure 4. Increase in dynamic on-state resistance for 0.2 µs long pulses into on-state from 65 V off-state bias (with respect to switching from 0 V drain bias) in relation to the device breakdown strength scaling. Test transistors with 0.25 mm gate width and different buffer compositions are compared.

In fact, the increase in dyn. R_{ON} after 65 V off-state bias is for the AlGaN-buffer based devices (42 V/µm blocking strength) much lower than for the 2e19 cm^{-3}-doped GaN:C buffer devices with 120 V/µm blocking strength, see figure 4. Lower carbon doping reduces both, the increase in dynamic R_{ON} but also the blocking strength. Using iron as buffer dopant results in a better trade-off between dyn. R_{ON} increase and blocking strength as compared to the AlGaN-buffer and GaN:C-buffer devices.
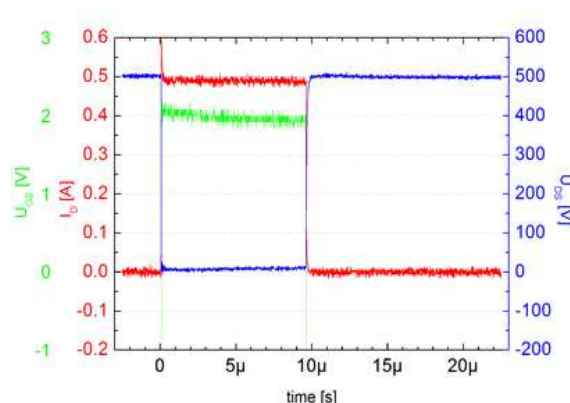
Figure 5. 500 V / 0.5 A switching transient for a GaN HFET with modified GaN:C buffer structure and 2.1 mm gate width. The dynamic R_{ON}, as extracted from the on-state voltage drop is 16 Ω, corresponding to a 2.6x increase of the R_{ON}.

For devices with 50 V/µm blocking strength, the increase in dyn. R_{ON} is factor 3 for the 2e18 cm^{-3}-doped GaN:C-buffer but only factor 1.4 for the GaN:Fe-buffer.

The complete semiconductor stack charge balance and the resulting potentials inside the device have to be taken into account for a deeper understanding of the dispersion phenomena [12]. Recent switching experiments with a modified composite GaN:C-buffer device that additionally had an AlGaN back-barrier and a GaN cap incorporated showed a successful combination of high blocking strength and low dispersion. The device with 80 V/µm blocking strength showed only a 1.2-times increase in dyn. R_{ON} for pulsing from 65 V (figure 4). Drain voltage and drain current transients during 500 V / 0.5 A switching with a packaged device were taken (figure 5). The measured dynamic R_{ON} was 16 Ω for the device with 2.1 mm gate width. This corresponds to an 2.6x increase in dyn. R_{ON} after switching from 500 V.

5. Temperature dependence

GaN-based switches can in principle operate at elevated temperatures of 300°C or more due to their high bandgap energy of 3.4 eV. The temperature dependence of the drain current and of the threshold voltage is important for the thermal stability of the device as thermal runaway can be avoided by a negative temperature coefficient of the drain current. Figure 6 shows the transfer and on-state output characteristics at ambient temperatures between 25 °C and 200 °C for small test transistors with low self-heating in the on-state.
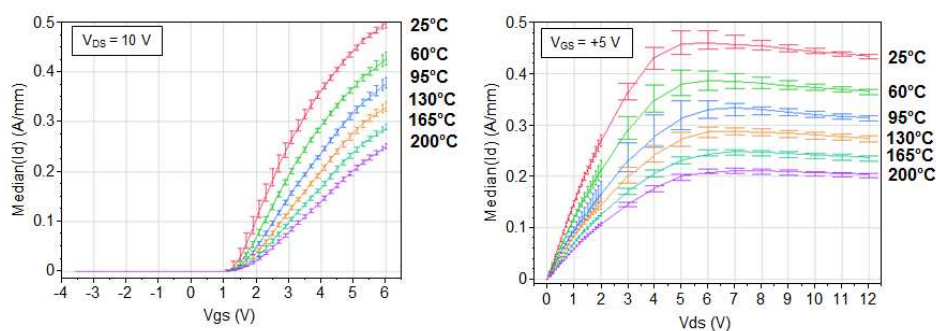

Figure 6. Temperature dependence of the transfer characteristic (left) and the on-state IV curve (right) of 30 p-GaN gate HFETs on one 3" wafer. The median currents with 25%/75%-quantiles (error bars) are shown. Gate width is 0.25 mm and gate drain separation is 6 µm.

The threshold voltage is within a variation of +/- 80 mV essentially independent on temperature. The on-state resistance increases with temperature ($\alpha = 8.2 \times 10^{-3}$ K^{-1}) and the maximum drain current in on-state shows a negative temperature coefficient $\alpha = -2.9 \times 10^{-3}$ K^{-1}. Stability of the threshold voltage is due to the essentially temperature-independent electron concentration in the 2DEG, the temperature dependent saturation current (and R_{ON}) is related to the phonon-scattering of the electrons, increasing with temperature [13].

There is no device operation point with a positive α for the drain current due to the temperature-independent V_{th}. Current focusing and hot spots on limited sub cells of the transistor get thus also avoided for operation conditions with not fully opened transistor.

6. Conclusion
250 V / 85 mΩ normally-off p-GaN gate transistors with 1 V threshold voltage and 5 V gate swing have been demonstrated. The threshold voltage is stable up to 200 °C. The device buffer structure has to be designed carefully for high-voltage operation and efficient switching. 500 V / 0.5 A switching with an only 2.6x increased dynamic on-state resistance has been demonstrated.

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