An Implantable Phase Locked Loop MEMS Based Readout System for Heart Transplantation

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***Abstract*—An implantable readout circuit using a MEMS pressure sensor has been designed and implemented to monitor the heart activity after heart transplant surgery. It features a time domain architecture using two identical voltage-controlled oscillators and phase locked loop circuits. The circuit was implemented in a 65 nm CMOS technology with 1 V power supply. It consumes 100 µW power and provides a digital output that is proportional to the analog sensor input with a bandwidth of up to 4 kHz. The SNR of the system is 53 dB. Measurements show the operation of the readout chip with the MEMS sensor.**

***Index Terms*— Implantable heart monitoring readout circuit, MEMS readout, resistor sensor, phase locked loop (PLL), voltage control oscillator (VCO), Wheatstone bridge.**

I.INTRODUCTION

EVERY year more than 50,000 people in the world are possible candidates for heart transplantation surgery (HTx) while only 5,000 among them have the opportunity to undergo this surgery. Although it is an established therapy for end-stage heart failure for both men and women with a one year survival of 91% and a median survival of 12 to 13 years, these patients suffer from limited exercise capabilities and quality of life due to complications as the result of inevitable heart denervation involved during the surgery [1]–[3]. Heart transplantation surgically interrupts the parasympathetic vagal neurons and the intrinsic postganglionic sympathetic nerve fibers traveling to the myocardium [2]. As a result, these patients have a higher-than-normal heart rate at rest, and, in response to exercise, the heart rate increases more slowly than normal to reach a lower maximal heart rate, which descends during recovery from exercise at a slower than normal rate [2]. As post- HTx reinnervation progresses with time, the intrinsic heart rate assumes a lesser contribution to the resting heart rate leading to a partially normalized resting rate [3]. Thus, it is important to investigate the physiology of a denervated heart and to develop a bioelectronic solution for monitoring the heart rate in HTx patients during post recovery to improve their quality of life.

To implement such an implantable monitoring system for the heart, a power budget of less than 200 µW is required. For a dynamic range of 80 mV, the chip size should not exceed 0.2 mm^2, in order to be easily integrated with the MEMS sensor and implanted on the left ventricle of the heart. The system requires 8 bit resolution with sampling frequency of higher than 10 kHz, due to the nature of low frequency ECG signals.

This brief describes the design and implementation of an implantable low power and small area analog to digital readout integrated circuit in 65 nm CMOS technology for monitoring heart activity based on the above specifications. It interfaces to a MEMS pressure sensor providing a novel, complete system solution for artificially re-establishing vagal control in a denervated heart while monitoring heart rate. The rest of the paper is organized as follows. Section II describes the system architecture. Section III details the circuit design. Section IV reports the performance of the prototype readout circuit when interfaced with a MEMS pressure sensor. Concluding remarks are drawn in Section V.

II. SYSTEM LEVEL DESIGN

The block diagram of the readout system is shown in Fig. 1. The phase locked loop (PLL) design was preferred to the delta sigma modulator design because it offers both small area and low power consumption. Although the sensor to digital converter based on PLL resembles a delta sigma modulator with first order quantization noise shaping due to frequency to phase conversion of the oscillators and over sampling ratio (OSR), it is important to note that, in this approach, due to the feedback mechanism the sensor to digital conversion is done inherently [4]. In addition, instead of comparing the voltages in amplitude domain, they are first converted to time/frequency domain using two voltage-controlled oscillators (VCOs) and are subsequently compared and processed in digital time. The operation is based on a Wheatstone bridge configuration. Its left arm is the resistive divider output of the MEMS sensor which generates V_S, and its right arm generates the balancing voltage V_L from a resistive digital-to-analog converter (R2R DAC) [5]. The two VCOs convert V_S and V_L to frequencies f_s and f_L. The voltage difference between V_S and V_L is recorded as the phase difference of their frequencies. A phase detector applies the difference ε to a digital proportional/integral (PI) filter which

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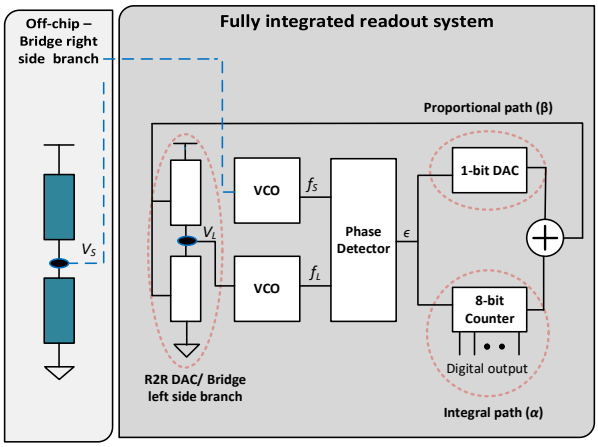

Fig. 1. System level architecture of the integrated readout circuit for monitoring heart activity in patients with heart transplantation.

comprises a proportional 1-bit DAC path (β) and an integral 8-bit counter path (α). Due to the PLL dynamics, both VCOs will run at the same frequency if the PLL is locked [5]. Since the VCOs are identical, the feedback loop will balance the Wheatstone bridge and the digital output is then proportional to V_S. The sensor input voltage V_S is translated to sensor frequency f_S:

$$f_S = f_o + K_{vco} V_S \tag{1}$$

where f_o is the free tuning frequency of the VCO and K_{vco} is the gain of the VCO.

The frequency f_L is generated by translating V_L,

$$f_L = f_o + K_{vco}(\varepsilon \cdot \beta + \alpha \cdot \psi) \tag{2}$$

where ε is the phase error between the two VCOs, ψ is the accumulation of phase error in time, α and β are the gain factors of the integral and proportional paths, respectively. Since the proportional path $\varepsilon \cdot \beta$ *is* oversampled, it can be shown that, if both VCOs are running at the same frequency ($f_S = f_L$) the average (oversampled) value of the proportional path (mean $\varepsilon \cdot \beta$) is equal to zero, and $V_S = \alpha \cdot mean(\psi)$ where ψ is the n-bit output of the counter in the integral path. Hence, the digital counter in the integral path tracks the input signal, while the proportional path ensures stability (more details in [5]).

III. Circuit Level Design

A. R2R DACs in Integral and Proportional Paths

The R2R DAC in the integral path functions as the adjustable branch of the Wheatstone bridge. Its dynamic range should be the same as the sensor branch to optimize the integral gain factor. In this application a sensor variation of ±8% corresponding to 80 mV_{pp} is of interest.

Fig. 2 shows the schematic of the 8-bit R2R DAC. Its structure based on [6] provides a voltage output directly without the use of amplifiers and reference voltages. An asymmetric subrange R2R is achieved when two separate equivalent

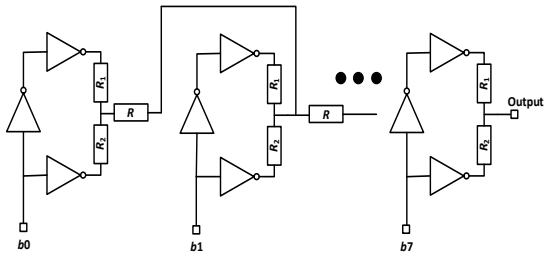

Fig. 2. Schematic of R2R DAC.

circuits are switched by utilizing CMOS devices [6]. The output voltage range of the R2R DAC is defined by the ratio of the resistances R_1 and R_2. By connecting R_1 and R_2 either to ground or V_{DD} using simple inverters, the equivalent reference voltage is

$$V_{\text{Output}} = \frac{R_1}{R_1+R_2} \cdot V_{DD}. \tag{3}$$

The value of R is half the parallel resistance of R_1 and R_2. The two added inverters on each stage optimally match the pull-up and pull-down resistances of the inverters in series with the resistances. The values for poly resistors used for R_1, R_2 and R were 110 kΩ, 90 kΩ and 24.7 kΩ, respectively. The DAC in the proportional path is implemented as a resistive divider since it has only two output states of 0 and 1.

B. Voltage Controlled Oscillator (VCO)

For low power and very low frequencies the VCO design was based on a chain of only four differential delay stages as shown in Fig. 3(a). For the circuit to oscillate, each stage must contribute a frequency dependent phase shift of 45° [7]. The delay stage, shown in Fig. 3(b), contains a source coupled pair with symmetrical load elements which consist of a diode connected PMOS in shunt with two halves of equally sized biased PMOS devices to facilitate the two VCOs. The control voltage (V_c) is the input signal provided from the sensor which defines the lower voltage swing limit of the delay outputs. V_p was set to the mid supply voltage (0.5 V). The delay changes with V_c because the effective resistance of the load elements changes with V_c. The load elements provide good control over delay and high rejection of dynamic supply noise [8].

The simple NMOS current source is dynamically biased by V_{Bias} to compensate for drain and substrate voltage variations, achieving the effective performance of a cascode current source. This also provides high static supply and substrate noise rejection avoiding the extra supply voltage required by a cascode current source [8]. The bias current is continuously adjusted in order to provide the correct lower swing limit of the delay stages which is achieved via a differential amplifier and a half buffer replica as shown in Fig. 3(c). To track all supply and substrate disturbances, the bandwidth of the bias generator is set to be approximately equal to the operating frequency of the delay stages [8]. The required bias voltage for this stage is generated by a cascade of two 2T voltage references including a native MOSFET and a thin oxide MOSFET which is a combination of two devices with a considerable threshold

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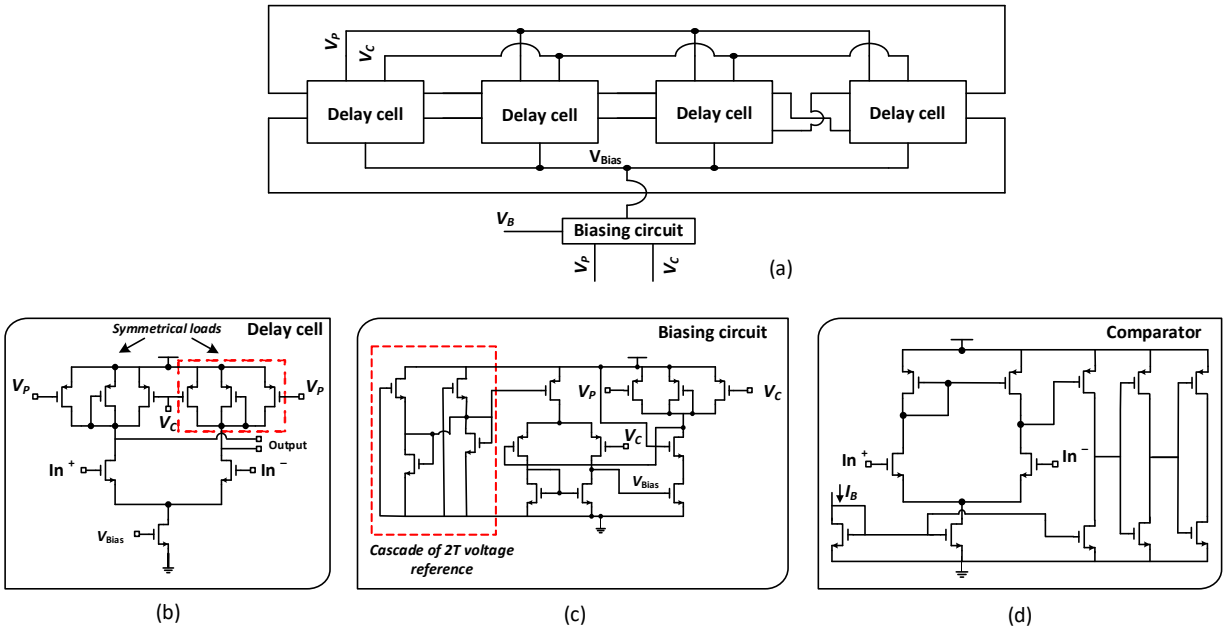

Fig. 3. Schematic of VCO system: (a) VCO system architecture based on delay cells, (b) delay cell schematic, (c) biasing circuit and (d) comparator schematic to generate equivalent square waves from VCO output.

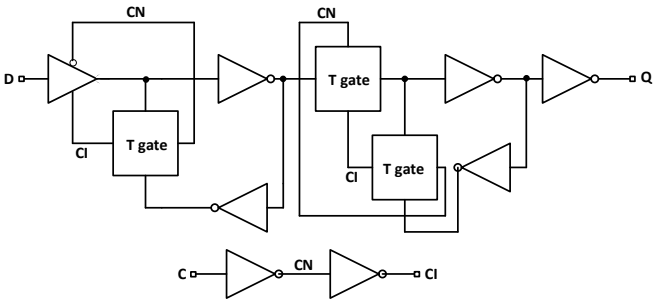

Fig. 4. Schematic of phase detector to compare the phase difference between the two VCOs.

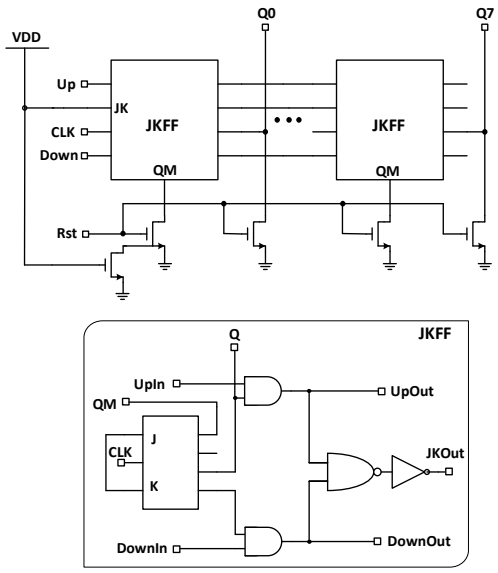

Fig. 5. Schematic of the up/down 8 bit counter.

difference to produce the 2T voltage reference [9]. Sizing of both transistors is chosen to minimize both power consumption and temperature sensitivity.

The overall delay D of the VCO is

$$D = n \cdot t = \frac{C_B}{2k(V_c - V_{th})} \tag{4}$$

where n is the number of stages, t is the buffer delay, $C_B = 2nC_{EFF}$, where C_{EFF} is the total buffer output capacitance, V_{th} is the threshold voltage and k is the transconductance of the PMOS device. A comparator [Fig. 3 (d)] at the output of each VCO generates the square waves required for phase comparison. In simulation at $V_{DD} = 1$ V, the free tuning frequency of the VCO is 3 MHz with a tuning range of ± 1 MHz and each VCO consumes 23.6 µW. The phase noise of the oscillator is -98 dBc/Hz at 100 kHz offset from the carrier frequency.

C. Phase Detector and Counter

The schematic of the phase detector used to detect the phase difference between the two VCOs is shown in Fig. 4 [10]. The output of the detector is triggered when the sensor signal is leading or lagging the feedback loop. The schematic of the 8 bit up/down counter based on JK flip flops is shown in Fig. 5 [10].

IV. Measured Results

The readout chip which converts the MEMS sensor output V_S to a digital output was fabricated in TSMC 65 nm CMOS process technology. It consumes 100 µW from a 1 V supply. The digital data from the ADC was sent to a SMOD A7 FPGA for further processing. The microphotograph of the readout chip is shown in Fig. 6. The active area of 384 µm × 185µm is identified by white rectangles.

The tuning range of the VCOs which corresponds to the dynamic range of the system was measured by sweeping the input voltage. A 16 bit DAC was used to provide the necessary

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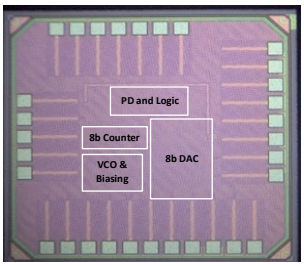

Fig. 6. Micrograph of the readout chip.

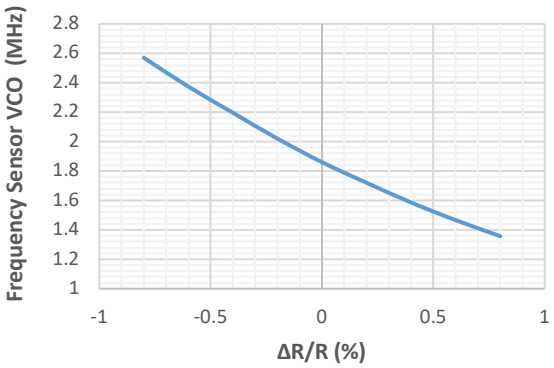

Fig. 7. Dynamic range of VCO for sensor variation (ΔR/R) of ± 8%.

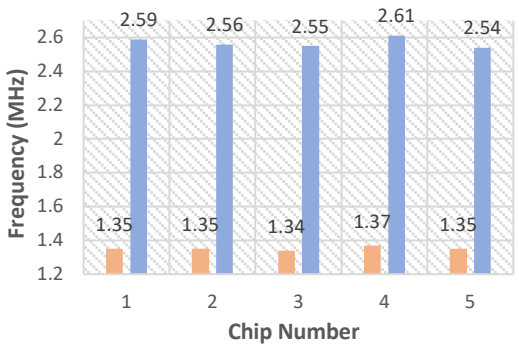

Fig. 8. Variation of the VCO at (ΔR/R) of ±8% in 5 chips.

input voltage sweep. The dynamic range of the readout exceeds 90 mV.

The VCO output frequency for a sensor variation (ΔR/R) of ±8% is plotted in Fig. 7. Although the relationship between the frequency and voltage is linear, there is a spread of the frequency range of the VCOs due to process and mismatch variations. The frequency span is more than 1.2 MHz for all measured results with a free tuning frequency of 1.86 MHz as compared with 3 MHz in simulation results due to process variations. Inter-die variation of the frequency of the sensor VCO with ΔR/R = ±8% at V_{DD} = 1 V was measured over five different chips. The minimum and maximum frequencies are annotated in Fig. 8. The minimum and maximum frequency variations at the lower band is 0.8 and 1.3% with respect to the average and 1.1 and 1.5% at the higher band of frequency with respect to the average for ΔR/R = ±8%.

The decimal code as a function of V_S characteristics of the

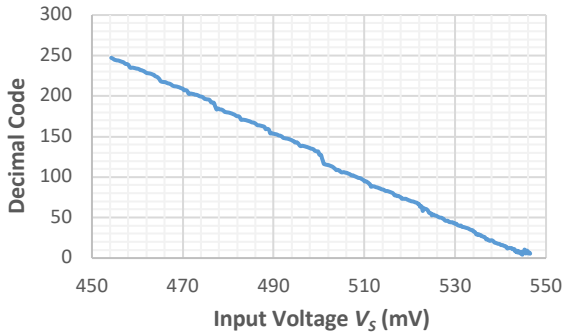

Fig. 9. Digital output of the readout with respect to sensor input voltage range.

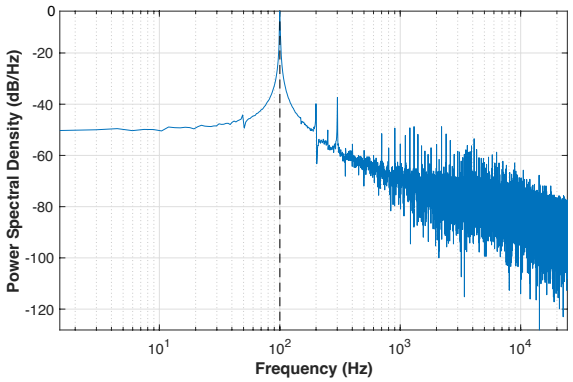

Fig. 10. DFT plot of an input sine wave of 100Hz with full scale amplitude. Number of samples is 32768.

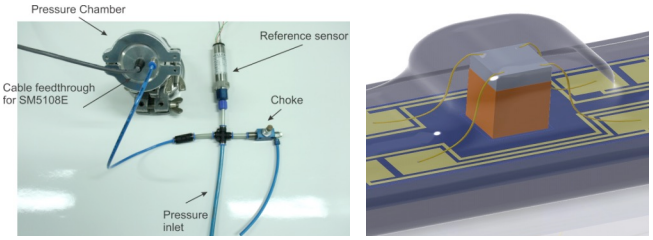

Fig. 11. (a) Measurement setup for MEMS sensor interfaced with implantable readout circuit. (b) MEMS sensor details.

average of five chips is shown in Fig. 9. It is presented as the decimal code vs. sensor input voltage with intervals of less than 1 LSB. The small glitch at V_S = 500 mV might be due to nonlinearity of the ADC. Fig. 10 shows the measured DFT spectrum from the digital output of the readout circuit with a full scale 100 Hz sinusoidal input signal. The SNR is 53 dB. A total of 32768 samples were used. The over sampling ratio (OSR) is 244.

In order to validate the performance of the readout circuit when used with a MEMS input for monitoring the heart rate, the ADC was interfaced with a MEMS sensor (SM5108E). It is an all silicon micro-machined, piezoresistive pressure sensing chip [11]. The die is extremely small (0.69 mm × 0.69 mm) and has been optimized to provide the highest possible accuracy for a die of this size. This sensor has been used in medical applications including wound therapy, so has the potential to be

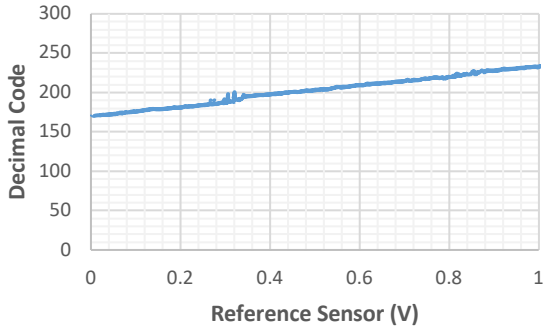

Fig. 12. Measured results of decimal readout with 1 Bar pressure variation subjected to the MEMS sensor. 0 Bar represents pressure near vacuum.

Table I: COMPARISON OF STATE-OF-THE-ART SYSTEMS

	This work	[12]	[13]	[14]	[15]	[16]
Technology (nm)	65	180	180	130	180	----
Supply voltage (V)	1	3.3/1.8	0.6	1	1.8	5
Power diss. (mW)	0.1	3.41	0.54	0.124	0.19	21.5
SNR (dB)	53	N/A	52	79.3	76.4	----
Active area (mm^2)	0.07	0.26	N/A	0.34*	0.82	----
Convers. time (ms)	0.02	0.02	0.014	0.05	N/A	2.1
Bandwidth (kHz)	4	N/A	0.25	10	1	----
ENOB	12.2	9.9	8.9	12.4	15.37	24
FOM**	2.12	50	13.3	1.4	0.19	2.7

* 0.12 mm^2 for preamplifier and 0.22 mm^2 for delta signa modulator.
** FOM = (Power × Conversion time)/2^{ENOB}.

stitched to the transplanted heart and interfaced with the implantable readout with proper encapsulation.

For this application the sensor is exposed to variable pressures in a small pressure chamber. For reference a pressure sensor from Omega Keller, type 21S/80549.3 (0-2 bar; 0-10V) was used. The setup in Fig. 11 shows the test sensor installed in a pressure chamber that was pressurized by compressed nitrogen. The resulting pressure on the sensor is detected as V_S (Fig. 1). The resulting digital output from the ADC was sent to an FPGA and read out from a DAQ system via UART. Fig. 12 shows the measurements of the sensor and readout as decimal code vs. the pressure applied to the MEMS sensor. The decimal code represents 25 mV change on the sensor readout. The small glitch is due to a large DC offset from the sensor which is in the range of tens of mV. Table I provides a comparison with other state-of-the-art systems. Importantly in this application both low power design and small area is achieved. Other state-of-the-art designs provide either low power or small area.

V. Conclusion

An implantable readout circuit has been presented for heart rate monitoring of patients having heart transplantation surgery. The ADC has been tested by interfacing it with a MEMS sensor via a resistive bridge. The small size, low power, and input signal bandwidth, sufficient for ECG signals, makes this design an attractive solution for this application. Future work will entail bonding the readout chip and sensor onto a small substrate which will be encapsulated to create a miniature implant, and subsequently tested in-vivo with a swine heart.

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