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Blackstart Capability of Modular Multilevel Converters from Partially-Rated Integrated Energy Storage

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Blackstart Capability of Modular Multilevel Converters from Partially-Rated Integrated Energy Storage

Zoe Blatsi [iD], *Student Member, IEEE,* Paul D. Judge [iD], *Member, IEEE,* Stephen J. Finney [iD], *Member, IEEE,*

Michael M.C. Merlin [iD], *Member, IEEE*

Abstract—This paper discusses blackstart provision enabled by Modular Multilevel Converters (MMC) with integrated partially-rated Energy Storage (ES) systems. It is demonstrated that ES units integrated in an MMC for ancillary service provision can be utilised to energise the auxiliary power supply electronics of the submodules (SMs), fully charge the converter capacitors, and establish voltage at the ac and dc terminals. This feature can prove especially useful during the converter start-up phase in passive grids or following a post-fault disconnection event. For an MMC with integrated ES, the added functionality of charging the converter capacitors and starting-up the adjacent networks requires no additional infrastructure – only an updated control scheme. The charging algorithm goes through successive steps: ES-SM charging, activation of the Auxiliary Power Supplies in the SMs, active charging of all SMs, and finally, connection to the grid. The effectiveness of the method is confirmed by simulation results where a fully disconnected MMC charges nominally within 2 seconds, and connects to a passive ac network. By using a grid forming control scheme, the converter ramps up the voltage at the ac terminals and supplies 5% of active and reactive power with only 4% of ES-SMs per stack.

Index Terms—Auxiliary Power Supply (APS), Converter Blackstart, Energy Storage (ES), Grid Forming (GF), Islanded Network, Modular Multilevel Converter (MMC).

I. INTRODUCTION

Energy Storage (ES) is a critical asset of the transmission and distribution grid. The variable nature of renewable generation in combination with the increasingly inertia-less ac grid require provision of ancillary services such as voltage and frequency regulation [1], power oscillation damping, and energy shifting [2], to ensure an available and stable grid. In the current technological and economic landscape, ES systems such as battery stacks and ultracapacitors are already deployed for grid-related ancillary services, mainly in the medium voltage (MV) and low voltage (LV) grid.

ES systems are most often interfaced through a single-stage ac/dc system or a bidirectional dc/dc converter fed into a grid-tied ac/dc inverter [3], [4]. In order to minimise the impact of non-uniformities among the different ES cells due to manufacturing process, cell aging or local temperature variations, the ES cells form series and parallel connections [5], [6]. This structure inadvertently increased the complexity of the system.

ES units can alternatively be installed in multilevel topologies, such as the Modular Multilevel Converter (MMC). In that case, the ES units can be subdivided into smaller strings which are interfaced independently to the Sub-Module (SM) capacitors [7]. As a result, higher reliability and availability is achieved. An HVDC-scale MMC targeted at providing ancillary services or peak shaving requires only partial ES [8].

In this paper it is shown that ES systems integrated in an MMC can also be utilised for blackstart, which is the ability of an HVDC system to start-up from shutdown, energise a part of the grid and be synchronised to the grid without an external electrical power supply. Blackstart capability can provide extra resilience to the grid in case of grid contingencies, such as faults resulting in line disconnection. It is a feature that can minimise the downtime of a part of a network in the event of a blackout, therefore it is classified by transmission system operators as an ancillary service [9].

Blackstart provision has been studied in the Offshore Wind Power Plant (OWPP) context. [10] demonstrates that wind power can be harvested from the Wind Turbines (WTs) so that maintenance and downtime due to adverse weather conditions is minimised. [11] presents a complete scenario of an OWPP sequentially charging the offshore ac network and offshore collector MMC before energising the dc cable and reaching the onshore ac grid. In this study the MMC capacitors are charged passively through a pre-insertion resistor from the WTs, with main focus on the strategy of harvesting the wind power in islanded mode and the coordinated grid control. The offshore collector MMC is powered externally, therefore the Auxiliary Power Supplies (APSs) embedded in each SM are considered available at all times and not regarded any further. The work in [12], [13] discusses on standalone start-up of a WT with the aid of an ES unit connected in the dc-link in the nacelle. The power harvested after start-up is fed back to the APS and control electronics through a tertiary winding in the WT transformer. However, the ES unit in the WT is

rated for assisting with start-up until wind power takes over, therefore blackstart and subsequent grid restoration is only feasible when wind power is available.

The main goal of this paper is to present a method of precharging a fully-disconnected MMC using only its internal ES. The method is suitable for OWPP applications, where ES originally installed for energy shifting in the offshore collector MMC could start up the network in case wind power is not sufficient. Similarly, interconnectors with integrated ES for ancillary service provision can benefit from the same feature.

The original contributions can be listed as:

- an analysis of parameters (SM topologies, APS type and minimum operation voltage) which affect the blackstart capability of an MMC from its integrated ES (Sec. II),
- an algorithm that first activates the APSs of the converter, and then charges the SM capacitors to nominal energy (Sec. III),
- a proposed procedure to establish ac voltage and supply partial load in an ac passive network (Sec. III-D2).

The analysis and proposed method is validated with simulation results.

II. CONSIDERATIONS FOR ES-ASSISTED START-UP

We will assume a three-phase MMC with integrated ES, as displayed in Fig. 1. Each phase has an upper and a lower arm; each arm consists of N SMs, of which N_{es} are interfaced to ES units. The SM stacks featuring ES are henceforth referred to as ES-stacks, and the capacitive-only stacks as C-stacks.

An interesting approach is investigated in [14]–[16], where the authors study MMCs with unbalanced distributed ES. This arrangement could facilitate standalone converter start-up, however it requires constant energy balancing during normal operation to counteract the asymmetric power contribution from different ES units and also affects the semiconductor ratings owing to the extra current flowing in the arms. In the following, an equal amount of ES per arm is considered.

The overall start-up process is presented with the aid of the flowchart shown in Fig. 5 at the beginning of Sec. III, before the step-to-step method is presented.

A. Submodule Topology

The most widely adopted submodule topologies in existing multilevel installations are the Half-Bridge Sub-Modules (HB-SMs) and Full-Bridge Sub-Modules (FBSMs), used in MMC applications. The main criteria driving the submodule design are the limited conduction losses, low cost, low volume, dc fault blocking capability and ability to overmodulate. While the first three criteria favour unipolar submodules with fewer semiconductor devices, the last two criteria require submodules with negative voltage insertion capability, thus necessitate bipolar submodule topologies.

Converter efficiency is very often driven by the number of devices, in which case the most prevalent MMC topology would consist entirely of HBSMs. However, HBSMs with ES can contribute with energy to the stack only during the part of the period where the ES power polarity is the same as the arm current polarity, since the output voltage of the HBSM
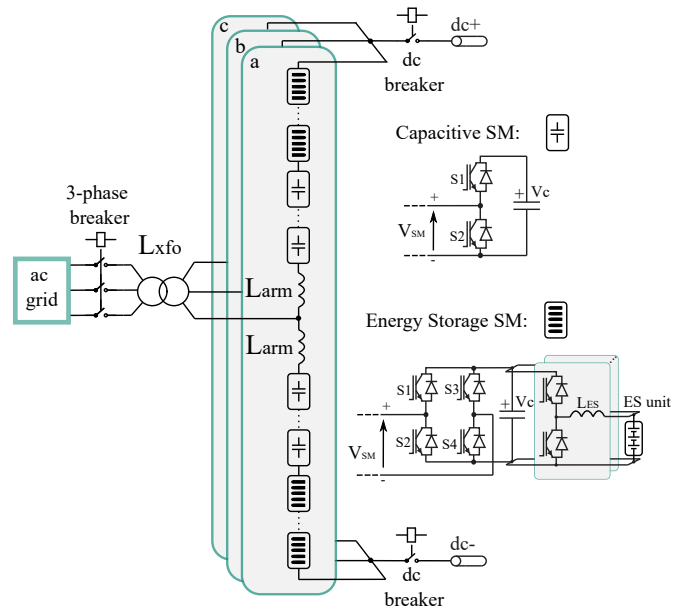

Fig. 1: The hybrid converter topology under study [7], [8].

can only be positive or zero. On the other hand, FBSMs (or other SM with negative insertion capability) can exchange power with the stack during the entire period regardless of the direction of the arm current [8]. This results in a considerably smaller voltage requirement for FBSM-ES than HBSM-ES for the same ES power rating. Therefore, the topology of study in the rest of the paper is a Hybrid HBSM MMC with FBSM-ES, as shown in Fig. 1. Nevertheless, the analysis of this section can be applied for any SM topologies, and modified to express an asymmetric distribution of ES among the arms.

The minimum number of ES-SMs is defined by the ES power rating provision in steady state [8], whereas the maximum number of ES-SMs is limited by the extra device losses incurred in the ES-stacks due to the extra semiconductor devices of the FBSMs, and other techno-economical aspects, such as the round-trip efficiency of the ES units, or the space available in the converter valve hall, among others.

In the following, indices st and sm denote stack and SM quantities respectively, pos and neg denote positive and negative insertion, and bip and blk stand for bipolar and block, respectively.

The *bipolar ratio* introduced in [17] is a useful figure of merit for an SM stack, defined as the ratio of the maximum negative stack voltage over maximum positive stack voltage.

$$r_{\mathrm{bip}} = \frac{\hat{V}_{\mathrm{st,neg}}}{\hat{V}_{\mathrm{st,pos}}} \tag{1}$$

For stacks consisting of a single SM type, r_{bip} simplifies to

$$r_{\mathrm{bip}} = \frac{\hat{V}_{\mathrm{sm,neg}}}{\hat{V}_{\mathrm{sm,pos}}}. \tag{2}$$

For all unipolar SMs such as the HBSM $r_{\mathrm{bip}} = 0$. Similarly, the *block ratio* is defined as the ratio of the stack voltage $V_{\mathrm{st,i<0}}$ when the current flowing is negative, to the stack

voltage $V_{\text{st,i}>0}$ when the current is positive, while the stack is blocked.

$$r_{\text{blk}} = \frac{V_{\text{st,i}<0}}{V_{\text{st,i}>0}} \qquad (3)$$

Again, for blocked stacks of a single SM type

$$r_{\text{blk}} = \frac{V_{\text{sm,i}<0}}{V_{\text{sm,i}>0}} \qquad (4)$$

In the topology of Fig. 1 where the arms are disconnected both from the dc and the ac grids, common mode voltage across the phases would result in no current flowing around the arms. It is therefore the maximum differential voltage the ES-stacks can produce between phases which defines the maximum attainable voltage across the C-stacks. An example is displayed in Fig. 2.
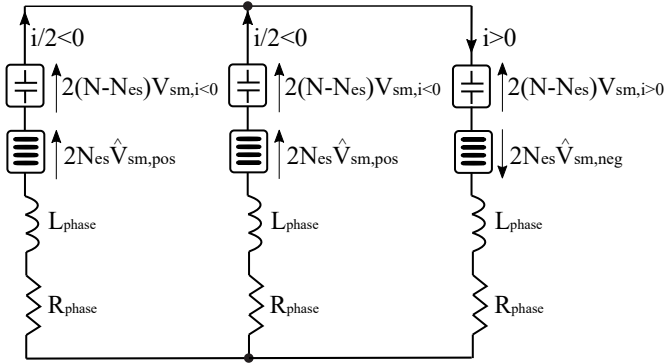

Fig. 2: Voltage distribution among C- and ES-stacks that results in maximum differential voltage drop onto the stacks. Positive and negative current directions are also displayed.

By equating voltages between phases, the relationship between the overall C-stacks and the ES-stack voltages is derived:

$$2N_{\text{es}}(\hat{V}_{\text{sm,pos}} - \hat{V}_{\text{sm,neg}}) = 2(N - N_{\text{es}})(V_{\text{sm,i}>0} - V_{\text{sm,i}<0}) \qquad (5)$$

For equal nominal voltage $V_{\text{sm,nom}}$ in the SM capacitors of both C- and ES-stacks, Eq. 5 can be reorganised to derive the initial attainable voltage of the C-stack:

$$V_{\text{Csm,init}} = k_{\text{ch}}V_{\text{sm,nom}}\frac{N_{\text{es}}}{N - N_{\text{es}}}\frac{1 - r_{\text{es,bip}}}{1 - r_{\text{c,blk}}}, \qquad (6)$$

where the parameter k_{ch} is introduced to account for the capacitor voltage fluctuation around the nominal voltage $V_{\text{sm,nom}}$, with values ranging from 0.9 to 1.1. In most applications, the SM capacitors are rated for $\pm 10\%$ of capacitor voltage fluctuation during normal operation. According to Eq. 6, the initial uncontrolled voltage up to which the C-stacks can be charged is defined by the ratio N_{es}/N and the type of SMs. A comparison for different SM topology combinations is displayed in Fig. 3. It should be noted that the combination of HBSM C- and FBSM ES-stacks maximises r_{bip} whilst minimising r_{blk}, leading to higher maximum voltage compared to other combinations. For $N_{es}/N = 33\%$ or greater, this configuration can even charge the C-stack capacitors to their nominal voltage. The maximum attainable voltage is halved when HBSM or FBSM are used both in C- and ES-stacks,
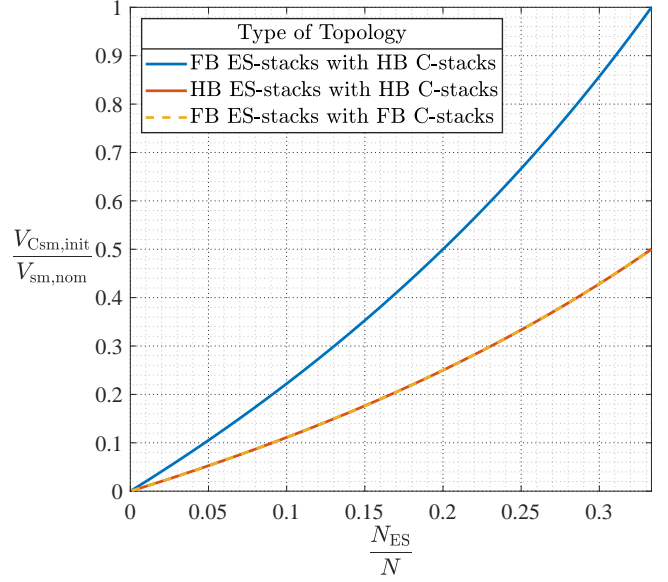

Fig. 3: The maximum attainable initial voltage of the C-stack SMs as a function of the relative number of ES-SMs, for different SM combinations and $k_{\text{ch}}=1$.

because for both topologies $r_{\text{bip}} = r_{\text{blk}}$, so the last term of Eq. 6 equals to 1.

B. Auxiliary Power Supply

The challenge of starting a power converter heavily depends on the type of APS used. In the case of MMC applications, different solutions have been investigated, such as the internal APS, Inductive Power Transfer [18], [19] or Power Over Fiber [20], [21]. In HV MMC applications, where multiple SMs are connected in series requiring high isolation, the APS of a SM is most often powered by the respective SM capacitor and its voltage floats at this voltage level. The isolation transformer has to withstand the voltage of a single capacitor, which is a few kilovolts, instead of the entire stack voltage. Variations of the flyback converter with multiple secondary inductor windings are used to provide isolated power supplies for the gate drivers of the switches, protection circuits and the local controller [22]–[24].

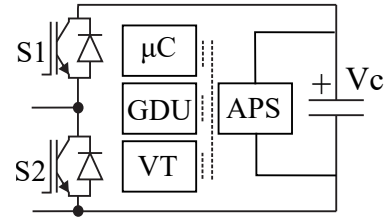Fig. 4: The SM APS powered internally from the SM capacitor. μC: microcontroller, GDU: Gate Driver Unit, VT: Voltage Transducer.

The internal APS requires a minimum capacitor voltage to start operating, therefore it relies on a start-up procedure

that charges passively the capacitors to the required voltage through a pre-insertion resistor from the ac or dc grid without using the switches. When the ES-stacks are intended to be used for blackstart purposes, then the minimum number of ES-SMs required is the value on the x-axis of Fig. 3 that corresponds to the minimum input voltage of the APS used. Fewer ES-SMs than this threshold would not be able to generate enough voltage to activate the APS of each C-stack SM. As an example, the author in [25] mentions a minimum APS input voltage of approximately 12%, which is attained with an installed ratio N_{es}/N of 5.7% according to Fig. 3.

C. Energy Storage System

The main electrochemical technologies available for grid-scale ES integration are mainly ultracapacitors and battery stacks [26]. The depth of discharge and the harmonic content of the ES current can severely affect the lifespan of the ES unit, and reduce the number of cycles an ES unit can run before losing capacity [27], [28]. The dc/dc interface plays a major role in shielding the ES unit against these aging factors, for example by connecting the ES unit and the SM capacitor [29] through an inductor, or using a bidirectional dc chopper [30].

For primary frequency control, where the ES units are required to cycle power quickly and frequently, ultracapacitors are preferable. When bulk energy buffering is required over longer periods of time, battery ES systems (BESSs) feature higher energy-to-mass and energy to-volume ratio [31], allowing for smaller footprint in the substation. Typically, grid-scale ES utilities can supply their rated power at least for a fraction of the hour [3], [32], whereas ultracapacitors usually can supply their rated energy for a few minutes.

The optimal ratio between rated power and stored capacitive energy for a conventional HB MMC is in the range of 35-40kJ/MVA [33], or 35-40ms supply of full rated power, which would cause a negligible depth of discharge for the ES units in the examined application.

The maximum current rating of each ES unit parallel to an SM for an ES system of power rating $P_{es} = p_{es}P_{conv}$ over a number of SMs $N_{es} = n_{es}N$ per arm with the SM voltage being $k_{ch}V_{sm,nom}$ is:

$$\hat{I}_{es} = \frac{P_{es}}{6N_{es}k_{ch,min}V_{sm,nom}} = \frac{p_{es}}{6n_{es}k_{ch,min}}I_{dc}. \qquad (7)$$

III. START-UP PROCESS FOR MMCs WITH ES

The ES-assisted start-up procedure is presented in the form of the flowchart of Fig. 5. These steps of the procedure are executed in the state machine of the converter controller.

For the method to work, it is required that:
1) the ES units are self-powered and they can unblock their dc/dc interface converter,
2) the ES units can charge and discharge the respective capacitors to a controlled value through their dc/dc converters,
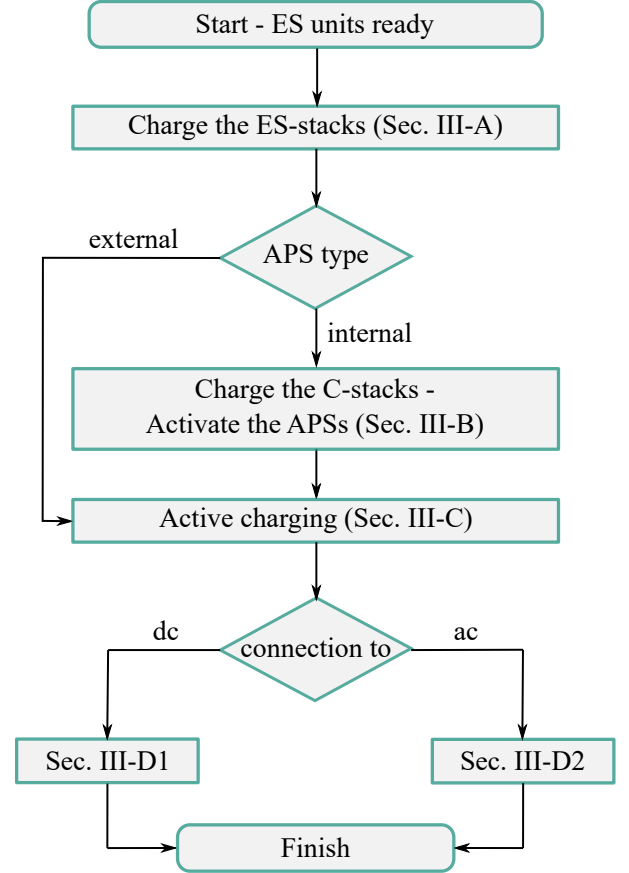3) arm current and SM voltage measurements are available for control purposes.

Fig. 5: Flowchart detailing the process.

The first step of the blackstart process in a fully disconnected MMC is to charge the ES-stacks (Sec. III-A) – once charged, they act as the controllable voltage source that circulates current around the C-stacks. The next stage depends on the type of APSs of the C-stacks. In the most likely case, the SMs feature an internal APS similar to Fig. 4, and current has to be circulated around phases to charge each SM capacitor at least up to the voltage that activates the APS (Sec. III-B). If the APS of the SMs is powered externally, the auxiliary electronics are already activated so the state machine can proceed directly to active charging (Sec. III-C).

Simulations are presented in this section to validate the effectiveness of the method. They are based on a vectorised simulation model implemented in MATLAB/Simulink which realises ES-assisted charging of the converter to the nominal energy, from zero initial energy stored in the converter. The specifications of the test converter are presented in Table I.

A. Start-up of the ES-stacks

Initially, the ES-stack capacitors are charged from their respective ES units, which are modelled as a controllable current source in parallel to the capacitor. The controller is fast enough to contain each capacitor voltage close to the voltage reference $V_{sm} = k_{ch}V_{sm,nom}$, hence the ES-stacks are considered as voltage sources.

TABLE I: Simulation model parameters

DC Voltage V_{dc}	$\pm$ 320 kV
AC Voltage (PCC) $V_{\text{LL}_{\text{rms}}}$	66 kV
Rated power P_{rated}	960 MW
Arm inductor L_{arm}	0.1 pu
Transformer leakage L_{xfo}	0.14 pu
Nominal submodule voltage $V_{\text{sm,nom}}$	3.3 kV
C-stack and ES-stack SM capacitance C_{sm}	5.3 mF
Equivalent capacitive energy E	35 kJ/MVA
Total number of SMs per arm N	194
Number of SMs in the ES-stacks N_{es}	8 (4%)
Number of SMs in the C-stacks $N_{\text{hb}} = N - N_{\text{es}}$	186
Peak arm current $\hat{I}_{\text{arm}}$	1676 A
Maximum ES unit current $\hat{I}_{\text{es}}$	673 A
Overcharging factor k_{ch}	1.08
Controller frequency f_{c}	10 kHz
Simulation timestep T_s	2 μs
AC load Z_L	$20 Z_{base}/\sqrt{2} < 45°$

Fig. 7: Start-up of the ES-stacks and semi-passive charging of the C-stacks. The grey lines in the top figure denote the available voltage of the ES-stacks. The legend of the middle figure also applies to the top figure.
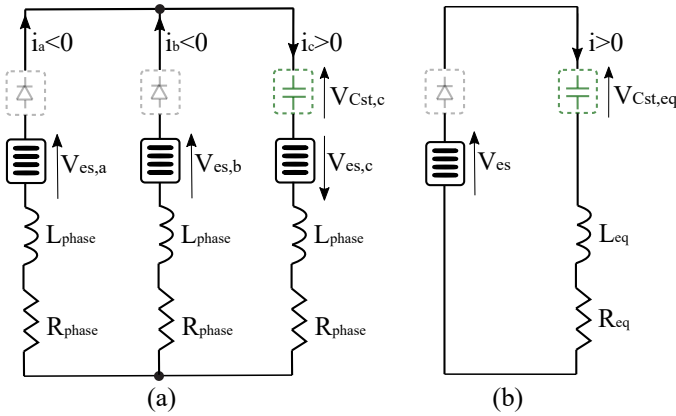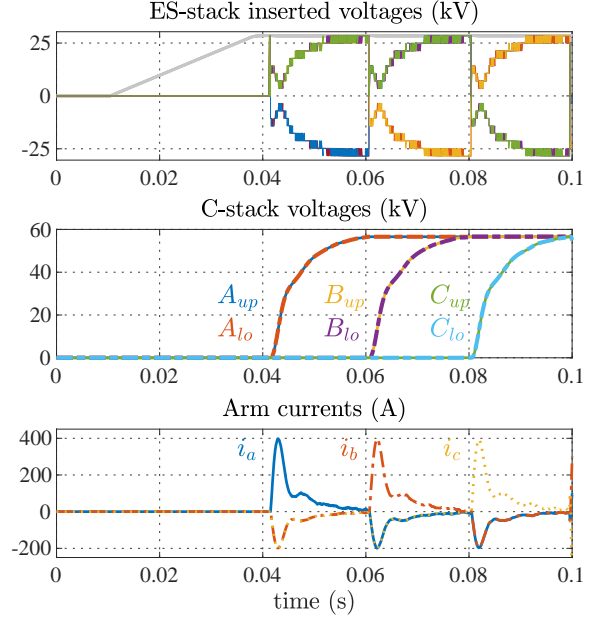

Fig. 6: (a) Simplified example of converter of Fig. 1 where phases A and B are charging phase C. (b) Equivalent circuit. Dashed: uncontrollable stacks, green: charging, grey: bypassed.

B. Semi-passive charging of the C-stacks

ES-stacks can charge the C-stacks up to the maximum voltage derived in Eq. 6 by creating a controlled differential voltage between phases. For the example pictured in Fig. 6a in which phase C is charged by A and B, the equivalent C-stack capacitance is:

$$C_{\text{Cst,eq}} = C_{\text{Cst,a}} || C_{\text{Cst,b}} + C_{\text{Cst,c}} \quad (8)$$

In the case where the C-stacks consist of HBSMs, for $i < 0$ the A and B C-stacks are bypassed, so the total equivalent capacitance is

$$C_{\text{Cst,eq}} = C_{\text{Cst,c}} = \frac{C_{\text{sm}}}{2(N - N_{\text{es}})}. \quad (9)$$

The total equivalent inductance shown in Fig. 6b is

$$L_{\text{eq}} = L_{\text{a}} || L_{\text{b}} + L_{\text{c}} = 3L_{\text{arm}} \quad (10)$$

The resistive component of the arms consists mainly of the parasitic inductor resistance, the equivalent series resistance of

the submodule capacitors and the losses of the semiconductor switches. In the following, the total equivalent resistance of an arm is denoted with R_{arm}. The total equivalent resistance shown in Fig. 6b is

$$R_{\text{eq}} = R_{\text{a}} || R_{\text{b}} + R_{\text{c}} = 3R_{\text{arm}} \quad (11)$$

The expression defining the ES-stack voltage per phase is

$$V_{\text{es,x}}(t) = 2N_{\text{es,x}}(t) k_{\text{ch}} V_{\text{sm,nom}} \quad (12)$$

where $x = a, b, c$, and $N_{\text{es,x}}(t)$ is the number of inserted ES submodules per phase as a function of time. The ES units of each submodule inject or absorb current. This action ensures that the available voltage of the ES stacks is regulated to a fixed voltage by the ES unit and can be treated as a voltage source. The differential voltage produced in the MMC by the ES-stacks is equal to

$$V_{\text{es}}(t) = V_{\text{es,a}}(t) || V_{\text{es,b}}(t) - V_{\text{es,c}}(t) \quad (13)$$

where $V_{\text{es}}(t)$ corresponds to the equivalent voltage source of Fig. 6b. The maximum equivalent voltage is:

$$V_{\text{es,max}} = V_{\text{es,max,a}} || V_{\text{es,max,b}} - V_{\text{es,min,c}} = 4N_{\text{es}} k_{\text{ch}} V_{\text{sm,nom}} \quad (14)$$

The RLC circuit of Fig. 6b is formed, the transfer function of which is

$$\frac{I}{V_{\text{es,eq}}} = \frac{1}{L_{\text{eq}}} \frac{s}{s^2 + \frac{R_{\text{eq}}}{L_{\text{eq}}} s + \frac{1}{L_{\text{eq}} C_{\text{Cst,eq}}}}. \quad (15)$$

A cascaded loop control scheme is adopted. The outer loop acts on the C-stacks voltage $V_{\text{Cst,eq}}$ and creates a current reference for the inner loop, which produces an output for

the ES-stacks $V_{es,eq}$. $V_{es,eq}$ is split into positive and negative insertion values which are then assigned to the right phases. The cascaded control scheme has the advantage of driving the current reference to zero when the C-stacks are charged to their maximum. Since the number of SMs in the ES-stacks is small, a Phase Shifted Pulse Width Modulation (PS-PWM) scheme is considered the best modulation choice.

Indicative results of the first steps of the charging process are shown in Fig. 7. The process starts at t = 0.001 s, where the ES-stacks draw constant maximum current from their respective ES units until they reach their reference voltage $k_{ch}N_{es}V_{sm,nom}$ = 28.5 kV. Then phases A, B, C start charging at t = 0.04, 0.06, 0.08 s respectively, with a controllable current that does not exceed the rated arm current:

$$I_{arm} = \frac{\hat{I}_{ac}}{2} + \frac{I_{dc}}{3} \quad (16)$$

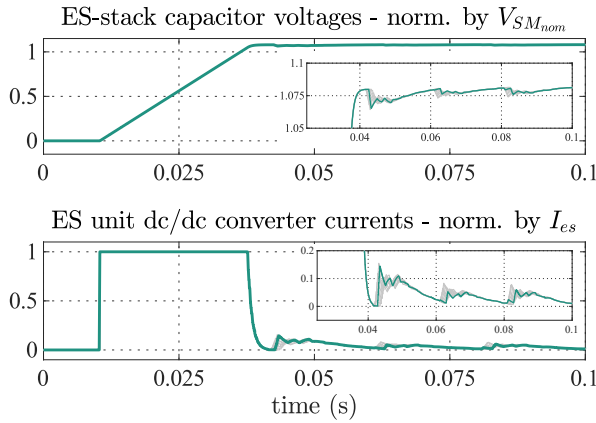At the same time, the current contributed by ES should not

Fig. 8: The capacitor voltages and dc/dc currents of the ES-stacks in the upper A arm, with values of submodule 5 highlighted. The voltages are normalised by $V_{sm,nom}$, and the currents by I_{es} derived in Eq. 7.

exceed the rated ES current given by Eq. 7. The final voltage of a C-stack at this stage agrees to the ratio provided by Eq. 6 for the converter parameters of Table I.

$$V_{Cst} = (N - N_{es})V_{c,init} = 2N_{es}k_{ch}V_{sm,nom} \quad (17)$$

In this example, the maximum C-stack voltage corresponds to 57kV, which is twice as high as the ES-stack voltage V_{es}, due to the symmetrical bipolar capability of the FBSMs. At t=0.1s, the active charging begins, described in the following section.

In Fig. 8, the ES-stack capacitor voltages and currents from the ES units are displayed. The control action of the ES units keeps the voltage deviation within $\pm 1\%$ of the reference, with the aid of a PI controller comparing the capacitor voltage to the nominal.

C. Active charging of the C-stacks

At the beginning of this stage the C-stacks are charged enough to have their APS activated, and the semiconductor devices in all submodules are controllable, as highlighted in Fig. 9. The MMC remains disconnected.
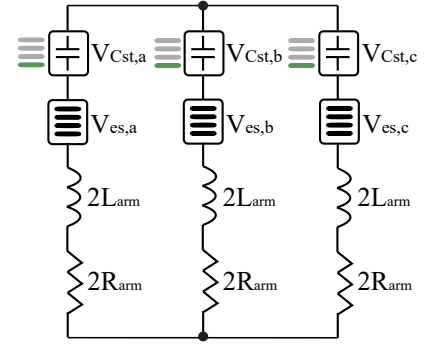
Fig. 9: Simplified representation of the converter after the first stage has been completed.

Charging simultaneously all the C-stacks requires harmonic current and voltage of the same frequency to exchange power from the ES-stacks to the C-stacks in an arm. In the absence of voltage at the ac terminals, the frequency and the phase angle of the current are arbitrary, therefore a fundamental harmonic controller is implemented. Fig. 10 displays the control functions required for active charging.
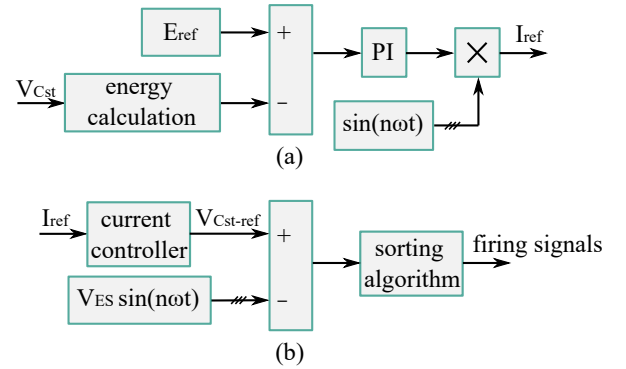
Fig. 10: The control scheme required during active charging stage with n=1.

The error of the C-stack energy passes through a proportional-integral controller; the circulating current reference is generated by multiplying the output of the controller with an arbitrary, balanced, three-phase sinusoidal signal. A closed-loop current controller generates the voltage references needed to drive the current around the phases. At the same time, the ES-stacks are set to track a fixed sinusoidal reference of same frequency and phase angle as the current. This reference is subtracted from the C-stacks, so that energy is transferred from the ES-stacks to the C-stacks. A sorting algorithm rotates the C-stack SMs to gradually increase their voltage to the nominal. When the C-stack energy reaches the nominal, the current settles to zero, and the insertion indexes reach 0.5. The results from this stage are shown in Fig. 11 and 12.

D. Connection to the grid

1) Connection to the dc network: Connecting to a dc grid requires the dc bus voltage and current measurements, so
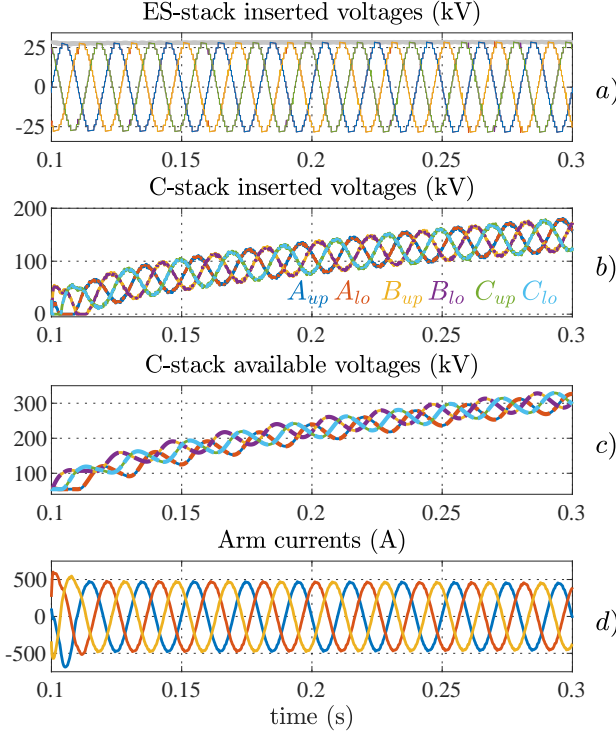
Fig. 11: A close-up on the ES-stack and C-stack voltages and arm currents during the active charging of the C-stacks.
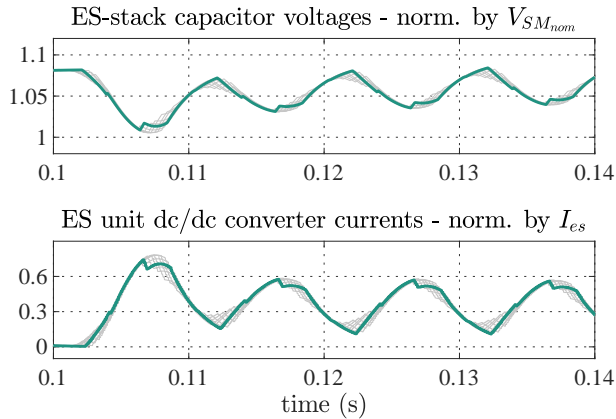

Fig. 12: The capacitor voltages and dc/dc currents of the ES-stacks in the upper A arm, with submodule 5 highlighted. The values are normalised as in Fig. 8.

that the right amount of SMs can be inserted per phase and minimise the inrush current. This work is out of the scope of this paper.

2) Connection to the ac network: In a typical application of an MMC on an offshore platform, the MMC is connected to the wind turbine clusters via a transformer and submarine cables. Assuming that the transformer has no residual flux in the core, the converter can soft-start the ac grid by ramping up the ac voltage in order to eliminate inrush current in the transformer. Assuming a passive R-L grid, grid forming
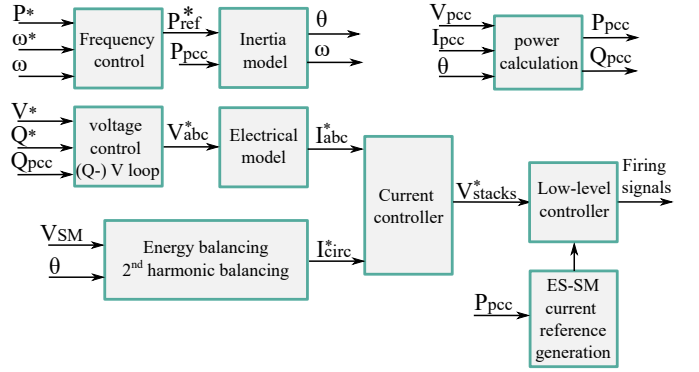

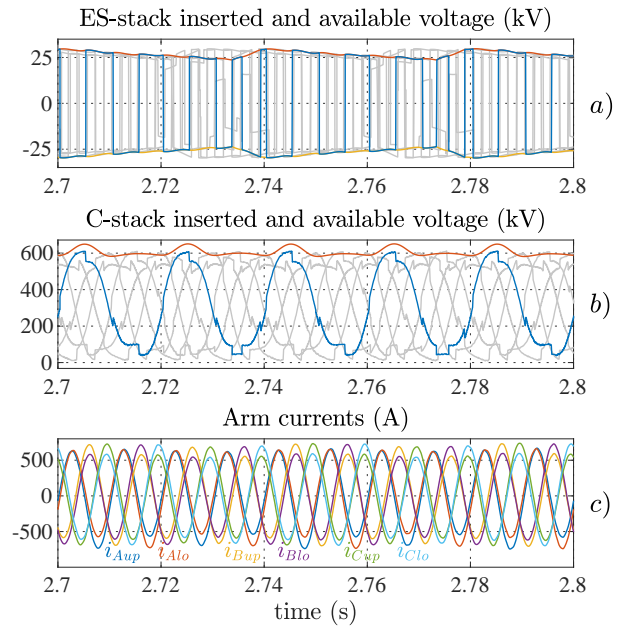Fig. 13: Top-level overview of the modified grid forming control scheme.

Fig. 14: Available and inserted voltages for upper phase A stack, during ramping-up of the voltage.

control such as the one detailed in [34], [35] is adopted, with the modification that the converter is not connected on the dc side, therefore the energy balance has to be maintained by circulating currents replenishing the C-stack energy from ES-stacks, as shown in Fig. 14. In order to maximise the power output from the ES-stacks to the ac grid, they are inserted in an opposite manner compared to the ac component of the respective C-stack, similar to the controller proposed in [8], also shown in Fig. 14a and b. Circulating currents have to flow around the converter so that the C-stack energy is replenished by the ES-stacks. The energy deviation of the stacks is transformed into a triplet of circulating currents -in this case second harmonic-, which results in a small harmonic component in the stack voltages, shown in Fig. 14. In this case, 4% of the submodules is used to charge the other 96% of the stack, so the circulating current is inevitably high, as shown in Fig.14, where the common mode current in a phase is much
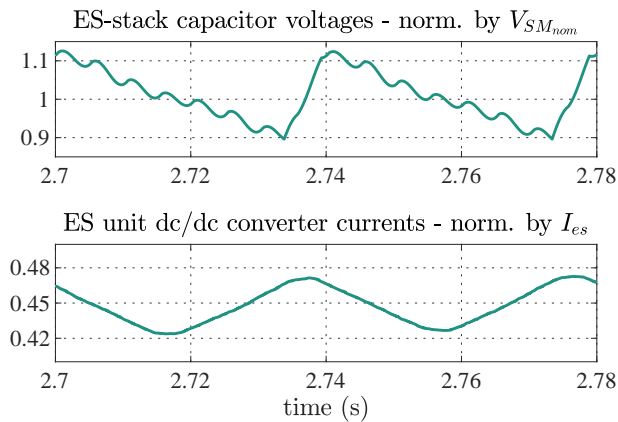
Fig. 15: Available voltage and current of submodule 5 of the upper A stack during ramping-up of the AC voltage.
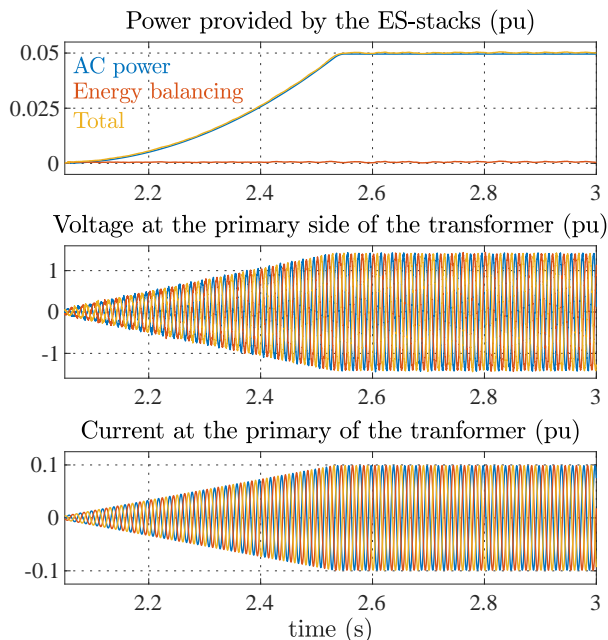

Fig. 16: AC power, voltage and current at the point of common coupling.

higher than the differential part (output ac current). However, for a scenario of passive ac grid energisation of small loads, the current limitation is not reached. The energy balance of the ES-stacks is regulated in the same manner as presented in [8], by introducing a hysteresis band of $\pm 10\%$ around the nominal SM voltage, and charge/discharge the ES-SMs according to whether they hit the upper or lower bound, as demonstrated in Fig. 15. This approach indirectly controls the energy in the ES-stack. Fig. 16 illustrates the voltage established at the point of common coupling by the output current of the converter.

IV. CONCLUSION

This paper demonstrates that partially-rated ES embedded in an HVDC MMC can be utilised for blackstart provision even without connection to the ac or dc grid. Design parameters such as the converter topology, the amount and topology of ES-SMs, the type of APS (external or internal) and its minimum operating voltage define whether ES-assisted start-up is feasible in a certain converter design.

The demonstrated start-up method can be analysed in four stages: a) charge the ES-stacks from the ES units in parallel to them, b) control the ES-stacks to circulate current around the MMC arms and activate the APS of the C-stacks while they are still blocked, c) unblock the C-stacks and controllably bring their voltage to nominal, d) connect to the ac or dc grid and establish nominal voltage. In the current analysis, simulation results showcased the re-energisation of a passive AC network. Approximately 4% of FBSMs integrated in each arm charged initially the C-stack capacitors up to 8% of the nominal voltage and then actively fully charged all the submodules. After connection to the ac, the voltage was controllably ramped-up and grid forming control was implemented to establish supply voltage for an ac load.

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Zoe Blatsi (Student Member, IEEE) received the diploma in Electrical and Computer Engineering from Aristotle University of Thessaloniki in 2015, specialising in power systems. From 2016 to 2018, she worked with the Electrical Power Converters Group at CERN, on control implementation for FACTS and power quality studies. Since 2019 she has been working toward the Ph.D. degree at the University of Edinburgh, on energy storage integration in multilevel converters. Her research interests include power converter design and control for grid applications such as integration of renewable generation and energy storage.

Paul D. Judge (Member, IEEE) received the B.Eng. (Hons.) degree in electrical engineering from University College Dublin in 2012 and the Ph.D. degree from the Department of Electrical and Electronic Engineering, Imperial College London, in 2016, for which he received the Eryl Cadwaladr Davies prize for best doctoral thesis. He also received a Best Paper Award for his submission to the IEEE Transactions on Power Delivery special issue on "Frontiers of DC Technology" in 2018. Since May 2020, he has been a Lecturer in Power Electronics and Smart Grids at the University of Edinburgh. Since January 2022 he is also a Royal Society Industry Fellow. His research interests include power converter design and control, as well as power system integration aspects of renewable energy technology.

Stephen J. Finney is Chair of Power Electronics at the University of Edinburgh, covering the fields of power semiconductor device applications, converter topologies and the application of power semiconductors to energy systems. He obtained his MEng degree in Electrical and Electronic Engineering from Loughborough University of Technology in 1988 and subsequently worked at the Electricity Council R&D centre at Capenhurst, Cheshire. In 1990 he embarked on an academic career, joining the power electronics research group at Heriot-Watt University where he received his PhD in 1994 and remained as a member of academic staff until 2005. In 2005 he moved to the University of Strathclyde where developed research into utility scale power electronics, taking over as head of Power Electronics research in 2010. During his academic career, Professor Finney's group has led teams pursuing research into the application of power electronics to energy system addressing issues such as electrification of transport, HVDC transmission, DC power networks, renewable generator interface and energy collection architectures.
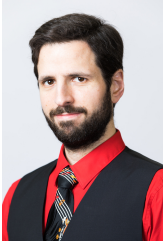
Michael M.C. Merlin (Member, IEEE) received his Electrical Engineering degree from the Ecole National Superieur de l'Electronique et de ses Applications, France, in 2008, as well as an MSc degree in control systems and Ph.D. degree in electrical engineering from Imperial College London, UK, in 2008 and 2013 respectively. In 2017, he became a Lecturer at the University of Edinburgh, UK. His research interests include the design, optimization, and control of power converters, more specifically of the modular types, for transmission and distribution networks, and renewable energy applications.