Available online at www.ijournalse.org

Emerging Science Journal

(ISSN: 2610-9182)

Vol. 6, No. 1, February, 2022

Review Article

A Review on Multilevel Inverter Topologies

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Abstract

In this paper, a brief review of the multilevel inverter (MLI) topologies is presented. The two-level Voltage Source Inverter (VSI) requires a suitable filter to produce sinusoidal output waveforms. The high-frequency switching and the PWM method are used to create output waveforms with the least amount of ripples. Due to the switching losses, the traditional two-level inverter has some restrictions when running at high frequencies. For addressing this problem, multilevel inverters (MLI) with lower switching frequencies and reduced total harmonic distortion (THD) are employed, eliminating the requirement for filters and bulky transformers. Furthermore, improved performance at the high switching frequency, higher power quality (near to pure sinusoidal), and fewer switching losses are just a few of the benefits of MLI inverters. However, each switch has to have its own gate driver for implementing MLI, which adds to the system's complexity. Therefore, reducing the number of switches of MLI is necessary. This paper presents a review of some of the different current topologies using a lower number of switches.

Keywords:

Traditional Two-Level Inverters;
Multilevel Inverter (MLI);
High Power Application.

Article History:

Received:	04	September	2021
Revised:	09	November	2021
Accepted:	23	December	2021
Published:	01	February	2022

1- Introduction

Inverters are used in applications, including air conditioning, uninterruptible power supply (UPS), high-voltage dc power (HVDC) transmission lines, electric cars, battery storage, and solar panels [1, 2]. Inverters are categorized as square-wave inverters, sinusoidal two-level pulse width modulation (PWM) inverters, and multilevel inverters [3, 4]. Power electronics, DC-DC converters, and inverters have seen a surge in the study due to the scarcity of fossil fuels and the diversity of renewable energy sources. The converters must be very dependable, efficient, and offer excellent performance due to the high prices of renewable energy supplies [5]. It must generate sinusoidal output waveforms that are synced with the national power grid [6]. Figure 1 shows the circuit diagram of a two-level inverter.

When SW1 is ON, then $V_0 = +(V_{dc}/2)$, and when SW2 is ON, $V_0 = -(V_{dc}/2)$ [7, 8]. No need to mention that the conventional two-level inverters without pulse width modulation (PWM) produce a square wave output voltage of two levels, as depicted in Figure 2.

This traditional inverter runs at a high switching frequency for high-power applications, with significant switching losses [9]. Harmonic distortion and excessive stress on power semiconductors are other issues. Because of these issues, connecting power electronic switches to the high-voltage grid is not feasible [10, 11]. These issues necessitate the use

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DOI: http://dx.doi.org/10.28991/ESJ-2022-06-01-014

of MLI inverters with different topologies. Improved performance at the high switching frequency, reduced harmonic distortion, higher power quality (near to pure sinusoidal), and fewer switching losses are just a few of the benefits of MLI inverters [3, 12]. However, each switch has to have its own gate driver for implementing MLI, which adds to the system's complexity. Therefore, reducing the number of switches of MLI is necessary [3, 13, 14]. This paper presents a review of some of the different current topologies using a lower number of switches.

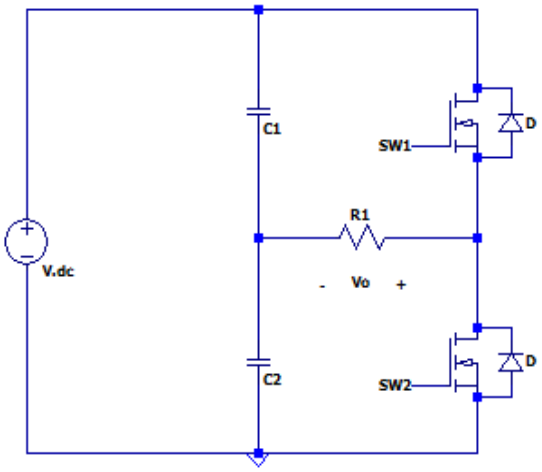

Figure 1. Diagram of a two level inverter

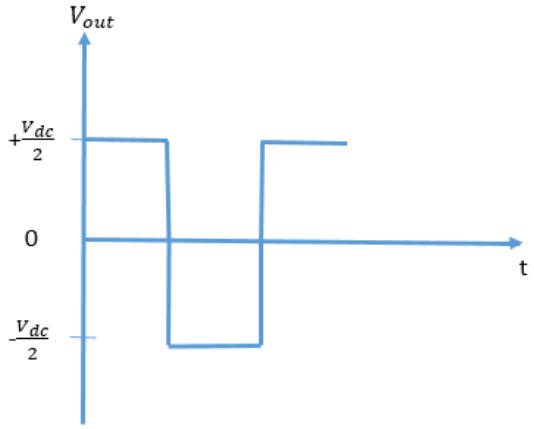

Figure 2. The output voltage of a two-level inverter

2- Three Types of Classical MLI

From various dc input sources, a multilevel inverter creates a smooth sinusoidal waveform. In addition, multi-level inverters play an important role in high-power industrial applications [15, 16]. Diode-clamped, flying capacitor (capacitor-clamped), and Cascaded H bridge multilevel inverters are the most common topologies [17]. The scheme of multilayer inverters is shown in Figure 3.

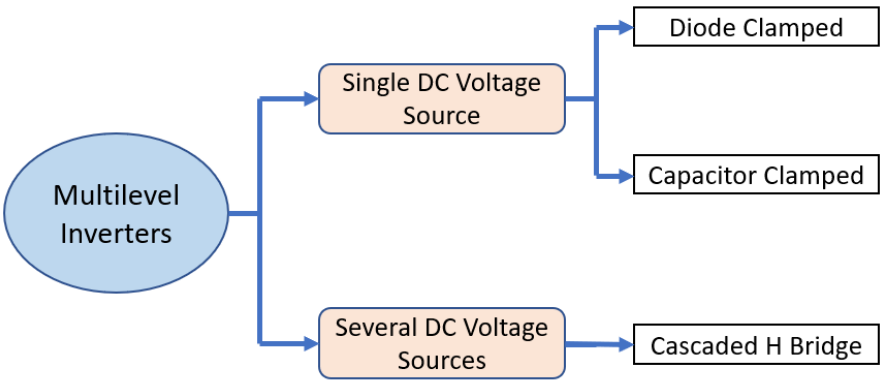

Figure 3. Multilevel inverter scheme

2-1-Diode Clamped Topology

By using diodes, a diode-clamped Multilevel inverter (n level) creates n voltage levels at the output and generally has (n-1) capacitors on the dc-link bus [18, 19]. Figure 4 shows a three-level half-bridge diode clamped multilevel inverter [20]. An n-level inverter requires (n-1) balancing capacitors, 2(n-1) switches and (n-1)(n-2) clamping diodes. Therefore, as shown from Figure 4, the three-level classical diode clamped inverter creates three levels of voltage at the output and has two capacitors at the DC bus and four switches, and two clamping diodes [21, 22].

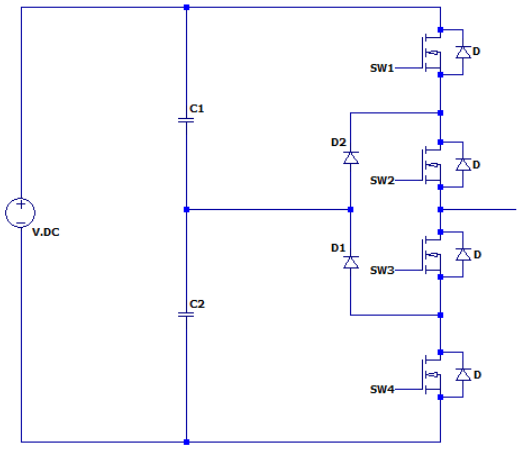

Figure 4. Three-level diode clamped MLI

According to Figure 5, three-level inverters provide a square wave output voltage of three levels without employing PWM.

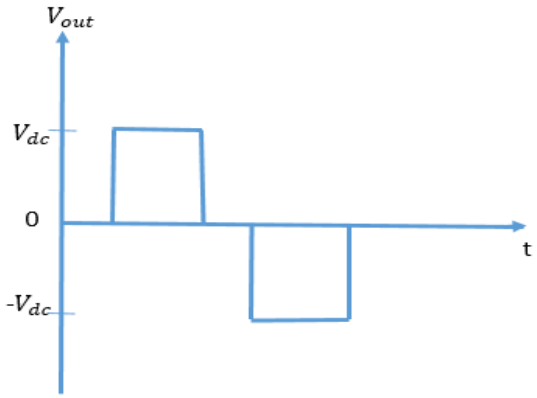

Figure 5. The output waveform of three-level diode clamped MLI

The benefits and drawbacks of diode clamped MLI are as follow [23-25]:

Benefits:

- The real and reactive power flow can be controlled.
- Filters are not required to decrease harmonics.
- The voltage of the switch is just half of the voltage of the dc-link.
- The efficiency is high at the fundamental frequency

Drawbacks:

- Clamping diodes are increased when each level is raised.
- Individual converter real power flow management is challenging

2-2-Capacitor Clamped Topology

It is different from the diode-clamped MLI topology because the capacitors are employed to restrict the voltage in this case [26, 27]. The voltage level of a capacitor's clamped inverter is the same as the diode clamped inverter [28, 29].

For an n-level inverter, the dc bus requires (n-1) capacitors, $\frac{(n-1)(n-2)}{2}$ number of flying capacitors, and the total number of (n-1) switches is required. For instance, based on Figure 6, a five-level flying capacitor MLI creates five voltage levels at the output and has four capacitors at the DC bus and also has eight switches and six clamping capacitors [30, 31].

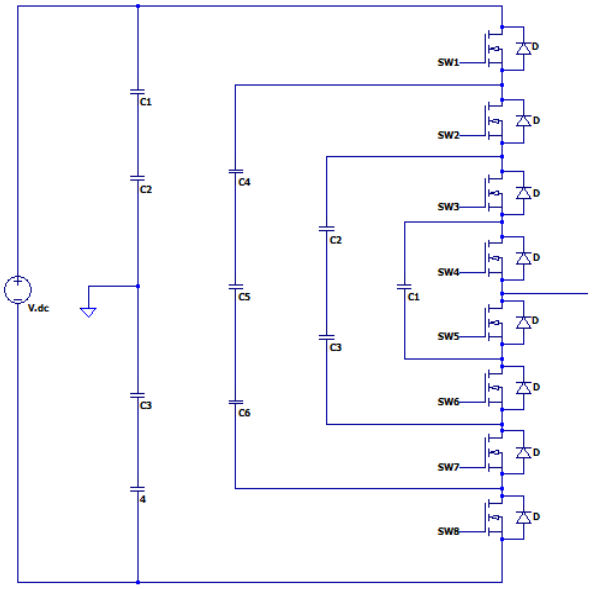

Figure 6. Five-level flying capacitor MLI

Also, according to Figure 7, the five-level inverters provide a square wave output voltage of five levels without employing PWM.

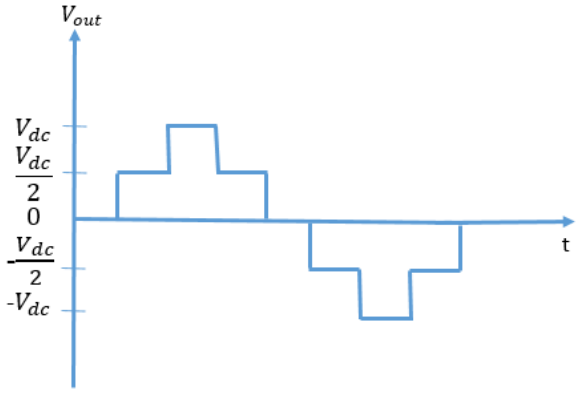

Figure 7. The output waveform of five-level flying capacitor MLI

The benefits and drawbacks of flying capacitor MLI are as follow [32-34]:

Benefits:

- Get rid of the clamping diode problems.
- Filters are not required to decrease harmonics.
- Reduces the amount of stress on the semiconductor switches.
- It provides the correct switching combination for balancing various voltage levels.
- It is possible to control both real and reactive power flow.

Drawbacks:

- Controlling the voltage across all of the capacitors is hard to achieve.
- A decrease in switching efficiency
- Higher cost because of using more capacitors

2-3-Cascaded H Bridge Topology

A cascaded MLI consists of succession of H-bridge inverters with independent DC sources [35-37]. In this inverter, the output voltage has a 2s+1 voltage level, and S is the number of DC inputs. Each cell provides three voltage levels, and the cascaded MLI is made up of connected H-bridge cells in series [38-40]. Therefore, the output voltage levels are equal to the total voltages generated by each H Bridge cell [35, 41]. Figure 8 indicates a seven-level cascaded MLI, which has three separate dc sources.

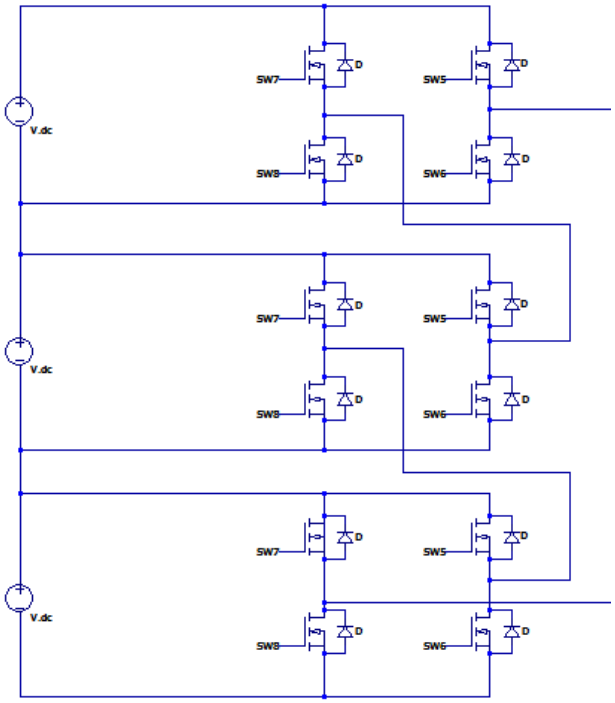

Figure 8. Seven-level H-bridge MLI

Based on Figure 9, the seven-level cascaded inverters provide a square wave output voltage of seven levels without employing PWM.

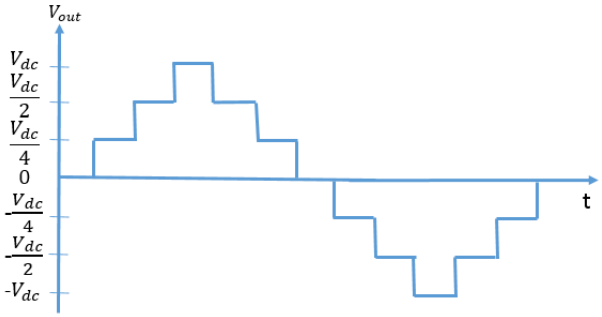

Figure 9. The output waveform of seven-level cascaded MLI

The benefits and drawbacks of cascaded H bridge MLI are as follow [42-44]:

Benefits:

- To decrease switching losses, a soft switching approach can be employed.
- Filters are not required to decrease harmonics.
- THD (total harmonic distortion) is extremely low.
- A lower number of components is used in this MLI.

Drawbacks:

- For power conversions, it requires independent dc sources

3- Review of New Different MLI Topologies

In [45], a new three phases transformer-less inverter design was suggested, which is shown in Figure 10. This suggested MLI has six switches and combines the benefits of dc-bypass and ac-bypass circuit designs.

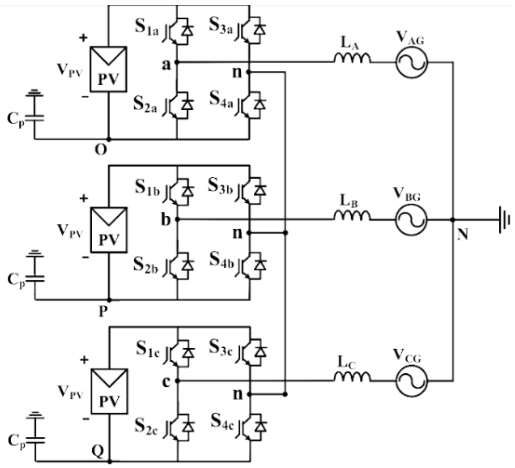

Figure 10. Proposed novel three-phase transformerless MLI [45]

For the suggested configuration, a new modulation approach based on a sine triangle pulse width modulation technique and specialized logic functions is created. As a consequence, there is less leakage current throughout the inverter's operation and the proposed topology and its modulation method can be utilized to generate more electricity. In [46], a novel MLI topology using fewer components was suggested, as shown in Figure 11. It can also be linked in a cascade to increase the number of levels of voltages at the end.

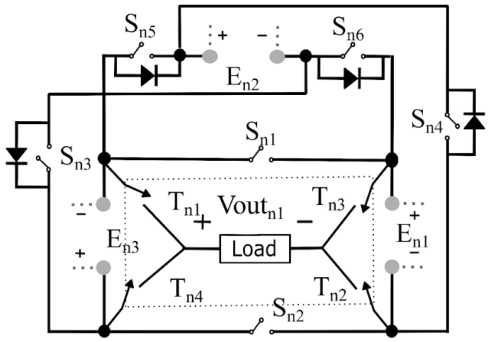

Figure 11. Proposed 15-level MLI [46]

The suggested inverter has the smallest DC-link source and minimal THD at the output voltage and current. In [47], a new MLI was proposed, which consists of series of proposed basic cells shown in Figure 12. Two dc voltage sources, six switches, and an H-bridge make up each basic cell or module

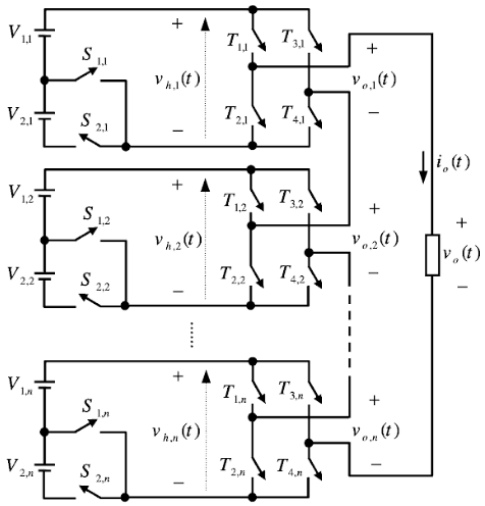

Figure 12. Proposed 9-level cascaded MLI with reducing DC voltage sources [47]

Compared to the standard symmetric multilevel inverter, the suggested topology in Figure 12 uses fewer switches in symmetric conditions. Furthermore, under asymmetric conditions, the magnitude diversity of dc voltage sources is smaller than in conventional conditions. In Grigoletto (2021) [48] study, a novel transformerless multilevel common-ground inverter was introduced, as shown in Figure 13. One dc source, seven switches, and three capacitors make up the suggested structure.

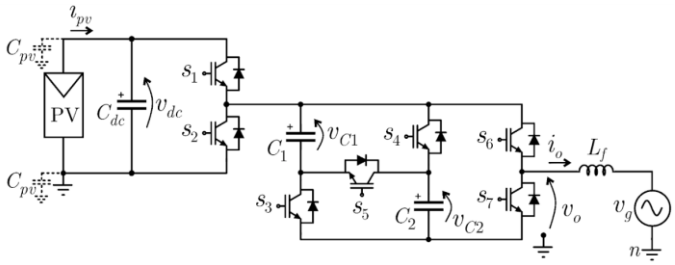

Figure 13. Proposed multilevel common-ground topology [48]

Furthermore, this topology eliminates leakage current. A feedforward modulation method is also presented to isolate the output variables from the voltage–capacitor oscillations. In [49], an improved topology of cascaded MLI was investigated. Each module in this topology consists of a Half-bridge, an H-bridge, two DC inputs, and an extra bi-directional circuit

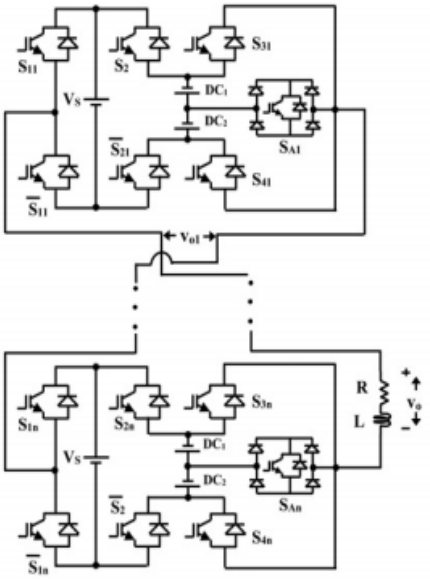

Figure 14. Proposed cascaded MLI topology with fewer circuit components [49]

Also, with fewer power circuit components, each module in the proposed MLI can synthesize a maximum of the 9-level output voltage waveform. Although the suggested topology may be switched at the fundamental frequency, it is impossible to achieve equitable power-sharing across modules. In [50], the article describes a dual-T-type five-level cascaded MLI topology shown in Figure 15. The Cascaded MLI has a high charging current and operates in a non-uniform manner. The proposed configuration solves these issues while maintaining the desired voltage-boosting characteristic.

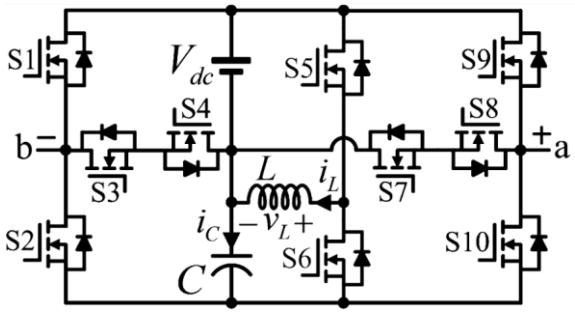

Figure 15. Proposed Dual T-type five-level cascaded MLI [50]

The capacitor boosts the voltage gain, while the dual structure's management of eight power switches allows for the creation of five voltages. In addition, cascaded extensions operate in a consistent manner. In Samsami et al. (2017) [51] study, a new topology was suggested. Figure 16 depicts a topology with three DC inputs and eight switches.

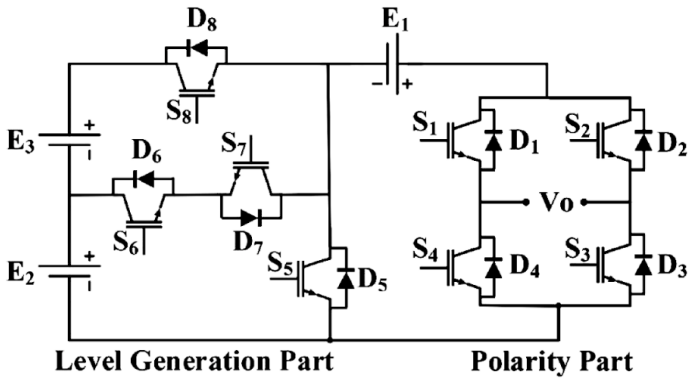

Figure 16. The proposed staircase cascaded MLI [51]

This suggested framework may be in cascade and modularly extended. According to Figure 16, switches of (S1, S2, S3, and S4) should have various voltage ratings and have a lowest blocking voltage capacity corresponding. Also, the suggested MLI reduces the number of switches. In [52], a single-source MLI based on the innovative K-type unit (KTU) was introduced. Due to their symmetric functioning in a cycle, may achieve self voltage balancing, decreasing control complexity compared to traditional MLIs.

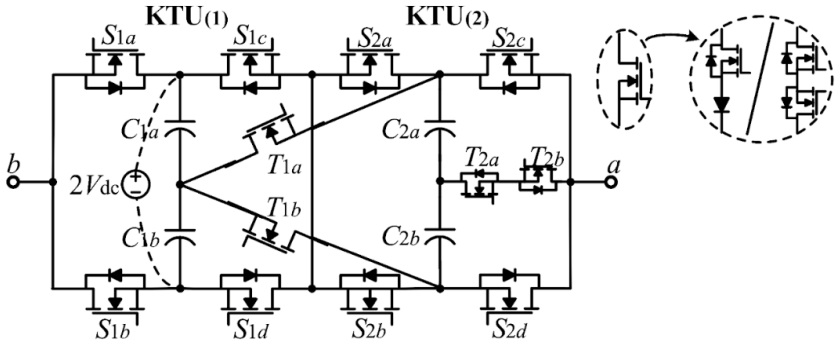

Figure 17. Proposed single-source MLI k-type unit [52]

Furthermore, with more KTUs, the output levels climb substantially, and the voltage gain will increase. Also, the benefits of the suggested KTU circuit are demonstrated in terms of decreased components, voltage stress, and total cost. In [53], a different setup MLI has been proposed and has been shown in Figure 18. The suggested topology comprises eight switches, two separate DC voltage sources, and two series capacitors as its fundamental structure.

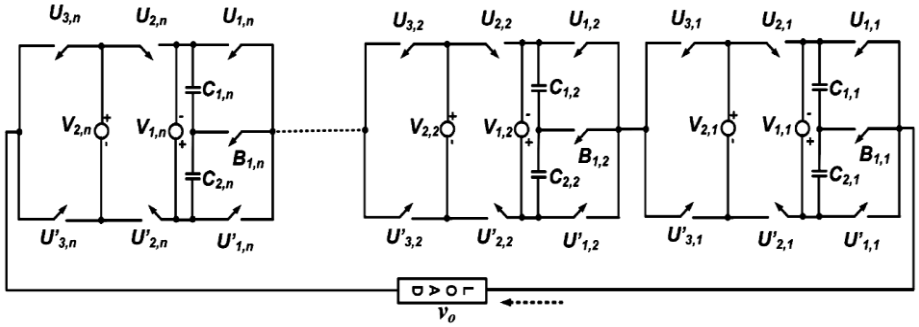

Figure 18. The proposed cross-connected source-based MLI [53]

The suggested topology works to reduce the amount of DC inputs, cost, switches, diodes, and so on. In Dekka et al. (2020) [54] study, for high-power applications, a novel five-level voltage source inverter is suggested as shown in Figure 19. The proposed topology consists of eight switches, three capacitors, and two dc sources. In addition, unlike hybrid converters, the suggested inverter has a simple construction.

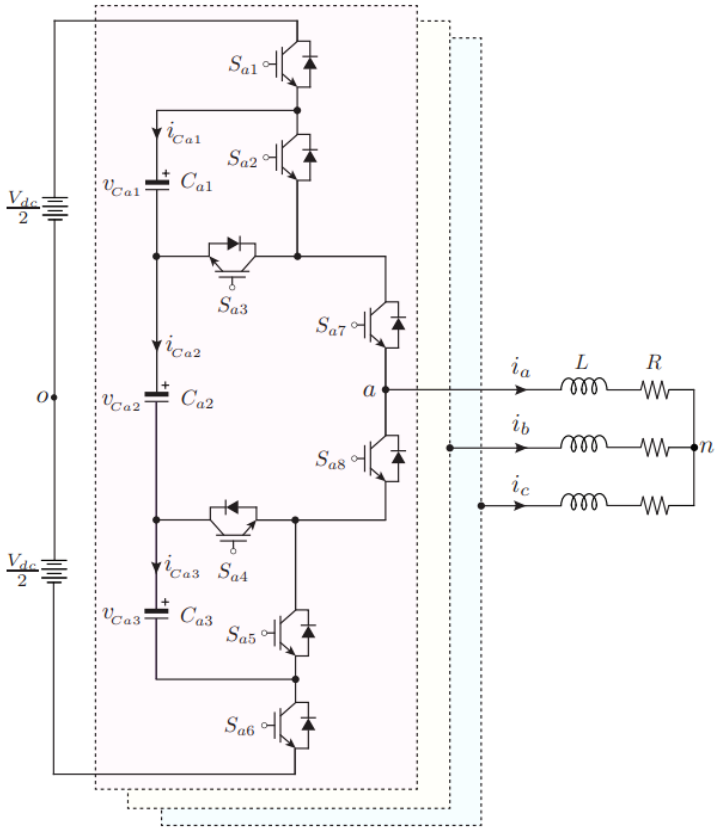

Figure 19. Proposed novel five-level voltage source inverter [54]

Due to the availability of a common dc-link, the suggested topology may also be linked back-to-back. Furthermore, an isolated dc supply and a complicated transformer are not required. In addition, to regulate the flying capacitor voltages, a simple technique based on pulse width modulation system is presented. In Oskuee et al. (2015) [55] study, 'Cascaded Innovative Cell-based Multilevel Inverter' was proposed as a novel MLI topology. Figure 20 depicts the suggested topology with four sources and ten power switches. This topology is implemented without the usage of any passive components.

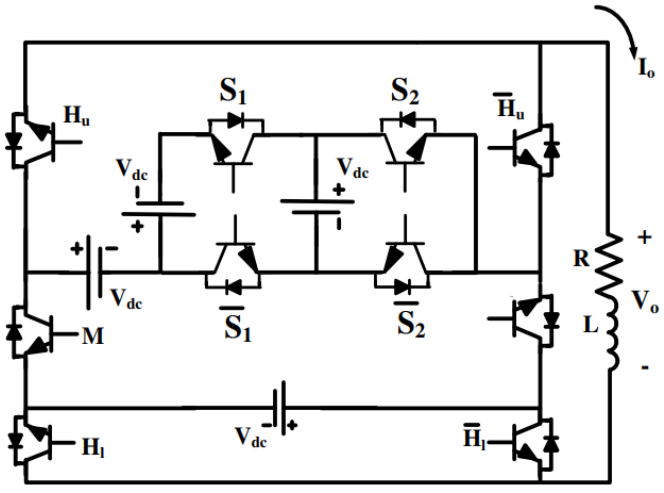

Figure 1. Proposed new cell base MLI [55]

This modular configuration uses fewer components, such as power semiconductor switches for gate driver circuits. The multilevel inverter recommended has the least amount of power loss. Also, because all voltage levels for a symmetrical source configuration cannot be synthesized by using all inputs, equitable power-sharing is not possible, and this circuit is appropriate for just symmetrical configuration. In [56], the author offers a novel Active-Neutral-Point-Clamped Inverters ANPC inverter shown in Figure 21, and may generate greater voltage levels while maintaining unity or enhanced voltage gain. By integrating only one more switch, the topology may give a voltage gain of 1.5 and increase the number of voltage levels to seven.

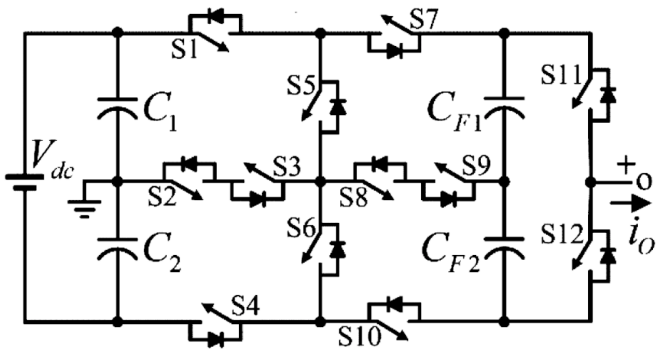

Figure 21. Proposed ANPC inverter [56]

Three switches and one capacitor are added to the design to provide 11 levels with a 2.5 voltage gain. In [57], another cascaded MLI was proposed. Figure 22 indicates the proposed structure with two DC sources and six switches in each modular cell. The structure is suggested for asymmetrical source configurations.

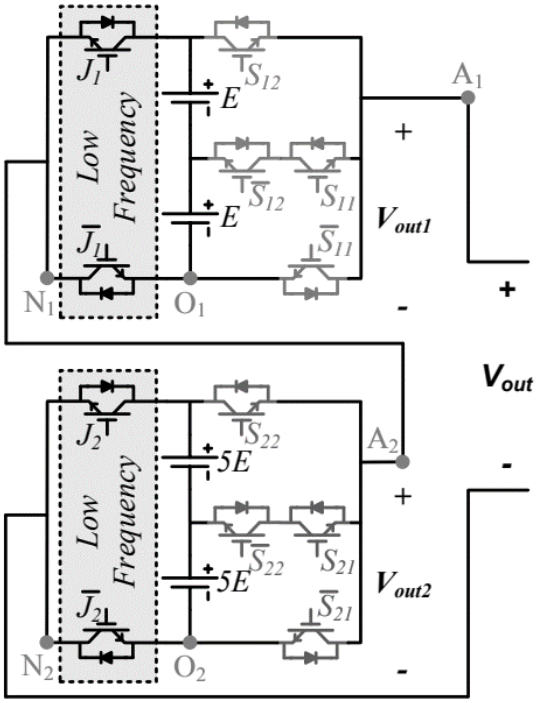

Figure 22. Proposed ANPC inverter [57]

Because of the extremely asymmetric design, the base frequency is not suitable for this case. Also, in the suggested converter, the number of dc links is reduced, decreasing the size and the installation space. In [58], the author proposes a new MLI set up with a small number of high-power electric components, which is indicated in Figure 23. The inverter is made up of two T-type modules coupled by two switches. This inverter may use dc inputs with the varying ratings voltage to function.

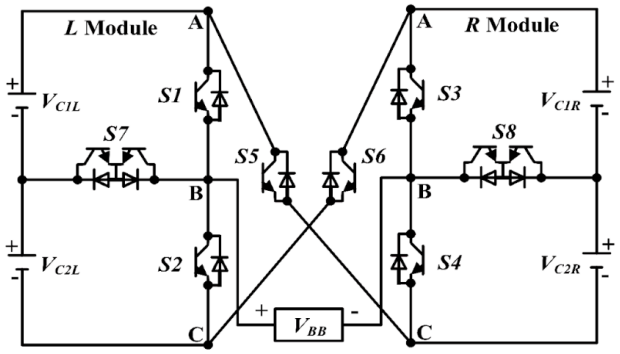

Figure 23. Proposed new MLI using two T-type modules [58]

To achieve greater voltage levels, the suggested inverter can be expanded utilizing cascaded connections. The creation of negative voltage levels without an H-bridge circuit is a key characteristic of this MLI. Low total harmonic distortion and excellent output efficiency can also be obtained. Furthermore, the high-quality output voltage is generated using a low-frequency modulation method. In [59], the author suggested an efficient and reliable MLI. Figure 24 shows the suggested configuration, which included a series of base modules and two power switches in parallel to the power grid.

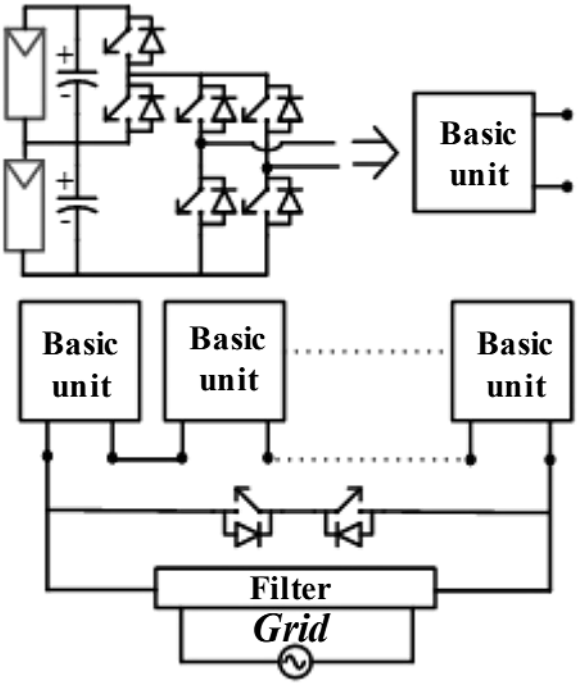

Figure 2. Proposed highly efficient and reliable MLI for solar PV system [59]

Two dc inputs, two MOSFETs, and an H-bridge make up each basic cell. Each cell can produce bipolar many levels. Also, this topology contains no passive components. The authors suggested this MLI for solar PV applications with the goal of reducing leakage current in the system. In [60] for PV systems, a five-level transformerless inverter with lower THD was proposed which can be seen in Figure 25. This case has six switches and three capacitors with a PV source. In addition, unlike half-bridge-based topologies, the suggested inverter can handle reactive power.

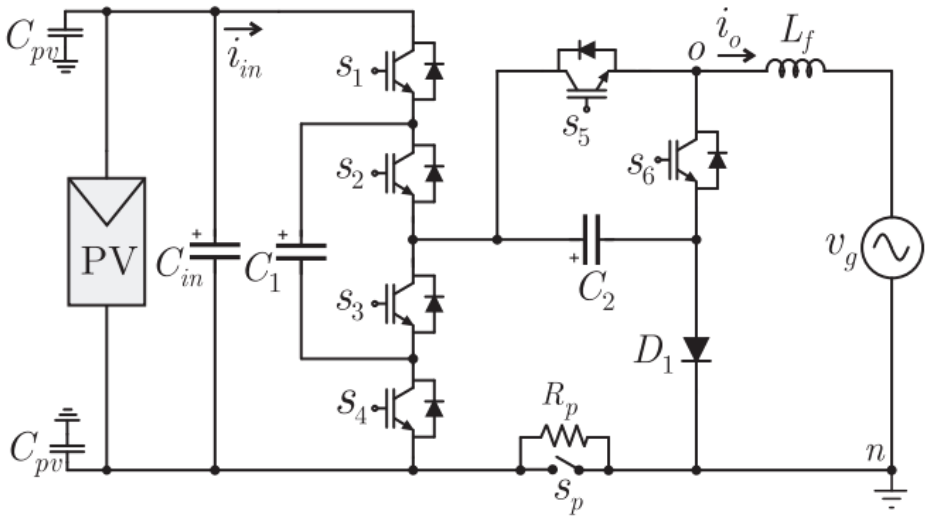

Figure 25. Proposed five-level common ground transformer-less inverter [60]

The inverter connects the grid to the PV system, resulting in very low leakage current. Furthermore, a modulation technique for maintaining balanced voltage over the capacitors has been presented, which can be readily implemented using standard PWM modulators. In [61], a new MLI has been proposed. Figure 26 indicates one module of the suggested architecture. For inverting the polarity of the level generator module, the suggested topology necessitates the use of an H-bridge inverter. A level generator is made up of an input, three capacitors, four power switches, and diodes.

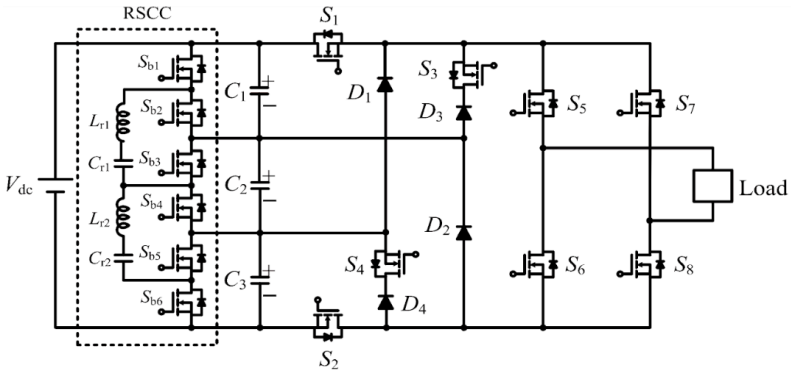

Figure 26. One module of the proposed MLI [61]

Because this configuration necessitates the use of a capacitor to divide the voltage of the DC bus, it necessitates the need for extra control circuitry to maintain the charge balance of the capacitors. A new converter is used to balance the voltage of the capacitors. The suggested topology also lowers the number of different DC sources, switches, and drivers. In [62], a novel three-phase multilevel inverter with fewer components is suggested, which is shown in Figure 27. This inverter creates several level output voltages from a single DC source.

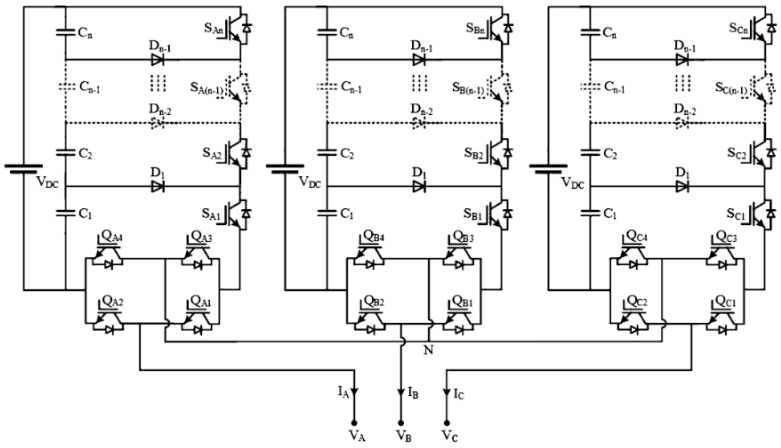

Figure 27. Proposed novel three-phase MLI [62]

Despite the fact that each element is subjected to voltage stress equal to V_{in}, the total standing voltage (TSV) is decreased due to the use of a smaller number of components in relation to the number of series linked capacitors. Also, the suggested inverter may operate at a low switching frequency, lowering switching losses. In [63], it was recommended that a transformerless multilevel topology be used, as shown in Figure 28. The suggested configuration included a half-bridge with two switches S1 and S2, a voltage source, as well as a second half-bridge with switches S3 and S4, and a capacitor.

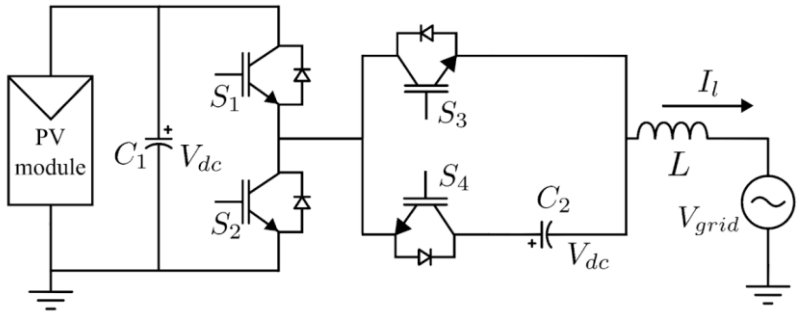

Figure 28. Proposed cascaded half bridge MLI [63]

The MLI described above cannot be used for fundamental switching. The suggested topology's major purpose is to fully remove leakage current in the PV applications by connecting the grid to the PV system, as well as using several levels at the end to ensure minimal filtering needs for the system. In [64], a novel switching capacitor-based multilevel inverter architecture is suggested, which can be seen in Figure 29. Using just one input voltage and two capacitors, the suggested configuration provides seven levels of output voltages.

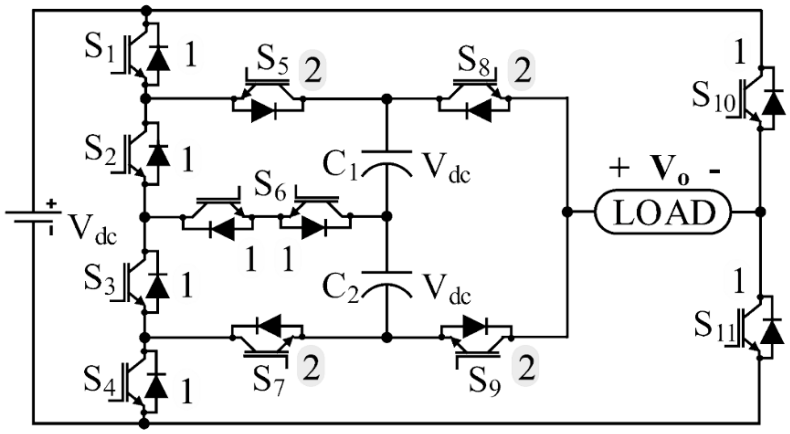

Figure 29. Proposed switching capacitor-based MLI [64]

In this topology, Vout is three times bigger than V_{in}. The suggested seven-level inverter, lowering the topology's overall standing voltage.

4- Conclusion

This paper includes a brief review of classical multilevel inverter topologies and the advantages and disadvantages of each method. In addition, the performance features, switching issues, and technological feasibility of several new multilevel inverter topologies were studied in this paper. These topologies provide a variety of advantages over traditional topologies, including a fewer number of switches, lower harmonics, and lower stresses on the power semiconductors. However, there are some drawbacks, including the necessity for a separate power supply in cascaded MLI, design complexity, and switching control circuits are the primary drawbacks of MLI.

5- Declarations

5-1- Author Contributions

Conceptualization, A.B. and S.D.; methodology, A.B., S.D., and F.S.; validation, F.S., M.H., and Y.L.C.; formal analysis, A.B. and S.D.; investigation, A.B., S.D., and F.S.; resources, A.B., S.D., and F.S.; writing—original draft preparation, A.B.; writing—review and editing, S.D., F.S., M.H., and Y.L.C.; visualization, S.D. and F.S.; supervision, A.B.; project administration, A.B.; funding acquisition, A.B., S.D., and F.S. All authors have read and agreed to the published version of the manuscript.

5-2- Data Availability Statement

No new data were created or analyzed in this study. Data sharing is not applicable to this article.

5-3- Funding

The authors received no financial support for the research, authorship, and/or publication of this article.

5-4- Conflicts of Interest

The authors declare that there is no conflict of interests regarding the publication of this manuscript. In addition, the ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, and redundancies have been completely observed by the authors.

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