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Design and Analysis of Low-power Millimeter-Wave SiGe BiCMOS Circuits with Application to Network Measurement Systems

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For my family and my wife

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Kurzfassung

In den letzten Jahren hat die Nutzung des Frequenzspektrums der Millimeter- (mm-) und Sub-Millimeter-Wellen (Sub-mm-) immer mehr an Attraktivität gewonnen. Mehrere Vorteile wie die größere verfügbare Bandbreite und der kleinere Formfaktor machen diesen Frequenzbereich für zahlreiche Anwendungen wie Hochgeschwindigkeitsverbindungen, Automotive Radar, Gesundheit, Weltraumforschung und Materialwissenschaft attraktiv. Da die Geschwindigkeit von CMOS selbst bei den fortschrittlichsten Technologieknoten noch nicht ausreicht, sind schnelle, aber kostengünstige Ersatzlösungen erforderlich. Mit der kontinuierlichen Entwicklung der fortschrittlichen Silizium-Germanium (SiGe) Heterojunction bipolar transistor (HBTs) und der entsprechenden BiCMOS-Technologie wurde ein Bauelement mit einer maximalen Oszillationsfrequenz ($f_{\max}$) von 720 GHz in Bezug auf die Spitzenleistung und die Integration in 55 nm CMOS erreicht. Diese Errungenschaften und die Vorhersage, dass in Kürze Grenzfrequenzen jenseits des THz-Bereichs erreicht werden, haben die SiGe-basierte Technologie perfekt für die oben genannten Anwendungen geeignet gemacht.

Für künftige mm- und Sub-mm-Wellenanwendungen wird eine der wichtigsten Anforderungen die niedrige DC-Verlustleistung (P_{dc}) sein, die eine erhebliche Reduzierung der Versorgungsspannung (V_{supply}) und des Stroms erfordert. Typischerweise führt eine Verringerung der V_{supply} zu Bauelementen, die nahe oder im Sättigungsbereich arbeiten, was in mm-Wellen-Schaltungen aufgrund der zu erwartenden Leistungsverschlechterung und der oft ungenauen Modelle vermieden wird, und die inverse Basis-Kollektor-Spannung (V_{BC}) wird in früheren Arbeiten im Allgemeinen zur Leistungsmaximierung gewählt. Da der moderate Betrieb in der Sättigung jedoch nicht notwendigerweise zu einem signifikanten Ladungsüberschuss im Kollektor führt, liegt die Transitfrequenz (f_{T}) der Spitzenstromverstärkung von SiGe-HBTs mit der vorwärtsgerichteten V_{BC} immer noch bei mehreren hundert GHz. Darüber hinaus wurde die ungenaue Modellierung durch das Kompaktmodell HICUM/L2 mit der genauen Beschreibung der gespeicherten Ladung im Sättigungs- und Quasi-Sättigungsbereich überwunden. Infolgedessen erscheinen die mm-Wellen-Schaltungen mit geringer Leistung und SiGe-HBTs, die in Sättigung arbeiten, interessant für Untersuchungen.

In dieser Arbeit werden mm-Wellen-Schaltungen mit geringer Leistung auf der Grundlage verschiedener SiGe-BiCMOS-Technologien entwickelt. Verschiedene niedrig-Leistung-mm-Wellen-Schaltungsblöcke werden im Detail diskutiert, darunter rauscharme Verstärker (LNAs), Abwärtsmischer und verschiedene Frequenzvervielfacher, die einen breiten Frequenzbereich von V-Band (50-75 GHz) bis G-Band (140-220 GHz) abdecken. Eine drastische Verringerung der Versorgungsspannung wird durch die vorwärtsgerichtete V_{BC} erreicht, die eine erhebliche Verringerung von P_{dc} ermöglicht, indem sie die Transistoren jeder Schaltung in die Sättigung zwingt. Um einen besseren Kompromiss zwischen P_{dc} und anderen wichtige RF-Leistungsparametern zu finden, beinhaltet die Diskussion jedes Schaltungsblocks die theoretische Analyse der wichtigsten Leistungskennzahlen (FoMs), die Auswahl der Topologie, die Dimensionierung der Bauelemente, die Auswahl der Vorspannung und Techniken zur Leistungssteigerung. In der Zwischenzeit wird eine zusätzliche Leistungsabstimmung in Verstärkern und Mischern realisiert, was der Verteilung der Systemleistung und der Erweiterung des Dynamikbereichs zugute kommt. Es werden verschiedene niedrig-Leistung Entwürfe mit hochmoderner RF-Leistung vorgestellt, darunter:

- Ein 173-207-GHz-Low-Power-Verstärker wurde mit 23 dB Verstärkung und 3,2 mW P_{dc} entwickelt. Im Vergleich zu den zuvor berichteten Low-Power-Verstärkern, die um 200 GHz arbeiten, erreicht dieser Artikel die höchste lineare Verstärkung relativ zum P_{dc} mit einem Verbesserungsfaktor von zehn und sehr wettbewerbsfähigen Leistungen in Bezug auf die Rauschzahl 3-dB-Bandbreite (BW).

- Es wird ein abstimmbarer Verstärker mit niedriger Leistung von 72-108 GHz mit 10-23 dB Verstärkung und 4-21 mW P_{dc} vorgestellt. Dank des regionalen Anpassungsnetzwerks wird

die Breitbandleistung über den Bias-Abstimmbereich beibehalten. Im Vergleich zu modernen W-Band-Verstärkern bietet dieser Entwurf nicht nur interessante Einblicke in die Leistungsmetrik der Abstimmung, sondern auch äußerst wettbewerbsfähige Leistungen in Bezug auf Verstärkung, 3-dB-BW, P_{dc} und 1-dB-Ausgangskompressionspunkt (oP_{1dB}).

- Es wird ein 97 GHz Low-Power Abwärtswandlungsmischer mit 9,6 dB Umwandlungsverstärkung (CG) und 12 mW P_{dc} vorgestellt. Mit der transformatorgekoppelten Gilbert-Zellen-Topologie wurden ein konkurrenzfähiger CG und die erforderliche LO-Leistung und Signalinjektion gleichzeitig mit sehr geringer Verlustleistung erreicht.

- Bei den Multiplizierern wurden ein 56-66 GHz Low-Power Frequenzvervierfacher mit -3,6 dB Spitzen-CG und 12 mW P_{dc} und ein 172-201 GHz Low-Power Frequenzverdreifacher mit -4 dB Spitzen-CG und 10,5 mW realisiert. Durch Kaskadierung dieser beiden Schaltungen wurde auch ein 176-193 GHz Low-Power 12 Multiplikator entwickelt, der eine Ausgangsleistung von -11 dBm bei nur 26 mW P_{dc} erreicht. Im Vergleich zu den zuvor berichteten Multiplizierern mit ähnlicher Betriebsfrequenz und ähnlichem Multiplikationsfaktor erreichen diese Entwürfe den niedrigen Pdc bei konkurrenzfähiger Leistung in Bezug auf Ausgangsleistung und BW.

Darüber hinaus wird der stromsparende mm-Wellen Empfänger vorgestellt. Diese Schaltung ist als ein Empfangskanal eines G-Band Frequenzverlängerers speziell für ein VNA-basiertes Messsystem konzipiert. Ein weiteres Ziel dieses Empfängers ist die Erforschung des niedrig möglichst P_{dc} bei gleichzeitiger Beibehaltung der äußerst wettbewerbsfähigen RF-Leistung für allgemeine Anwendungen, die einen großen LO Abstimmbereich erfordern. Das Kernstück des Empfängers besteht aus einem LNA, einem aktiven abstimmbaren Grundwellenmischer, einem Zwischenfrequenz (IF) Pufferverstärker und einem aktiven inversen Balun. Um den Empfänger für Anwendungen, die einen abstimmbaren LO erfordern, geeignet zu machen, ist eine breitbandige, hochkomplexe Lokaloszillatorkette (LO) integriert, die einen 12-Multiplikator und einen Treiberverstärker enthält. Um die bestmögliche Leistung bei extrem niedrigem P_{dc} zu erzielen, wurden die Low-Power Entwurfsmethoden des Mischers und des LNA implementiert. Bei einer festen IF Frequenz von 1 GHz weist dieser Empfänger einen Spitzen-CG von 49 dB mit einem Abstimmbereich von 14 dB und eine minimale Einseitenband-Rauschzahl (NF) von 16,5 dB auf und verbraucht nur 29 mW statische DC-Leistung für den Kernteil und 171 mW insgesamt einschließlich der LO-Kette. Innerhalb des CG-Abstimmungsbereichs erreicht dieser Empfänger eine RF-BW von 6 dB zwischen 25 und 32 GHz. Im Vergleich zu früher berichteten Empfängern mit ähnlichen Frequenzen wurden der höchste CG und der niedrigste P_{dc} mit sehr wettbewerbsfähiger Leistung in Bezug auf BW, CG-Abstimmungsbereich, 1-dB-Ausgangskompressionspunkt und NF erreicht.

Dank des genauen kompakten Modells HICUM/L2 wird der First-Pass-Zugang für alle Schaltungen erreicht, und die Simulationsergebnisse stimmen insgesamt hervorragend mit den Messungen überein. Darüber hinaus kann eine Sensitivitätsanalyse einen tieferen Einblick in die Abhängigkeit der mit den Transistorparametern verbundenen physikalischen Effekte von den kritischen Leistungsparametern der Schaltung geben. Solche Studien sollen aussagekräftiges Feedback für die Prozessverbesserung und die Modellentwicklung liefern.

Abstract

In recent years, the attraction of the utilization of the millimeter (mm-) and sub-millimeter (sub-mm-) wave frequency spectrum has been steadily enhancing. Several benefits, such as the larger available bandwidth and the smaller form-factor, make this frequency region attractive for numerous applications, such as high-speed links, automotive radar, health, space exploration, and material science. Since the speed of CMOS is still insufficient even with the most advanced technology nodes, high-speed but cost-efficient substitutes are necessary. With the continuous development, the advanced silicon-germanium (SiGe) heterojunction bipolar-transistors (HBTs) and the corresponding BiCMOS technology have achieved the device with the peak power gain related maximum oscillation frequency ($f_{\max}$) of 720 GHz and the integration with 55 nm CMOS. These accomplishments, along with the prediction of beyond THz cutoff frequencies shortly, have made SiGe-based technology perfectly suitable for addressing the applications mentioned above.

For the future mm- and sub-mm-wave applications, one of the key demands will be the low DC power dissipation (P_{dc}), which requires a substantial reduction of the supply voltage (V_{supply}) and current. Typically, reducing the V_{supply} will lead to devices operating close to or in the saturation region, which is avoided in mm-wave circuits due to expected performance degradation and often inaccurate models, and inverse base-collector voltage (V_{BC}) is generally chosen in previous work for maximizing performance. Nevertheless, since the moderate operation in saturation does not necessarily lead to a significant excess charge in the collector, the peak current gain cutoff frequency (f_{T}) of SiGe HBTs with the forward-biased V_{BC} still remains at several hundreds of GHz. Furthermore, the inaccurate modeling has been overcome by the compact model HICUM/L2 with the accurate description of the stored charge in the saturation and quasi-saturation region. As a result, the low-power mm-wave circuits with SiGe HBTs operating in saturation appear intriguing for investigation.

In this thesis, the low-power mm-wave circuits are developed based on several SiGe BiCMOS technologies. Different low-power mm-wave circuit blocks are discussed in detail, which include low-noise amplifiers (LNAs), down-conversion mixers, and various frequency multipliers, covering a wide frequency range from V-band (50-75 GHz) to G-band (140-220 GHz). A drastic decrease of the V_{supply} is realized by forward-biased V_{BC}, enabling a substantial reduction of P_{dc} by forcing transistors of each circuit to operate in saturation. To discover a better trade-off between P_{dc} and other core RF performance parameters, the discussion of each circuit block contains the theoretical analysis of the key figure of merits (FoMs), topology selection, device sizing, bias selection, and performance enhancement techniques. Meanwhile, additional performance tunability is realized in amplifiers and mixers, beneficial to system performance distribution and dynamic range extension. Various low-power designs with cutting-edge RF performance are introduced, including:

- A 173-207 GHz low-power amplifier is designed with 23 dB gain and 3.2 mW P_{dc}. Compared with the previously reported low-power amplifiers operating around 200 GHz, this work realizes the highest linear gain relative to the P_{dc} with an improvement factor of ten, together with highly competitive performances containing noise figure and 3-dB bandwidth (BW).

- A 72-108 GHz low-power tunable amplifier is presented with 10-23 dB gain and 4-21 mW P_{dc}. Thanks to the regional matching network, the broadband performance over the bias tuning range is maintained. Compared with state-of-the-art W-band amplifiers, this design presents not only intriguing insights into performance metrics tuning but also highly competitive performances in terms of gain, 3-dB BW, P_{dc}, and 1 dB output compression point (oP_{1dB}).

- A 97 GHz low-power down-conversion mixer is presented with 9.6 dB conversion gain (CG) and 12 mW P_{dc}. With the transformer-coupled gilbert-cell topology, competitive CG and

required LO power along with signal injection have been achieved simultaneously with very low-power dissipation.

- For multipliers, a 56-66 GHz low-power frequency quadrupler with -3.6 dB peak CG and 12 mW P_{dc}, and a 172-201 GHz low-power frequency tripler with -4 dB peak CG and 10.5 mW are realized. By cascading these two circuits, a 176-193 GHz low-power $\times$12 multiplier is also designed, achieving -11 dBm output power with only 26 mW P_{dc}. Compared to the previously reported multipliers with similar operating frequency and multiplication factor, these designs achieve the low P_{dc} with competitive output power and BW.

Furthermore, the low-power mm-wave receiver is presented. This circuit is designed as one receiving channel of a G-band frequency extender specifically for a VNA-based measurement system. Another goal of this receiver is to explore the lowest possible P_{dc} while keeping its highly competitive RF performance for general applications requiring a wide LO tuning range. The core part of the receiver consists of a LNA, an active tunable fundamental mixer, an intermediate frequency (IF) buffer amplifier (BA), and an active inverse balun. A wide-band, high-CG local oscillator (LO) chain is integrated to make the receiver suitable for applications requiring tunable LO, which contains a $\times$12 multiplier and a driver amplifier. To exploit the best possible performance with ultra-low P_{dc}, the low-power design methods of the mixer and LNA are implemented. With a fixed IF frequency at 1 GHz, this receiver exhibits a peak CG of 49 dB with 14 dB tuning range, and a minimum single-sideband noise figure (NF) of 16.5 dB, consuming only 29 mW static DC power for the core part and 171 mW overall including the LO chain. Within the CG tuning range, this receiver achieves a 6 dB RF BW from 25 to 32 GHz. Compared with previously reported receivers at similar frequencies, the highest CG and lowest P_{dc} with highly competitive performance in terms of BW, CG tuning range, 1 dB output compression point, and NF have been achieved.

Thanks to the accurate compact model HICUM/L2, the first-pass access is achieved for all circuits, and the overall simulation results show excellent agreement with measurement. Based on that, the sensitivity analysis is enabled, which obtains a deeper insight into the dependence of transistor parameter associated physical effects on the critical circuit performance parameters. Such studies are supposed to provide meaningful feedback for process improvement and modeling development.

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1 Introduction

1.1 Motivation

Millimeter-wave (mm-wave) and sub-millimeter-wave (sub-mm-wave) are defined by signals with wavelengths of 1-10 and 0.1-1 mm in the vacuum, respectively, which can be directly converted to the frequencies of 30-300 GHz and 0.3-1 THz, respectively. The utilization of these frequency ranges is advantageous compared to microwaves. Larger absolute bandwidth with higher carrier frequency enables data transmission with a higher bit rate in wireless communication and enhances lateral resolution in sensing and imaging systems. In addition, the higher operating frequencies with a smaller form-factor of the circuits and systems is always beneficial in applications with more compact size. As a result, the interest in mm- and sub-mm-wave frequency spectrum has been steadily increasing in recent years [1]. Numerous applications, such as high-speed point-to-point wireless communication [2], sensing and imaging [3], and frequency-modulated continuous-wave (FMCW) radar [4], which cover a wide variety of fields such as material science (including material characterization and identification test) [5], health, chemistry and biology [6], as well as the space exploration, are predicted to play significant roles in modern life.

Modern semiconductor technologies keep developing towards mm-wave, sub-mm-wave, and even THz frequencies to catch up with the rapidly growing demands. The complementary metal-oxide-semiconductor (CMOS), III-V-based technologies, and the silicon-germanium heterojunction bipolar transistor (SiGe HBT) with bipolar CMOS (BiCMOS) technology are, among others, the frequently used solutions for addressing the applications listed above. The selection of the most suitable solutions in the future market is mainly driven by several significant aspects, such as performance, cost, and energy efficiency. The current gain cutoff frequency/power gain related maximum oscillation frequency ($f_{\mathrm{T}}/f_{\mathrm{max}}$) is a critical figure-of-merit (FoM) for evaluating device performance (speed). In addition, the cost and energy efficiency of technology not only depends on the lithography node but also the yield, process variation, model accuracy (which significantly affects the time and cost), and the integration level with the digital portion. The characteristics of the three leading technologies are summarized as follows:

- CMOS has dominated the manufacturing platform for the digital and mix-signal integrated circuits and systems for a long time owing to its low cost, high volume, and high level of integration between radio frequency (RF) and digital. Although CMOS features state-of-the-art technology nodes, the speed of RF-CMOS is still insufficient even with the finest and most scalable device compared to the other two counterparts [7]. On the other hand, implementing the most advanced technology node makes the CMOS process no longer low-cost.

- III-V technologies offer both HBTs and High-Electron-Mobility Transistors (HEMTs) with state-of-the-art device speed, owing to superior material mobility. The 1.2 THz [8] and 1.5 THz [9] f_{max} have been realized by indium phosphide (InP) HBT and HEMT, respectively, using at least two generations of depreciated lithography node of 130 nm for HBT

and 25 nm for HEMT technologies. Additionally, featuring the same speed, the III-V HBTs benefit from higher breakdown voltage than that of the SiGe HBTs, enabling higher available output power(P_{out}). However, due to obstacles such as the low integration level into digital CMOS processes, low yield, considerable process variation, and lack of accurate models, III-V-based technologies are unlikely to serve the fast-growing and sizeable high-volume market in the future both from cost and energy efficiency point of view.

- SiGe HBTs and the corresponding BiCMOS technology combine the strengths of the above two competitors, which integrates the SiGe HBTs with good RF performance and the digital CMOS with high computing power. With a much-relaxed technology node of 130 nm, over 700 GHz f_{max} has been achieved [10], which is highly competitive for applications towards THz. More importantly, the integration of SiGe HBTs into the CMOS environment is much simpler since they are both silicon-based technologies, which enables the high-level integration of mm-wave and sub-mm-wave front-end circuits and systems with digital control and signal processing portion on a single chip.

A detailed comparison of the $f_{\mathrm{T}}/f_{\mathrm{max}}$ as a function of critical lithography dimension (either emitter width or channel length) among CMOS [11–16], SiGe HBTs [10,17–22], and InP HBTs [8,23–29] is presented in Fig. 1.1. The state-of-the-art device with the highest f_{max} was realized by 130 nm InP HBTs from Teledyne [29], featuring a peak $f_{\mathrm{T}}/f_{\mathrm{max}}$ of 520/1150 GHz. Apart from that, NTT reported their 250 nm InP HBTs with the leading-edge room temperature f_{T} of 813 GHz [24], but at the expense of a much lower f_{max} of 286 GHz. A slightly lower speed with $f_{\mathrm{T}}/f_{\mathrm{max}}$ of 505/720 GHz was achieved using 130 nm SiGe HBT by IHP [10], which is still about one generation behind InP HBTs in terms of f_{max}. As a comparison, the latest results with the $f_{\mathrm{T}}/f_{\mathrm{max}}$ of 350/370 GHz for the 22 nm fully depleted silicon on insulator (FD SOI) by Globalfoundres (22FDX) [11] and of 300/450 GHz for the 22 nm fin field-effect transistor (FinFET) by Intel (22FFL) [12] have been presented recently after specific device optimization for RF performance. Nevertheless, the achievements of RF-CMOS are still inferior compared to that of SiGe and InP HBTs, even with the much more advanced technology node of 22 nm. Moreover, since the RF-CMOS has been significantly downscaled, the continuous shrink of the transistor size would no longer be helpful to the further device speed improvement, owing to the surface scattering effects in the very thin silicon layer [30], which will lead to the degradation of the transconductance (g_{m}). In another word, the RF-CMOS has already reached its speed limitation.

Please notice that the above discussion of device speed only focuses on the pure transistor level after de-embedding of parasitics and interconnection structures, known as the device-level f_{T}. However, those impacts must be considered at the actual circuit design level because the interconnection with passive devices and components is mandatory. Therefore, the extrinsic f_{T} becomes more attractive for circuit designers. Thanks to the simultaneously much higher g_{m} and device capacitances, HBTs present much less deterioration than that of CMOS by parasitics and interconnections, which even widen this speed disparity between CMOS and HBTs in the circuits world. As noted in [7], with the same device-level f_{T} value of about 300 GHz after de-embedding, the extrinsic f_{T} of the 28 nm MOSFET decreases more than a factor of two, making the implementation of mm-wave and sub-mm-wave front-ends even trickier. By comparison, the extrinsic f_{T} of the 130 nm SiGe HBTs remains at about 80%. Additionally, HBTs provide several distinctive superiorities over CMOS in terms of circuit design level. For instance, HBTs offer a larger device size with higher current resulted unit P_{out}, which reduces the number of required devices in power amplifiers and in turn reduces the interconnect parasitics introduced by the devices stack, the number of stages, and chip area.

Furthermore, the higher affordable collector-emitter voltage (than the drain-source voltage of CMOS) of HBTs is a further benefit in high P_{out} designs, such as power amplifiers and signal sources. Moreover, a lower flicker noise of HBTs contributed by the much lower corner frequency

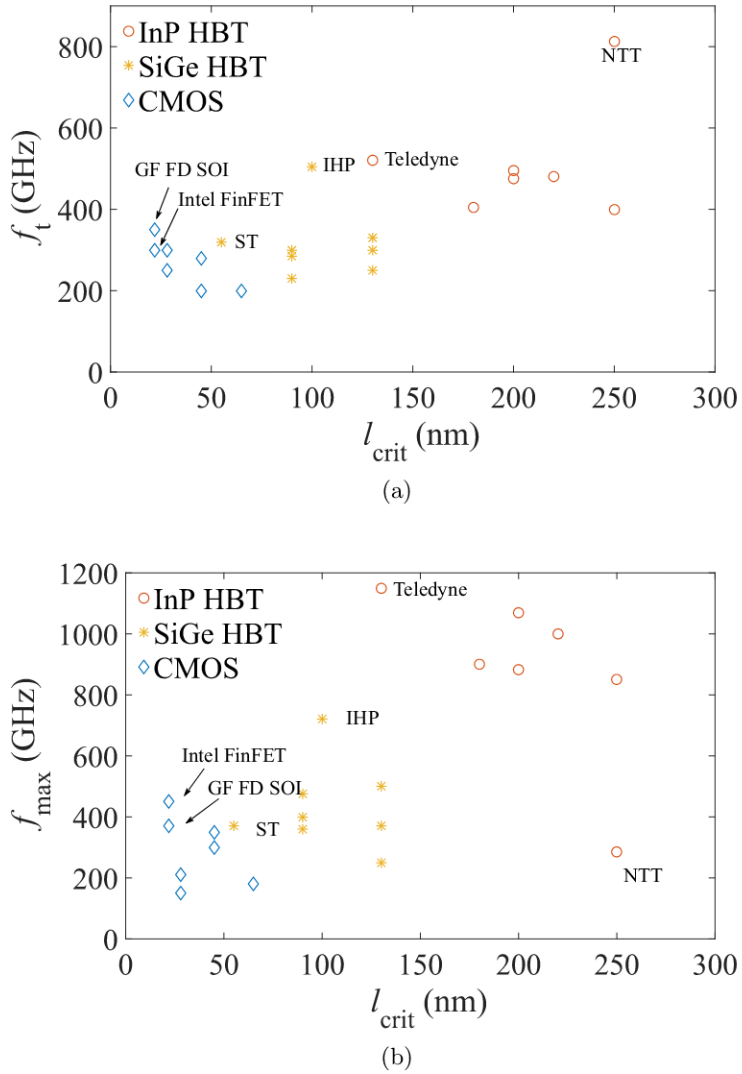


Figure 1.1: Comparison of (a) f_T and (b) f_{max} versus the critical lithography dimensions (either emitter width or channel length) of the device among three technologies.

is attractive for voltage-controlled oscillators (VCO). In summary, with a relaxed lithography node (and in turn low cost), the prediction of beyond THz cutoff frequencies [7], and the recent development of the integration with 55 nm CMOS [31], the SiGe HBTs and the corresponding BiCMOS technology has been proved to be an excellent candidate [32] for addressing mm-wave and sub-mm-wave applications with mass-market wafer volume in the future market.

Circuit design and fabrication always rely on compact device models. For circuit simulation and optimization, a physics-based model is preferable due to its accurate representation of the characteristics of the fabricated devices with comprehensive coverage of the operation conditions. Apart from that, the design cost and efficiency are also of interest, which require the model to be sufficiently straightforward. With the continuous development of modern semiconductor technologies towards higher speed, the significance of device modeling has been proliferating due to the enormously increased device complexity, fabrication time, and manufacturing cost. To stay competitive, the first-pass success of the mm-wave design has become a core demand in the industry. For SiGe HBT technologies, an advanced bipolar transistor compact model HIgh CUrrent Model/level 2 (HICUM/L2) has been developed [30] based on the generalized integral charge control relation, which preserves the physical basis of SiGe HBT structures.

As a simple (and hence fast) but physics-based model, HICUM/L2 adequately predicts various physical effects, especially in high-frequency regions such as non-quasi-static effect and substrate coupling. Besides, HICUM/L2 covers a broad region of temperatures, geometry, and bias, enabling the circuit optimization for different goals with a high degree of freedom.

In recent years, the development of high-speed SiGe HBTs has made many mm-wave aforementioned applications available. Common to these applications is the demand for low energy consumption. For given duty cycles, this demand boils down to minimizing the DC power consumption (P_{dc}), which requires the substantial reduction of supply voltage and current of the mm-wave circuits and systems during operation. Especially for the DC power-constrained applications such as mobile communication and portable systems, saving DC power prolongs the standby period and product life significantly. The biggest challenge here is to achieve the best possible trade-off between P_{dc} and performance, i.e., minimizing P_{dc} with the lowest constraint on other key FoMs of circuits, such as (conversion) gain, noise, and bandwidth (BW), etc. Reducing the supply voltage will lead to HBTs operating close to or in the saturation region, which is often not encouraged due to perceived performance degradation and inaccurate modeling in the saturation region.

Nevertheless, since the moderate operation in saturation does not necessarily lead to a significant excess charge in the collector, the peak f_{T} of SiGe HBTs with the forward-biased V_{BC} up to around 0.5 V still remains at several hundreds of GHz. More importantly, the compact model HICUM/L2 has overcome the inaccurate modeling problem thanks to the accurate description of the stored charge in the saturation and quasi-saturation region. Hence, low-power mm-wave circuits with SiGe HBTs operating in saturation appear intriguing for investigation, which will be explored in this thesis based on several 130 nm SiGe BiCMOS technologies.

1.2 Objectives

The primary focuses of this thesis are the design, analysis, fabrication, and measurement of low-power mm-wave circuits and systems. Based on the advanced SiGe BiCMOS technology and the compact model HICUM/L2, different low-power circuits are investigated in this thesis towards a better trade-off between P_{dc} and other key performance parameters, including low-noise amplifiers (LNAs), down-conversion mixers, frequency triplers, quadruplers, and $\times 12$ multiplier chain. The operating frequency of the designed circuits covers V-band (50-75 GHz), W-band (75-110 GHz), and G-band (140-220 GHz). Additionally, based on the low-power LNA and down-conversion mixer design methods, a $\times 12$ LO chain integrated low-power G-band receiver is introduced. This receiver is supposed to be used as one receiver channel of a network measurement system, and is also suitable for general applications requiring a wide LO tuning range.

Along this line, several significant steps in the design process are studied in this thesis:

- Device analysis. Device sizing and bias selection directly link to the P_{dc} and performance of a single device. Based on the accurate and geometry scalable model HICUM/L2, the deeper insight of the critical FoMs as a function of device size and bias need to be explored at first. Three essential parameters are analyzed and selected carefully, including supply voltage (V_{supply}), collector current density (J_{C}), and emitter area (A_{e}). Notice that the careful consideration of connection structures (such as vias) close to devices is also significant because of the noticeable speed deterioration caused by parasitics in mm-wave frequencies. Such impacts should be accurately estimated by the electromagnetic (EM) simulation.

- Circuit design contains topology selection, performance enhancement approaches, and realization of passive components and networks. Circuit topology determines the overall required device number. Meanwhile, special measures are implemented to compensate

for performance degradation due to parasitics and saturation operation, such as inductor-based gain-boosting techniques in LNAs and transformer-coupled gilbert-cell mixers. Better stage efficiency not only relaxes the critical demand on device speed but also reduce the number of devices and stages required in the circuits, saving P_{dc} both at the device and circuit level. Additionally, passive components and networks are also essential: a properly designed DC distribution network helps circuit stabilization; the matching network strongly influences noise figure, gain, and BW; transmission line design helps reducing loss and cross-talk at mm-wave frequencies.

- System analysis. The key FoMs of the system are the primary concern, such as conversion gain, noise, P_{out}, linearity, and harmonic suppression. By the precise analysis of dynamic range and careful performance distribution, the design priority of each block can be adjusted according to its position. Meanwhile, the number of circuit blocks can also be minimized by combing functionalities into one block so that the system P_{dc} can be further reduced.

- Experimental verification. Accurate results at mm-wave frequencies depend on a reliable measurement environment both for small- and large-signal operation.

- Physical-effect-related analysis. Thanks to the accurate compact model HICUM/L2, sensitivity analysis is enabled to obtain a deeper insight into the dependence of transistor parameter associated physical effects on the critical circuit performance parameters. Such studies are supposed to provide meaningful feedback for process improvement and modeling development.

This thesis contains seven chapters and four appendices, which are organized as follows. The motivations and main objectives of this thesis have been emphasized in this chapter. The second chapter introduces the main features of several SiGe BiCMOS technologies utilized in this thesis. Commonly used passive components and networks are also introduced, including grounded-sidewall-shielded microstrip line, zero-impedance transmission line (ZTL), active and passive baluns. Different low-power circuits, such as low-power amplifiers, mixers, and multipliers, are discussed in the following three chapters. A G-band low-power receiver with $\times 12$ LO chain integration is presented in the sixth chapter. Summaries and conclusions of this thesis are given in the final chapter. The detailed derivations of the essential equations are presented in appendices.

r

2 Technology

The features of the fabrication technologies need to be studied at first as they usually dominate the overall RF performance of circuits and systems under design. Meanwhile, the passive elements also play a vital role in practical circuit designs, for instance, biasing, filtering, and impedance matching networks. In this chapter, the manufacturing technologies and the significant and commonly used passive elements in the designs of this thesis are introduced. The first part presents the main features of several utilized SiGe BiCMOS processes, including the basics of devices and the back-end process. The second part shows the commonly used passive components, such as GSSML, ZTL, balun, etc.

2.1 Fabrication Technologies

As an excellent solution for addressing a large number of the present and prospective mm-wave and sub-mm-wave applications, the recent development of the advanced SiGe BiCMOS technology relies on two large-scale research projects funded by the European Commission, namely DOTFIVE and DOTSEVEN. The predecessor DOTFIVE project successfully demonstrated SiGe HBTs for the first time with peak f_T/f_{max} of 300/500 GHz, minimum gate delay of the ring oscillator of 2 ps [33], and systems operating at 160 GHz. In addition, the following DOTSEVEN project reached the challenging goal of SiGe HBTs with f_T/f_{max} of 505/720 GHz, the minimum gate delay of the ring oscillator of 1.34 ps [10], and systems operating at 240 GHz. With these significant achievements, several advanced SiGe BiCMOS processes have become available in the research and commercial field, which were employed in this thesis for circuit and system designs.

2.1.1 SiGe HBT performance

The speed of a transistor can be directly linked to f_T and f_{max}. f_T is the transit frequency, defined as the extrapolated frequency of unity small-signal current gain, i.e., $|h_{21}|$=1 assuming a single-pole low-pass frequency dependence. f_{max} is the maximum oscillation frequency, as the maximal frequency for power amplification of the device, and the commonly used definition is Mason's unilateral power gain, as U(f)=1. As mentioned in Chapter 2, for a fabrication process, the former is typically used to measure the speed of a transistor in switching circuits (such as dividers), while the latter usually represents the capability of the device in amplifiers or oscillators.

The transit frequency f_T can be found as [7]

$$\frac{1}{2\pi f_T} = \frac{C_{BE} + C_{BC}}{g_m} + (R_E + R_C)C_{BC}. \tag{2.1}$$

Here, g_m is the transconductance, which is proportional to I_C (and J_C) and can be approximately

described by an exponential relationship using Boltzmann statistics, as

$$g_{\mathrm{m}} = \left.\frac{dI_{\mathrm{c}}}{dV_{\mathrm{BE}}}\right|_{V_{\mathrm{CE}}} \approx \frac{I_{\mathrm{c}}}{V_{\mathrm{T}}}, \tag{2.2}$$

with V_{T} is the thermal voltage. R_{E} and R_{C} are the emitter and collector series resistance. C_{BE} and C_{BC} represent the total capacitances (depletion, etc.) connected to the base terminal. C_{BE} includes the diffusion capacitance C_{diff} for storage of minority carriers in forward device operation, which directly links to the forward transit time τ_{f} as [30]

$$\tau_{\mathrm{f}} = \frac{C_{\mathrm{diff}}}{g_{\mathrm{m}}} = \tau_{\mathrm{E}} + \tau_{\mathrm{EB}} + \tau_{\mathrm{B}} + \tau_{\mathrm{BC}}. \tag{2.3}$$

As can be seen, τ_{f} results form charge storage in base-collector and base-emitter junction, as well as in the base, and emitter, respectively.

The f_{max} can be approximated by

$$f_{\mathrm{max}} \cong \sqrt{\frac{f_{\mathrm{T}}}{8\pi R_{\mathrm{B}} C_{\mathrm{BC}}}}. \tag{2.4}$$

Here, R_{B} is the total base resistance including internal and external portions.

Now let's discuss the dependency of device dimension on f_{T} and f_{max}. Generally=the emitter width of the transistor in the same technology usually stays at its minimum value, and larger device dimensions are obtained by enlarging the emitter length. Based on equation (2.2), with the same biased J_{C}, larger HBTs with longer emitter have higher I_{C} and thus g_{m}. However, higher g_{m} does not necessarily lead to higher f_{T} because larger devices also have larger capacitances, which more or less neutralize the contribution from g_{m}, as shown in the first term of (2.1). In the second term, the series resistance R_{E} and R_{C} of the devices reduce with device size and counteract the increased C_{BC}. As a result, f_{T} is more or less independent with device emitter length. Similarly, R_{B} and C_{BC} in f_{max} show inverse variation with device emitter length.

2.1.2 B11HFC

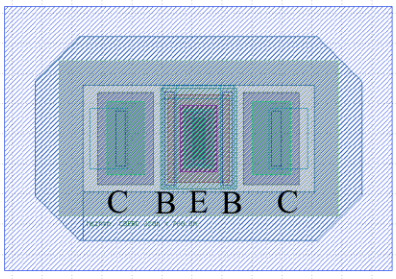


Figure 2.1: Example of a transistor layout of the CBEBC configuration with the smallest emitter length of 700 nm.

The B11HFC is a 130 nm SiGe BiCMOS process from Infineon Technologies AG, which was developed during the DOTFIVE project and commercialized for the high-performance and power-efficiency analog and mix-signal applications at mm-wave frequencies. For RF designs, this technology offers high-speed, medium-speed, and high-voltage transistors with different HBT contact configurations like BEC, BEBC, CBEC, CBEBC, CEBEC, and CBEBEBC, along with emitter mask lengths between 0.7 to 10 µm with 0.1 µm steps, which provide a high degree of freedom for circuit design and optimization. A layout example of a double base transistor

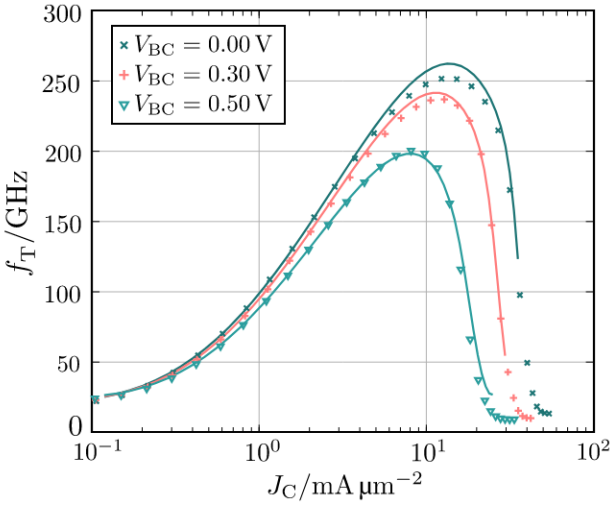


Figure 2.2: Measured (symbols) and HICUM/L2 simulated (lines) f_T versus J_C of a CBEBEBC transistor with $A_{e\text{-}w}$=0.13 µm ×9.91 µm and varied V_{BC} from 0 to 0.5 V [34].

(CBEBC) with the smallest emitter length is demonstrated in Fig. 2.1. The typical high-speed npn HBT with emitter window area ($A_{e\text{-}w}$) of 0.13 µm ×2.71 µm features f_T/f_{max} of 250/370 GHz at base-collector voltage (V_{BC}) of -0.5 V, with the collector-emitter breakdown voltage (BV_{CEO}) of 1.5 V. Fig. 2.2 presents the comparison of measured and HICUM/L2 simulated f_T versus J_C of CBEBEBC type device with $A_{e\text{-}w}$=0.13 µm ×9.91 µm in this process as an example. As shown, a peak f_T of around 250 GHz is obtained at J_C of 10.5 mA/µm^2 with V_{BC}= 0 V.

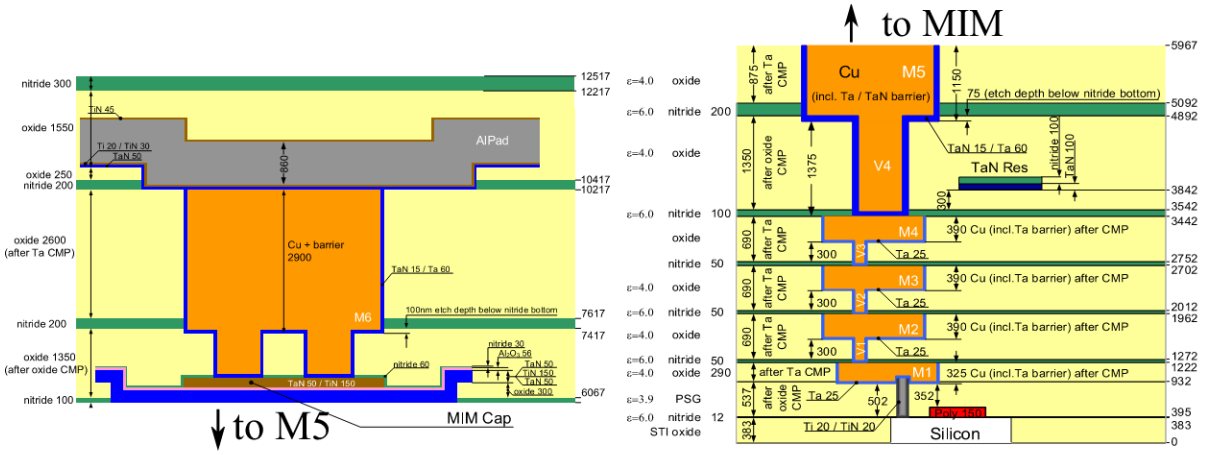


Figure 2.3: (a) Upper and (b) lower part of the cross-section of B11HFC 130 nm SiGe BiCMOS process [35].

The cross-section of the back-end process is presented in Fig. 2.3. The back-end process of this technology offers four thin copper layers (M1-M4), two thick copper layers (M5, M6), and an aluminum (Al) layer for pads, allowing different types of TL with various dielectric thicknesses. The silicon dioxide (SiO_2) with the permittivity ϵ=4 is located between metal layers. Also included in this technology are RF metal-insulator-metal (MIM) capacitors, RF-TaN, and poly resistors, which are also well modeled. The MIM capacitor is located between M5 and M6 with a typical unit capacitance of 1.4 fF/µm^2. The TaN and poly resistors offer different sheet resistances from 20 to 325 Ω/µm, which are suitable for low and high resistance applications.

Other devices are also available for digital and analog utilizations, such as N- and P-FET, varactor, and PIN diodes. A W-band low-power tunable amplifier and a down-conversion mixer were designed using B11HFC, which will be introduced later in this thesis.

2.1.3 SG13G2

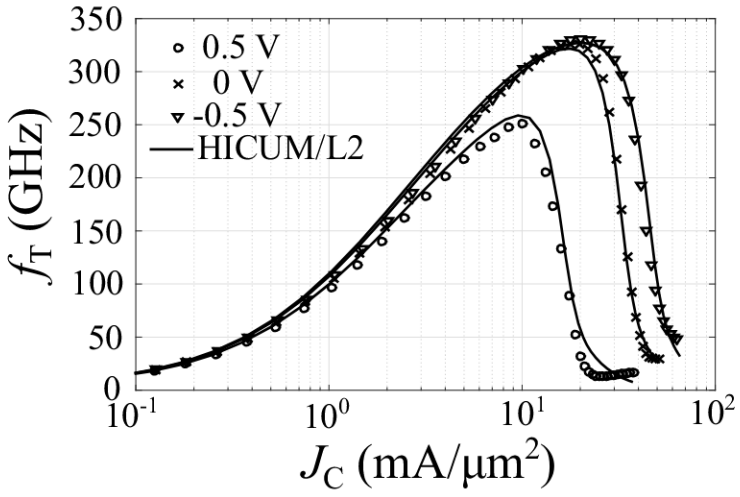


Figure 2.4: Measured (symbols) and HICUM/L2 simulated (lines) f_T versus J_C for different V_{BC} of an HBT with $A_{e\text{-}w}$=4×70 nm×900 nm [36].

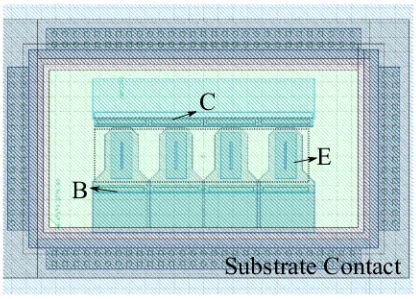


Figure 2.5: Layout of the four-finger device with $A_{e\text{-}w}$=4×70 nm×900 nm.

Based on the excellent outcome of the DOTFIVE project, IHP Microelectronics offers a high-performance 130 nm SiGe BiCMOS process named SG13G2 with the fastest commercially available npn HBTs to date featuring peak f_T/f_{max} of 300/500 GHz. Fig. 2.4 presents the measured and HICUM/L2 simulated f_T versus J_C for different V_{BC} of an HBT with $A_{e\text{-}w}$=4×70 nm×900 nm in this technology. As seen, a peak f_T of around 330 GHz is achieved at J_C of 20 mA/µm^2 at V_{BC} of -0.5 V. The PDK provides SiGe HBT cells with just a single emitter area, but a larger size of the transistor is available by connecting N_x cells in parallel up to ten, i.e., $A_{e\text{-}w}$=N_x×70 nm×900 nm, where N_x is the multiplication factor. The layout of the device with the N_x of 4 is shown in Fig. 2.7. Fig. 2.6 shows design relevant characteristics of the single-finger transistor (N_x=1) with V_{BC} of 0 V: the simulated total base-collector capacitances C_{BC}, total base-emitter capacitance C_{BE}, and g_m as a function of J_C.

The cross-section of the back-end process of this technology is shown in Fig 2.7. It contains seven metal stacks, which provides a high degree of freedom for routing the different types of transmission lines (TLs), such as microstrip line (ML), stripline, coplanar waveguide (CPW), and coplanar waveguide with Lower ground Plane (CPWG) with different dielectric thicknesses. The two thick topmost metal stacks TM1 and TM2 with low sheet resistance enable low loss, high

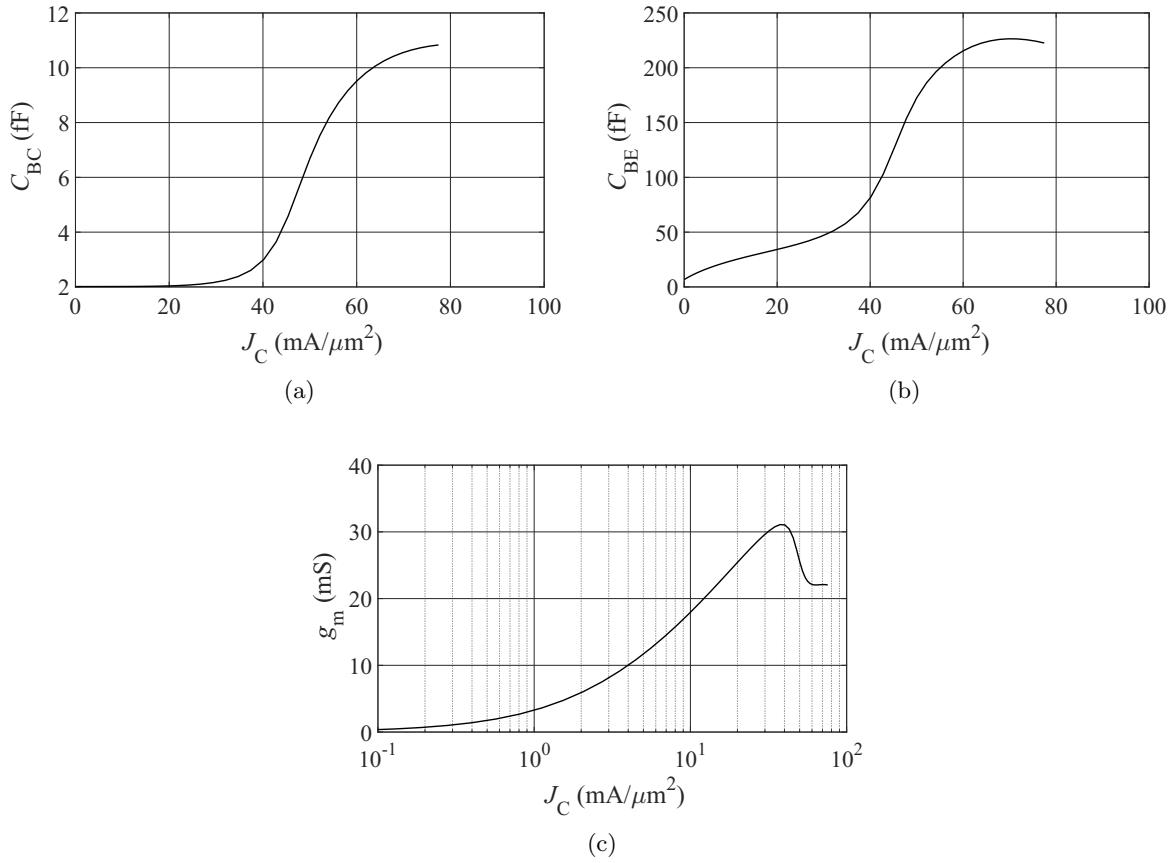


Figure 2.6: Simulated (a) total C_{BC}, (b) total C_{BE}, and (c) g_m versus J_C of the single-finger device (N_x=1) at V_{BC}=0 V. The two capacitances are extracted based on simulated Y-parameters at 10 GHz [36].

current densities and reliability electromigration. SiO_2 with ϵ=4 is implemented between metal layers. Moreover, the essential passive components are available, such as the MIM capacitors between TM1 and M5 with the unit capacitance of 1.5 fF/µm^2.

Meanwhile, three types of polysilicon resistances, namely R_{sil}, R_{ppd}, and R_{high}, respectively, are provided by this process. The former uses salicided p-doped polysilicon with a low sheet resistance of 7 Ω/µm. In contrast, the later two are unsalicided with n-doped and partially compensated gate polysilicon with medium and sheet resistance values of 260 and 1360 Ω/µm, respectively. In addition, different MOS transistors such as N-MOS, P-MOS, and isolated NMOS are also available with gate oxide of both thin and thick thickness, aiming to 1.2 V digital logic or 3.3 V V_{supply}, respectively. In this thesis, the multipliers and the G-band receiver were implemented in this technology.

2.1.4 SG13D7

Moving towards the goal of the DOTSEVEN project, the SG13D7 is an experimental SiGe BiCMOS technology run also at IHP Microelectronics. Based on the standard 130 nm BiCMOS technology SG13G2 with a similar device configuration and back-end process, several device-related improvements are employed to boost the high-speed performance of the device. To begin with, the vertical profile is optimized with new processes for the emitter formation and the selectively implanted collector. Secondly, the emitter-base spacer width, emitter window width, and the resistivity of the external base regions are reduced with a low-temperature back-end

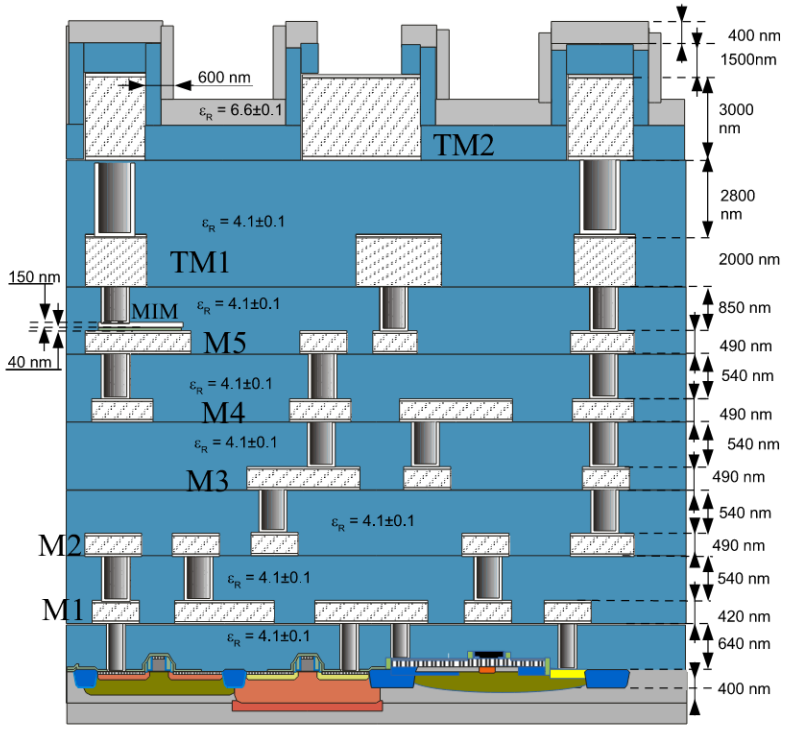


Figure 2.7: The cross-section of the IHP SG13G2 process (provided by IHP Microelectronics, https://www.ihp-microelectronics.com/services/research-and-prototyping-service/mpw-prototyping-service/sigec-bicmos-technologies).

with NiSi, which contribute to a lower base resistance. Compared to [10], in which state-of-the-art speed of SiGe HBT was presented, no millisecond annealing is applied. Consequently, the device with a peak f_T/f_{max} around 460/600 GHz is realized. Fig. 2.8 presents the measured and HICUM/L2 simulated f_T for different V_{BC} of a transistor with $A_{e\text{-}w}$=2×100 nm ×1000 nm, and a peak f_T of 460 GHz is offered at J_C of 30 mA/µm^2 with V_{BC} of -0.5 V. In this thesis, an ultra-low-power G-band amplifier was realized using this technology.

2.2 Commonly Used Components

2.2.1 Grounded-sidewall-shielded microstrip line

TLs are one of the core passive components for signal transmission in RF and microwave systems. Typically, Waveguide and coaxial lines are two commonly used low-loss TLs, but they are not suitable for microwave integrated circuit designs due to the size and on-chip integration with active devices. Instead, planar TLs have become more popular, owing to their compact size, low-cost, and much easier on-chip integration. With the increase of operating frequency, the physical length of TLs becomes electrically large and comparable with the wavelength, and the parasitic effect becomes noticeable. As a result, a careful selection and design of TLs is required for maximal signal delivery and minimal reflection between two ports at mm-wave frequencies. EM-simulation using Momentum in Keysight Advanced Design System (ADS) is used in the TL design and optimization.

The RLGC lumped-element-based equivalent circuit [38] is necessary for TL study, as presented in Fig. 2.9. Here, an infinitesimal piece (Δz) of TL is analyzed, with L as the total self-inductance, C as the shunt capacitance, R as the resistance, and G as the dielectric conductance. According to the traveling wave solution of the sinusoidal steady-state condition of the

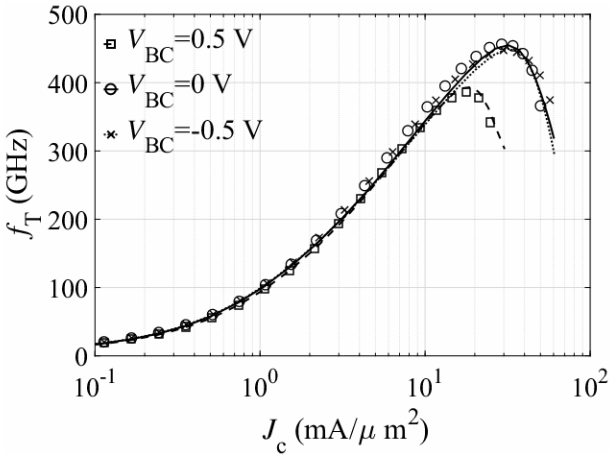


Figure 2.8: Measured (symbols) and HICUM/L2 simulated (lines) f_T versus J_C for different V_{BC} of the device with $A_{e\text{-}w}$=2×100 nm×1000 nm [37].

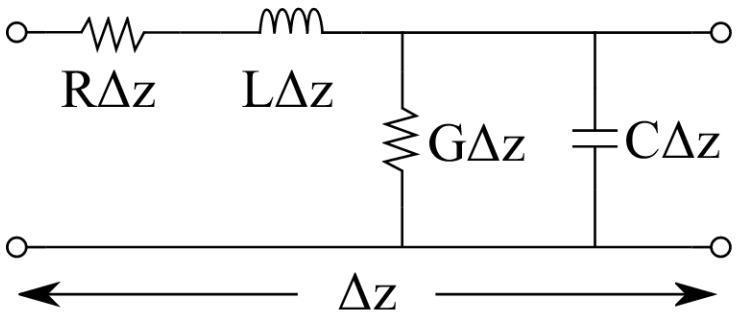


Figure 2.9: RLGC lumped-element equivalent circuit of an infinitesimal TL segments Δz.

telegrapher equations, the characterization impedance Z_0 of the TL can be written as [38]

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}. \tag{2.5}$$

The complex propagation constant γ can be shown as

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}, \tag{2.6}$$

where α and β are the attenuation and phase constant, respectively. For low-loss TL with G$\ll \omega C$ and R$\ll \omega L$, α can be calculated as [39]

$$\alpha \cong \frac{1}{2}(R\sqrt{\frac{C}{L}} + G\sqrt{\frac{L}{C}}), \tag{2.7}$$

where the first and second term represent the conductor and dielectric losses, respectively. The proper R, L, G, and C values should be realized by optimizing the physical dimension of the TL cross-section so that the desired Z_0 together with low loss can be simultaneously obtained.

ML and CPWG are two of the most popular used TL types, and their cross-section view is presented in Fig. 2.10a and Fig. 2.10b, respectively. ML consists of a single conductor strip at the top and a single ground plane at the bottom. Unlike the stripline, in which the dielectric materials fully wrap the upper conductor layer, the ML conductor is placed on top of dielectrics with direct contact with the air. ML has the major portion of the electric field (E-field) to be located vertically inside the dielectric from the top metal to the bottom ground, whereas a

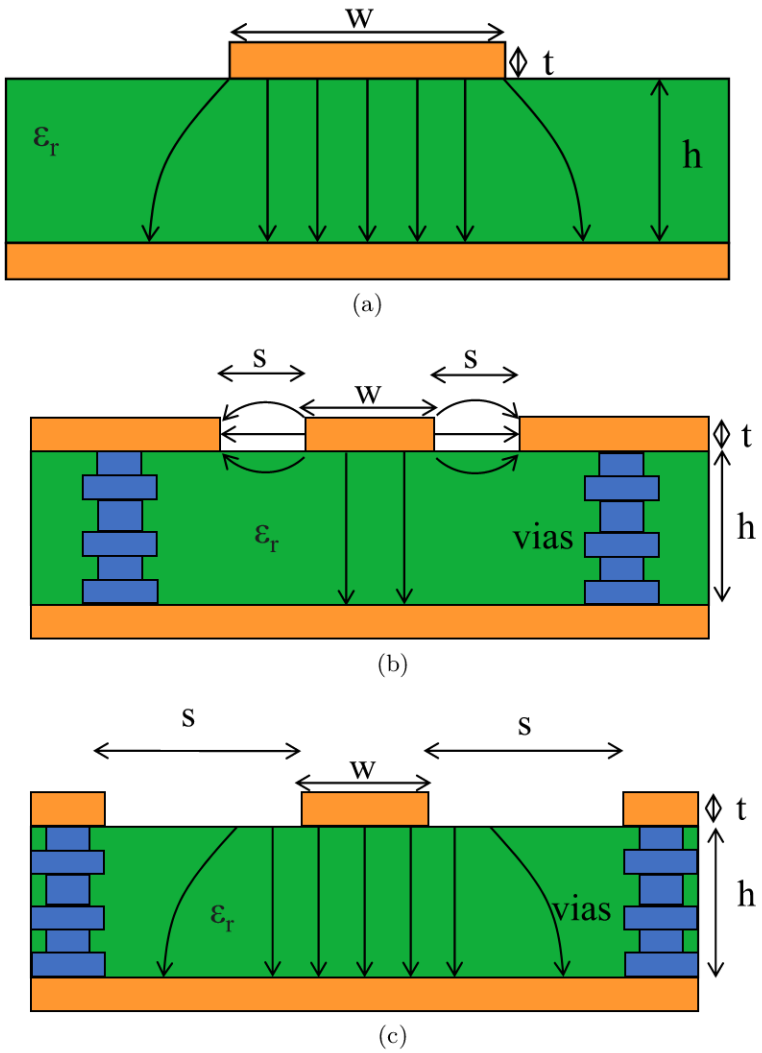


Figure 2.10: Cross-section view of (a) ML, (b) CPWG, and (c) GSSML used in this thesis with important parameters and E-field of the wave propagation.

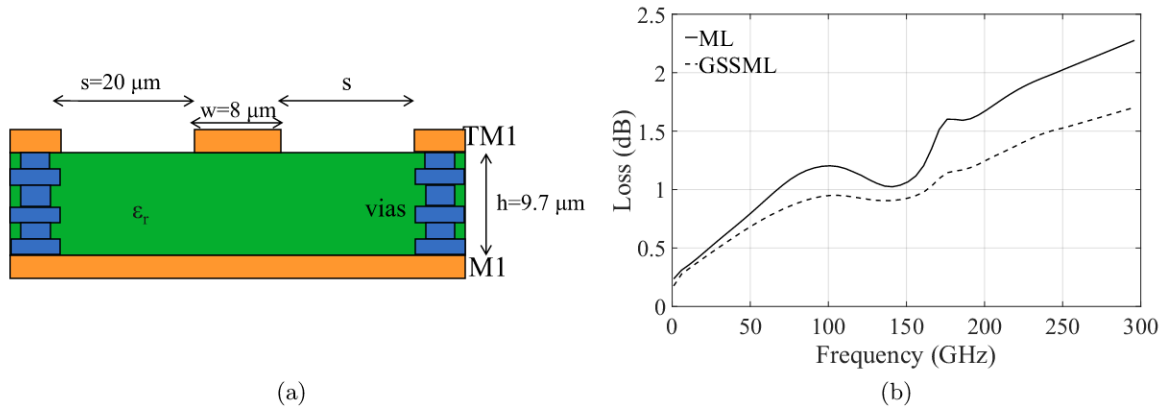
minor fraction is radiated through the air above the chip. This is mainly due to the different permittivity ε of the dielectrics and air, leading to the boundary discontinuity. As a result, ML supports only the quasi TEM wave.

CPWG is an updated version based on standard CPW for high-frequency applications. As presented in Fig. 2.10b, compared to the standard CPW with a center strip in the middle and two parallel ground planes on both sides, an extra ground plane at the bottom is added in CPWG in order to reduce the dielectric losses of the silicon substrate and thus desensitize the impact of substrate thickness [40]. Since the conductor layer is also in contact with the air, both the CPW and CPWG support a signal propagating with a quasi-TEM mode, similar to ML. However, due to the typically much smaller s than h in CPWG, much stronger E-fields exist between the ground-signal-ground coplanar layer, whereas much fewer filed lines exist between the upper signal plane to the bottom ground. Consequently, compared to ML, more signals propagate in the air in CPWG, leading to a lower effective permittivity ε_r, if the dimensions of their cross-section and substrate materials are the same [41]. As can be seen from the equation (2.7), a lower ε_r reduces C as well as the dielectric loss, but at the expense of higher conductor loss. Nevertheless, such an increase of the conductor loss can be compensated mainly by choosing a wider w. Therefore, with a proper design, the CPWG generally provides a lower signal loss and

higher isolation preventing crosstalk between different components and circuits.

However, there are some constraints in practical CPW/CPWG designs. First, the on-chip ground uniformity in CPW/CPWG becomes critical because the ground plane aside from the signal strip is usually severed and thus cannot be connected with each other in the same metal layer. Hence, special measures, either air bridges or bottom-layer connections are required. Since such connections will go across the signal metal, the parasitic and coupling effects at mm-wave operating frequencies have to be considered, thus significantly adding extra costs and efforts during EM simulation. Additionally, in multi-stage circuits such as the four-way combined differential PAs or stacked gilbert-cell based mixers/multipliers, or some complicated passive structures such as on-chip transformers or couplers, TLs with different layers are usually necessary. This can be easily realized by ML with common bottom ground plane but is difficult by CPW/CPWG.

To combine the benefits of ML and CPWG, the GSSML is implemented in this thesis, and the cross-section view is shown in Fig. 2.10c. Similar to the CPWG, the basic configuration of the GSSML also contains two ground planes with a center strip in the middle and an extra ground plane at the bottom. However, the space s in the GSSML is larger than twice of h, which enables the same vertical quasi-TEM mode as the ML, and the two ground planes on both sides here only act as the grounded sidewall. The first advantage of the GSSML is lower loss than the ML. By connecting the ground plane to the topmost thick metal layer, the overall resistance of the ground plane is decreased, leading to reduced eddy-current losses [42]. Fig. 2.11b shows the simulated loss of the GSSML in SG13G2 technology compared to standard ML with the same dimension as presented in Fig. 2.11a, with approximately 0.5 dB loss optimization at 200 GHz.



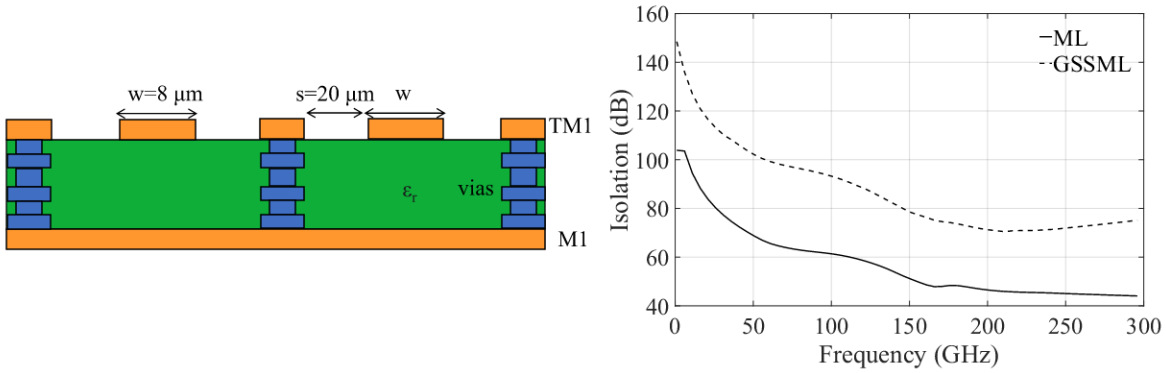
(a) (b)

Figure 2.11: Cross-section view of (a) the GSSML and ML without grounded sidewall in SG13G2 technology used in simulation, and (b) simulated loss versus frequency. The length of the test line is 1 mm.

Like CPW/CPWG, GSSML also offers higher isolation and prevents the crosstalk between different components and circuit blocks than ML. Two parallel lines using the SG13G2 process (the cross-section view shown in Fig. 2.12a) are simulated to compare the isolation of the GSSML and ML, as presented in Fig. 2.12b. After implementing grounded sidewalls between two parallel lines, more than 15 dB higher isolation is observed.

2.2.2 Zero-impedance Transmission Line

The general goal of the TL is to realize the lowest RF loss to avoid distortion. The DC distribution networks in practical circuit design require structures with opposite characteristics, i.e., the ideally infinite attenuation of all RF signals but with perfect delivery of DC power so as to distribute the supply voltages and currents. However, such networks are especially challenging in



(a) (b)

Figure 2.12: Cross-section view of (a) two parallel GSSML and ML without grounded sidewall, and (b) simulated isolation versus frequency. The length of the test line is 1 mm.

mm-wave and sub-mm-wave wide-band circuits and systems. Owing to the practical restriction of DC pad numbers and orientation, the DC biases usually have to pass through DC lines before arriving at the circuit core. Such lines become electrically long at high frequencies, and their parasitics and coupling effects become huge. Hence, to desensitize such impacts and guarantee the proper operation of the circuit, a good DC distribution network has to be designed [43].

This network can be conventionally achieved by decoupling capacitors at low frequencies. However, this approach is no longer optimal at mm-wave frequencies due to the potential resonance with the parasitic inductances introduced by the (electrically-) long DC lines, which lead to a noticeable performance degradation above the resonance frequencies. Since the parasitic inductance strongly depends on the length of DC paths (from the circuit core to DC pads), the value of decoupling capacitors for each DC path has to be carefully selected by accurate EM simulation to get rid of the unwanted resonance. Hence, extra design effort and time are added, especially in a complicated system with a large number of DC biases.

In this thesis, ZTL is implemented as the DC distribution network. Fig. 2.13 presents a TL

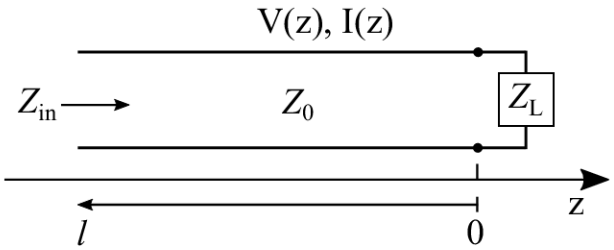


Figure 2.13: A TL terminated by an arbitrary load impedance Z_{L}.

terminated by an arbitrary load impedance Z_{L}. According to the traveling wave solution [38], the input impedance of the TL (Z_{in}) at location l (l<0) seen towards Z_{L} can be defined based on the total voltage and current (as the sum of incident and reflected waves, $V_{\mathrm{i/r}}$ and $I_{\mathrm{i/r}}$), as

$$Z_{\mathrm{in}}(l) = \frac{V_{\mathrm{i}}e^{-\gamma l} + V_{\mathrm{r}}e^{\gamma l}}{I_{\mathrm{i}}e^{-\gamma l} - I_{\mathrm{r}}e^{\gamma l}} Z_0 = \frac{1+\Gamma e^{-2\gamma l}}{1-\Gamma e^{-2\gamma l}} Z_0. \tag{2.8}$$

Here, γ is the complex propagation constant shown in equation (2.6), and Γ is the voltage reflection coefficient, defined as

$$\Gamma = \frac{Z_{\mathrm{L}} - Z_0}{Z_{\mathrm{L}} + Z_0}. \tag{2.9}$$

As presented in Fig. 2.13, the traveling distance of the reflected wave is 2l longer than that of the incident wave. For good DC distribution networks, as high as possible RF attenuation ($e^{\alpha l} \longrightarrow 0$) is required, leading to an extinguished reflected wave, as seen in equation (2.8). Then, Z_{in}(l) depends on only the incident wave and is independent of the load termination, which becomes

$$Z_{\text{in}}(l)|_{e^{\alpha l}\longrightarrow 0} = \frac{V_{\text{i}}}{I_{\text{i}}} = Z_0, \tag{2.10}$$

where Z_0 is the characteristic impedance of connected TL, as shown in Fig. 2.13. As a result, high isolation is obtained between the circuit core and DC source parts, eliminating the impedance uncertainty introduced by the components of the ZTL, such as long DC lines, pads, or the possible future packaging structures like wire bonds. Such high isolation significantly enhances the predictability of the DC distribution networks and relaxes the design effort and time of the complicated EM simulations.

Based on the RLGC model of infinitesimal TL segments shown in Fig. 2.9, α for low-loss TL with neglectable dielectric loss can be roughly expressed as

$$\alpha \cong \frac{R}{2}\sqrt{\frac{C}{L}}. \tag{2.11}$$

Since low conductor loss (R) is also desired for the DC signal to minimize the voltage drop, the high α can only be realized by increasing the ratio C/L per length of the line, which results in Z_0 close to 0, as

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \longrightarrow 0. \tag{2.12}$$

Therefore, this line is the so-called zero-ohm transmission line, which provides an RF short. Even though in practical design, exactly 0 Ω is usually hard to realize, the value of nearly 0 is still possible by enlarging the shunt capacitance C per length of the ZTL.

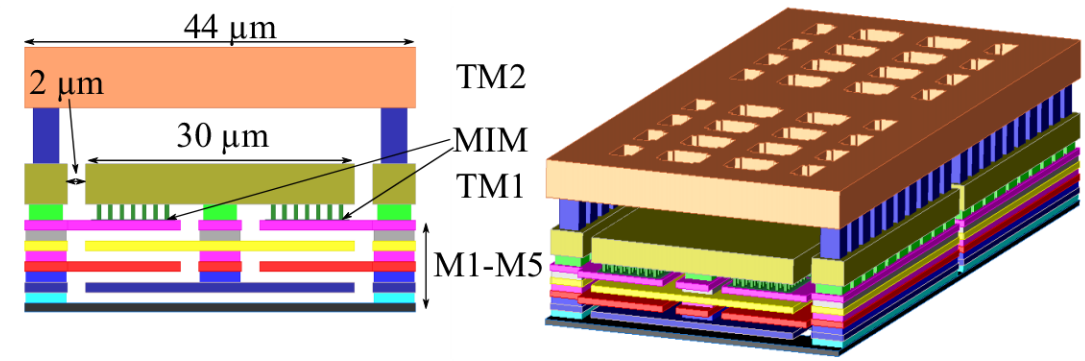


Figure 2.14: (a) Cross-section with detailed dimensions and (b) 3D view the ZTL example designed using IHP SG13G2/D7 technology.

For a general parallel-plate capacitor, C is determined by

$$C = \varepsilon\frac{A}{d}, \tag{2.13}$$

where A, d, ε is the coupling area, the distance between two layers, and the dielectric permittivity, respectively. For a particular process with fixed ε, the value of the shunt C has to be increased by maximizing A while minimizing d. Fig. 2.14 shows the cross-section with detailed dimensions

and 3D view of an example of the designed ZTL using IHP SG13G2/D7 technology. As shown, all the metal layers from M1 to TM2, are utilized for ZTL. Starting from the bottommost layer M1, all even layers are connected in the middle as DC signal layer, whereas all odd layers including the topmost layer TM2 are connected from two sides as ground. Since the distance between the adjacent two layers is much smaller than that between TM2 and M1, the effective d is significantly reduced. Furthermore, the presented interleaved configuration is implemented to sandwich the signal layers between the multi-ground layers, resulting in a much larger A. To further improve C, a large number of small shunt MIM capacitors are added between TM1 and M5.

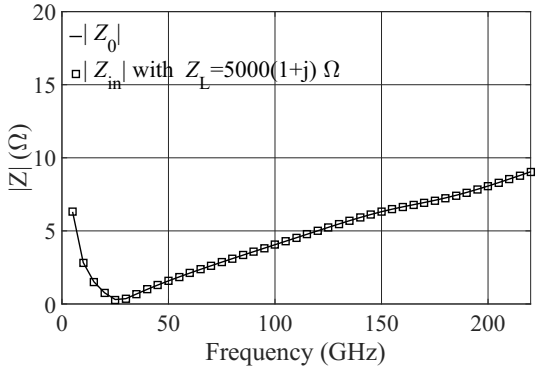


Figure 2.15: Simulated Z_0 of 150 µm ZTL (in Fig. 2.14) compared with the simulated Z_{in} of the same ZTL with a large load termination Z_{L}=5000(1+j) Ω up to 220 GHz.

Fig. 2.15 shows the simulated Z_0 of the designed ZTL with 150 µm length compared to the simulated Z_{in} of this ZTL with a large load termination (Z_{L}=5000 (1+j) Ω). As presented, the Z_0 of this ZTL is below 10 Ω up to 220 GHz. Furthermore, according to Fig. 2.16b, $Z_{\text{in}}{\approx}Z_0$ with a large terminated load, indicating a perfect isolation. Fig. 2.16a presents the chip photo of the fabricated test ZTL with 150 µm length. The measurement compared to simulation (including pads) at G-band is shown in Fig. 2.16b. As can be seen, the ZTL S_{11} presents a fairly low real part, indicating a low Z_0. The observed good agreement between simulation and measurement indicates a good accuracy of the EM-simulation up to G-band. In summary, ZTLs ensure the low Z_0 with perfect isolation, thus significantly saving the simulation time and effort during the DC distribution network design.

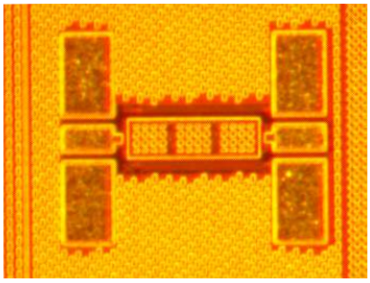
2.2.3 Balun

The differential (or balanced) configuration is one of the most popular topologies in modern mm-wave and sub-mm-wave applications. Thanks to the symmetry configuration, the virtual ground plane provides higher robustness against the parasitics introduced by connections and passive structures, resulting in much higher circuit stability at high frequencies. In addition, a theoretically doubled output power can be realized compared to the single-ended counterparts. The differential configuration is also beneficial to reduce signal distortion in nonlinear designs, owing to the natural cancellation of half unwanted harmonics in multipliers.

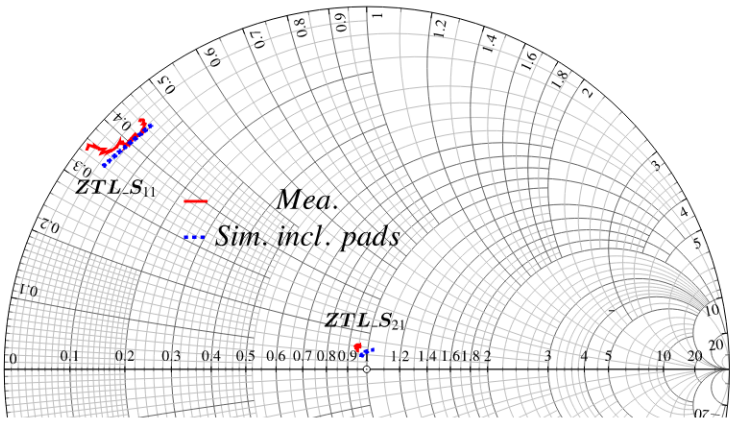
To convert the signal between single-ended and differential, the balun is one of the most commonly utilized components in a large variety of circuits, such as Gilbert-cell-based mixers [44], multipliers [45], and differential amplifiers [46]. The balun is a three-port component. Theoretically, the operation of the balun can be expressed by S-parameters

$$S_{11} = 0, \tag{2.14a}$$

$$S_{21} = -S_{31}. \tag{2.14b}$$



(a)



(b)

Figure 2.16: (a) Micrograph of the fabricated 150 µm ZTL test structure in the SG13G2/D7 process. (b) Comparison of the simulated and measured S-parameters of the test ZTL with two RF pads from 140 to 220 GHz.

Three main performance parameters are used to determine the overall balun quality, i.e., insertion loss, amplitude, and phase imbalance, respectively. A low insertion loss is desired for a lower noise figure (NF) and a higher output power. For the input balun (in differential LNAs), the insertion loss has to be added to the overall NF directly, and for the output balun (in differential PAs), the output power and efficiency will be reduced due to such loss. Meanwhile, a lower amplitude and phase imbalance are also advantageous for reducing signal distortion caused by non-perfect differential signals. A balun can be realized as passive or active structures. Depending on the operating frequency, both passive and active baluns are used in this thesis.

2.2.3.1 Active Balun

At frequencies below 30 GHz, the passive balun is usually achieved by the inductance-capacitance (LC) tanks [47] and thus occupies a large chip area due to the size of the planar inductor. Furthermore, owing to the frequency-selective networks (LC), the available bandwidth of passive baluns at low frequency is limited. Please notice that the theoretically lowest available insertion loss is -3 dB because the total power equally splits into two outputs. As a comparison, the active ones are much more attractive at this frequency range because of the compact size, wider available bandwidth, and possible insertion gain.

Fig. 2.17 presents a 15 GHz active balun using IHP SG13G2 technology, which is used as the input stage of a differential ×12 local oscillator (LO) multiplier chain for the receiver system in this thesis. This balun consists of a common-base transistor (T2) and a differential pair (T4-T7). Here, T2 acts as a front-stage CB amplifier as well as an active matching network. At the

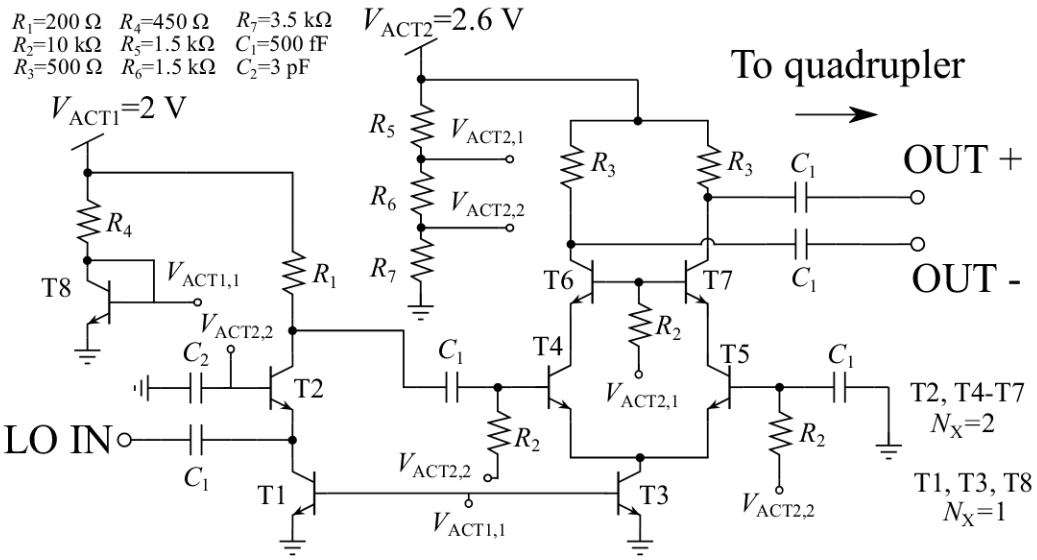


Figure 2.17: Schematic diagram of the designed 15 GHz active balun using IHP SG13G2 technology.

frequency of operation around 15 GHz, the assumption

$$1/g_{\mathrm{m}} \ll 1/\omega C_{\mathrm{be}} \tag{2.15}$$

is still valid, where C_{be} is the total base-emitter capacitance of the HBT, and ω is the angular frequency. Then, the Z_{in} of a CB transistor is mainly resistive, which can be expressed as [48]

$$Z_{\mathrm{in}} = \frac{1}{g_{\mathrm{m}} + j\omega C_{\mathrm{be}}} \approx \frac{1}{g_{\mathrm{m}}}. \tag{2.16}$$

By carefully selecting the size and bias of the device, $1/g_{\mathrm{m}}$ can be optimized to achieve good match with the system impedance. As discussed in Section 2.1.1, selecting larger devices does not improve $f_{\mathrm{T}}/f_{\mathrm{max}}$ but directly increases the DC power consumption. In addition, this CB pre-amplifier is placed as the first stage with small-signal operation, the large-signal performance is not the prior goal. Hence, a device with N_{x} of 2 is chosen for T2. An extra emitter follower (T1) enables the further improvement of the signal amplification. The smallest device (N_{x}=1) is chosen for T1 to reduce the overall P_{dc} of this balun. The balanced outputs are generated by the differential pair with the CB amplifier driven from one side (T4) and AC ground shorting the other side (T5), resulting in further amplified differential mode whereas the cancellation of common mode. As mentioned, this active balun is supposed to be used as the first stage of the LO multiplier chain with high CG and low input power level. Hence, the output power does not necessarily be too large. Thus, devices with N_{x}=2 are selected for the differential pair for a better DC power efficiency. Larger devices can be selected here for higher output power. As shown, totally seven transistors are used in this balun, leading to a large number of biases. Hence, two voltage distributors are implemented to save the number of DC pads and thus reduce the complexity of future off-chip packaging processes, such as wire-bonding or transition design, but at the expense of the extra P_{dc}. The DC voltage distributors can be either achieved by several resistors (R_5-R_7) or a HBT with resistors (T8 and R_4).

Fig. 2.18a presents the simulated S-parameters of this active balun. The circuits provide a peak gain of 12 dB at 9 GHz, with a 3 dB BW of 15 GHz from 4.5 to 19.5 GHz. The gain is higher than 5 dB over a wide frequency range from 2 to 35 GHz. The observed S_{11} is lower than 5 dB starting from 6 GHz, which indicates a reasonable input match achieved by T1 and T2. The slightly higher input return loss is due to the imaginary mismatch of the active

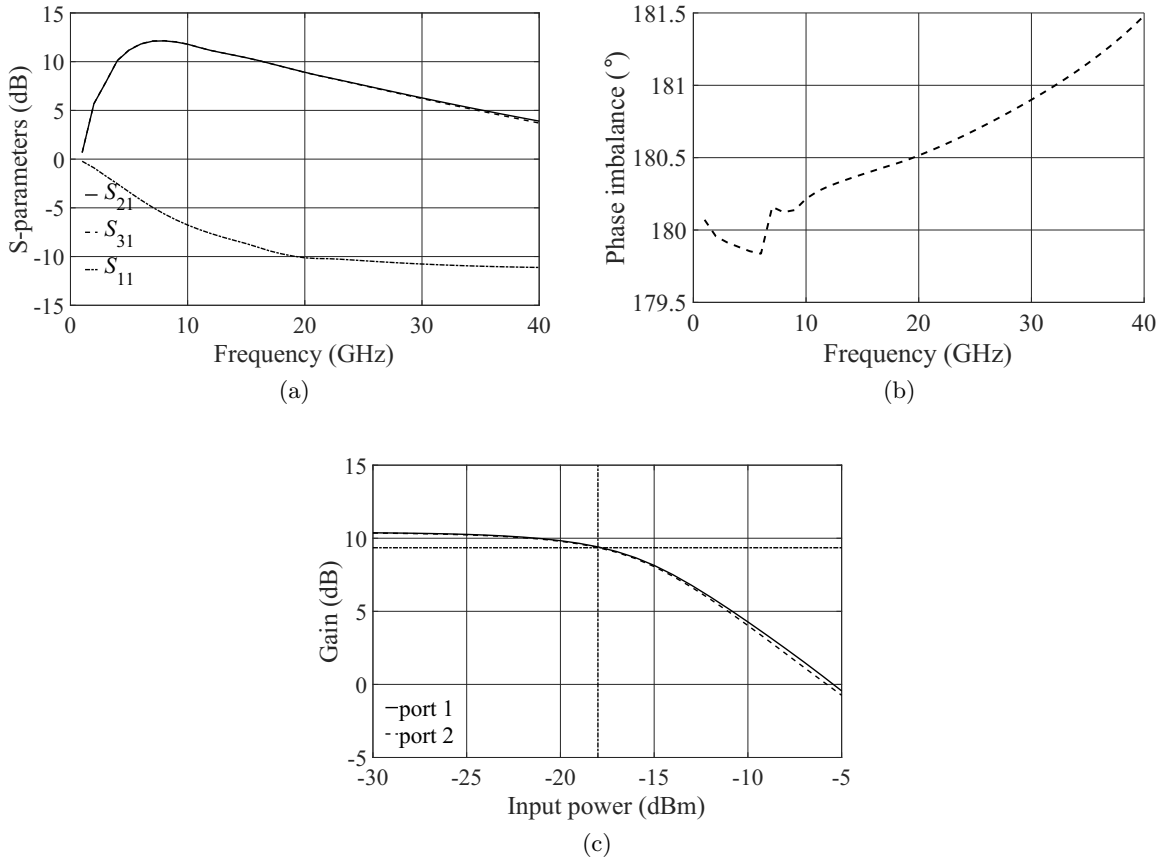


Figure 2.18: Simulated (a) S-parameters, output (b) phase imbalance, and (c) gain compression with 1 dB reference line (dash) at 15 GHz of the active balun.

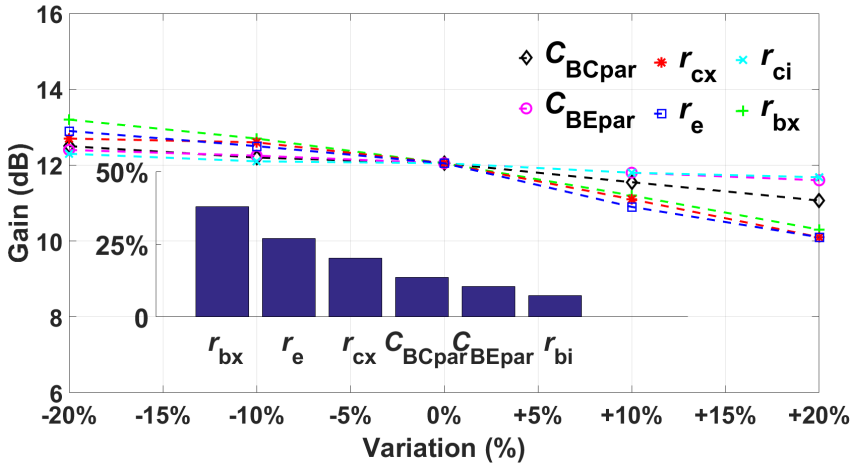


Figure 2.19: Sensitivity analysis of the gain of this active balun at 9 GHz with some important parameters varied ±20 %.

matching (T2). More importantly, less than 0.05 dB and 0.1° amplitude and phase imbalance are observed in Fig. 2.18a and 2.18b, indicating a low signal distortion. Meanwhile, Fig. 2.18c shows the gain compression at 15 GHz with the simulated 1 dB output/input compression point ($oP_{1\text{dB}}/iP_{1\text{dB}}$) of -8.7/-18 dBm. As shown, this designed active balun provides high insertion gain and low amplitude and phase imbalance over a wide frequency range, which is suitable

to generate the differential signal at low frequencies. All transistors (T4 and T5, T6 and T7) in the differential pairs is assumed to be identical during simulation, and the practical process variation may slightly increase the amplitude and phase imbalance.

The small-signal gain sensitivity of this designed active balun is analyzed by varying parameters by ±20 % at 9 GHz, as presented in Fig. 3.46c. Here, the transistor resistances and capacitances are included. For this active balun, the external base resistance R_{bx} shows the greatest impact of around 31 %. Additionally, the emitter resistance R_e, external collector resistance R_{cx}, base-collector parasitic capacitance C_{BCpar}, base-emitter parasitic capacitance C_{BEpar}, R_{ci}, with the impacts of 21 %, 16 %, 10 %, 8 %, 5.5 %, respectively.

2.2.3.2 Passive Balun

As the frequency increases to several tens of GHz, the operation of active baluns with good performance is tricky due to the noticeable inherent parasitics of transistors, and instead, the passive balun then becomes suitable. Notice that the size of a passive balun also becomes compact at higher frequencies since it is somewhat proportional to wavelength. Here, the planar Marchand balun is a popular type as it provides broadband performance and easier integration into circuits. Composed of two coupled-line sections, a Marchand balun can be achieved by different coupling structures, such as multilayer [49], broadside [50], or spiral-shaped [51] coupling.

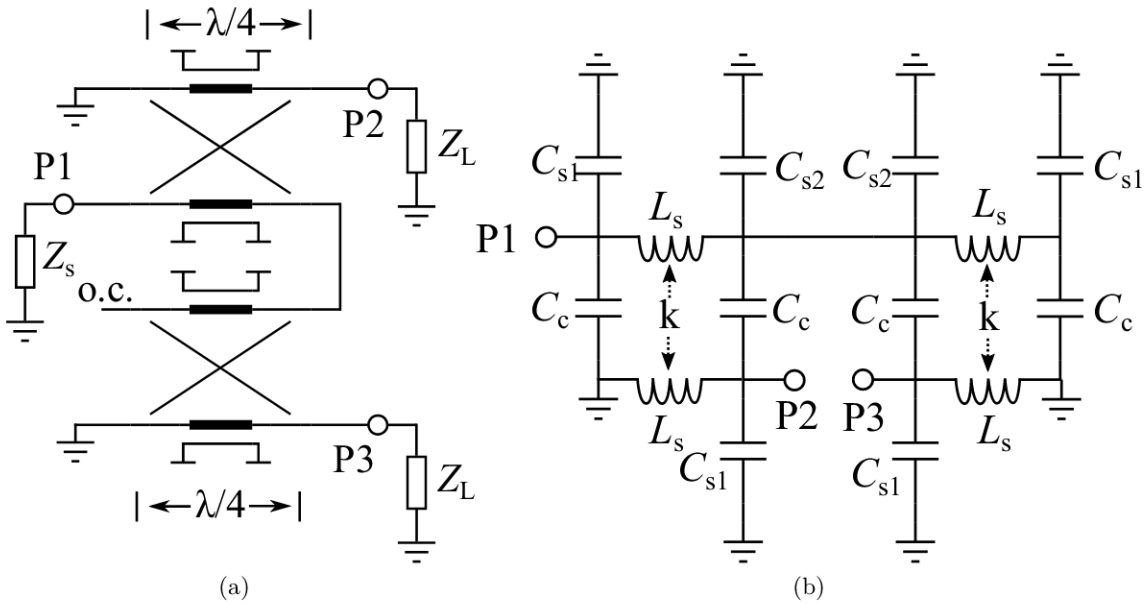


Figure 2.20: (a) Schematic, and (b) first-order lumped element equivalent circuit of the Marchand balun.

The schematic diagram of Marchand balun is presented in Fig. 2.20a. Similarly, this balun also offers two differential signal ports (P2 and P3) driven by the signal-ended one (P1), together with the impedance transformation between source and load impedance Z_s and Z_L. Based on equation 2.14, the ideal passive balun should provide -3 dB gain (power splitting) with identical amplitude but 180° phase difference. To achieve the desired performance of the balun, the careful design of the coupled-line section is the key. For a given impedance transformation ratio (Z_L/Z_s), the coupling factor C of the coupled-line section can be expressed as [52]

$$C = \frac{1}{\sqrt{2Z_L/Z_s + 1}}. \tag{2.17}$$

Then, the even- and odd-mode impedances of the coupled-line section can be easily determined by from C [52], as

$$Z_{oe} = Z_s\sqrt{\frac{1+C}{1-C}}, \tag{2.18a}$$

$$Z_{oo} = Z_s\sqrt{\frac{1-C}{1+C}}. \tag{2.18b}$$

For the sake of clarifying the relationship between the dimension and the even- and odd-mode impedance, a simplified first-order lumped element equivalent circuit of the Marchand balun needs to be introduced here [53], as presented in Fig. 2.20b, where L_s, C_s, C_c, and k are the self-inductance, capacitance to ground, mutual coupling capacitance, and mutual inductive coupling factor, respectively. Here, we assume that the balun is resistanceless and the capacitance to the ground is equally divided to both sides (C_{s1}=C_{s2}=C_s). By implementing the even/odd mode analysis on each coupled line section, the relations are as follows [54]:

$$L_s = \frac{Z_{oe}+Z_{oo}}{2\omega}, \tag{2.19a}$$

$$k = \frac{Z_{oe}-Z_{oo}}{2\omega L_s}, \tag{2.19b}$$

$$C_s = \frac{1}{\omega Z_{oe}}, \tag{2.19c}$$

$$C_c = \frac{1}{2\omega Z_{oo}} - 0.5C_s, \tag{2.19d}$$

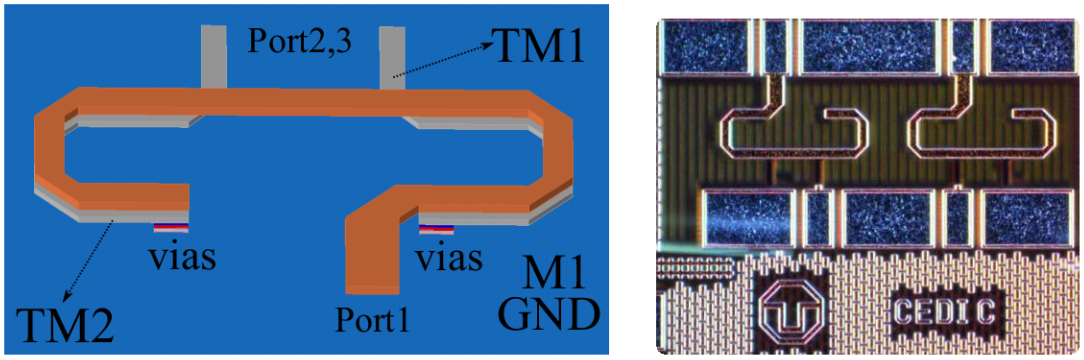
where ω is the angular frequency. Therefore, the coupling factor C of the balun can be finally determined by carefully tuning the physical dimension of each metal layer and the corresponding lumped element parameter.

A multilayer type 190 GHz Marchand balun was designed based on IHP SG13G2 technology. The impedance transformation ratio of 2, i.e., the 1:2 balun is generally chosen for the differential system. Based on equation 2.19, the parameters can be calculated as presented in table 2.1. As shown in the 3D view in Fig. 2.21a, this balun is implemented by two transmission lines

Table 2.1: Value of parameters for 1:2 balun at 190 GHz

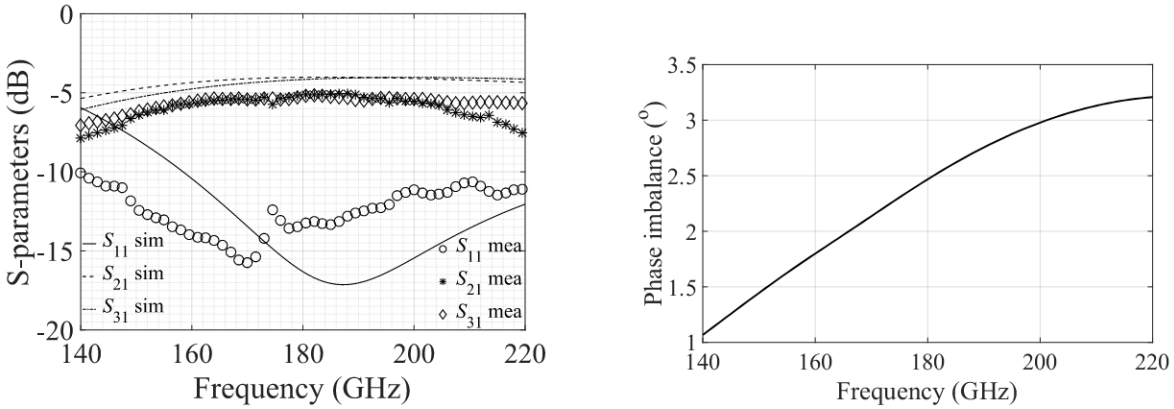
Z_{oe}	Z_{oo}	L_s	k	C_s	C_c
80.9 Ω	30.9 Ω	46.8 pF	0.45	10.35 fF	8.37 fF

in the two topmost metal layers, TM1 and TM2, to reduce the signal loss, and the bottom layer M1 is used as ground plane. Both lines are designed in a ring shape with the initial length of $\lambda/2$ in total (two pieces $\lambda/2$, as shown in Fig. 2.20a) to obtain L_s. The bottom line is shorted to ground. The C_c value is realized by the complete overlap of two lines. The final dimension of each line and connection port is optimized by EM-simulation for better matching and bandwidth performance. Fig. 2.21b shows the chip micrograph of the fabricated test balun. Since differential HF probes are unavailable at G-band, two identical baluns are separately fabricated, with one output port connecting to the pad and another terminated by a 50 Ω resistor. Additionally, the input and output port are extended with an extra 30 µm TL to widen the distance between two probes, which helps to reduce the mutual coupling. The total size of the balun is 90 µm × 200 µm. The measured and simulated insertion and return loss of the designed balun is presented in Fig. 2.22a. The minimum insertion loss of this balun



(a) (b)

Figure 2.21: (a) 3D view of the designed balun, and (b) micrograph of the balun test structure. The core area is 90 µm × 200 µm without pads.



(a) (b)

Figure 2.22: (a) Measured and simulated insertion/return loss and (b) simulated phase imbalance of the balun.

is measured to be 5 dB at 180 GHz. The overall insertion loss covering the entire G-band frequency range is less than 7.5 dB, with approximately 0.3 dB amplitude imbalance between two ports. Due to the incoherent measurement of this G-band balun, the phase imbalance can not be measured. Hence, only simulation results are shown in Fig. 2.22b and less than 4° is observed. The return loss is measured below 10 dB within the whole G-band, which indicates a good port match and broadband performance. The simulation agrees reasonably well with the measurement but with a 5 GHz shift towards lower frequency band. The observed around 1.2 dB higher measured insertion loss is partly due to the loss of RF pads (around 0.5 dB of each based on EM-simulation), and partly owing to the non-perfect 50 Ω termination.

2.3 Conclusion

The fundamentals in designing mm-wave low-power circuits and systems have been introduced in this chapter and will be used in circuit designs in the following chapters. Firstly, several different SiGe BiCMOS technologies with their features and layer information have been presented. Furthermore, the commonly used components in the following designs are also summarized, including GSSML, ZTL, active and passive baluns. The detailed studies of technologies and careful design of the above components are the key to proper operation and the first-pass success of circuits.

3 Low-power Low-noise Amplifiers

The low-noise amplifier (LNA) is a vital component as the first block of mm-wave and sub-mm-wave receivers [55–59]. In principle, a LNA should amplify the signal while introducing an acceptably small amount of noise. Thus, both gain and noise are the most critical performance parameters here, since the first-stage block typically determines the overall receiver noise, and a higher gain is always beneficial to improve the conversion gain (CG) of the system. On the other hand, an LNA also consumes a relatively large P_{dc} because of its multi-stages and required high RF gain. As a result, the top pursuit for low-power LNAs is to achieve the best possible trade-off between P_{dc} and other key performance parameters.

Several low-power SiGe HBT-based LNAs have been reported recently for mm-wave frequencies. In W-band, a 94 GHz LNA was designed with 10 dB gain, 6.3 dB NF, and 8.8 mW P_{dc} [60]; an 80 GHz LNA was reported with 20.5 dB gain, 6.2 dB NF and 16.6 mW P_{dc} [61]; a 75 GHz LNA was presented with 22 dB gain, 5 dB NF, and 8 mW P_{dc} [62]. In G-band, several amplifiers were designed in [63–66], with 10-20 dB gain and P_{dc} of 6.4-42 mW. However, those LNAs were designed by biasing the transistor close to peak f_T with negative V_{BC}, and the P_{dc} reduction methods of all amplifiers listed above were only achieved by transistor selection.

In this chapter, the design process of mm-wave low-power amplifiers is presented. Towards the best possible P_{dc}-performance trade-off, discussions contain the topology selection, transistor sizing, bias optimization, gain enhancement techniques, the experimental characterization and model related analysis. Moreover additional performance tuning capability is realized in one amplifier design, which is beneficial to system performance distribution and dynamic range extension. Two designs with state-of-the-art results are demonstrated, in particular, a G-band 173-207 GHz ultra-low-power amplifier using IHP SG13D7 technology [37], and a W-band 72-108 GHz low-power tunable amplifier based on IFAG B11HFC technology.

3.1 173-207 GHz Ultra-low-power Amplifier

This design was implemented in an experimental 130 nm SiGe BiCMOS process SG13D7 with peak f_T /f_{max} of 460/600 GHz. The process details were introduced in Section 2.1.4.

3.1.1 Topology Selection

The commonly utilized topologies for mm-wave amplifiers are the common-emitter (CE), the common-base (CB), and the cascode configuration [48], with the simplified schematics of the above three topologies presented in Fig. 3.1. Assuming a perfect impedance matching network at both input and output port, the maximum stable gain (MSG)/maximum available gain (MAG) is usually used to evaluate the amplification capability of different topologies, which is defined

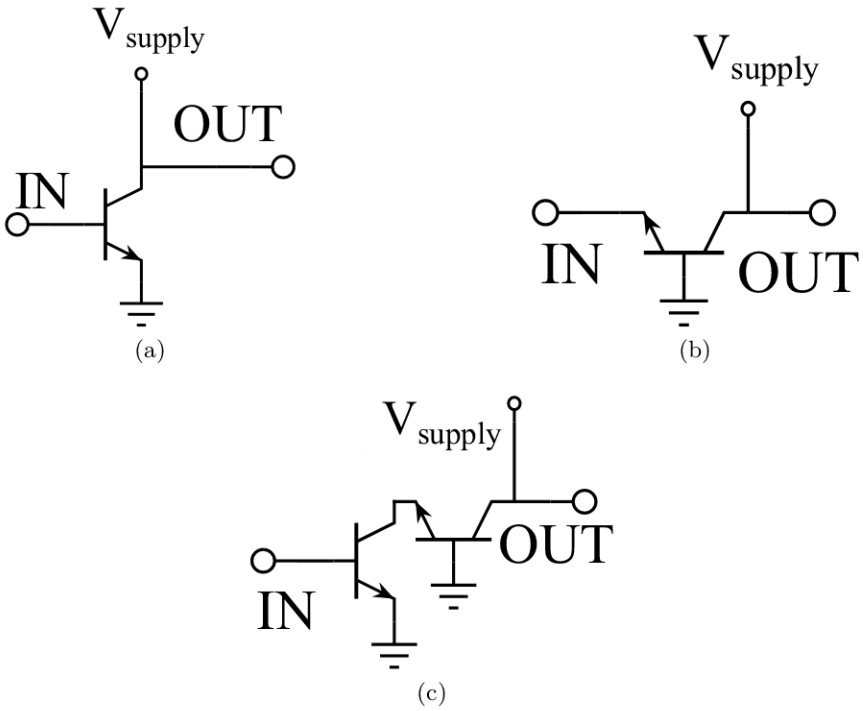


Figure 3.1: Commonly used mm-wave amplifier topologies: (a) CE, (b) CB, and (c) cascode. The DC bias and matching networks are omitted due to the simplification.

as

$$\mathrm{MAG} = \frac{|S_{21}|}{|S_{12}|}(k - \sqrt{k^2 - 1}), \tag{3.1a}$$

$$\mathrm{MSG} = \frac{|S_{21}|}{|S_{12}|}. \tag{3.1b}$$

where k is the stability factor [38], S_{21} and S_{12} are the S-parameters of the topology block. MAG is valid only if the block is unconditionally stable (k>1).

Fig. 3.2 and Fig. 3.3 present the simulated MAG/MSG, NF_{min}, and S-parameters (S_{12}, S_{11}, and S_{22}) for the three amplifier topologies up to 250 GHz. The transistor used in the simulation is in SG13D7 technology with two fingers (N_{x}=2, $A_{\mathrm{e\text{-}w}}$=2×1 µm×0.1 µm) and biased at the same J_{C} of 5.8 mA/µm^2. Although the device performance strongly relies on the transistor size and biases, such comparison of characteristics for different topologies remains similar. As demonstrated in Fig. 3.2a, the cascode topology offers much better gain of around 5-7 dB higher than the CB and CE topologies at 200 GHz, which is advantageous to reduce stage numbers for more compact chip size. Additionally, the S_{12} presented in Fig. 3.2c indicates significantly higher reversion isolation of the cascode topology. Nevertheless, the noise of the cascode cell is worse than that of the CE and CB types by around 1-1.5 dB at 200 GHz (cf. Fig. 3.2b). Meanwhile, the cascode stage requires a higher V_{supply} than CE and CB, directly leading to higher consumed P_{dc} at the same J_{C}.

The input and output impedance characteristics, S_{11}, and S_{22} of the three configurations, are shown in Fig. 3.3a and Fig. 3.3b. The input and output impedance of CE are close to the 50 Ω, which helps in realizing broadband performance and simplifying the matching network. For CB amplifier, the imaginary part of the output impedance is higher, which requires a much larger matching network for compensation. As a combination, cascode stage shows a similar input impedance as CE and output impedance as CB.

Finally, the cascode configuration has been chosen in these two amplifier designs in this thesis

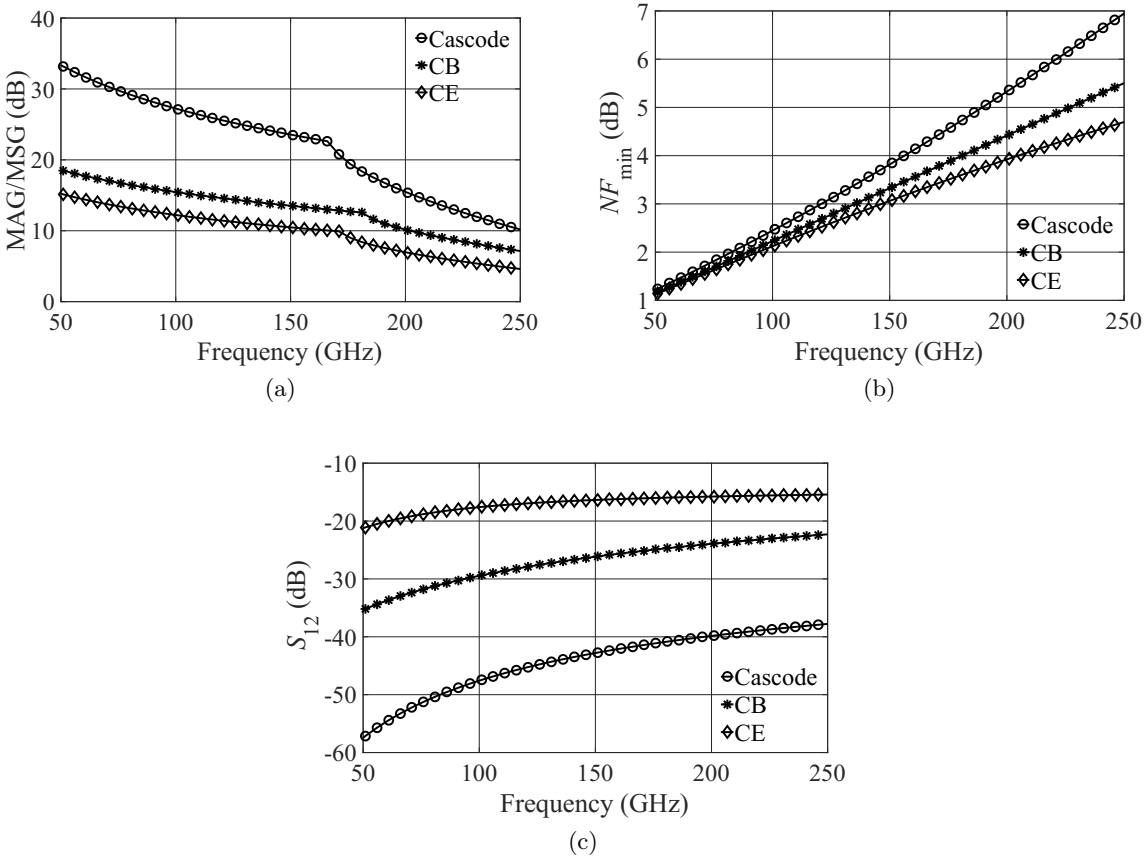


Figure 3.2: Simulated (a) MAG/MSG, (b) $NF_{\min}$, and (c) S_{12} for the three topologies: cascode, CB, and CE. The same double-finger (N_{x}=2, $A_{\mathrm{e\text{-}w}}$=2×1 µm×0.1 µm) SiGe HBT in SG13D7 technology is used for this comparison, with the same J_{C} of 5.8 mA/µm^2.

because of the following reasons:

- Capacitive feedback from output to input at high frequencies is minimized, thus increasing the isolation between different stages.
- Due to a much lower Miller-effect, the input capacitance C_{in} and corresponding input admittance of the cascode stage are reduced, making the inter-stage broadband matching easier [48].
- Much higher gain/stage can be achieved with acceptable NF.

3.1.2 Bias Dependency of the Small-signal Performance

Based on power level, the key performance parameters of amplifiers can be generally divided by small- and large-signal operation. The large-signal FoMs include linearity and maximum saturation power. The small-signal FoMs contain noise and gain. Stability is a common goal for both conditions. For LNAs, the small-signal FoMs are more critical due to its front-stage location, whereas the overall linearity and saturation power of a system are more or less dominated by the end stages, such as the IF buffer amplifiers in receivers.

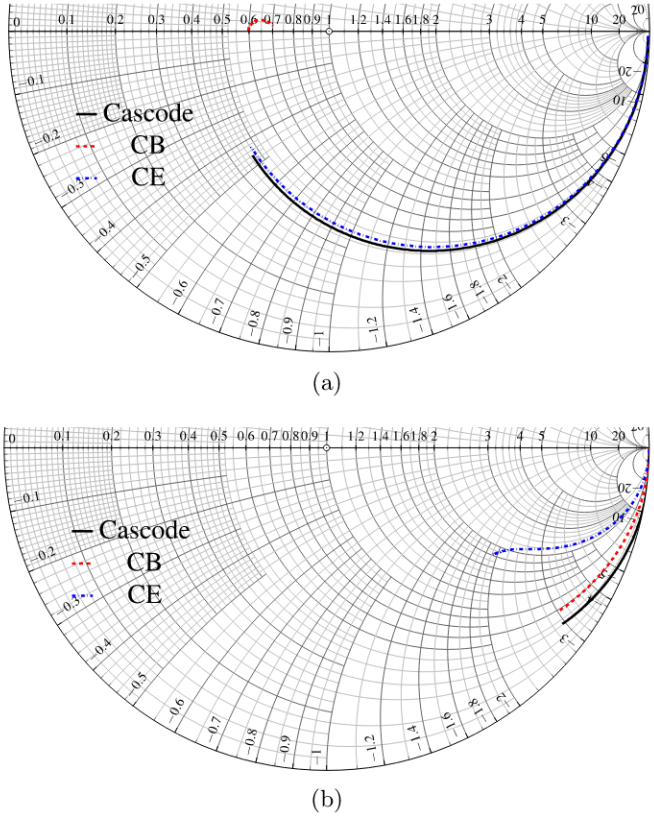


Figure 3.3: Simulated (a) S_{11}, and (b) S_{22} for the three topologies: cascode, CB, and CE. Simulation conditions are the same as Fig. 3.2.

3.1.2.1 Bias

For low-power mm-wave amplifiers, the first challenge is bias selection. Since the P_{dc} of an amplifier always links to V_{supply} and J_{C} (and in turn the collector current (I_{C})) of transistors, a better trade-off between performance parameters and lower P_{dc} requires a careful bias selection,by reducing either V_{supply} or I_{C} while keeping other essential performance competitive. Hence, for the cascode stage, the relationship between operation point and performance should be analyzed at first.

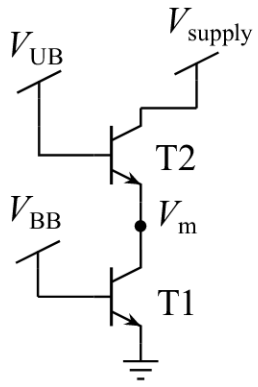


Figure 3.4: Schematic of the ideal cascode stage. The DC bias network is omitted here for simplification.

The simplified schematic of an ideal cascode stage with only DC bias node is presented in Fig. 3.4. There are three required biases in total, i.e., the supply voltage V_{supply}, the upper base

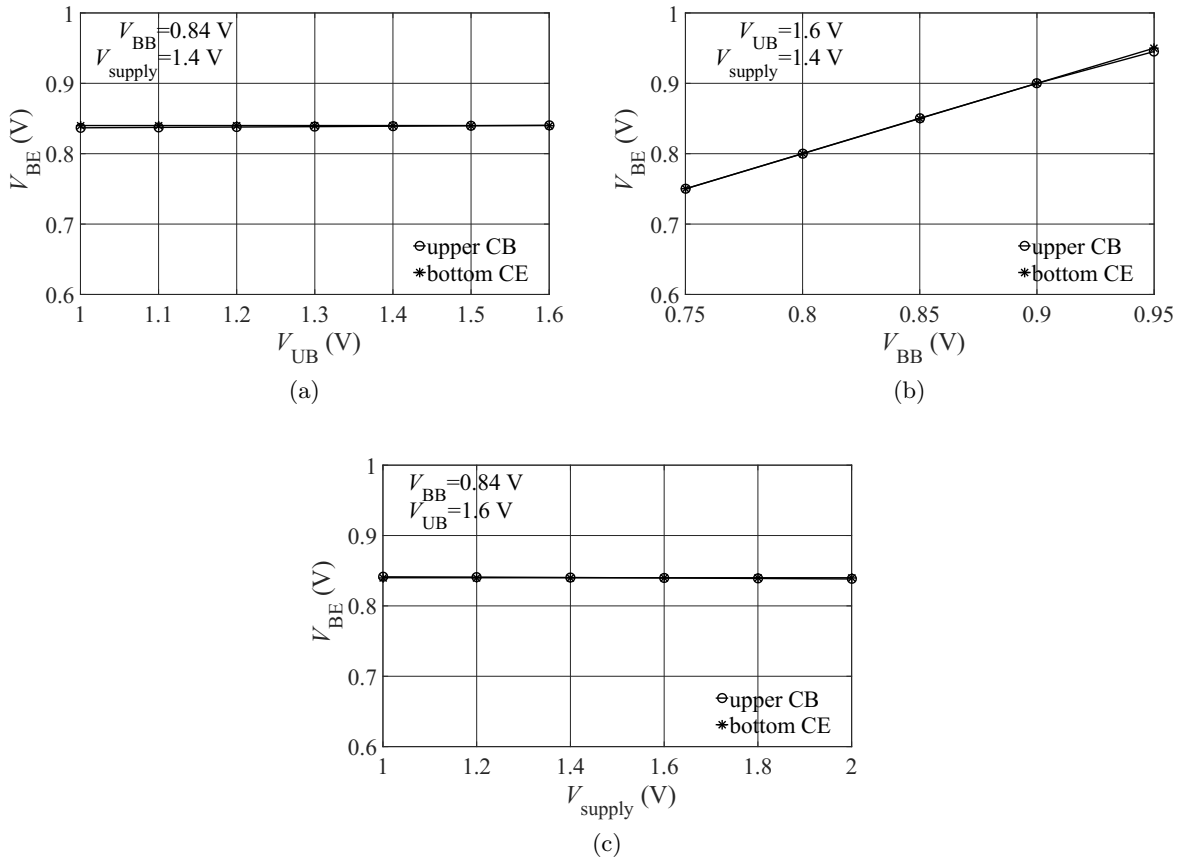


Figure 3.5: Operation point simulated actual V_{BE} of T1 and T2 in the cascode stage versus swept bias (a) V_{UB} from 1 to 1.6 V, (b) V_{BB} from 0.75 to 0.95 V, and (c) V_{supply} from 1 to 2 V. V_{UB}, V_{BB}, V_{supply} are biased at 1.6 V, 0.84 V, and 1.4 V, respectively, when they are not selected as the swept bias. The device size of the stage is the same as specified before, i.e., N_x=2, $A_{e\text{-}w}$=2×1 µm×0.1 µm.

voltage (V_{UB}), and the bottom base voltage (V_{BB}). For analysis reasons, the voltage at the node between T1 and T2 is defined as V_m. Here, T1 and T2 are selected with the same dimension for the simplification.

Fig. 3.5 presents the operation point (OP) simulation of the actual V_{BE} of T1 and T2 versus one of the cascode bias condition while keeping the other two constant. The OP simulation based on HICUM/L2 provides detailed information of the actual bias for each device. For the bottom CE device, $V_{BE,CE}$=V_{BB}. In addition, since the two transistors are stacked, the I_C and in turn J_C (with same device size) throughout the stage is identical. The dependency of J_C is shown instead of I_C, allowing an easier comparison between devices with different configurations and dimensions. First, the actual base-emitter voltage (V_{BE}) of the upper CB and bottom CE transistor are almost equal due to the shared collector current of two device, i.e., $V_{BE,CB}$≈$V_{BE,CE}$. In addition, $V_{BE,CB}$ and $V_{BE,CE}$ are mainly controlled by V_{BB}, given as $V_{BE,CB}$≈$V_{BE,CE}$=V_{BB} (cf. Fig. 3.5b), which is valid during each bias sweep. The slight variation might be due to the different high current effect caused by different actual collector-emitter voltage (V_{CE}).

Generally, for an HBT, V_{BC} is a significant parameter since it determines the operation region of the device [30], which is also directly related to V_{supply}. Assuming $V_{BE,CB}$=$V_{BE,CE}$, the bias

relation of the cascode stage can be expressed as

$$V_{\mathrm{BE,CB}} = V_{\mathrm{UB}} - V_{\mathrm{m}} = V_{\mathrm{BB}} = V_{\mathrm{BE,CE}}, \tag{3.2a}$$
$$V_{\mathrm{BC,CE}} = V_{\mathrm{BB}} - V_{\mathrm{m}}, \tag{3.2b}$$
$$V_{\mathrm{BC,CB}} = V_{\mathrm{UB}} - V_{\mathrm{supply}}. \tag{3.2c}$$

Then, V_{supply} can be described as

$$V_{\mathrm{UB}} = 2V_{\mathrm{BB}} - V_{\mathrm{BC,CE}}, \tag{3.3a}$$
$$V_{\mathrm{supply}} = V_{\mathrm{UB}} - V_{\mathrm{BC,CB}}. \tag{3.3b}$$

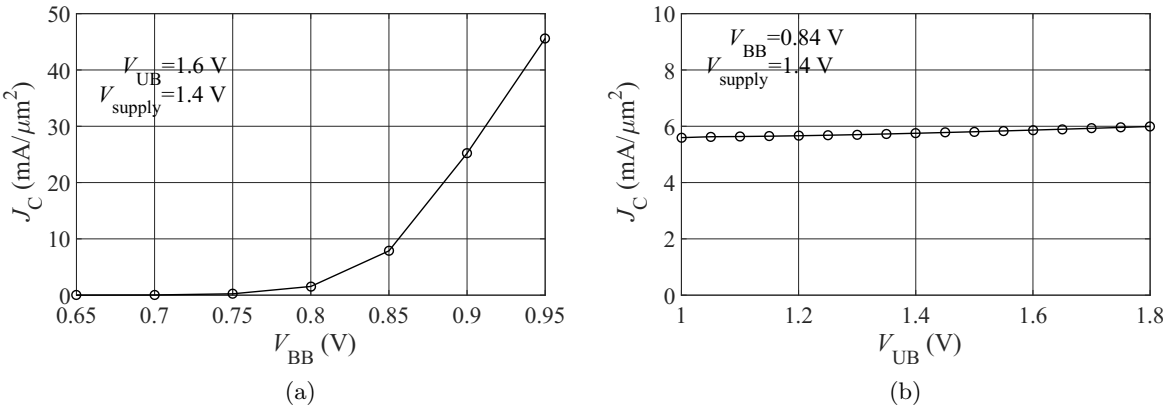


Figure 3.6: J_{C} versus (a) V_{BB} and (b) V_{UB} of the cascode stage, with the same V_{supply} of 1.4 V. Device size of the stage is the same as specified before, i.e., N_{x}=2, $A_{\mathrm{e\text{-}w}}$=2×1 µm×0.1 µm.

Fig. 3.6 shows the J_{C} versus V_{UB} and V_{BB} of the cascode stage. As shown, V_{BB} determines the actual V_{BE} of two transistors, and hence controls the J_{C} throughout the stage. Meanwhile, V_{UB} also slightly influences the J_{C} due to the variation of the actual V_{BC} (and in turn the Early effect) of two devices, as presented in Fig. 3.6b. Therefore, J_{C} and V_{BC} are two key bias parameters, and unless otherwise noted, the V_{BC} of two devices in the cascode stage in the following analysis is assumed to be equal for simplification.

3.1.2.2 Bias vs Gain

As the core performance of the amplifier, the relationship between gain and bias needs to be analyzed first. The simulated f_{T}, f_{max} and g_{m} as a function of J_{C} for various V_{BC} is demonstrated in Fig. 3.7. A double-finger device is used in the simulation. As seen, this transistor offers the simulated peak $f_{\mathrm{T}}/f_{\mathrm{max}}$ of 460/600 GHz at J_{C} around 30 mA/µm^2 with V_{BC} of -0.5 V. Besides, the collector current determines g_{m} and in turn f_{T} and f_{max}. In the J_{C} range up to around 20 mA/µm^2, g_{m}, f_{T}, and f_{max} are keeping increased with J_{C} and I_{C}, and the tendency of g_{m} agrees reasonably with the simulated f_{T} and f_{max} shown in Fig. 3.7a. Then, f_{T} /f_{max} reduce after J_{C} reaches high injection region, and the peak value comes out before reaching the peak g_{m} value as presented in Fig. 3.7b. Such fall-off towards high J_{C} is mainly due to high current effects leading to the significant increase of the minority charge and in turn τ_{f} (base storage time and collector storage time). Additionally, due to additional circuit-related capacitances, a higher g_{m} is more desirable than a higher f_{T}, especially for the operation at higher collector current densities.

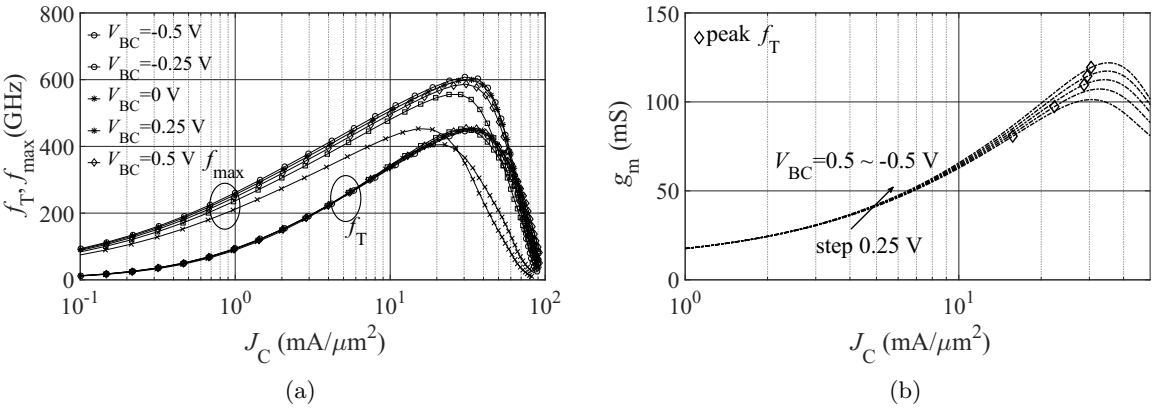


Figure 3.7: Simulated (a) f_T and f_{max}, and (b) g_m versus J_C with different V_{BC} from 0 to 0.5 V with the step of 0.25 V, for the transistor with the same finger number as specified before.

Additionally, the impact of V_{BC} on the RF performance of the transistor is equally essential. For the npn-HBT, V_{BC}<0 in forward active region offers better RF performance than that with the V_{BC}>0 in saturation region. As presented in Fig. 3.7a, from V_{BC}=-0.5 V until V_{BC}=0.25 V, the peak f_T/f_{max} decreases slightly. Then, a rapid reduction to 400/460 GHz at V_{BC} of 0.5 V is observed. Such performance decline with the increased V_{BC} is also mainly because of the high current effect, which results in the reduced I_C (g_m) and the τ_f.

The dependency between bias and gain of the cascode stage also follows with the device analysis above. The simulated MAG/MSG of an ideal cascode stage versus J_C with different V_{BC} at 200 GHz in Fig. 3.8. J_C and V_{BC} demonstrate similar impacts on MAG/MSG as device f_T /f_{max}, and their peak positions agree reasonably well.

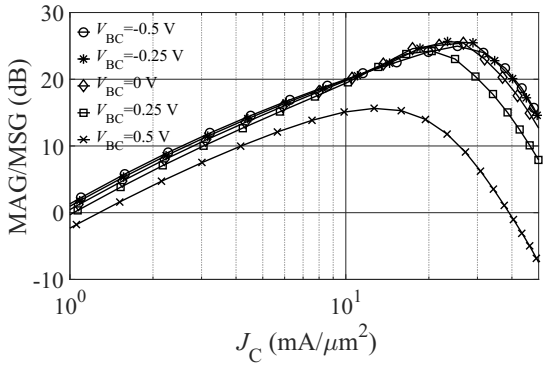


Figure 3.8: Simulated MAG/MSG of the ideal cascode stage versus J_C with different V_{BC} at 200 GHz. The device dimension is the same as specified before.

In summary, the cascode stage should be biased at the high J_C region close to peak f_T with negative V_{BC} for the best possible gain in general amplifier design, and P_{dc} can be saved by either reducing biased J_C or increasing V_{BC}, but with degraded RF gain as a sacrifice.

3.1.2.3 Bias vs Noise

Noise performance is another core FoM for the LNA. According to the Friis formula [48], the total noise factor of a cascaded system is mainly determined by the first-stage noise as long as the first-stage gain is high enough (usually higher than around 15 dB [67]) to compensate the

noise generated by the subsequent stages. Therefore, a good LNA requires both high gain and low NF.

The noise factor is defined as the degradation of the SNR, as

$$F = \frac{SNR_{\text{in}}}{SNR_{\text{out}}}, \tag{3.4}$$

Where SNR_{in} and SNR_{out} are the input and output signal-to-noise ratio (SNR), respectively. For an amplifier with power gain G in linear scale, the above two can be expressed as

$$SNR_{\text{in}} = \frac{S_{\text{in}}}{N_{\text{in}}}, \tag{3.5a}$$

$$SNR_{\text{out}} = \frac{S_{\text{in}} \cdot G}{N_{\text{in}} \cdot G + N_{\text{amp}}}. \tag{3.5b}$$

Here, N_{in} and S_{in} are the input noise and signal, and N_{amp} is the noise generated by the amplifier. Then, the NF_{min} of an amplifier in dB level becomes

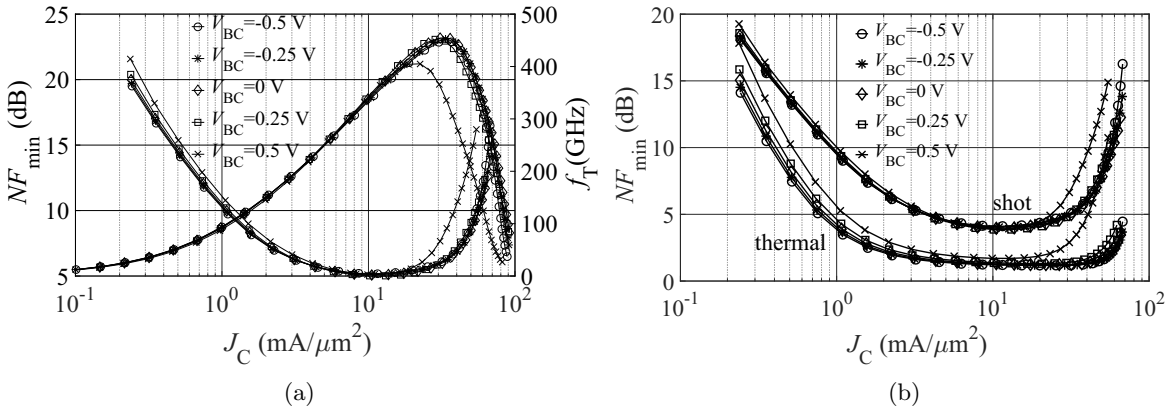
$$NF_{\text{min}} = 10log_{10}(1 + \frac{N_{\text{amp}}}{N_{\text{in}}G}). \tag{3.6}$$

As seen, a higher gain is also attractive for the noise reduction of the amplifier. NF_{min} is defined as the minimum available NF assuming perfect input and output matching networks. For a non-perfect source termination admittance Y_{s}=G_{s}+jB_{s}, NF becomes

$$NF = NF_{\text{min}} + \frac{R_{\text{n}}}{G_{\text{s}}}|Y_{\text{s}} - Y_{\text{nf,opt}}|^2, \tag{3.7}$$

where $Y_{\text{nf,opt}}$ is the optimal source admittance with perfect noise matching, and R_{n} is the noise resistance which is typically proportional to the total base resistance of the HBT. As shown, NF reduces to NF_{min} when Y_{s}=$Y_{\text{nf,opt}}$, and the ratio $R_{\text{n}}/G_{\text{s}}$ indicates the NF sensitivity, since it amplifies the mismatch effect of the source matching network. To achieve the lowest possible NF, both the lowest NF_{min} (contributed mostly by transistor sizing and biases) and perfect matching (determined by input noise matching network) are required. For device analysis, NF_{min} is discussed here at first.

The simulated NF_{min} as a function of J_{C} for an ideal cascode stage with various V_{BC} at 200 GHz is presented in Fig. 3.9a. Firstly, NF_{min} remains at a similar level with V_{BC} until



(a) (b)

Figure 3.9: Simulated (a) total NF_{min} with f_{T} of the HBT as references, and (b) NF_{min} with only shot or thermal noise contribution versus J_{C} with different V_{BC} of the ideal cascode stage at 200 GHz. Identical transistors sizes are selected as before.

0.25 V, then degrades rapidly with the further increase of V_{BC}, which agrees reasonably with the RF gain (f_T/f_{max} and MAG/MSG) variation shown before. However, the lowest NF_{min} of around 5.5 dB appears at J_C of around 15 mA/µm^2, which is only half of J_C for peak gain (f_T/f_{max}) shown in Fig. 3.7a and 3.8. This is mainly due to the significantly increased device noise with J_C in the high current region, which compensates the contribution of increased gain and degrade the overall NF performance, based on equation 3.6.

At mm-wave frequencies, the thermal noise of the device resistive components of the transistor and the shot noise dominate the overall noise of SiGe HBTs, and their actual contribution should be analyzed separately. Thanks to the advanced model HICUM/L2, the contribution of each noise source can be investigated separately by tuning on only the focused noise source, and the simulated NF_{min} with just thermal or shot noise tuned on is presented Fig. 3.9b. Since the shot noise is proportional to current, the transfer current from emitter to collector ($\approx I_C$) dominates the overall shot noise contribution due to its much larger amount. The noise spectral density can be expressed as [30]

$$\bar{I_T^2} = 2qI_T\Delta f, \tag{3.8}$$

where Δf is the frequency interval.

In HICUM, the ohmic-resistance-related thermal noise is modeled by the equivalent noise current source, and its noise spectral density can be described as [30]

$$\bar{I_r^2} = \frac{4k_BT\Delta f}{r}. \tag{3.9}$$

k_B, T are the Boltzmann constant and transistor temperature, respectively, and the r is the ohmic resistance value of each resistive component, including emitter resistance r_E, internal and external base resistance r_{Bi}, and r_{Bx}, as well as the external collector resistance r_{Cx}.

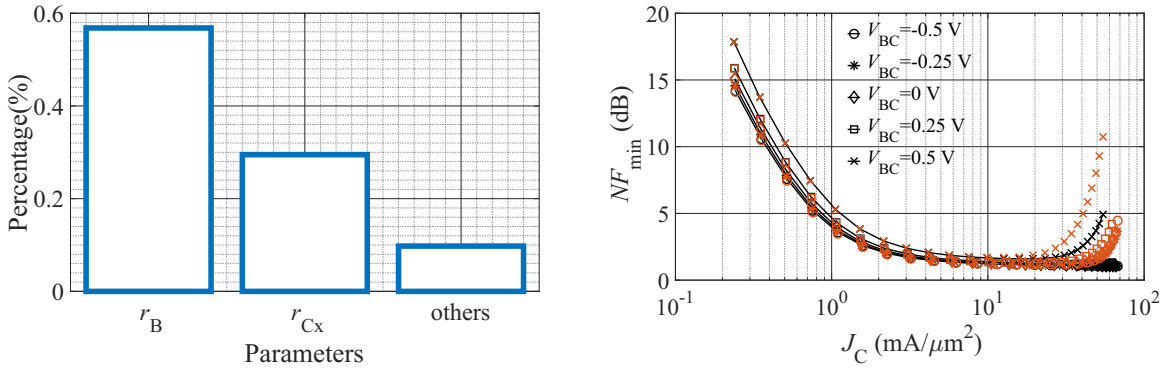


Figure 3.10: (a) Thermal noise contributions of each resistive component, and (b) thermal noise contributed NF_{min} with/without (symbols with lines/symbols) self-heating effect (flsh=1 or 0).

As presented in Fig. 3.9b, shot noise contributes more than 70% to the overall noise performance, whereas the thermal one brings 20%. Please notice that this ratio is technology-dependent. The much lower contribution of thermal noise might be due to the reduced base resistance in fabrication for high speed transistor in this specific technology. In general, an increasing transfer current density and J_C enhance the shot noise but also the gain via g_m before reaching the peak f_T. At the low injection region, the increase of g_m and the gain leads to shot-noise-related NF_{min} decreases with J_C. After the J_C of around several mA/µm^2, shot noise increases rapidly, thus the partial compensation of these two mechanisms results in a minimum NF_{min} which shifts with J_C also due to the strong bias dependent base-emitter diffusion

capacitance C_{dE}.

The total thermal noise is a weighted sum of the noise spectral density of each resistive component of the transistor. Similarly, by switching on one and off all other contributions in the HICUM model, the thermal noise generated by base resistance r_{B} (internal and external) as well as the external collector resistance r_{Cx} turn out to be the major portion, with 55% and 29% contributions, respectively, as shown in Fig. 3.10a. Here, r_{B} shows a higher impact because its noise contribution is amplified by the transistor, whereas the contribution from r_{Cx} is not amplified. Since the value of the series resistances is almost bias independent, the corresponding thermal noise contribution decreases with J_{C} due to the increased gain. Another important effect in high-current region is the self-heating, the impact of which on thermal noise is compared in Fig. 3.10b. With large J_{C}, the self-heating becomes considerable [68] due to the increasing temperature of the resistive components, thus introducing extra thermal noise, while the increase in C_{dE} and g_{m} cancel each other.

Apart from NF_{min}, the actual NF of the LNA is also influenced by the quality of the noise matching network. Since the optimum impedance point for the source and NF_{min} are usually different, the perfect gain and noise match can not be achieved at the same time. By careful selection of the transistor size, the position of these two points can be tuned closer, which simplifies the input matching network design. More details will be discussed later in the matching network design part.

3.1.2.4 Bias vs Stability

Stability is a core concern in amplifier design, because the potential oscillation will lead to a huge degradation of the amplifier performance. More importantly, the unstable operation will make the amplifier no longer predictable and controllable. The instability issue comes from the negative input and output impedance of the active components, i.e., negative $\mathrm{Re}\{Z_{\mathrm{in}}\}$ and $\mathrm{Re}\{Z_{\mathrm{out}}\}$, due to the corresponding reflection coefficient Γ_{in} and Γ_{out} higher than unity [69]. In contrast, the passive networks is always stable because their Γ is less than 1. The investigation of stability relies on S-parameters. Both active and passive components can be represented by a 2-port S-parameter network, with

- S_{21}: Forward transmission, with $S_{21}>1$ for active devices as gain and $S_{21}<1$ for passive components as loss.
- S_{12}: Reverse transmission, as the reverse isolation from output to input.
- S_{11} and S_{22}: input and output reflection.

For the bilateral device with $S_{12} \neq 0$, Γ_{IN} and Γ_{OUT} are described as [70]

$$\Gamma_{\mathrm{IN}} = S_{11} + \frac{S_{12}S_{21}\Gamma_{\mathrm{L}}}{1 - S_{22}\Gamma_{\mathrm{L}}}, \tag{3.10a}$$

$$\Gamma_{\mathrm{OUT}} = S_{22} + \frac{S_{12}S_{21}\Gamma_{\mathrm{S}}}{1 - S_{11}\Gamma_{\mathrm{S}}}. \tag{3.10b}$$

The network is unconditionally stable if both the $|\Gamma_{\mathrm{in}}|$ and $|\Gamma_{\mathrm{out}}|$ of an active component are smaller than 1 for all frequencies. Otherwise, it becomes conditionally stable (or potentially unstable), and the stabilization is only valid for certain impedance values of the load and source terminations. In the general amplifier design, the instability risk must be avoided by ensuring $|\Gamma|<1$, and unconditionally stability is highly recommended in order to minimize the potential risk of inaccurate simulation and fabrication variation. Obviously, to keep $|\Gamma_{\mathrm{in}}|$ and $|\Gamma_{\mathrm{out}}|$ small, good input and output matching for smaller S_{11} and S_{22}, a lower gain and a higher reverse isolation for smaller S_{12} and S_{21} are both required. Here, stability and high gain become a

conflicting target, and the reverse isolation can be enhanced by a cascode topology with a reduced Miller effect, as discussed in Section 3.1.1.

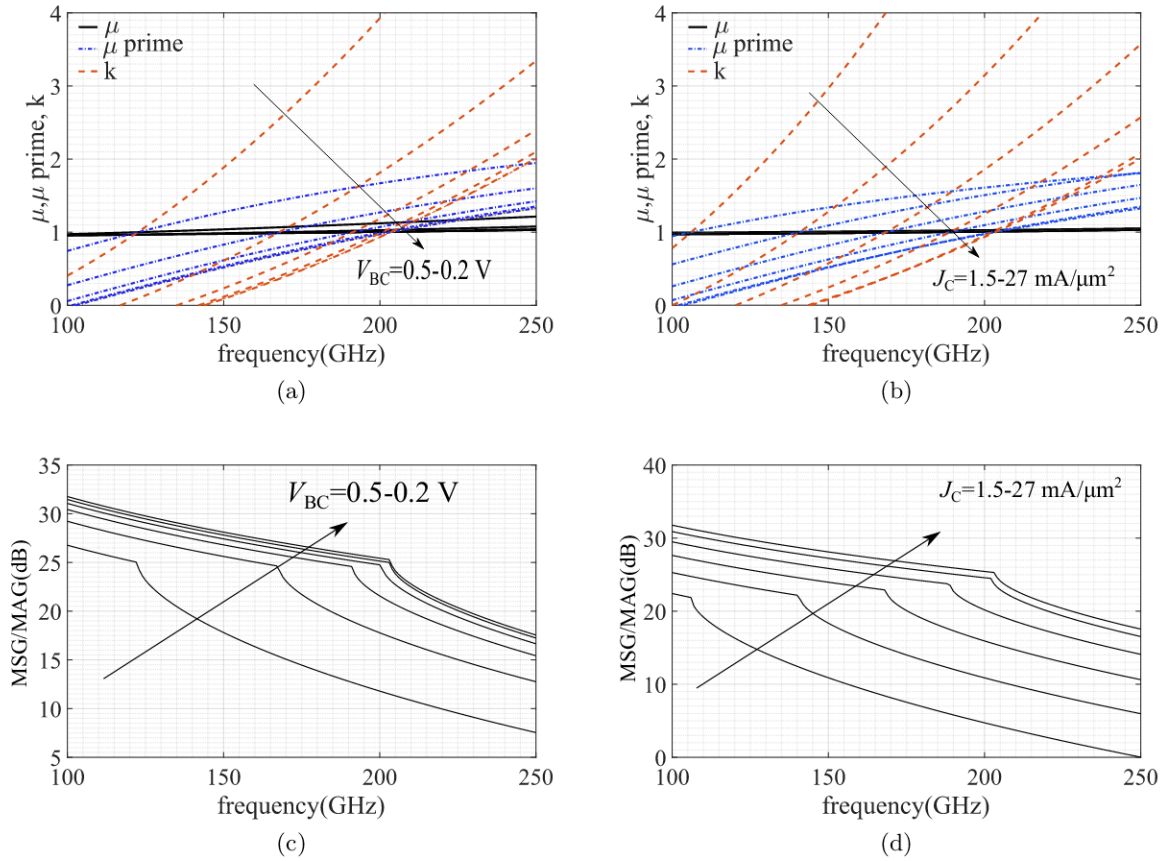


Figure 3.11: Simulated (a), (b) stability factor μ, μ', and k, and (c), (d) MAG/MSG of the ideal cascode stage versus frequency from 100 to 250 GHz with varied (a),(c) V_{BC}, and (b), (d) J_C. V_{BC}=0 V at J_C=27 mA/μm² are chosen with the other one sweeping. The device size of the stage is the same as specified before, i.e., N_x=2, $A_{e\text{-}w}$=2×1 μm×0.1 μm.

A traditional criterion for the stability condition is the k factor calculated by the S-parameters of the network, as [71]:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}, \tag{3.11a}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}. \tag{3.11b}$$

Here, the fulfillment of k>1 and $|\Delta|$<1 are simultaneously necessary for unconditional stability. However, the evaluations of multiple parameters covering a wide frequency range make the criterion a bit inconvenient. More importantly, the absolute value of the k factor does not provide a hint about the degree of stabilization as it offers only a limited physical insight. For example, k=0.7 and k=0.9 both mean a potentially unstable network, but we can not say 0.9 is more stable than 0.7. Instead, another approach using parameter μ or μ', which are defined as

[72],

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \Delta| + |S_{12} S_{21}|}, \tag{3.12a}$$

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^* \Delta| + |S_{12} S_{21}|}, \tag{3.12b}$$

is pursued. μ>1 or μ'>1 alone is sufficient for the unconditional stability of a network since μ>1⇔μ'>1 [71]. Meanwhile, μ and μ' describe the distance between the origin point of the Smith chart and the closest impedance point on the input/output stability circle, which indicates the degree of stability. Therefore, factors μ and μ' are used here for the dependency between bias and stability.

Fig. 3.11a and Fig. 3.11b display the stability factor μ, μ' as well as k versus frequency with swept J_C or V_{BC}. As presented, the intersection point between stability and instability of three factors coincide, i.e., μ=1⇔μ'=1⇔k=1. Besides, μ and μ' increase with frequency and V_{BC} but decrease with J_C, mainly due to the gain variation (S_{21}). Based on equation 3.12, a higher gain (S_{21}) decreases μ and μ' and in turn reduces the stability of the cascode stage. Meanwhile, the presented much larger variation of μ' than μ indicates that the output of the cascode stage is more difficult to stabilize than the input. Meanwhile, since MAG=MSG when k=1 (see equation MSG/MAG), the position of the intersection point between MSG and MAG shown in Fig. 3.11c and Fig. 3.11d turn out to be a good and fast indication of the stabilization check.

3.1.3 Bias selection and Device sizing

3.1.3.1 Bias Selection

As discussed before, gain and noise are a trade-off in the bias selection. In this technology, a J_C of 30 mA/µm^2 is necessary for biasing the device at around peak f_T position, whereas the minimum NF_{min} requires only 15 mA/µm^2. Since the increase of NF_{min} after the lowest J_C point remains slow for a quite wide J_C range until around 50 mA/µm^2 (cf. Fig. 3.9a), biasing LNAs close to peak f_T with a slightly higher NF_{min} of around 1-1.5 dB is still acceptable. On the other hand, since the gain performance of the amplifier in the mm-wave and sub-mm-wave range is very critical, achieving high enough gain becomes a priority while NF is usually regarded as the secondary goal. Therefore, most of the previously presented small-signal LNAs were biased close to peak f_T for maximizing their gain performance [63–66,73–76]. Unlike J_C, negative V_{BC} is advantageous both for gain and noise. Hence, all LNAs listed above are biased with negative V_{BC} in the forward-active region, while the saturation operation with forward-biased V_{BC} is generally discouraged because of the performance degradation.

The additional constraint of P_{dc} for low-power LNAs requires a substantial reduction of biased J_C or V_{supply}. According to equation 3.3, the V_{supply} of a cascode stage is determined by the base voltage of the bottom CE transistor V_{BB} and V_{BC} of both CE and CB transistors. Since the operation of SiGe HBTs up to moderately positive-biased V_{BC} does not necessarily lead to high injection and the significant excess charge in the collector, SiGe HBTs operating in saturation still offer several hundreds of GHz peak f_T even with reasonably positive V_{BC}. As shown in Fig. 3.7a, a peak f_T/f_{max} of around 430/580 GHz can be realized by biasing the device with a forward V_{BC} of 0.25 V. Even with a V_{BC} of 0.5 V, the device still offers the peak f_T/f_{max} over 400/560 GHz. This performance is still acceptable for the LNA at 200 GHz, but with significantly reduced V_{supply} and in turn P_{dc}. For the same J_C (V_{BB}=0.9 V) and assuming identical V_{BC} of two devices in the cascode stage, biasing at V_{BC} of 0.25 V instead of at -0.5 V leads to a f_T/f_{max} degradation of around 30/40 GHz, whereas the V_{supply} is significantly reduced from 2.8 V to 1.3 V. This can be directly transferred to less than half of P_{dc}. Additionally, as presented in Fig. 3.7a, the peak f_T/f_{max} shifts towards lower J_C region with positive V_{BC}, which

is closer to the minimum NF_{min} J_C point, and thus is better for noise-gain tradeoff.

However, the above P_{dc} reduction achieved by decreasing V_{supply} may not suffice because the J_C of the device even with the minimum emitter dimension (and in turn minimum I_C) at peak f_T is still high. Therefore, to further reduce P_{dc}, a further reduction of J_C is also required. Considering the impact of parasitics in mm-wave and sub-mm-wave range, LNAs with good performance are still feasible until the operating frequency grows up to around 2/3 of f_T [73]. Thanks to this advanced technology, by biasing two devices in the cascode stage at f_T of around 270 GHz, corresponding to a reduction of J_C from 30 mA/μm^2 to 6 mA/μm^2, the P_{dc} can be further decreased about 80%. In addition, compared to the region of the peak f_T, the dependency between f_T and V_{BC}, i.e., the f_T decline with positive V_{BC} is also somewhat alleviated, which makes the even larger forward-biased V_{BC} and in turn lower V_{supply} possible, as demonstrated in Fig. 3.7a.

Finally, in order to minimize P_{dc} while keeping competitive performance in terms of gain and noise, J_C of 6 mA/μm^2 and V_{BC} of around 0.2 V are selected for this low-power LNA, and the bias conditions of the cascode stage are selected as V_{BB}=0.84 V, V_{UB}=1.5 V, and V_{supply}=1.3 V.

3.1.3.2 Device Sizing

Device sizing is also critical in circuit optimization, which can be achieved by tuning emitter dimensions or transistor configurations. At the time of design, this technology provides only a single-finger device with an emitter area with $A_{e\text{-}w}$ of 1 μm×0.1 μm, but a larger area is available by duplicating the emitter finger with the same layout N_x times up to 10 (cf. Fig. 2.5).

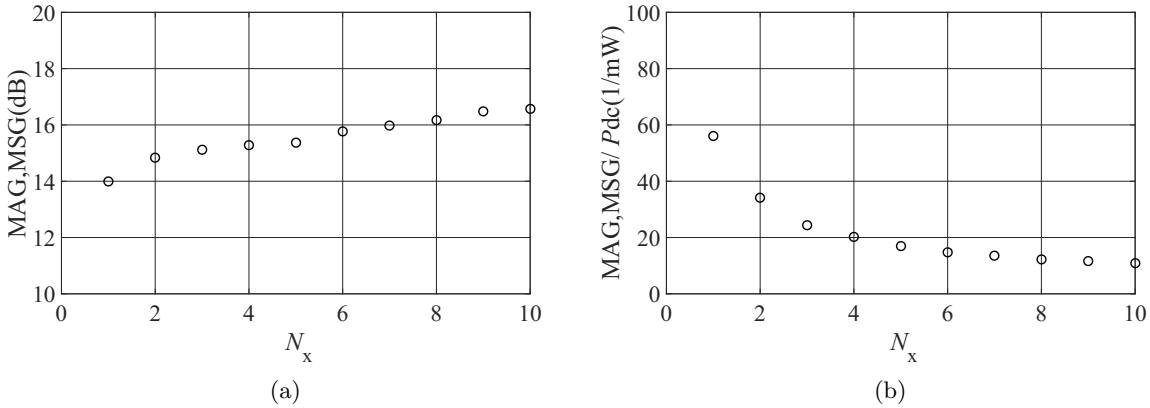


Figure 3.12: Simulated (a) MAG, MSG, and (b) (MAG, MSG)/P_{dc} of the ideal cascode stage with varied finger number N_x at 200 GHz with V_{BC}=0.2 V and J_C=6 mA/μm^2.

To find out the optimal size of the device for low-power amplifier design, the dependency of key parameters on N_x is significant. Unless otherwise noted, an ideal cascode stage with the same bias conditions chosen before is used, and the simulation frequency is fixed at 200 GHz. As long as the emitter is long enough, J_C at peak f_T is relatively independent of emitter length. Therefore, choosing devices with a larger N_x directly increases I_C and in turn P_{dc} with the same biased J_C and V_{supply}. Fig. 3.12a demonstrates the relationship between MAG/MSG and N_x. As shown, multiplying the finger number does not necessarily leads to a significant improvement of gain. The observed slight increase of gain with N_x may be due to the larger I_C caused g_m and smaller base resistance, yet is somehow compensated by the increased capacitances. The ratio of MAG/MSG to P_{dc} shown in Fig. 3.12b indicates the efficiency of amplification. The described much higher ratio obtained by the smaller transistors (N_x of 1 and 2) predicts a better trade-off between gain and dc power dissipation.

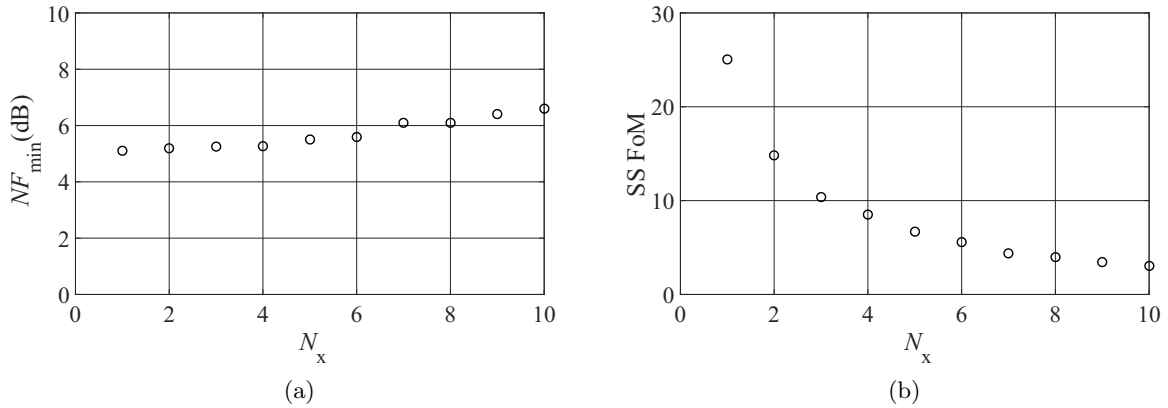


Figure 3.13: Simulated (a)NF_{min} and (b) small-signal FoM of the ideal cascode stage with transistors with varied finger number N_{x} at 200 GHz with V_{BC}=0.2 V and J_{C}=6 mA/µm^2.

The NF_{min} of the cascode stage with different device sizes is compared in Fig. 3.13a. Increasing the emitter length results in a weak increase of NF_{min}. Like f_{T}, NF_{min} is also dominated by J_{C}, and emitter length shows limited impact. Larger devices with reduced base resistance and in turn smaller contribution of thermal noise, and slightly higher gain also help in overall NF_{min} reduction. In contrast, multiplying the finger number N_{x} direct duplicate the I_{C} and the associated shot noise with the same factor. Such partial compensation finally results in a slightly increased NF_{min} with N_{x}, as shown in Fig. 3.13a. Taking noise into consideration, a reasonable small-signal(SS) FoM can be defined as

$$\text{SS FoM} = \frac{\text{gain}(1)}{(F-1)\cdot P_{\mathrm{dc}}(\text{mW})}, \tag{3.13}$$

and the smaller devices with N_{x} of 1 and 2 also illustrate a higher SS FoM, similar to the ratio of gain and P_{dc} shown in Fig. 3.12b.

The impact of device sizing on large-signal (LS) performance should still be analyzed although it is somewhat less significant for the LNAs as the first stage of the receiver chain. The P_{out}

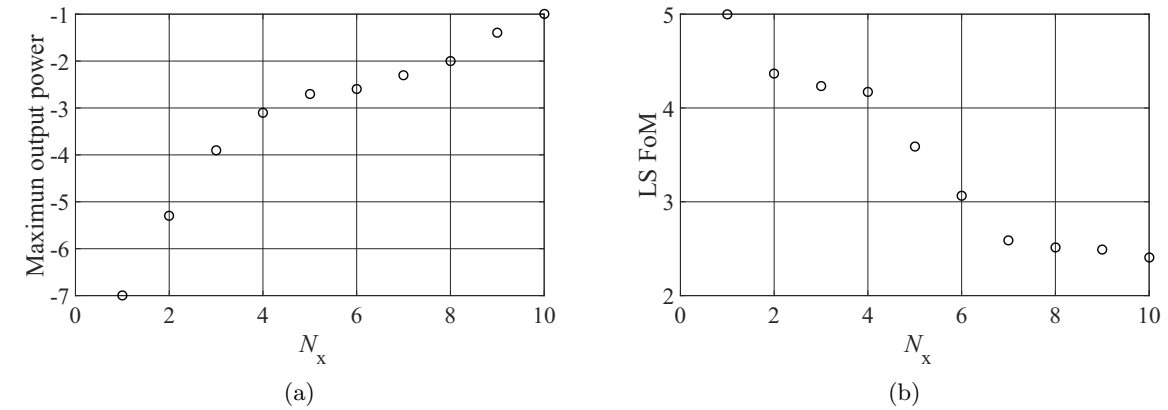


Figure 3.14: Simulated (a) maximum P_{out} and (b) large-signal FoM of the ideal cascode stage with transistors with varied finger number N_{x} at 200 GHz with V_{BC}=0.2 V and J_{C}=6 mA/µm^2.

level is highly related to the V_{supply} as well as I_{C} due to the provided voltage and current swing. Thus, the largest device (and in turn highest I_{C}) with negative V_{BC} is typically encouraged in power amplifier designs [77, 78]. For low-power circuits with positively biased V_{BC} and reduced V_{supply}, however, the maximum available P_{out} is indeed compromised. Biasing at forward V_{BC}, P_{out} can still be improved by enlarging I_{C} (larger device), as demonstrated in the comparison of maximum P_{out} shown in Fig. 3.14a. Based on the LS performance into equation 3.13, an LS FoM can be defined as

$$\text{LS FoM} = \frac{\text{gain}(1) \cdot P_{\text{out,max}}(\text{mW})}{(F-1) \cdot P_{\text{dc}}(\text{mW})}, \tag{3.14}$$

and the comparison is presented in Fig. 3.14b. Still, small transistors with N_{x} of 1 and 2 provides higher LS FoM and thus are recommended for low-power LNA design here in this work.

All discussions above only focus on the device and the cascode stage, under the assumption of perfect input and output matching. Theoretically, any impedances can be realized by matching networks. However, the practical circuit design should pay extra attention to the difficulty and quality of the matching network. Especially in the mm-wave frequency range, the realization of a good matching network becomes much more critical due to the noticeable losses and parasitics effects. Fig. 3.15 shows the basic block diagram of the amplifier including input and output

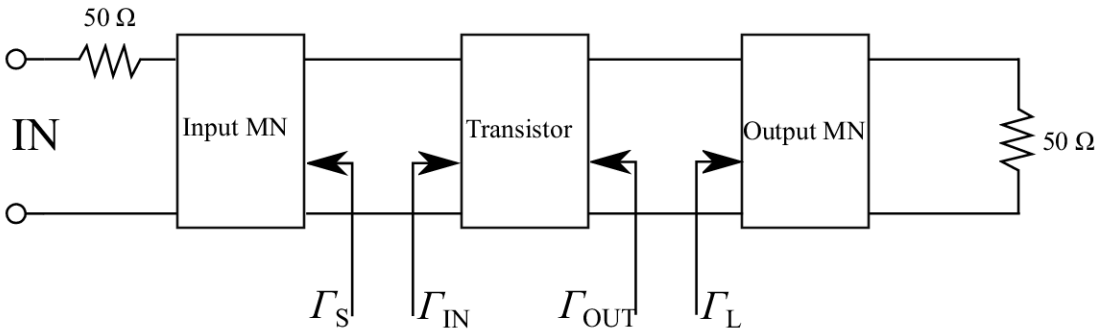


Figure 3.15: Block diagram example of the general amplifiers, MN: matching network.

matching networks, and Γ_{S}, Γ_{IN}, Γ_{OUT}, and Γ_{L} are the reflection coefficient looking into the source (to input matching network), the input of transistor, the output of transistor, and the load (to output matching network), respectively. Simultaneous conjugate matches, i.e., $\Gamma_{\text{S,opt}}=\Gamma_{\text{IN}}^{*}$ and $\Gamma_{\text{OUT,opt}}=\Gamma_{\text{L}}^{*}$, are necessary for achieving MAG/MSG shown before. Apart from the conjugate match, noise match at the input port is another key concern for LNAs. Recall equation 3.7, the noise performance reduces to NF_{min} only when $\Gamma_{\text{S}}=\Gamma_{\text{nf,opt}}$ ($Y_{\text{S}}=Y_{\text{nf,opt}}$). However, for most devices, $\Gamma_{\text{nf,opt}} \neq \Gamma_{\text{S,opt}}$, hence the perfect conjugate source match and noise match can not be achieved simultaneously. As a result, additional considerations for device sizing in terms of the matching network design are as follows:

1. Closer position between $\Gamma_{\text{nf,opt}}$ and $\Gamma_{\text{S,opt}}$;
2. Less mismatch sensitivity for input, output, and noise match networks;
3. Smaller physical size.

To begin with, the closer distance between $\Gamma_{\text{nf,opt}}$ and $\Gamma_{\text{S,opt}}$, the better gain and noise performance can be achieved simultaneously. Such distance can be adjusted by device sizing, and less mismatch sensitivity is an additional advantage here.

Besides, since the matching network is highly frequency-dependent, the perfect match is only valid for discrete frequency points. Then, the available bandwidth depends on mismatch sensitivity, especially for those frequency points away from the center. Meanwhile, a larger mismatch tolerance alleviates the crucial demand for the accuracy of EM simulation in high

frequencies. For example, a smaller total base resistance by choosing a larger transistor leads to a lower R_n and $Z_{S,opt}$, which in turn reduces the sensitivity both in input and noise match (see equation 3.7). Here, cutting down the impedance variation of the network is the key. Such variation includes the source match between system impedance (50 Ω) and first stage $Z_{S,opt}$, the load match between last-stage $Z_{L,opt}$ and 50 Ω, as well as the interstage match between front-stage $Z_{L,opt}$ and following-stage $Z_{S,opt}$. Notice that the real and imaginary portion of the impedance is of equal importance.

Furthermore, reducing the physical size of the matching network is encouraged for both compacting the circuit size and reducing the overall loss of transmission lines.

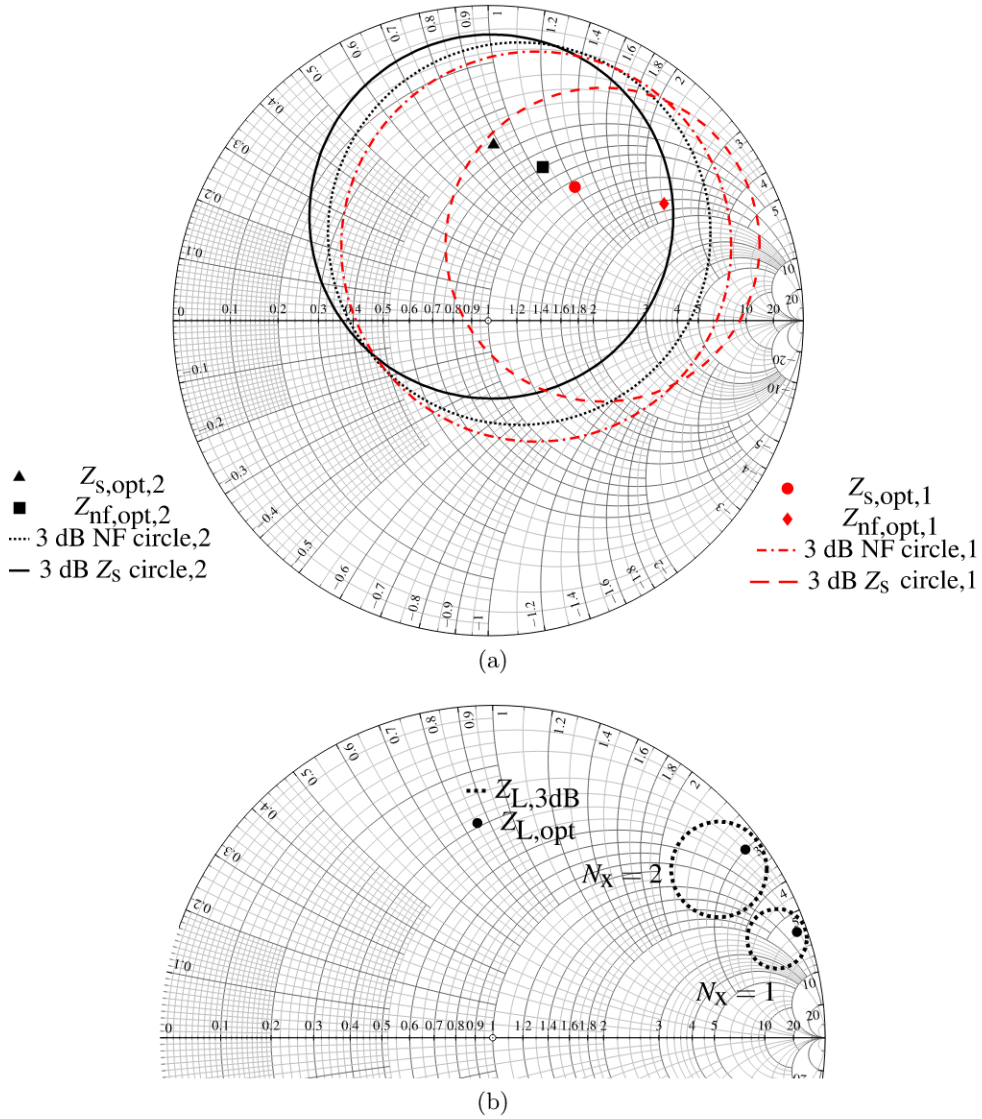


Figure 3.16: Simulated (a) $Z_{S,opt}$, $Z_{nf,opt}$ and (b) $Z_{L,opt}$ together with their -3 dB contours of constant gain/noise circle. The ideal cascode stage with transistors with N_x of 1 and 2 at 200 GHz is implemented with V_{BC}=0.2 V and J_C=6 mA/μm^2.

The simulated optimum source, load, and noise impedance of the ideal cascode stage with the device of N_x=1 and 2 are shown in Fig. 3.16. As seen, the real part of $Z_{S,opt}$ for both sizes is close to 50 Ω, while N_x=1 offers a slightly higher imaginary part. The $Z_{nf,opt}$ of N_x=1, however, is much larger than 50 Ω compared to that of N_x=2, both for real and imaginary part, mainly due to its larger series base resistance and smaller device capacitances (1/jωC). Meanwhile, the distance between optimum source and noise point for N_x=2 is closer to each other, and both of

them are closer to 50 Ω, which is advantageous for simplifying the input matching network.

To evaluate the mismatch sensitivity visually, the -3 dB constant gain/noise circle showing the loci of impedances with gain/noise 3 dB lower than the optimal value is generated in Fig. 3.16. The circle size represents the total number of impedances with gain/noise performance degradation less than 3 dB due to mismatch, and thus indicates the mismatch sensitivity and the difficulties of matching network realization. Obviously, the device with an N_x of 2 is a better choice in this work with less mismatch sensitivity of both source and noise. Similarly, the point and circle of the load match presented in Fig. 3.16b recommends N_x of 2 as the single-finger device has a fairly large imaginary part of output impedance. Therefore, the device with an N_x of 2 has been employed in this work.

3.1.4 Performance Enhancement Technologies

Fig. 3.17 presents the simplified circuit schematic of the proposed cascode stage utilized in this design. As can be seen, compared to the standard cascode stage shown in Fig. 3.1c, two

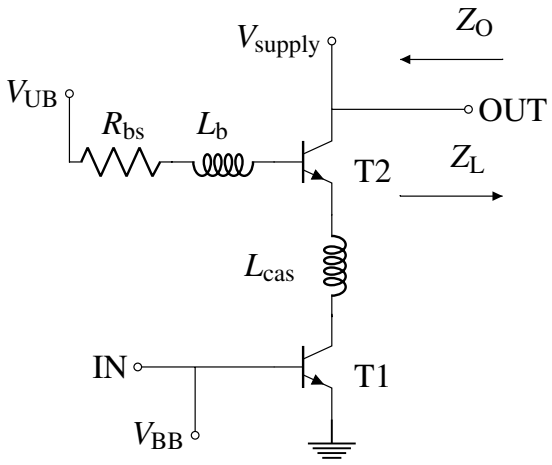


Figure 3.17: Simplified circuit schematic of the proposed cascode stage used in this design. The bias networks are omitted here.

inductors, L_b and L_{cas}, are added at the upper base and between two devices, respectively. Additionally, an extra resistance R_{bs} is implemented at the upper base in series of L_b. These additional passive components are utilized for the performance enhancement of the stage, and the details are discussed below.

3.1.4.1 G_m-boosting Inductors

As discussed in Section 3.1.2.2, due to the aggressively reduced J_C and V_{supply}, the transconductance g_m of the transistor is significantly decreased. As a result, the corresponding MAG/MSG of the standard cascode stage becomes insufficient and has to be improved by some specific measures. In this design, two G_m-boosting inductors, L_b and L_{cas}, are implemented simultaneously at the upper base and between emitter and collector of CB and CE transistors of the stage. As the name indicated, the main goal of the two inductors is to boost the small-signal short-circuit transconductance G_m of the stage and the MAG/MSG.

Unlike the g_m for the device, G_m focuses on the whole stage, which is defined as the ratio of output current i_{out} to the input voltage v_{in} under the situation of output short (zero output voltage v_{out}), as

$$G_m = \left.\frac{i_{out}}{v_{in}}\right|_{v_{out}=0}. \tag{3.15}$$

Based on the analysis in [48], the amplification of the cascode stage can be presented by the output loaded voltage gain v_g, which is approximately expressed as

$$|v_g| \approx G_m(Z_O \| Z_L). \tag{3.16}$$

Here, Z_L and Z_O are the load impedance and the output impedance looking from the load into the cascode stage, respectively. For a certain Z_L (usually 50 Ω), higher Z_O and G_m is encouraged for achieving v_g. The typical cascode stage enables higher gain mainly due to the increased Z_O compared to that of the CE stage by the factor β_0, which is the small-signal current gain of the bottom CE device, as

$$Z_{O,cas} \approx Z_{O,CE} \cdot \beta_0. \tag{3.17}$$

As a consequence, the stacked configuration [79], which includes one or even two extra CB transistors together with the standard cascode topology, enables a higher gain performance by further enhancing Z_O. However, this topology is not suitable here in this design due to the required higher supply voltage and in turn higher consumed P_{dc}. Instead, G_m has to be boosted in order to improve v_g without adding extra P_{dc}.

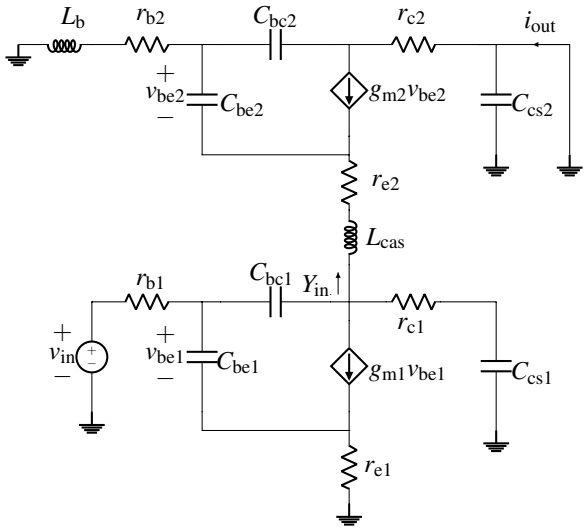


Figure 3.18: Simplified small-signal equivalent circuit of the gain cell with L_{cas} and L_b.

To evaluate the impact of the two inductors, a simplified small-signal equivalent circuit for the conventional cascode but with two inductors L_{cas} and L_b is presented in Fig. 3.18. Here, C_{bc}, C_{be}, C_{cs}, r_b, r_c, and r_e are the total base-collector, base-emitter, collector-substrate capacitance, total base, collector, and emitter resistance, respectively. The most important components are retained only in this equivalent circuit for analysis simplification.

Neglecting all the resistance elements and two inductors in Fig. 3.18, the G_m of the traditional cascode can be analytically described as

$$G_m = \frac{g_{m2}(g_{m1} - j\omega C_{bc1})}{g_{m2} + j\omega(C_{bc1} + C_{be2} + C_{cs1})}, \tag{3.18}$$

where ω is the angular operating frequency. Notice that at the bias conditions of selection, the exact V_{BC} of the CE and CB devices are slightly different, and the elements of the two transistors may also differ due to the variation of the fabrication process in practice, and thus are separately noted here. The impact of two the inductors are included separately, and adding

only L_{cas} to the expression modifies equation 3.18 to

$$G_m = \frac{g_{m2}(g_{m1} - j\omega C_{bc1})}{g_{m2}[1 - (\frac{\omega}{\omega_{r1}})^2] + j\omega[C_{bc1} + C_{cs1} + C_{be2}[1 - (\frac{\omega}{\omega_{r1}})^2]]}, \tag{3.19}$$

with

$$\omega_{r1} = \frac{1}{\sqrt{L_{cas}(C_{cs1} + C_{bc1})}}. \tag{3.20}$$

Compared to equation 3.18, a resonance at ω_{r1} has been introduced by L_{cas} into the denominator of equation 3.20. For sufficiently small values of L_{cas} (keeping $\omega_{r1}>\omega$), the resonance decreases the denominator and improves G_m and v_g. Including L_b and removing L_{cas}, the influence of L_b on G_m can be analyzed similarly, and equation 3.18 becomes

$$G_m = \frac{(g_{m2} + j\omega\frac{C_{be2}}{1-(\omega_{r3}/\omega)^2})(g_{m1} - j\omega C_{bc1})}{g_{m2} + j\omega[C_{be2} + \frac{C_{bc1}+C_{cs1}-(\omega/\omega_{r2})^2}{1-(\omega/\omega_{r3})^2}]}, \tag{3.21}$$

with

$$\omega_{r2} = \frac{1}{\sqrt{L_b(C_{be2} + C_{bc2})(C_{bc1} + C_{cs1})}}, \tag{3.22a}$$

$$\omega_{r3} = \frac{1}{\sqrt{L_b C_{bc2}}}. \tag{3.22b}$$

The detailed derivation of the equation 3.18-3.22 is shown in Appendix A. Since the G_m expression of the cascode with two inductors is complicated, the quantitative evaluation is necessary to observe their contributions. According to the OP check of the two transistors with the previously selected bias conditions using the HICUM model, the values of each element in the equivalent circuit can be extracted and listed in Table 3.1. Based on the listed parameter values, the $|G_m|$

Table 3.1: Value of parameters at selected bias conditions

g_{m1}	g_{m2}	C_{bc1}	C_{bc2}	C_{be2}	C_{cs1}
40.5 mS	48 mS	3.9 fF	4.05 fF	18.4 fF	2.7 fF

of the cascode stage with varying L_b and L_{cas} are calculated and compared to ideal cascode stage with the same two inductors using transistors with N_x=2 and selected bias conditions, as shown in Fig. 3.19. A resonance (peak) is observed in the numerical analysis of $|G_m|$ after adding L_b and L_{cas}, and the peak value shifts towards lower frequency with the increase of inductor values. By tuning the inductor values, the resonance peak can be adjusted close to the frequency of interest, enabling an improvement of $|G_m|$ by about a factor 3 (L_{cas}) and 1.5 (L_b). Similar trends are also seen by the simulated $|G_m|$ of the ideal cascode stage when varying two inductor values as presented in Fig. 3.19c and Fig. 3.19d. Therefore, the analytical calculation of equation (3.19) and (3.21) demonstrates a reasonable estimation and is a good starting point for parameter value selection.

3.1.4.2 Stability Enhancement

Since L_b at the upper base introduces positive feedback [80], a potential instability of the cascode stage becomes an essential issue and thus needs to be avoided by special measures. To explain the impact of L_b on the stability of the stage, the input admittance Y_{in} looking into the emitter of the upper CB transistor from the collector of the CE device can be expressed after neglecting

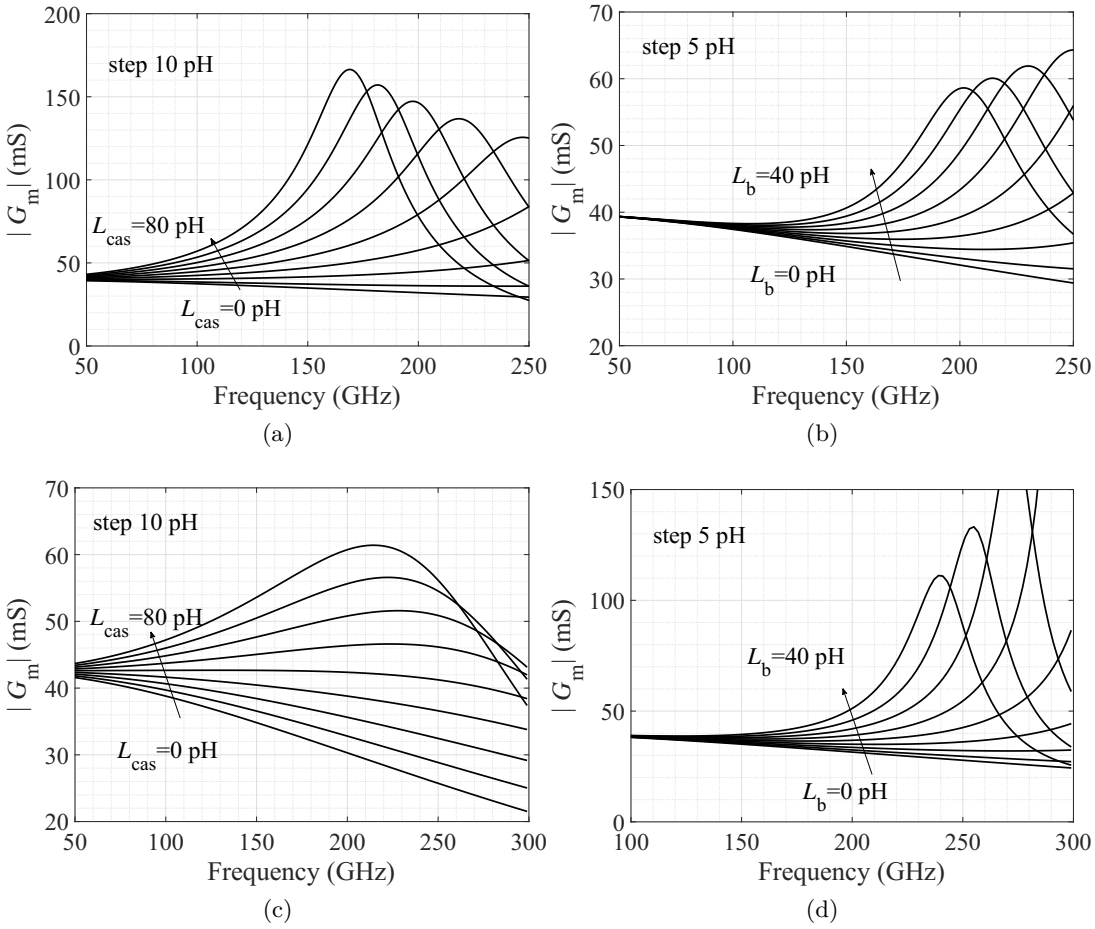


Figure 3.19: (a), (b) Calculated $|G_{\mathrm{m}}|$ based on equation (3.19) and (3.21) and (c), (d) simulated $|G_{\mathrm{m}}|$ for ideal cascode stage with L_{cas} and L_{b} varied from 0 to 80 pH and 0 to 40 pH, respectively.

the resistive elements in Fig. 3.18, as

$$Y_{\mathrm{in}} = \frac{(g_{\mathrm{m2}} + j\omega C_{\mathrm{be2}})[1-(\omega/\omega_{\mathrm{r3}})^2]}{1-(\omega/\omega_{\mathrm{r4}})^2}, \tag{3.23}$$

with

$$\omega_{r4} = \frac{1}{\sqrt{L_b(C_{be2}+C_{bc2})}}. \tag{3.24}$$

The boundary conditions of the real part of Y_{in} can be written as

$$\begin{cases} Re\{Y_{\mathrm{in}}\} \geqslant 0, & \omega_{\mathrm{r3}} \geqslant \omega_{\mathrm{r4}} \geqslant \omega \\ Re\{Y_{\mathrm{in}}\} \leqslant 0, & \omega_{\mathrm{r3}} \geqslant \omega \geqslant \omega_{\mathrm{r4}} \\ Re\{Y_{\mathrm{in}}\} \geqslant 0, & \omega \geqslant \omega_{\mathrm{r3}} \geqslant \omega_{\mathrm{r4}} \end{cases} \tag{3.25}$$

The detailed derivation of the above expression is shown in Appendix B. With the increase of L_{b}, $\mathrm{Re}\{Y_{\mathrm{in}}\}$ first becomes negative after the increased value of L_{b} making $\omega_{\mathrm{r3}}>\omega>\omega_{\mathrm{r4}}$, which indicates the potential instability. Then, $\mathrm{Re}\{Y_{\mathrm{in}}\}$ returns positive when L_{b} is large enough to make $\omega>\omega_{\mathrm{r3}}>\omega_{\mathrm{r4}}$. Based on the parameter values listed in Table 3.1, the boundary condition of L_{b} can be calculated at 200 GHz, as listed in Table 3.2. At around 200 GHz, L_{b} should be larger than 160 pH to fulfill the condition $\omega>\omega_{\mathrm{r3}}>\omega_{\mathrm{r4}}$. As demonstrated in Fig. 3.19, such value

Table 3.2: Calculated L_b for the boundary condition at 200 GHz

$\omega_{r3}>\omega_{r4}>\omega$	$\omega_{r3}>\omega>\omega_{r4}$	$\omega>\omega_{r3}>\omega_{r4}$
L_b <28 pH	28 pH<L_b <160 pH	160 pH<L_b

range is too large to boost G_m, which already leads to a rapid decrease after the resonance peak and thus is beyond the scope of this discussion. Therefore, L_b should be sufficiently small so that the condition $\omega_{r3}>\omega_{r4}>\omega$ is valid to enhance the gain and hence to make Y_{in} still positive.

In order to overcome the gain degradation due to the aggressively selected forwarded-biased V_{BC} as well as reduced J_C, the value of L_b requires careful selection, which makes the circuit stabilization critical. Meanwhile, the growing parasitic effects of vias and connections at such high frequencies introduce extra uncertainties in circuit stabilization. A small series resistor

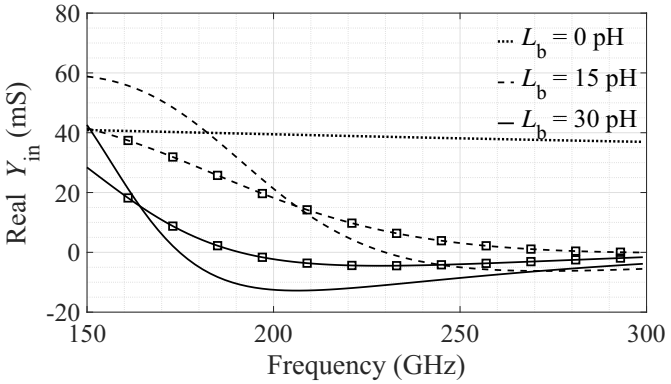


Figure 3.20: Simulated real part of Y_{in} versus frequency of the ideal cascode stage with L_b varied from 0 to 30 pH and with (marker) and without (line) R_{bs}=4 Ω.

after L_b at the upper base of the cascode stage is helpful to compensate for the negative Y_{in}. Fig. 3.20 demonstrates the simulated Re{Y_{in}} of the ideal cascode stage with L_b of 15 and 30 pH, and an apparent offset is observed after adding a small resistor of 4 Ω. Therefore, R_{bs} is added to mitigate the potential instability and thus to improve the tolerances during the fabrication process in this design.

3.1.4.3 Noise Improvement

As analyzed in Section 3.1.2.3, the transfer-current-related shot noise and the thermal noise of the resistive components (nearly 60% generated by the base resistance) are the main contributors in SiGe HBTs. Generally, the noise factor of the SiGe-HBT-based cascode stage can be approximately expressed as [81]

$$F = 1 + F_{CE} + (F_{CB} + F_{Rbsn})(1 + (\frac{\omega(C_{p1} + C_{p2})}{g_{m2}})^2). \tag{3.26}$$

Here, F_{Rbsn} is the noise term contributed by the R_{bs}. F_{CE}, and F_{CB}, respectively, represent the total noise factor of the CE and CB transistor. C_{p1} and C_{p2} represent the sum of parasitic capacitances at the collector of the CE transistor and the emitter of the CB transistor, respectively. As can be seen, adding extra resistance R_{bs} at the upper base introduces extra thermal noise of the upper CB device. Additionally, due to the increasing impact of the parasitic capacitances with frequencies (shown by ω), the overall noise from the CB transistor itself together with R_{bs} is further amplified by the term (C_{p1}+C_{p2}). Here, such noise amplification caused by

the parasitic capacitances can be fortunately reduced by the previously added L_{cas} by forming a resonance close to the operating frequency, and the optimum value of L_{cas} for the maximum noise reduction is [82]

$$L_{cas,opt} = \frac{C_{p1} + C_{p2}}{\omega^2 C_{p1} C_{p2}}. \tag{3.27}$$

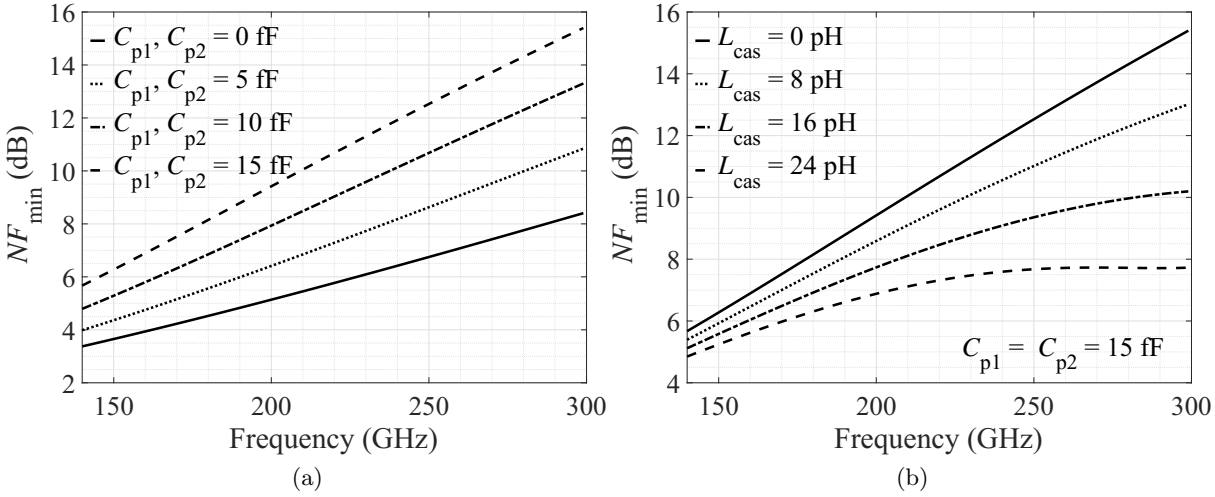


Figure 3.21: Simulated NF_{min} versus frequency for the ideal cascode stage with (a) C_{p1}, C_{p2} varied from 0 to 15 fF, and (b) L_{cas} varied from 0 to 24 pH with 15 fF for C_{p1} and C_{p2}.

With the same previously selected bias condition and device dimension, Fig. 3.21a presents the simulated NF_{min} of an ideal cascode stage after adding two varied capacitors at the upper emitter and lower collector representing the parasitic capacitances. The overall NF_{min} degrades with frequency, and around 4.5 dB degradation of NF_{min} is observed due to the introduced 15 fF C_{p1} and C_{p2}. The amount of such noise degradation also increases with frequency due to the ω in equation 3.27. In addition, the NF_{min} improvement by L_{cas} is shown in Fig. 3.21b, with a specific value of C_{p1} and C_{p2} (15 fF) but varied L_{cas} from 0 to 24 pH. At 200 GHz, approximately 3 dB NF_{min} can be compensated by the resonance of 24 pH L_{cas} with C_{p1} and C_{p2}.

3.1.5 Circuit Realization

3.1.5.1 Layout Scheme

The first step of circuit realization is the consideration of the layout scheme. In this technology, the topmost thick layer TM2 with 3 μm thickness is selected as the main routing layer due to its lowest sheet resistance and the lowest overall signal propagation loss at high frequencies. A thicker routing layer enables higher current density, which is also beneficial for large current circuit designs such as power amplifiers. Aiming for achieving the matching networks and connections with good properties, a large selectable characteristic impedance (Z_c) of the TLs is recommended to enlarge the degree of freedom during the wide-band matching network design [83]. Typically, the Z_c of the TL can be adjusted by tuning the ratio W/d, with W and d as the width and distance between signal and ground layer, respectively. For a specific technology, the number of the layer and the distance between layers is fixed. Therefore, d can be changed by choosing different ground and metal layers only. Meanwhile, the W range is also limited by the fabrication process. For instance, the selectable W range of TM2 is 2-30 μm due to the resolution (minimum) and local metal density (maximum). Using this range, the achievable Z_c

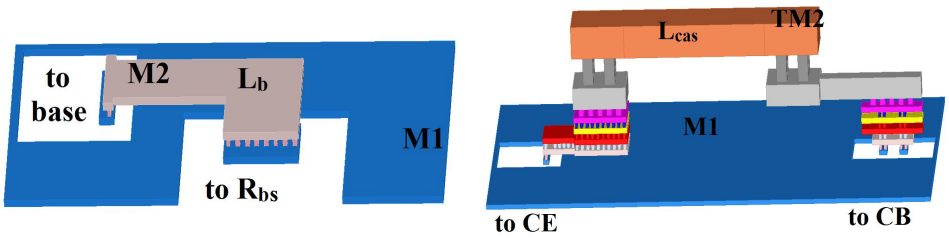
Table 3.3: Calculated Z_c range for MLs with different d

M1-TM2	M2-TM2	M3-TM2	M4-TM2	M5-TM2	TM1-TM2
36-108 Ω	35-101 Ω	34.5-98 Ω	33-94 Ω	30-89 Ω	18-65 Ω

range of the MLs with different d (choosing different ground layers) is summarized in Table 3.3. With a slightly higher minimal Z_c but a much larger maximal Z_c, M1 as ground metal layer provides the largest Z_c range and thus is implemented in this design.

3.1.5.2 Inductors Design

At the frequency of operation, the realization of lumped inductors with accurate inductor value and good performance is tricky due to the parasitics. Instead, a short piece TL with a specific length has become a popular solution for an on-chip inductor with a value of around several pHs. Notice that the parasitics, mainly introduced by the via transitions, have a significant impact at around 200 GHz. For example, in the process used here, a via transition from M1 to TM2 generates around 1-4 fF shunt capacitance, 2-5 pH series inductance, and a small series resistance around 1-4 Ω [74]. Such parasitics are already comparable with the target inductance value, and thus have to be taken into consideration by electromagnetic (EM) simulation during the design and optimization process.



(a) (b)

Figure 3.22: 3D view of (a) L_b and (b) L_{cas} together with via transitions.

Fig. 3.22 displays the 3D view of the two designed inductors with via transitions to the terminals (transistors or R_{bs}). As can be seen, two different metal layers are selected: M2 for L_b but TM2 for L_{cas}. Since L_b is very sensitive to circuit stabilization, introducing as few as possible parasitic effects is the key. The two terminals of L_b, i.e., the base of the upper CB device and R_{bs} located right below M1, choosing M2 as L_b helps to minimize the required via transition and its parasitics. On the other hand, due to L_{cas} placed in the collector current path, TM2 is selected for a high maximum current density and low loss (voltage drop). Their actual dimensions are optimized by EM simulation of the whole cascode stage, which contains the two inductors and all via transition structures.

The simulation of $|G_m|$ and the MSG/MAG of the complete cascode stage with various scenarios are demonstrated in Fig. 3.23. Due to the aforementioned severe parasitics involved by via transitions and connections of metal layers, the MSG/MAG of the complete stage degrades 6-8 dB compared to the ideal one, as presented in Fig. 3.23b. For this design, the gain degradation caused by the forward-biased V_{BC} and reduced J_C becomes more critical. Thus, particular emphasis on the enhancement of G_m and in turn MSG/MAG is required when selecting inductor values, whereas NF has lower priority. Here, L_{cas} is chosen at first with a relatively larger value,

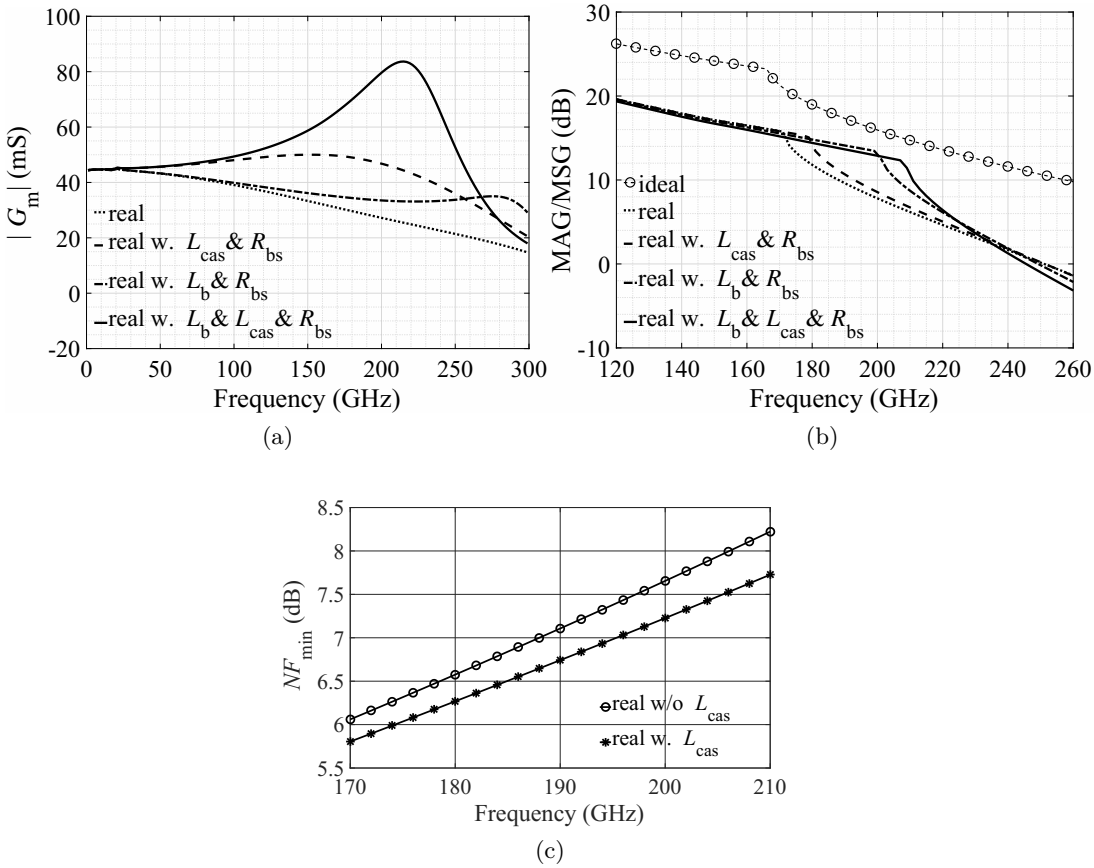


Figure 3.23: Simulated (a) $|G_m|$ and (b) MSG/MAG of the complete cascode stage with and without L_{cas}, L_b and R_{bs}, and (c) NF_{min} of the real stage with/without L_{cas} for noise optimization.

but L_b needs to be sufficiently small as it is sensitive to circuit stability. Meanwhile, the value of L_{cas} should also be as close as possible to $L_{cas,opt}$, and the overall goal is to adjust the $|G_m|$ peak at around 200 GHz, as presented in Fig. 3.23a. Eventually, the optimized L_b with 10 pH formed by M2 TL with 2 µm width and 35 µm length as well as L_{cas} with 21 pH by the TL of TM2 with 3 µm width and 35 µm length are selected, resulting in the improvement of $|G_m|$ from 27 to around 80 mS. Compared to the numerical analysis shown before, smaller values of two inductors are selected for the resonance at the frequencies of interest mainly due to the extra introduced parasitic capacitance. According to Fig. 3.23b, a significant enhancement by around 3 dB of the MSG/MAG of the complete stage is realized by implementing two inductors. Additionally, NF_{min} is improved (reduced) by around 1-1.5 dB by L_{cas}, as shown in Fig.3.23c. Notice that larger values of L_b and L_{cas} enable further enhancement of the gain at a higher frequency range but at the expense of extra measures for ensuring stability and an increase in noise figure. Furthermore, R_{bs} is selected as 4 Ω.

3.1.5.3 Dual-band Matching Network

A dual-band matching network is commonly utilized in the mm- and sub-mm-wave circuit design [65,66,84] for realizing wide-band performance, which achieves a much wider bandwidth due to its simultaneous match at two frequency points while keeping an acceptable mismatch inside the frequency band.

The simplified block diagram of A dual-band matching network is shown in Fig. 3.24a, which contains two L-type matching networks (TL1-TL2, TL5-TL6) at both sides and an impedance

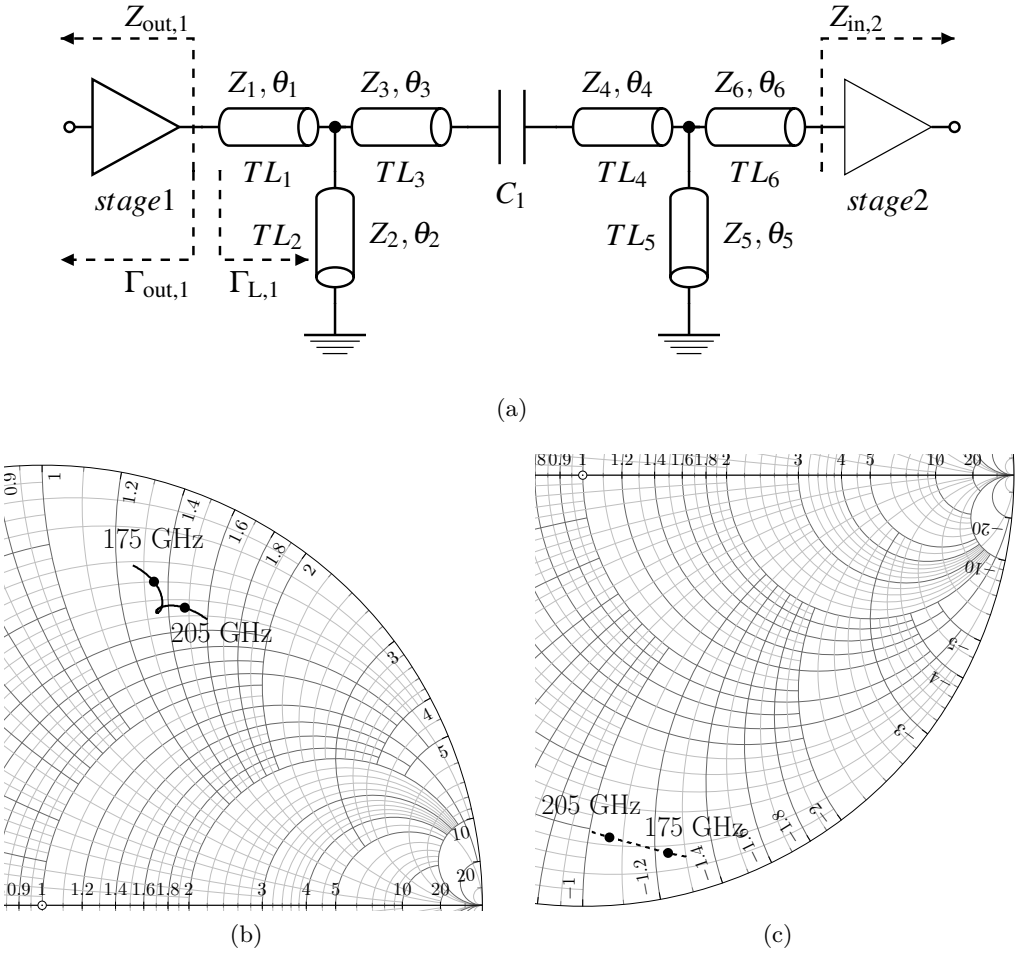


Figure 3.24: (a) Simplified diagram of dual-band inter-stage matching network, and Smith chart representation of (b) $\Gamma_{L,1}$ and (c) $\Gamma_{out,1}$, with the frequency range of 160-220 GHz. Dots represent values at frequencies 175 GHz and 205 GHz.

transformer including two series lines (TL3 and TL4) with varied Z_c in between. The reactance $\mathrm{Im}\{Z_{out,1}\}$ and $\mathrm{Im}\{Z_{in,2}\}$ is compensated by the closeby L-type networks, while the resistances $\mathrm{Re}\{Z_{out,1}\}$ and $\mathrm{Re}\{Z_{in,2}\}$ are matched by the transformer TL3 and TL4. As shown before, the output impedance (of the former stage) is relatively high, whereas the input one (of the subsequent stage) is low. Therefore, instead of a single piece of line, Z_3 and Z_4 of TL3 and TL4 are selected with a resistance value close to that of the respective stage, which helps to improve the impedance transformation of the resistive mismatch between stages.

EM-simulation using Momentum in Keysight Advanced Design System (ADS) is used in the matching network design and optimization. The Simulated $\Gamma_{out,1}$ of the complete stage and $\Gamma_{L,1}$ provided by the matching network are demonstrated in Fig. 3.24b and Fig. 3.24c. A practical trade-off here is the perfect conjugate match and loss of the network. Due to the relatively large magnitude of $\Gamma_{out,1}$, a larger size and more complicated network would be required for achieving the perfect conjugate matching, while the contribution will be almost compensated by the extra introduced line loss. Therefore, $|\Gamma_{L,1}| \approx 0.7\text{-}0.8$ is finally selected for the best available power gain.

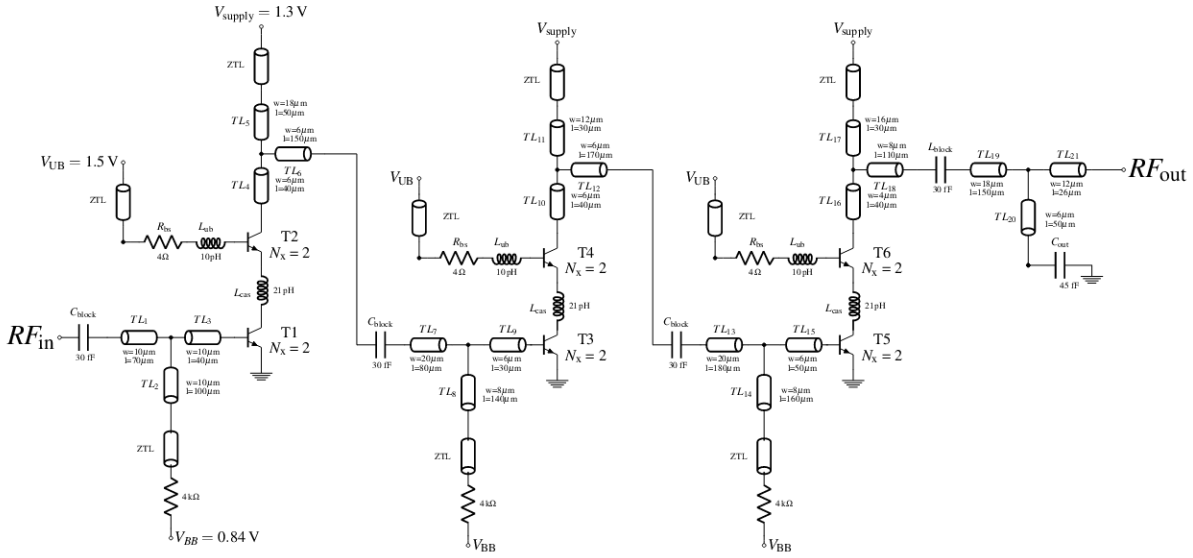
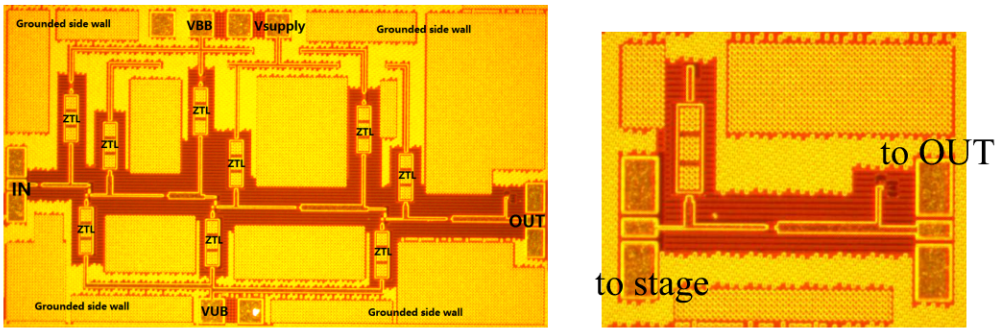


Figure 3.25: Circuit schematic of the amplifier, including the selected element values and dimensions of each TL.



(a) (b)

Figure 3.26: Micrograph of (a) the fabricated amplifier and (b) test output matching network. The chip size is 0.7 mm×1.5 mm, including pads.

3.1.5.4 Circuit Implementation

The complete schematic of the designed amplifier is displayed in Fig. 3.25. Based on the careful device analysis, the designed cascode stage using transistors with N_x of 2 provides a fairly close position of the optimum noise impedance and source impedance (for the conjugate match). As a result, the traditional T-type matching network is easily implemented here to save chip area. The dual-band matching is utilized both at inter-stage and output. The aforementioned ZTLs are simultaneously used after each shunt line (TL2, TL5, TL8, TL11, TL14, and TL17) as the AC ground with impedance close to 0. Grounded sidewalls are implemented to prevent the crosstalk inside the circuits. The micrograph of the fabricated amplifier is displayed in Fig. 3.26a. The total chip area is 0.7 mm×1.5 mm containing all pad structures. An output matching network block was fabricated also for performance verification, and the micrograph is presented in Fig. 3.26b.

3.1.6 Results and Discussions

3.1.6.1 Measurement Setup

This work was characterized on-wafer. A VNA (Keysight PNA N5242A) with VDI WR5.1 frequency extenders was employed for S-parameter and large-signal verification from 140-220 GHz. VDI Erickson PM5 power meter was utilized for power calibration loss characterization of the waveguide connections and probes. MMWAVE STUDIO was used to guide and automatically control the calibration and measurement process.

3.1.6.2 Measurement Results

Firstly, the S-parameter comparison of the fabricated output matching network is shown in Fig. 3.27, with all pad structures included. The displayed good agreement between measurement and simulation confirms the accuracy of the EM simulation and the proper operation of the designed matching network. The displayed slight discrepancy maybe due to the imperfect probe contact during the measurement.

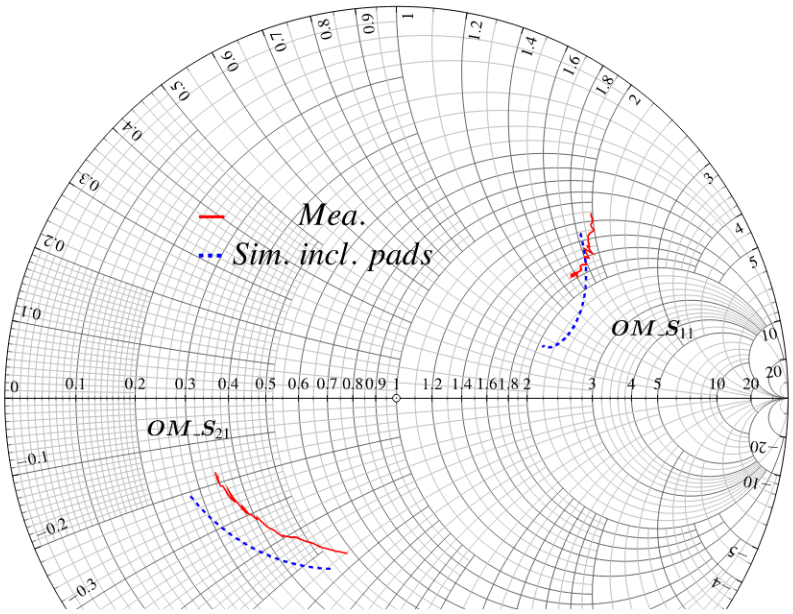


Figure 3.27: Measured and simulated S_{11} and S_{21} of the output matching network (OM) from 160 to 210 GHz, where ports 1 and 2 are connected with the third stage and output pad, respectively. Pads are included in the simulation.

Fig. 3.28a and Fig. 3.28b demonstrate the measured S-parameters of the circuit with four different bias conditions compared to the simulation results. With the V_{supply} of 1.3 V, V_{UB} of 1.5 V and V_{BB} of 0.84 V (V_{BC}≈0.2 V), this amplifier provides a peak power gain of 23.5 dB both at 179 and 203 GHz, while consuming only 3.2 mW static DC power. Thanks to the dual-band matching network, a 3 dB bandwidth of 34 GHz from 173 to 207 GHz is yielded. Maintaining V_{UB} and V_{BB} but reducing V_{supply} to 1.1 V (V_{BC}≈0.3 V), a peak gain of 21.3 dB at 183 GHz with a 3 dB bandwidth of 26 GHz from 178 to 204 GHz is observed with 2.7 mW DC power consumption. As shown, with a tuned V_{UB} of 1.3 V, this amplifier still offers 19.6 dB and 18.3 dB gain at 180 GHz and 175 GHz, respectively, with the aggressively reduced V_{supply} of 0.9 and 0.7 V (V_{BC}≈0.4 and 0.5 V), dissipating an extremely low DC power of 2.22 and 1.73 mW, respectively. The in-band measured input and output reflection coefficients S_{11} and S_{22} are observed to be below -8 and -5 dB, which indicate good input and output match. The below -35 dB S_{12} presents a good output-to-input isolation of this circuit. The overall simulation

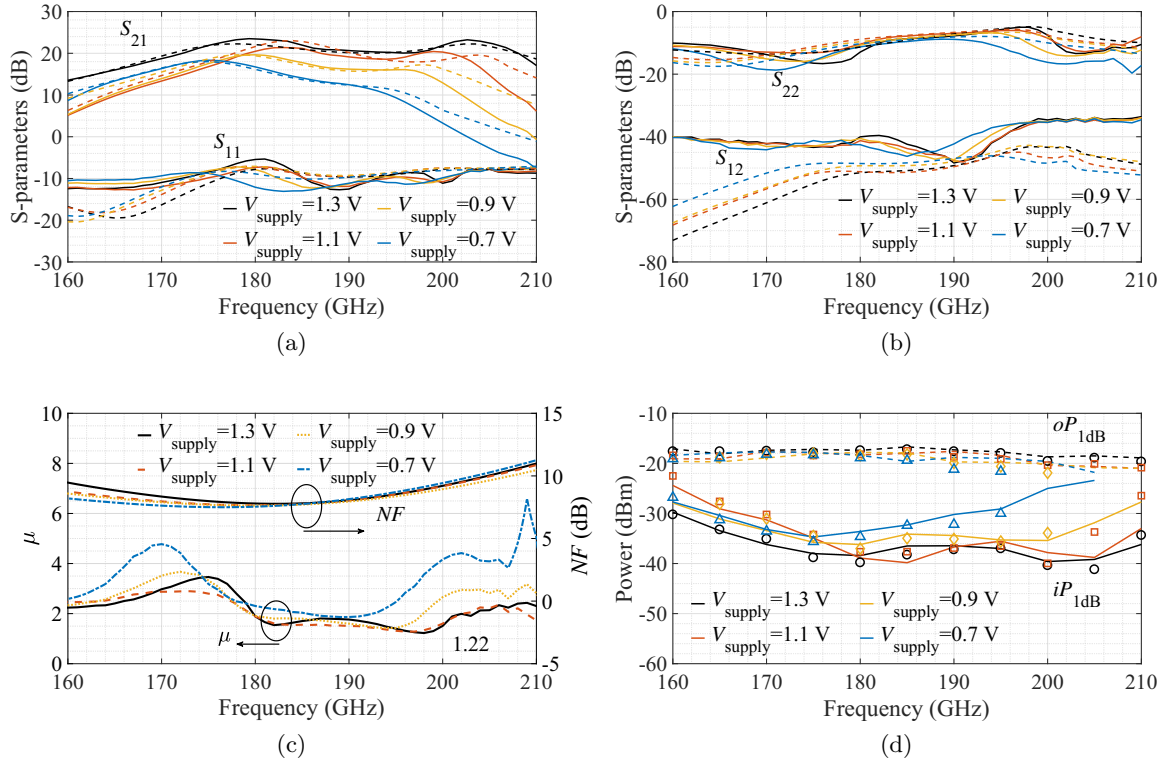


Figure 3.28: (a), (b) Simulated (dashed lines) and measured (solid lines) S-parameters, (c) calculated μ-factor (left) and the simulated NF (right), (d) Simulated (lines) and measured (symbols) oP_{1dB} and iP_{1dB} from 160 GHz to 210 GHz. $V_{supply}/V = 1.3$, 1.1, 0.9, 0.7. V_{UB} is 1.5 V for the former two and 1.3 V for the last two values of V_{supply}, and V_{BB} is 0.84 V for four bias cases.

and measurement of S_{11}, S_{22}, and S_{21} show good agreement under all bias cases. For S_{12}, the presented deviation may be attributed to substrate coupling.

Based on the S-parameters measurement data, the stability factor μ is calculated and displayed in Fig. 3.28c. For the four different bias cases, the minimum value is 1.22 at 203 GHz, representing the in-band stability of the amplifier. In the frequency of operation, suitable equipment for precise noise measurement was not available, and thus the simulated NF of the amplifier is shown in Fig. 3.28c. Over the in-band frequencies, the minimum NF of the four bias conditions is 7.7, 7.65, 7.6, and 7.5 dB at 181, 180, 178.5, and 177 GHz. Even though the V_{BB} is maintained, the J_C still slightly decreases with V_{supply} and V_{UB} (cf. Fig. 3.7), resulting in a slightly reduced NF here.

Fig. 3.28d shows the comparison of large-signal characterization between simulation and measurement for four biases. The measured peak oP_{1dB} of this amplifier is -17.2, -17.5, -18 and -18.3 dBm at 185 GHz, respectively, with the corresponding input 1 dB compression point iP_{1dB} of -38.2, -37.6, -37.2 and -35.6 dBm, respectively. The slightly reduced oP_{1dB} is mainly due to the decreased J_C, and the measurement results are well approximated by simulations.

The performance summary of this amplifier compared with recently reported amplifiers operating around 200 GHz is shown in Table 3.4. The achieved 3.2 mW DC power consumption is the lowest value and just half of that of the latest presented state-of-art low-power amplifier [64], with also highly competitive performances in terms of gain, NF as well as bandwidth. A reasonable index to evaluate the performance of small-signal low-power amplifiers is the ratio of gain and DC power dissipation (gain(1)/P_{dc}(mW)). This circuit realizes the highest value of this ratio with around ten times and six times, respectively, higher than the best reported

Table 3.4: Comparison with published amplifiers operating around 200 GHz

Reference	Technology	f_T/f_{max} (GHz)	Center frequency (GHz)	Gain (dB)	3 dB BW (GHz)	P_{dc} (mW)	oP_{1dB} (dBm)	NF (dB)	Gain/P_{dc} (1/mW)	FoM
MWCL2017 [66]	130 nm SiGe HBT	300/500	182.5	10	55	16.8	-10	10.5*	0.6	0.32
MWCL2014 [65]	130 nm SiGe HBT	300/500	190	16.9	44	18	-4.1	9.6*	2.72	5.7
MWCL2018 [64]	130 nm SiGe HBT	300/500	187.5	16	25	6.4	-14.3	11*	6.22	0.49
T-MTT2016 [74]	130 nm SiGe HBT	300/500	183	17.2	22	16.1	-9.6	7.6	3.3	1.65
T-MTT2012 [85]	130 nm SiGe HBT	300/500	210	15	20	150	-	13*	0.21	-
EuMIC2014 [75]	130 nm SiGe HBT	300/500	233	27	10	68	-	12.5*	7.4	-
EuMIC2017 [76]	130 nm SiGe HBT	300/500	190	24.7	16	37.2	-6.5	9.8*	7.9	3.3
This work (1.3 V)	**130 nm SiGe HBT**	**460/600**	**190**	**23.5**	**34**	**3.2**	**-17.2**	**7.7***	**70**	**9.2**
This work (1.1 V)	**130 nm SiGe HBT**	**460/600**	**191**	**21.3**	**26**	**2.7**	**-17.5**	**7.65***	**50**	**4.8**
This work (0.9 V)	**130 nm SiGe HBT**	**460/600**	**180**	**19.6**	**17**	**2.22**	**-18**	**7.6***	**41.8**	**2.35**
This work (0.7 V)	**130 nm SiGe HBT**	**460/600**	**175**	**18.3**	**15**	**1.73**	**-18.3**	**7.5***	**39.1**	**1.9**
MWCL2015 [86]	50 nm GaAs mHEMT	370/670	180	24.5	7	24	-	3.5	11.7	-
T-TST2014 [87]	50 nm GaAs mHEMT	370/670	184	22	17	41	-	6.7	4	-
JSSC2014 [88]	32 nm SOI CMOS	250/320	210	18	20	44.5	-	11	1.4	-
EL2016 [89]	32 nm SOI CMOS	250/320	184	25	20	33	-	9	9.6	-
T-TST2016 [90]	35 nm InP HEMT	400/1100	220	15	120	36	-	5.2	0.87	-
IMS2010 [91]	35 nm InP HEMT	400/1100	175	21	28	12	-	-	10.5	-
T-TST2014 [92]	250 nm InP DHBT	370/650	255	24	20	81.7	-	10.4	3.1	-
EuMIC2018 [93]	500 nm InP DHBT	350/400	120	10	110	96	-	8	0.1	-

*Simulated; - not presented

SiGe amplifiers [64,76] as well as state-of-the-art amplifiers using 50 nm GaAs mHEMT [86], 35 nm InP HEMT [91], and 32 nm SOI CMOS [89], respectively. Additionally, if taking both the small-signal and large-signal performance of amplifiers into consideration, including oP_{1dB}, 3 dB Bandwidth (BW), and noise performance, a suitable FoM can be defined as

$$\mathrm{FoM} = \frac{\mathrm{gain}(1) \cdot \mathrm{BW(GHz)} \cdot oP_{1dB}(\mathrm{mW})}{(\mathrm{F}(1) - 1) \cdot P_{dc}(\mathrm{mW})}, \tag{3.28}$$

Even though the oP_{1dB} obtained in this design is lower, the highest FoM outperforming all other listed SiGe amplifiers with an improvement factor close to two compared to [65], which indicates the best trade-off among all key performance parameters is achieved.

3.1.6.3 Analysis

The observed good agreement achieved using HICUM/L2 allows deeper studies about the impacts of the physical effects on circuit characteristics. By varying the related parameter by ± 10%, the sensitivities on gain and noise performance of this amplifier are presented in Fig. 3.29. Parameters involved in this analysis include the internal and external series base (r_{bi} and r_{bx}), emitter (r_e), and collector resistances (r_{cx}), transconductance-related parameters (c_{10} and h_{f0}), the transit time (t_0), as well as the parasitic base-emitter and base-collector capacitances (C_{bepar} and C_{bcpar}). Five parameters with the highest impact are sorted here from the highest to the lowest. As can be seen, the transconductance-related c_{10} is among the top impact both for gain and noise, also the t_0. The r_{bx}, C_{bcpar}, and r_e also present noticeable impacts.

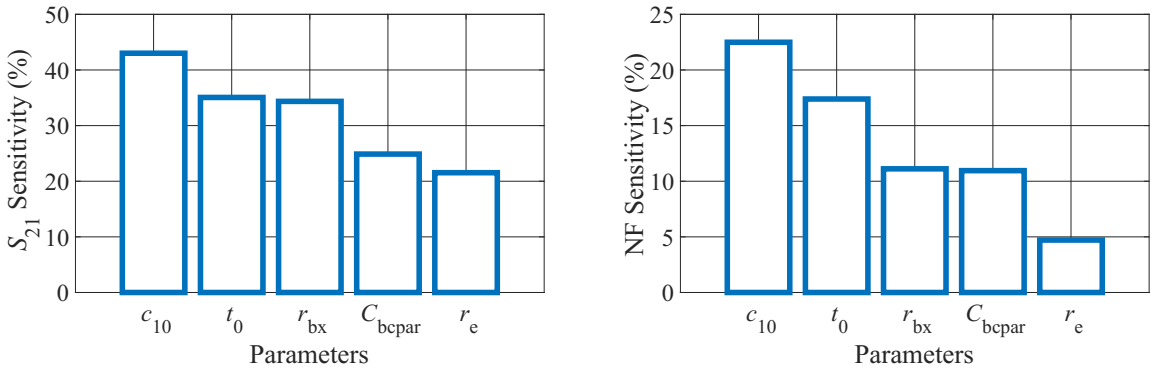


Figure 3.29: Gain and noise performance sensitivities with respect to physical-effects-related model parameters with 10% variation.

The influences of parasitic capacitances and resistances of the transistor on amplifier performance are analyzed in Fig. 3.30. The potential parasitic effects are predicted by doubling the parameter value of external capacitance parameters C_{bepar} and C_{bcpar}, and the external resistances r_{bx}, r_{cx}, and r_e of the HICUM model compared to the nominal simulation results. As demonstrated, the parasitic capacitances and resistances lead to a huge performance degradation in gain and noise. Meanwhile, around 40 GHz shift of the frequency band towards lower frequencies is cased by parasitic capacitances. Because of the extremely reduced J_C and V_{BC}, the high-current effect, self-heating effect, and non-quasi-static effect do not play much of a role in this amplifier.

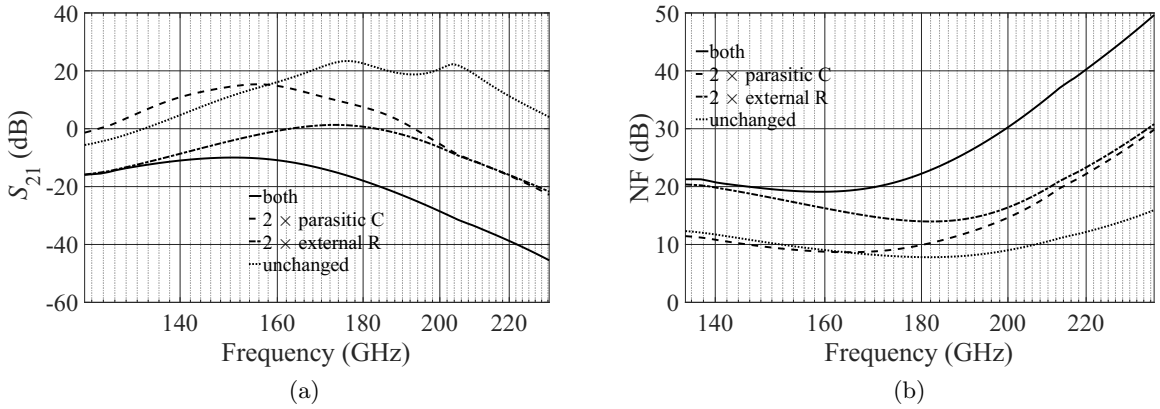


Figure 3.30: Impact analysis of parasitic capacitances and resistances on (a) gain, and (b) NF of this amplifier.

3.2 72-108 GHz Low-Power Tunable Amplifier

Apart from the low DC power dissipation, the tuning capability of key metrics with P_{dc} is an additional benefit for performance optimization, dynamic range extension, and DC power distribution, especially at the system level. Following the design flow discussed in Section 3.1, a 72-108 GHz low-power amplifier is presented here. This design was implemented in a 130 nm SiGe BiCMOS technology from Infineon Technologies AG, featuring high-speed npn-HBTs with (f_T, f_{max}) = (250, 370) GHz at V_{BC}=-0.5 V, as described in Section 2.1.2.

3.2.1 Configuration, Sizing, and Bias Tuning Range

Due to the advantages discussed before, the cascode configuration is also utilized in this design. A similar schematic is implemented in this work, as presented in Fig. 3.17, with two inductors L_b and L_{cas}, and one resistor R_{bs} aiming at G_m enhancement as well as stage stabilization.

As discussed in section 3.1.3.2, HBTs with sufficiently long emitter stripes possess similar peak f_T values. For low-noise and high-gain amplifiers, the minimum emitter width is generally the most beneficial because P_{dc} increases with emitter length if the current density and associated cut-off frequency remain the same. However, smaller devices usually provide fairly large input and output impedances, making the broadband matching network tricky. Therefore, by selecting the larger emitter length, the real part of the input or output impedance of a transistor can be optimized towards 50 Ω, which significantly simplifies the broadband matching network. Hence, the middle-size BEC device with emitter window area of $A_{e\text{-}w}$≈0.13 μm×4.91 μm (drawn area $A_{e\text{-}m}$=0.22 μm×5 μm) was chosen here finally.

As one of the significant performance parameters in the front-end amplifier design, the small-signal gain is proportional to the biased f_T. Generally, a negative V_{BC} close to peak f_T is typically used to maximize the gain performance. However, a better trade-off between high gain and low P_{dc} requires a significant reduction of V_{supply}, resulting in a potential positive V_{BC} value. Similarly, the peak f_T of this technology is still beyond 200 GHz even when operating SiGe HBTs up to a moderately positive V_{BC}=0.5 V, which is acceptable for W-band mm-wave circuit design, as shown in Fig. 2.2. Therefore, the low-power design method with device operating in saturation is implemented in this design.

Theoretically, the gain and DC power of the front-stage amplifier can be tuned by selecting different V_{BC}. However, this tunable range achieved only by voltage bias may be not enough. Aiming at further reducing P_{dc} and expanding the performance tuning capability, the transistors can also be biased with a tunable J_C. With a further but acceptable sacrifice of f_T, a lower

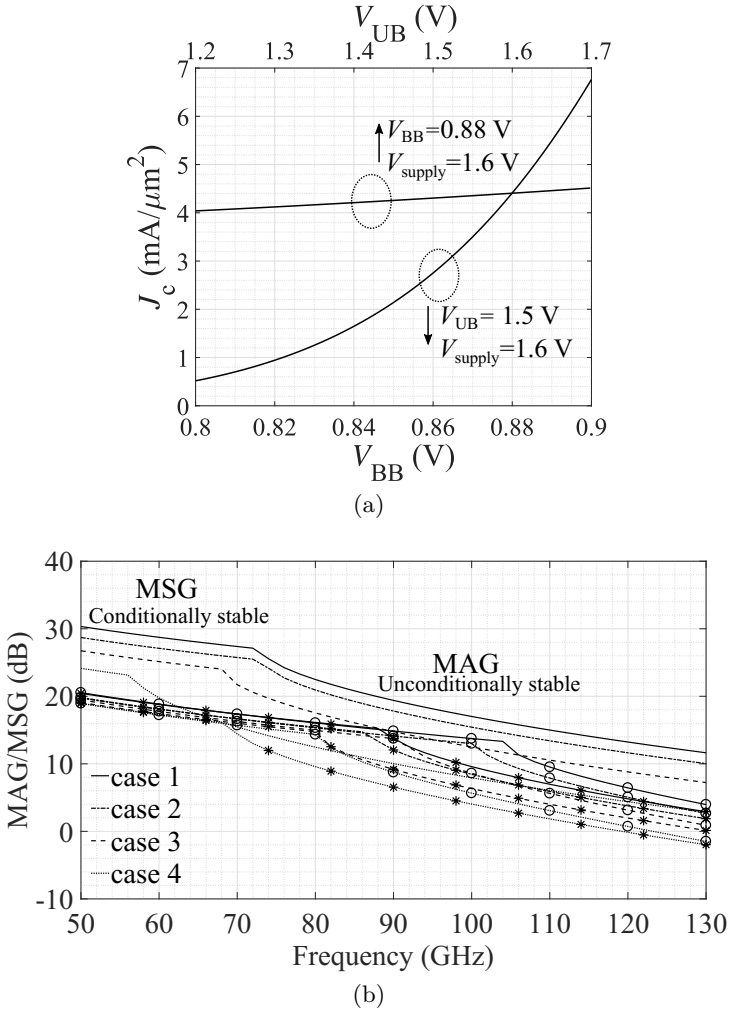


Figure 3.31: (a) Simulated J_C vs two base biases with V_{supply}=1.6 V. (b) Simulated MAG/MSG of the ideal stage (lines) and complete gain stage with (circle) and without (asterisk) two inductors and R_{bs}. For the bias cases 1-4, V_{supply}/V=1.6, 1.4, 1.2, 0.9, V_{UB}/V=1.7, 1.6, 1.5, 1.3 (V_{BC}/V≈0.1, 0.2, 0.3, 0.4), and V_{BB}/V=0.9, 0.88, 0.86, 0.84.

J_C will be selected for further reduction of P_{dc}. For instance, with the same V_{BC} of 0.5 V but the declined J_C from around 8 to 1.5 mA/μm^2, the f_T can be reduced aggressively to around 150 GHz, leading to more than 80% tunable P_{dc}.

The gain performance with the most significant bias reduction should be verified to find out the limit of the bias tuning. Using equation 3.2 and equation 3.3, the relationship of J_C with V_{UB} and V_{BB} of the transistor in this technology is shown in Fig. 3.31a. Based on this and the f_T value shown in Fig. 2.2, the eventual V_{BC} range of the gain stage is chosen from 0.1 to 0.4 V, which corresponds to V_{UB} and V_{supply} varying from 1.3-1.7 V and 0.9 V to 1.6 V, respectively. The V_{BB} is selected between 0.84 and 0.9 V, with which the biased J_C varies from around 8 to 1.5 mA/μm^2. Fig. 3.31b illustrates the simulated maximum available gain/maximum stable gain (MAG/MSG) of the ideal cascode stage for four different bias examples covering the entire selected tuning range. Even with the lowest bias, i.e., the V_{supply} of 0.9 V (forward-biased V_{BC} up to around 0.4 V) and the J_C of 1.5 mA/μm^2(V_{BB} of 0.84 V), the ideal stage still provides above 6 dB MAG at 110 GHz, which is still acceptable for this tunable low-power design in this work.

The realization and value optimization of two inductors and resistors of the complete gain

stage follows the procedure introduced in Section 3.1.5.2 and thus is not discussed here in detail. Highlighted here is that the actual dimension of inductors and the value of R_{bs} were optimized using EM-simulating the gain stage with all connection structures surrounding the devices under the most critical biases with the highest J_{C} and V_{supply} and in turn the most critical stability condition. Finally, L_{b} of 13 pH by M2 layer, L_{cas} of 15 pH by M6 layer, and R_{bs} of 15 Ω by TAN resistor were chosen. The EM simulated MAG/MSG of the optimized single gain stage for the four example bias cases is also demonstrated in Fig. 3.31b. Compared with the simulation of the ideal cascode stage, MAG/MSG of the complete stage involving parasitics caused by vias and connection structures decrease about 5-7 dB. However, about 3-4 dB can be compensated by the G_{m}-boosting inductors.

3.2.2 Regional Matching Network

3.2.2.1 Impedance Variation

Based on the analysis of bias dependency in Section 3.1.2, the P_{dc} as well as the small-signal performance such as gain and noise are determined by the bias condition and thus can be tuned directly by the bias. Besides, the large-signal performance like maximum P_{out} level is also highly relevant to the chosen biases. However, the variation of the impedance of the cascode with bias makes maintaining of the broadband performance challenging. As can be seen in the gain performance of the first design in Fig. 3.28a, the changed bias lead to a noticeable variation of the device impedance response making the matching network no longer valid and thus results in a relatively large bandwidth degradation.

In order to maintain the wide-band performance within the tuning range, the analysis of the input impedance Z_{in} and output impedance Z_{out} of the cascode stage is important. Fig. 3.32a displays the simplified small-signal equivalent circuit of the cascode stage, retaining only the most relevant elements for the analysis and omitting the series resistances. C_{bc} is the total base-collector capacitance, C_{be} is the total base-emitter capacitance, and C_{cs} is the total collector-substrate capacitance. Compared to Fig. 3.18 implemented in the first design, the equivalent output resistance r_{o} is required for the real part impedance analysis. L_{b}, L_{cas}, and R_{bs} are omitted here for simplification. Under the condition of zero output voltage v_{out} (shorted), this equivalent circuit can be simplified as in Fig. 3.32b, and the input impedance Z_{in} can then be approximated by

$$Z_{\mathrm{in}} \approx \frac{1}{j\omega[C_{\mathrm{be1}} + (1 + g_{\mathrm{m1}} Z_{\mathrm{t}}) C_{\mathrm{bc1}}]}, \tag{3.29}$$

where

$$Z_{\mathrm{t}} = \frac{1}{j\omega[C_{\mathrm{be2}} + C_{\mathrm{cs1}}] + g_{\mathrm{m2}} + \frac{1}{r_{01}} + \frac{1}{r_{02}}}, \tag{3.30}$$

is the equivalent load impedance of the bottom CE transistor. Z_{in} is mostly capacitive since the real part of Z_{in} is mainly given by the base resistance of the bottom CE transistor, which is usually much smaller than 50 Ω for achieving better high-frequency performance.

With the condition of zero input voltage v_{in} (shorted), the output impedance Z_{out} of the ideal cascode stage can be calculated from in Fig. 3.32c as

$$Z_{\mathrm{out}} = (r_{02} + \frac{g_{\mathrm{m2}} r_{02} + 1}{\frac{1}{r_{01}} + j\omega C_1}) || \frac{1}{j\omega C_2}. \tag{3.31}$$

with

$$C_1 = C_{\mathrm{bc1}} + C_{\mathrm{cs1}} + C_{\mathrm{bc2}}, \tag{3.32a}$$

$$C_2 = C_{\mathrm{bc2}} + C_{\mathrm{cs2}}. \tag{3.32b}$$

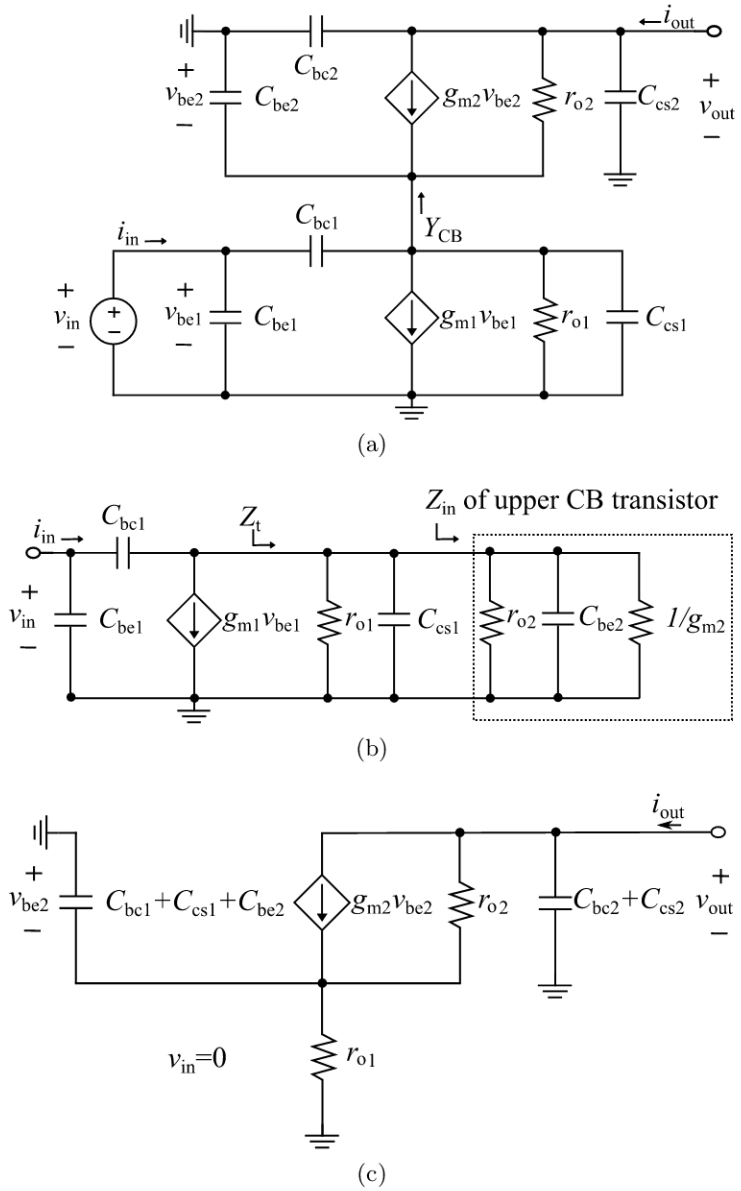


Figure 3.32: (a) Simplified small-signal equivalent circuit of the cascode stage. Further simplified equivalent circuit for (b) Z_{in} and (c) Z_{out} analysis.

The detailed derivation of the above equations at presented in Appendix A.

With the tuned V_{BC} and J_C, the transconductance g_m is strongly varied. Such bias-dependent variation also happens to the two capacitances C_{be} and C_{bc}. The linear increase with J_C in Fig. 3.33a indicates that C_{be} is dominated by the internal BE diffusion capacitance. In contrast, based on the operation point check using the HICUM model, the C_{bc} is mainly given by the internal and external BC depletion capacitance, and the J_C dependence observed in Fig. 3.33b is caused by the voltage drops across the emitter and collector series resistance and the reduction of space charge region. The large capacitive variation needs to be compensated during the bias tuning and introduces additional challenges for the input-and inter-stage MN design.

For Z_{in} up to the frequency of interest, varying g_m only results in a limited impact on Z_{in} due to the compensation between g_{m1} and $1/g_{m2}$ in Z_t. Nevertheless, Z_{in} still varies over a fairly large range due to the bias-dependent variation of $C_{be1,2}$ (by a factor of 2.5) and C_{bc1} (by around 30 %), both of which are operated here at forwarded bias as shown in Fig. 3.33. However, an increase of g_{m2} with J_C is somewhat compensated with the increased C_1 ($\sim C_{be2}$), resulting in a

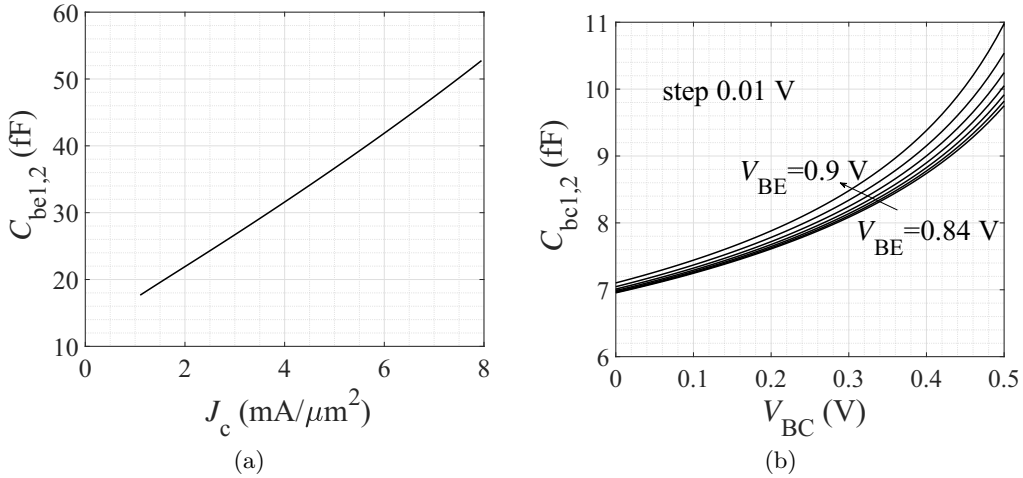


Figure 3.33: Extracted (a) $C_{\mathrm{be1,2}}$ and (b) $C_{\mathrm{bC1,2}}$ versus J_{C} and V_{BC}, respectively, based on operation point simulation using HICUM.

smaller variation of Z_{out}.

Table 3.5: Values of parameters at selected bias cases

	g_{m1}	g_{m2}	$r_{\mathrm{o1}}(\Omega)$	$r_{\mathrm{o2}}(\Omega)$	C_{be1}	C_{be2}	$C_{\mathrm{cs1,2}}$	C_{bc1}	C_{bc2}
Case 1	106.5	103.6	31	31.1	52	56	10	7.3	7
Case 2	71.6	69.6	31.1	31.2	43	45	10	7.7	7.2
Case 3	48.8	44.85	31.1	31.2	33	31	10	7.9	7.6
Case 4	33	35.1	31.2	31.4	20	22	10	8.9	8.8

Unit: gm (mS), C (fF), r (Ω)

In order to observe the variation quantitatively, equation 3.29 and equation 3.31 are evaluated based on the parameters listed in Table 3.5, which are extracted under four bias cases as selected before, and the comparison between simulations and calculations are presented in Fig. 3.34. At 100 GHz, the real and imaginary part of Z_{in} varies around 30% and 60% for the different bias conditions, respectively. In contrast, Z_{out} varies only maximal 7%, which is beneficial for the regional matching network design, which will be discussed later. As shown, the variation tendency is reasonably estimated by the equation, and the deviation of the absolute value may be due to the neglect of the resistive components and the zero voltage assumption. For example, Adding the total series (external and internal) base resistance leads to a similar amount of real part of the calculated Z_{in} as the simulation, as shown in Fig. 3.34a.

The impact of such impedance variation of the transistor on circuit stabilization needs also be checked. According to equation 3.23, $\mathrm{Re}\{Y_{\mathrm{in}}\}$ turns out to be negative when $\omega^2 L_{\mathrm{B}}(C_{\mathrm{be2}}+C_{\mathrm{bc2}})$ becomes larger than 1. As a result, the risk of instability of the bias case with larger J_{C} and V_{supply} is higher due to the increase of C_{be2} (J_{C}). This agrees with the simulated μ factor of the first amplifier displayed in Fig. 3.11, is can also indicated by the position of the intersection point of MSG and MAG shown in Fig. 3.31b, which represents the stability factor k=1. Therefore, the amplifier should be stabilized for the worst bias condition, which is given by the highest J_{C} (V_{BB}) and V_{supply} in the bias tuning range.

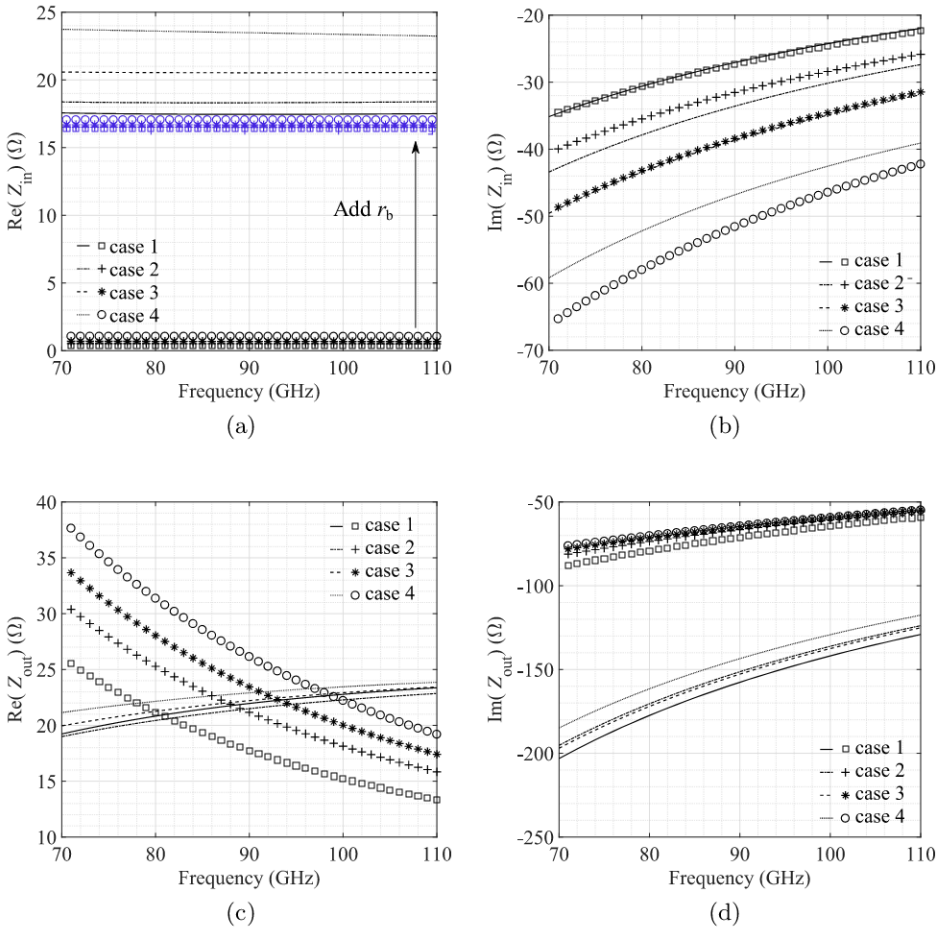


Figure 3.34: Simulated (lines) and calculated (symbols) real (left) and imaginary (right) part of simulated (a), (b) Z_{in}, and (c), (d) Z_{out} of the ideal cascode stage for the four bias cases defined earlier.

3.2.2.2 Regional Matching Network Design

Impedance matching is significant to reduce voltage standing wave ratio (VSWR) and to obtain the maximal power delivery of circuits. In the mm-wave and sub-mm-wave circuit and system designs, the matching network is typically realized by TLs instead of lumped elements due to its easier realization and integration on-chip and reduced parasitics. Generally, the TL utilized in the matching network is located either in series or shunt, as shown in Fig. 3.35a. Based on the standard TL theory, the reflection coefficient at position 1 at frequency f is

$$\Gamma_1(f) = \frac{Z_{\text{L}}(f) - Z_0}{Z_{\text{L}}(f) + Z_0}, \tag{3.33}$$

where Z_{L} is the load impedance with frequency-dependent imaginary part, and Z_0 is the characteristic impedance of the TL and system. A series TL with electric length θ shifts the phase of the reflection coefficients, as

$$\Gamma_{2,\text{ series}}(f) = \Gamma_{1,\text{ series}}(f)e^{-j2\theta} = \frac{Z_2(f) - Z_0}{Z_2(f) + Z_0}. \tag{3.34}$$

Z_1 and Z_2 are the impedance looking towards the load (Z_1=Z_{L} in this case). Since the series TL does not change the $|\Gamma|$ and thus the VSWR remains the same, Z_{L} moves towards Z_2 along

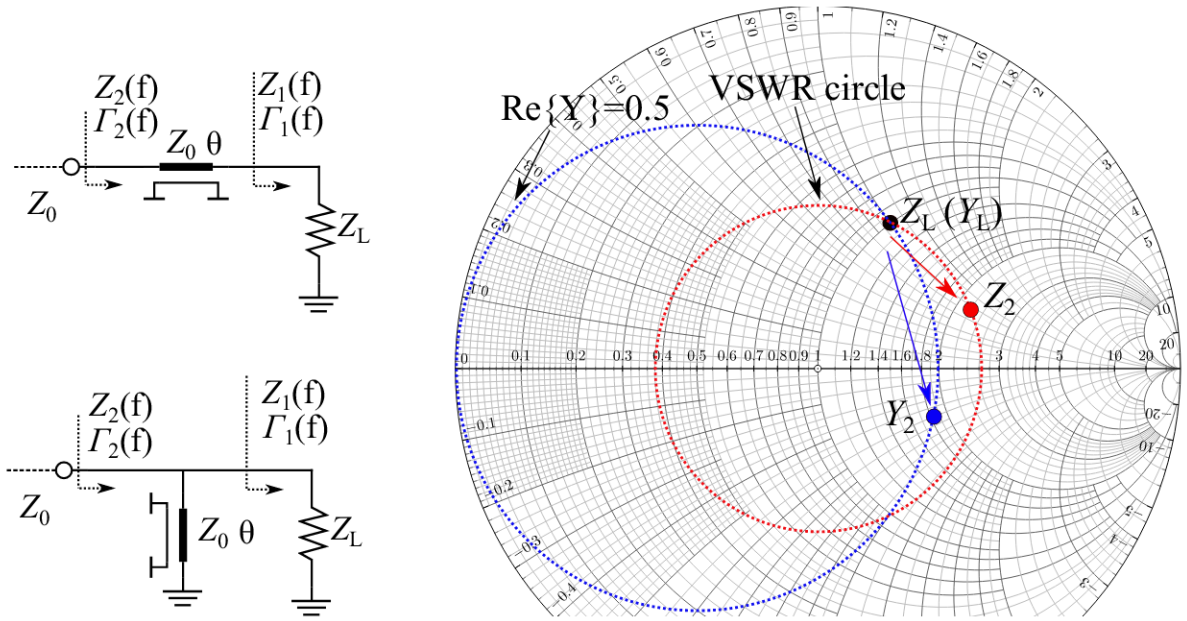


Figure 3.35: (a) Simplified schematic diagram of two types of TLs (series or shunt) used in matching network design, and (b) their loci of movement in the Smith chart with TL length.

the VSWR circle.

The admittance after adding a shunt TL can be obtained as

$$Y_{2,\,\text{shunt}}(f) = \frac{1-\Gamma_1(f)e^{-j2\theta}}{1+\Gamma_1(f)e^{-j2\theta}}Y_0 - j\frac{Y_0}{tan\theta}. \tag{3.35}$$

Hence, the shunt TL makes $Y_L(Z_L)$ move on the Re{Y} circle, as presented in Fig. 3.35b because it only changes the imaginary part.

As mentioned before, the biggest challenge in this design is to achieve wide-band performance and to maintain it over a wide bias tuning range, which turns out to be especially difficult with the considerable impedance variation of the device and the cascode stage. Z_{out} and Z_{in} of the complete gain stage (with two inductors, R_{bs}, as well as all via connections) are simulated from 70 to 110 GHz, and their loci are shown in Fig. 3.36. Notice that the five circles at one bias condition are because of the selected five frequency points, which show the movement loci of the best noise matching point and 1 dB noise circle versus frequency. Each noise circle is drawn for a single frequency point. Due to the bias dependence of the capacitances, Z_{in} varies during bias tune, and the variation increases with frequency. Z_{out}, however, varies relatively little. As also can be seen, thanks to the careful device selection, the Z_{in}^* of 70-110 GHz is very close to or even inside the 1 dB noise circle within the tuning range, and thus makes the simultaneous gain and noise match at the input relatively easier.

For the frequency range of interest, various conventional matching networks have been used in previous amplifier designs, such as L-type [94], π-type [95], and the T-type [96, 97]. However, those conventional conjugate matching methods can only be realized at a single frequency point because of the frequency dependency of the impedance for the passive matching network and device. Expanding the bandwidth up to around 20% can be achieved with a dual-band matching network, which keeps an acceptable mismatch in the frequency range between the two matched frequency points, as implemented in the G-band low-power amplifier before. A wider bandwidth is still possible with a more sophisticated matching method, such as multi-frequency matching

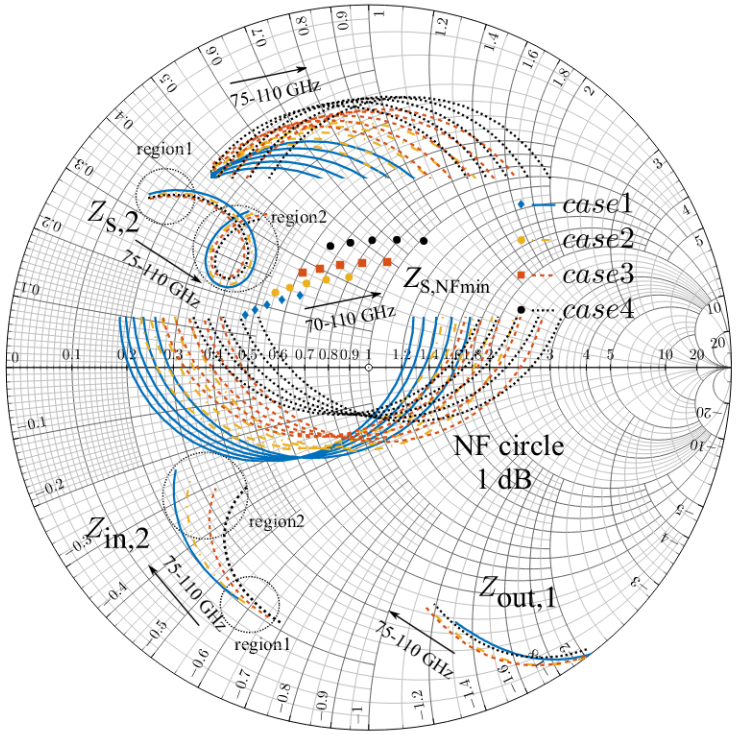


Figure 3.36: Smith chart with the loci of simulated Z_{out}, Z_{in}, the optimum source impedance for minimum noise figure $Z_{s,\,NFmin}$, the 1 dB NF circle, and Z_S matched by the designed regional matching network of the complete gain stage for four bias cases as specified before. Five frequency points with 10 GHz steps from 70 to 110 GHz are displayed for each bias case. The subscript 1, and 2 in Z_S, Z_{in}, and Z_{out} represent the front and following stage of the cascaded amplifier, respectively (cf. Fig.3.37b).

[64], but at the cost of a larger chip area.

Fig. 3.37 demonstrates the simplified schematic comparison of the T-type, dual-band, and the regional matching network utilized in this design. As shown, the T-type network provides one shunt TL (TL_2), which enables the imaginary part compensation at one frequency point only. The dual-band network offers the imaginary part compensation at two different frequency points by two shunt lines (TL_2 and TL_5) with reasonable mismatch between two frequency points. Similarly, the regional matching network also processes two shunt lines. However, instead of matching at two points, the two shunt lines in the regional matching network are used to maintain an acceptable mismatch covering a wide frequency region, and more importantly, covering the impedance variation caused by bias tuning.

For a better comparison and understanding, a single-stage amplifier example was designed. At the input port, different matching networks (T-type, dual-band, regional) are implemented. The same ideal T matching network at the output and the same gain stage designed before are used during the comparison, as shown in the block diagram in Fig. 3.38g. Also in Fig. 3.38, Z_{in}^* is compared with the achieved Z_S by different networks over the frequency range from 70 to 110 GHz, for the four bias examples in the tuning range as specified before. The closer position of the loci of Z_S and Z_{in}^* indicates a better match at this frequency.

As shown in Fig. 3.38a and Fig. 3.38b, the T-type matching offers the best match at a single frequency point in the 85-95 GHz range for four bias cases, which leads to a highest gain of around 8.8 dB for bias case 1 at 90 GHz, with 28 GHz 3 dB bandwidth from 75-103 GHz. As a comparison, the dual-band network consists of an additional shunt TL representing an inductor. Because of the different frequency responses of the two shunt TLs, a loop trace of Z_S is generated [43]. This trace is designed with two symmetric matched frequency points, while

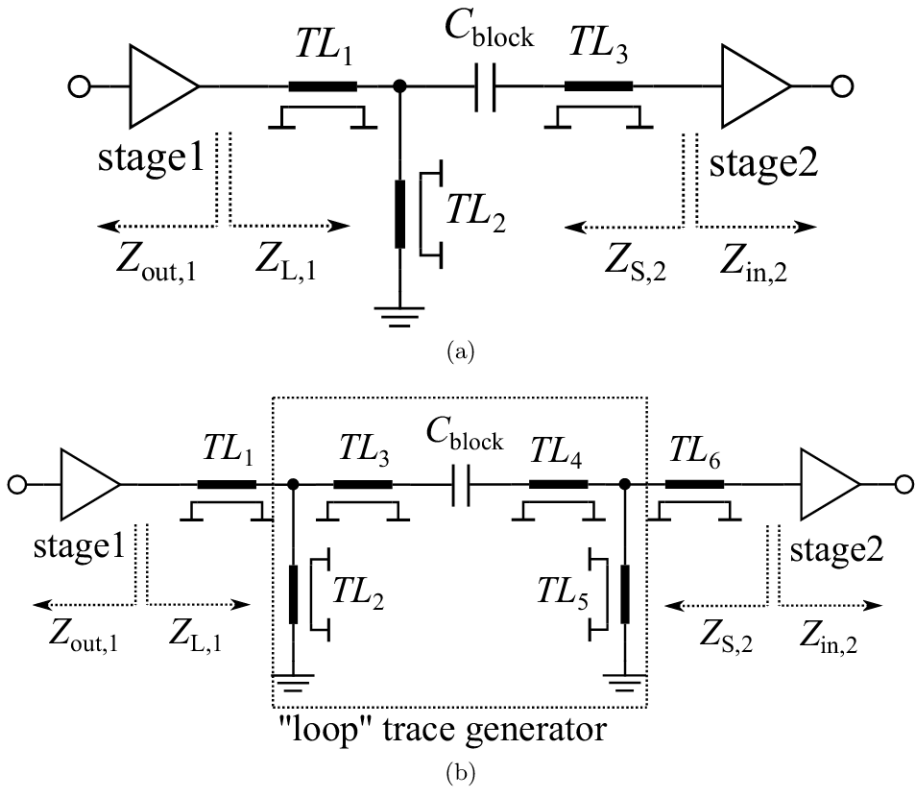


Figure 3.37: (a) simplified schematic of the (a) T-type, (b) dual-band, and the proposed regional matching network used in this design.

the other points obtain acceptable mismatch. In the gain response, two peak gains appear at the two matched frequency points, while the notch in the middle indicates mismatch level [43]. By selecting the characteristic impedance Z_c of the series TLs TL_3 and TL_4 in between the two shunt lines (cf. Fig. 3.37b), the trace size can also be controlled, which results in different matched points and different mismatch level in between. As shown in Fig. 3.38c and Fig. 3.38d, the dual-band matching network offers a good match for two frequencies at 78 and 101 GHz for case 1, resulting in an 8.5 dB gain at two frequencies with the 3 dB bandwidth of 35 GHz. However, as displayed, this bandwidth deteriorates noticeably to 26 GHz during bias tuning, and the second peak at 101 GHz disappears. Such deterioration is mainly due to the variation of Z_{in}, resulting in continuously worse match at the high-frequency region.

Instead, as shown in Fig. 3.38e, the regional matching network is realized by tuning such loop trace of Z_S located in the high-frequency region (region 2 in the figure), where the impedance variation of Z_{in}^* (Z_{in}) caused by varied capacitances is much more considerable. As a result, all frequencies in this region (and on the loop trace) keep an acceptable mismatch over the entire bias tuning range and thus the observed match degradation at higher frequencies is well compensated. Also notice that for region 1 in the low-frequency range from around 70 to 80 GHz, the observed relatively larger mismatch is somewhat acceptable and also beneficial for the flatness of the gain response due to the generally higher amplification capability of the device at a lower frequency (see the MAG/MSG curve in Fig. 3.31b). The position of the loop trace of Z_S is optimized by the careful selection of the length and Z_c of TL_2-TL_5 in Fig. 3.37b. Despite a slightly lower achieved peak gain of 8.3 dB, a wide BW of 35 GHz from 73 to 109 GHz is achieved by the regional matching network, and more importantly, the wide-band performance is maintained over the whole tuning range, as shown in Fig. 3.38f.

The final realized Z_S of the complete amplifier is presented in Fig. 3.36. As shown, thanks to the much less varying Z_{out} as the starting point, the Z_S realized by regional matching network

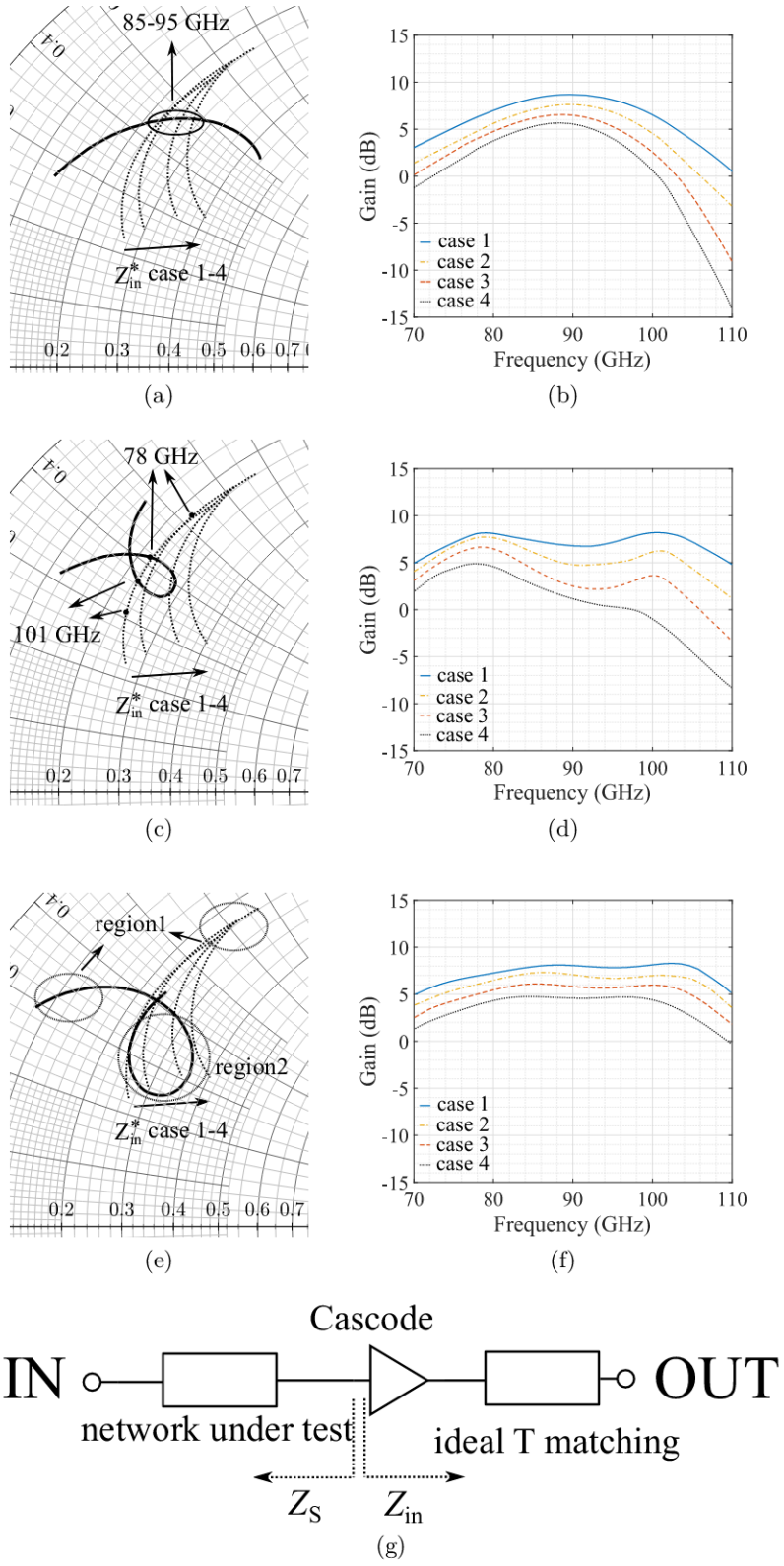


Figure 3.38: Simulated Z_S compared with the conjugate input impedance Z_{in}^* (left), and Gain (right) of the single-stage amplifier example with (a), (b), T-type, (c), (d), dual-band, and (e), (f), regional input matching network. Same bias cases 1-4 as before. (g) Simplified block diagram used in this matching network comparison.

shows only a slight variation within the bias tuning range, which enables to maintain bandwidth performance of this amplifier during the bias tune.

3.2.3 Circuit Implementation

The topmost metal layer M6 with 3 μm thickness was used as the main routing layer due to its lowest sheet resistance resulting in the lowest high-frequency propagation loss, while M1 was used as the ground plane. The Z_c and length of TLs were optimized by EM simulation in Keysight's Momentum.

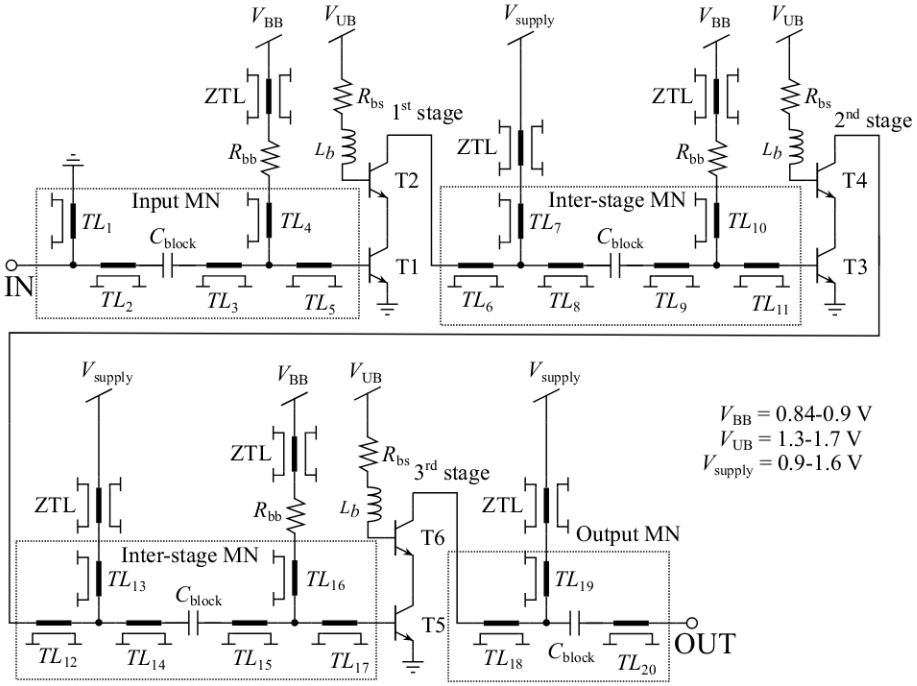


Figure 3.39: Circuit schematic of the designed amplifier.

The circuit schematic of the designed amplifier is shown in Fig. 3.39. Regional matching networks are employed at the input and between stages. Starting from the system impedance (including pads) and the output impedance of the front gain stage, the required Z_S is generated to compensate for the Z_{in} variation of each gain stage and to maintain the broadband performance over the bias tuning range. Because of the careful selection of transistor size and configuration, the optimum noise impedance of the gain stage is already close to the conjugate source impedance. Thus a relatively good noise match can be directly achieved by the designed input matching network. Because of the much smaller variation of Z_{out}, the conventional T-type network is sufficient. All the long TLs are bent to save chip space. ZTLs and SWs are implemented here for the same reason as discussed before. Fig. 3.40 presents the micrograph of the fabricated amplifier, with a core area of 1.5 mm×0.5 mm.

3.2.4 Results and Discussion

3.2.4.1 Results

This amplifier was measured on-wafer. For S-parameters measurements, the signal was automatically controlled by a VNA (Keysight PNA E8361C), and its frequency was extended to 110 GHz using a W-band T/R module N5260A. The latter was also used for large-signal characterization, where a W-band harmonic mixer (Keysight 11970) and a W-band waveguide tunable attenuator (RPG R&S, WTA75-110) together with a spectrum analyzer (Keysight 4448A) were

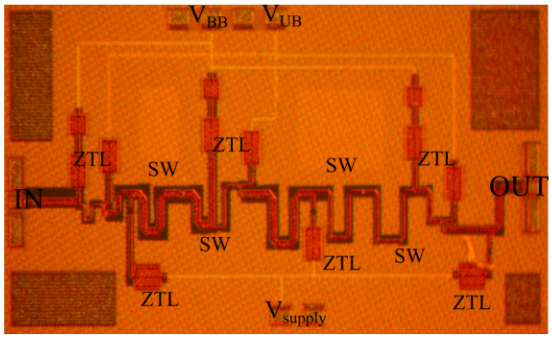
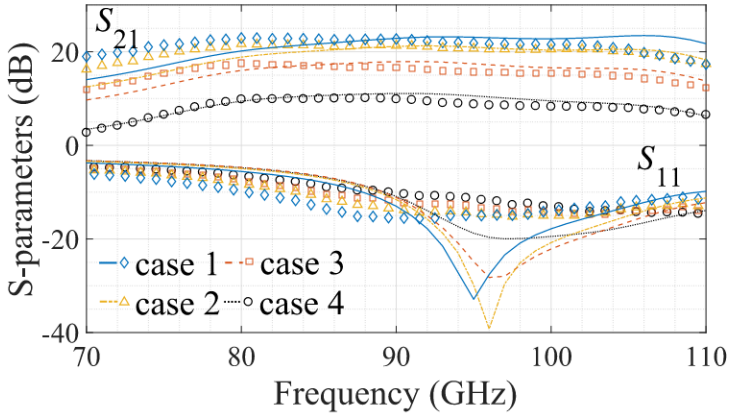
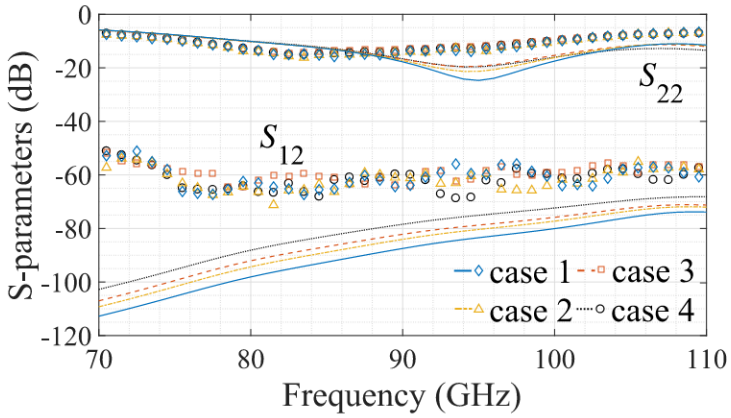


Figure 3.40: Micrograph of the fabricated amplifier. The chip core area of this amplifier is 1.5 mm×0.5 mm without pad structures.



(a)



(b)

Figure 3.41: S-parameters from 70 to 110 GHz for the four bias cases specified before: comparison between measurement (symbols) and simulation (lines).

utilized to monitor the power of the output signal. A VDI Erickson PM5 power meter was used for power calibration, and the probe loss was subtracted for accurately calculating the on-chip power level.

Fig. 3.41 shows the comparison of measured and simulated S-parameters of the complete amplifier with the four bias cases specified before. The highest gain of 23 dB at 80 GHz is achieved with bias case 1, corresponding to the highest V_{supply} and J_{C} of the bias tuning range with 21 mW static DC power. For almost the full W-band from 72 to 106 GHz, the gain is above 20 dB, yielding a 3 dB bandwidth of 34 GHz (38.2 % relative bandwidth). For the bias case 2

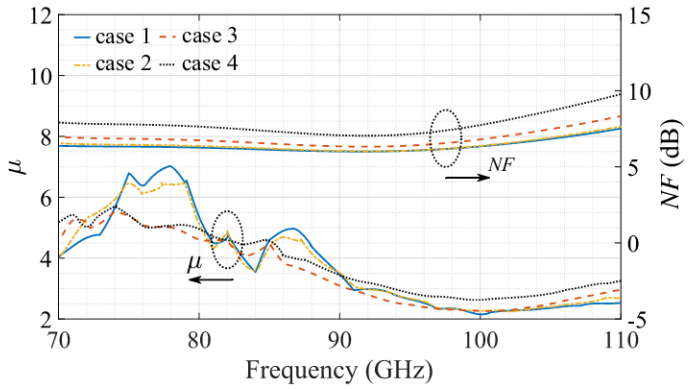


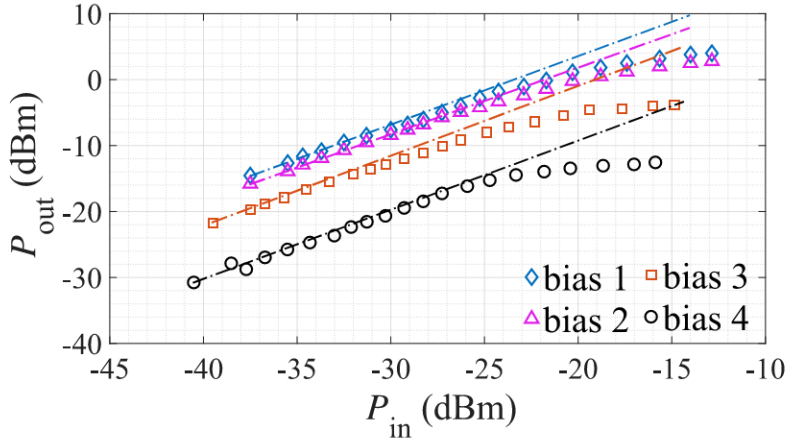
Figure 3.42: μ-factor (left axis) calculated from measured S-parameters and simulated NF (right axis) versus frequency for the four bias cases specified before.

with slightly reduced V_{supply} and J_{C}, a peak gain of 21.7 dB at 81 GHz and a 3 dB bandwidth of 34 GHz from 73 to 107 GHz are observed, with a significantly reduced DC power consumption of 13.4 mW. Further reducing V_{supply} and J_{C}, resulting in $V_{\text{BC}}\approx$0.3 V for case 3 and a low DC power of 7.9 mW, yields a peak gain of 17.6 dB and 33 GHz 3 dB bandwidth from 73 to 106 GHz. Aiming at realizing extremely low DC power dissipation, aggressively reduced V_{supply} and J_{C}, corresponding to $V_{\text{BC}}\approx$0.4 V, still, 10-dB peak gain with a bandwidth of 33 GHz at very low 3.8 mW DC power are achieved. Within the bias tuning range, the wide-band performance is maintained, indicating the proper operation of the designed regional matching networks.

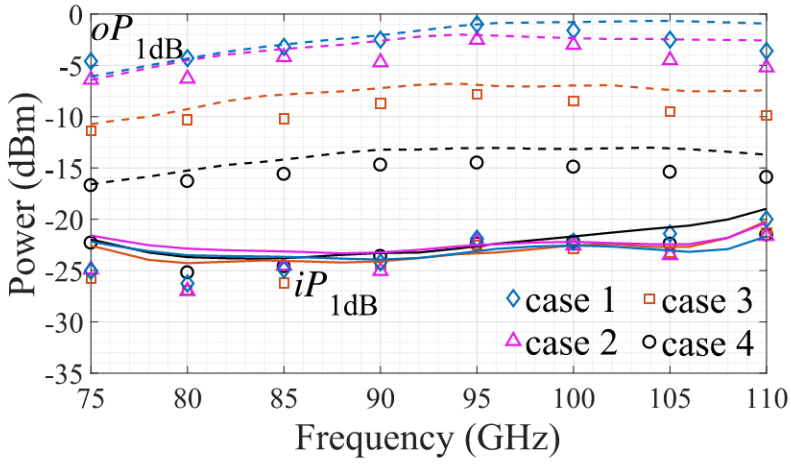
The stability μ-factor is calculated based on the measured S-parameters and is shown in Fig. 3.42. The overall value is higher than two, which confirms the in-band stability of this circuit. The smaller μ-factor from 95 to 110 GHz indicates a better matching in region 2 than region 1 (70 to 80 GHz). Since equipment suitable for accurate noise measurements was not available, simulated NF data are presented in Fig. 3.42. The minimum simulated NF for the bias case 1-4 is 6.1, 6.2, 6.4, and 7 dB at 92, 92, 91, and 93 GHz, respectively. The variation of in-band NF of this circuit within the bias tuning range is within 1 dB due to the careful design of the input regional matching network and the transistor sizing. The lowest NF value at bias case 1 is mainly due to a closer match between Z_{S} of the input matching network and $Z_{\text{S,NFmin}}$, as shown in Fig. 3.36. The simulated NF of this amplifier represents the actual results reasonably well for the following reasons. Firstly, the noise-related measured and simulated S-parameters S21 and S11 of this amplifier agree pretty well. Secondly, HICUM was demonstrated in [98] to accurately match the experimental data from various HBT technologies up to 50 GHz and the Boltzmann transport equation simulation data up to 500 GHz. Thirdly, the NF simulation data of two LNAs designed in the same process technology using HICUM [99] agreed reasonably well with measurements in the same operating frequency range.

The measured output and input 1-dB compression points (oP_{1dB} and iP_{1dB}) are shown in Fig. 3.43. The peak oP_{1dB} is measured at -1, -2.5, -7.8, -14.5 dBm at 95 GHz, with a corresponding iP_{1dB} of -21.9, -22.5, -22.55, -22.4 dBm. The significant decrease of oP_{1dB} is mainly caused by the aggressively reduced J_{C} and V_{supply} tuning. The figures show that the simulations match the large-signal measurement well.

Table 3.6 summarizes the performance of this amplifier compared to recently reported work operating in similar frequency ranges using various process technologies. Despite utilizing HBTs with 50 GHz lower peak f_{T} than in other SiGe HBT amplifiers [60, 99–101], this amplifier still provides highly competitive performance in terms of gain, 3 dB bandwidth, oP_{1dB}, NF, and DC power dissipation. The same FoM in equation 3.28 is utilized in this comparison. Using SiGe HBTs with the relaxed lithography (130 nm) and lower available f_{T}, this amplifier achieves a slightly lower FoM than the highest one in [100]. Furthermore, compared with state-of-the-art



(a)



(b)

Figure 3.43: (a) Measured P_{out} (symbols) at 95 GHz with the corresponding 1dB/dB line (lines), and (b) oP_{1dB} and iP_{1dB} from 75 to 110 GHz: comparison between simulation (lines) and measurement (symbols) for the four bias cases specified before.

CMOS work listed in the Table, this circuit competes well with significantly more advanced and costly CMOS technology. More importantly, as a front stage of a low-power receiver, the wide range of tunability for gain and DC power consumption while maintaining broadband performance is beneficial for performance optimization, dynamic range extension, and DC power distribution of a receiver. With further packaging process, the DC source module could be integrated on PCB off-chip so that the bias functionality can be automatically controlled.

3.2.4.2 Analysis

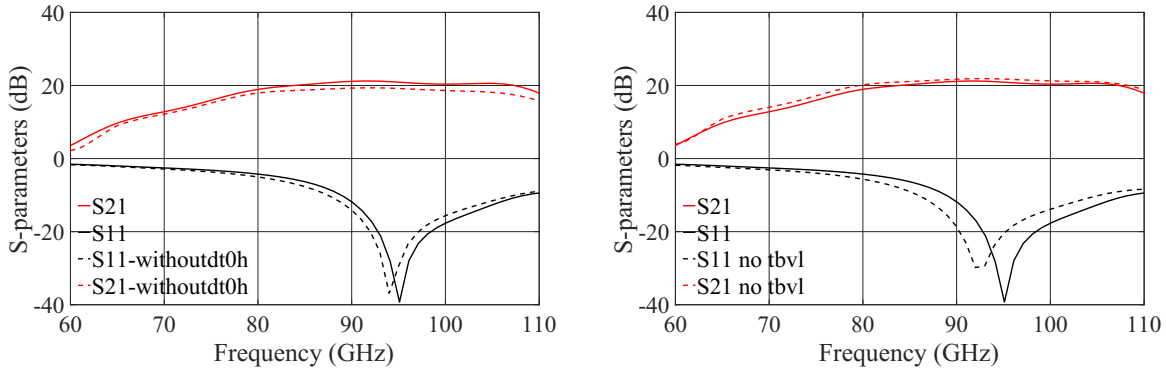
The observed excellent agreement between measurements and simulations achieved in this design using the HICUM model also allows deeper studies about the impacts of the physical effects on circuit characteristics. Unless otherwise noted, the bias condition 2 is used in the following analysis. Firstly, the impact of two forward-bias-related parameters, dt0h (time constant for base and B-C space charge layer width modulation) and tbvl (time constant for modeling carrier jam at low collector-emitter voltage), on S-parameters is checked by turning on/off parameters, as shown in Fig. 3.44. Around 0.9-2 dB deviation (23 %-58 % variation) and 3-5 GHz frequency shift towards lower frequency is observed.

Then, the influence of t0 and tef0 (neutral emitter storage time) on S-parameter is presented

Table 3.6: Comparison with published W-band amplifiers

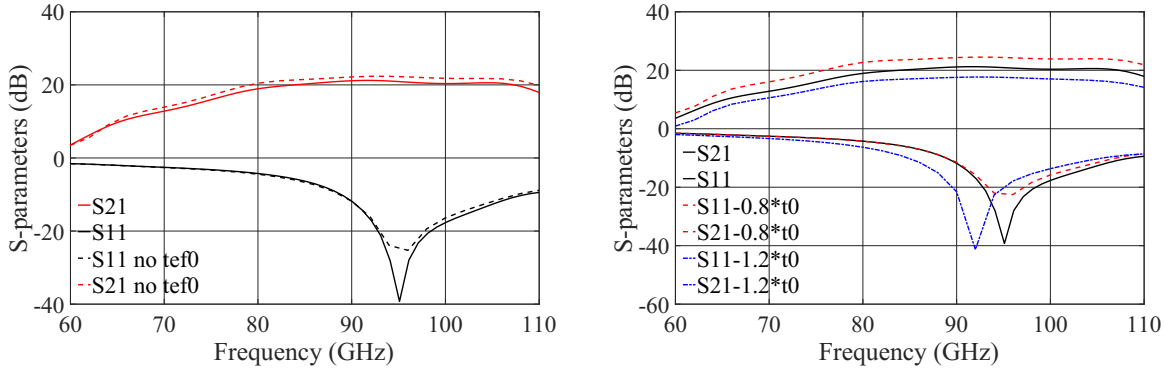
Ref.	Tech.	f_T/f_{max} (GHz)	Center (GHz)	Gain (dB)	3 dB BW (GHz)	P_{dc} (mW)	oP_{1dB} (dBm)	NF (dB)	FoM
[99]	130 nm SiGe	300/500	93/88	14.3/12	14/43	2.8/12	-7.5*/-8*	5.4/5.2	9/3.5
[100]	90 nm SiGe	300/350	80	25	10	15.6	-1	4	88.5
[60]	90 nm SiGe	300/350	94	10	19	8.8	-2.5	4.2	7.5
[101]	130 nm SiGe	300/350	110	20.5	10	17	-5	4	12.3
This	**130 nm SiGe**	**250/370**	**89...92**	**10...23**	**33...34**	**3.8...21**	**-14.5...-1**	**6.1*...7***	**0.9...87**
[97]	65 nm CMOS	200/210	75/77.5	13.3/18.5	27.5/30	12/27	-2/2.5	6.4/5.5	9.2/54.9
[102]	65 nm CMOS	200/210	75	14.2	30	33.5	2.5	6.3	14.4
[103]	22 nm FD-SOI	360/375	77/93	24/18.2	13/31	16/16	-3.8/-5.6	4.6/5.8	45.2/12.6
[104]	45 nm RFSOI	260/290	86	12	25	4.7	-10	4.2	5.2
[105]	32 nm SOI	330/450	93	18	10	24	-8	5.3	1.5
[106]	22 nm FinFET	230/284	74	20	10.4	10.8	-3.8	4	31.9
[107]	28 nm FD-SOI	290/410	75	15	64	38.2	1.5	6	25.1

*Simulated;



(a) (b)

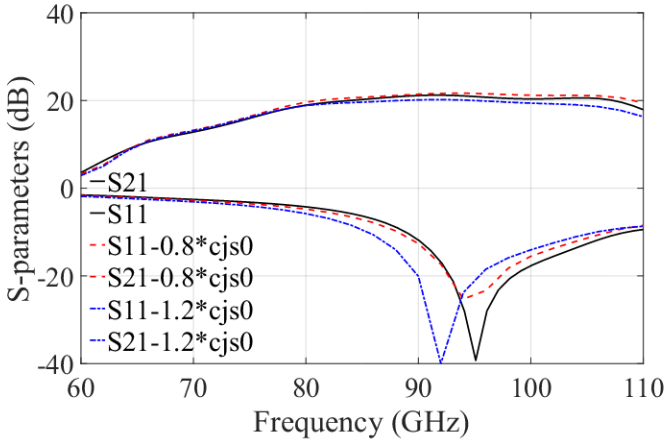
Figure 3.44: Simulated S_{21} and S_{11} of this amplifier with/without tbvl and dt0h.



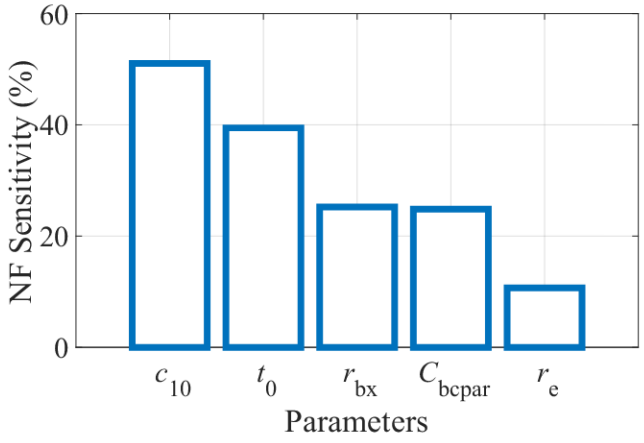
(a) (b)

Figure 3.45: Simulated S_{21} and S_{11} of this amplifier with ±20 % t0 and on/off def0.

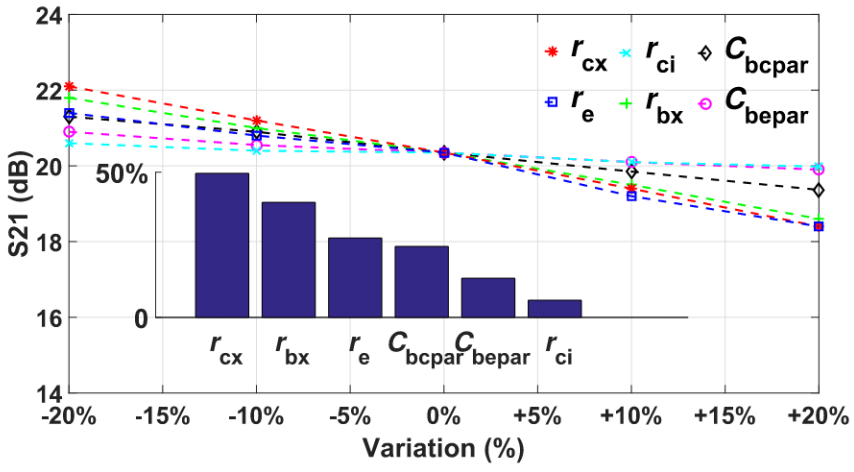
in Fig. 3.45. 1.4 dB difference can be seen by turning on/off tef0, which is transferred to 39 %. t0 shows a more significant impact on the gain, with 2.5-3 dB change caused by ±20 % t0 sweep.



(a)



(b)



(c)

Figure 3.46: (a) Simulated S_{21} and S_{11} of this amplifier with ±20 % Cjs0. Sensitivity analysis on (b) noise and (c) gain at 95 GHz with parameter variation of ±20 %.

The substrate coupling effect is also checked here, and three related parameters are substrate

series resistance Rsu, shunt capacitance (by the substrate permittivity) Csu, and C-S zero-bias depletion capacitance cjs0. ±20 % variation of Cjs0 introduces nearly 1 dB change with larger impact at higher frequencies, as shown in Fig. 3.46a. The influence of Rsu and Csu is simulated by changing the default value (75 Ω and 10 fF) to either 0 or a substantial value (1k Ω and 1 pF), and around 10-20 % discrepancy is observed (not shown in figures).

The noise sensitivity of the amplifier is shown in Fig. 3.46b, with parameters varying ±20 % at 95 GHz. The varied parameters include the internal and external series base (r_{bi} and r_{bx}), the emitter (r_{e}), and the collector resistances (r_{cx}), transconductance-related parameters (c_{10} and h_{f0}), the transit time (t_0), as well as the parasitic base-emitter and base-collector capacitances (C_{bepar} and C_{bcpar}), and five parameters with the biggest impact are shown in the figure. Similar to the noise sensitivity of the G-band amplifier, the transconductance related c_{10} shows the highest impact on noise of 51%. t_0, r_{bx}, and C_{bcpar} also present strong impact higher than 20%.

The gain sensitivity of this amplifier is analyzed by varying the related parameter of ±20 % at 95 GHz as shown in Fig. 3.46c. Here, the transistor resistances and capacitances are joined. For this amplifier, R_{cx} shows the highest impact of 49 %, followed by R_{bx}, R_{e}, C_{BCpar}, C_{BEpar}, R_{ci}, with the impacts of 39 %, 27 %, 24 %, 13 %, 6 %, respectively.

3.3 Conclusion

The low-power LNA design method has been enabled by operating transistors in saturation. The design flow includes topology selection, bias selection, device sizing, and performance enhancement technologies. The impact of a drastic reduction of supply voltage and collector current on the performance of G-band and a W-band amplifier have been discussed in this chapter. Additionally, the performance tuning method has been described for the W-band design. Highly competitive amplifier performance parameters have been achieved simultaneously with the lowest reported DC power dissipation with a considerable improvement of the linear gain to dc power ratio. Thanks to the accurate HICUM compact model, overall good agreement between simulation and measurement and first-pass success were achieved. Finally, based on such good agreement, the impact of physical effects on circuit performance has been studied.

4 Low-power Down-conversion Mixers

Mixers are generally used to achieve frequency conversion in a transceiver system. With two input frequency signals f_1 and f_2, multiple frequency components are generated, as

$$f_{\text{out}} = af_1 + bf_2, \tag{4.1}$$

and a, b, respectively, are integers (0, ±1, ±2...). According to the desired output frequencies, the mixer can be divided into: the down-conversion mixer for receivers with the intermediate frequency (IF) signal, f_{IF}=|f_1-f_2|, as the output, and the up-conversion mixer for transmitters with the RF signal, f_{RF}=|f_1+f_2|, as the output.

A typical receiver requires the down-conversion mixer offering good performance parameters as follows:

- Conversion gain (CG). CG describes the relationship between the input and output signal of the mixer. Here, the power CG is usually utilized in most designs, while the voltage CG is reported in some publications, mainly due to the higher impedance than 50 Ω [108,109].

- Linearity. Mixer linearity is defined in a similar way as in amplifiers. The 1 dB compression point is often used to describe the linearity at mm-wave frequencies.

- Noise figure (or noise factor). NF is also defined as the SNR ratio between input and output signal. In mixers, the single-sideband (SSB) NF is theoretically 3 dB higher than that of double-sideband (DSB). NF is especially essential in mixer-first receivers with a mixer as the front stage instead of LNAs [110,111].

- Port Isolation. Since the mixer is a three-port component, minimizing the interactions among RF, LO, and IF ports is desired.

- LO pumping power level. The LO pumping power level is another critical issue because the on-chip LO power realization brings extra difficulties and DC power dissipation at mm-wave frequencies.

Generally, less DC power consumption is always beneficial and is another critical consideration of the mixer design in this Chapter.

The nonlinear performance of the mixer is realized by its current-voltage characteristic. Depending on the nonlinear elements, mixers are commonly classified by passive and active ones. The active mixer is mainly realized by the nonlinear g_{m}, whereas the passive ones are achieved by the nonlinearities of zero DC bias resistances or reactances. Passive mixers are typically realized by diodes, CMOS, or III-V HEMTs [112–115], and also by HBTs but with a diode-connected configuration [116]. The major advantages of passive mixers are zero DC power consumption and good linearity, but at the expense of much higher conversion loss and higher LO pumping power, introducing additional difficulties and consuming more DC power dissipation duo to the

extra on-chip PA in the LO chain. Active mixers, however, become much more prevalent at mm-wave frequencies since they offer6 CG instead of loss and less LO power.

Also, according to the different harmonics of LO used for signal mixing, the mixer types can be separated as fundamental, subharmonic, or higher-order. Increasing the LO order in mixer design releases the demand of LO source in terms of frequency while suffering from a higher required LO power level and lower available CG.

There have been several SiGe-based mixers reported recently at the mm- and sub-mm-wave frequencies. A 90 GHz down-conversion mixer was realized with CG of 17.2 dB and P_{dc} of 92.4 mW [117]; A 85 GHz down-conversion mixer was achieved by CG of 7 dB, consuming 110 mW P_{dc} [118]; A 200 GHz down-conversion mixer were designed with CG of 5.5 dB and P_{dc} of 22.5 mW [119]. However, all mixers listed above are biased in the active forward region with negative V_{BC}, aiming at maximizing the RF performance. In this chapter, a 97 GHz down-conversion low-power mixer is demonstrated. Aiming to explore the lowest possible P_{dc} while maintaining other mixer performance parameters mentioned above, this design reduces P_{dc} significantly by biasing transistors with positive V_{BC}. Meanwhile, the mixer topology is enhanced by special measures for the sake of P_{dc} reduction.

4.1 97 GHz Low-power Down-conversion Mixer

A 97 GHz low-power down-conversion mixer is presented in this section. This circuit was designed using B11HFC from Infineon Technologies AG with npn-HBTs featuring peak (f_T, f_{max}) = (250, 370) GHz at V_{BC}=-0.5 V, as described in Section 2.1.2.

4.1.1 Mixer Design and Implementation

4.1.1.1 Mixer Topology

In bipolar transistor technologies, two main types of active mixers dominate, namely the g_m-based and the Gilbert-cell-based mixers, and the simplified schematics are shown in Fig. 4.1. The g_m-based mixer is realized by one (single-ended [120]) or two devices (single-balanced [121]). Both LO pump and RF signals are injected into the base of devices, resulting in a time-varying V_{BE}, I_C (J_C), and thus g_m for signal mixing. The Gilbert-cell-based mixer consists of two cross-coupled differential pairs in parallel as the upper switching quad (SQ) stage and two transistors at the bottom as the transconductance (TC) stage. In the Gilbert-cell-based mixer, the RF signal is first amplified by the bottom TC stage. Then, it goes to the upper SQ stage and multiplies with the LO pump signal for signal mixing.

Table 4.1: Comparison of SiGe-based mixer topologies

	Single-ended	Single-balanced	gilbert
P_{dc}	low	moderate	high
CG	low	moderate	high
NF	good	moderate	moderate
linearity	moderate	moderate	moderate
isolation	low	moderate	high
LO power	low	moderate	moderate

The performance of the SiGe-based mixer topologies is summarized in table 4.1 [67]. Firstly, the linearity of the above three active mixers is more or less similar since it depends on the biased V_{supply} and J_C [122]. The single-ended g_m mixer has the simplest configuration, but at

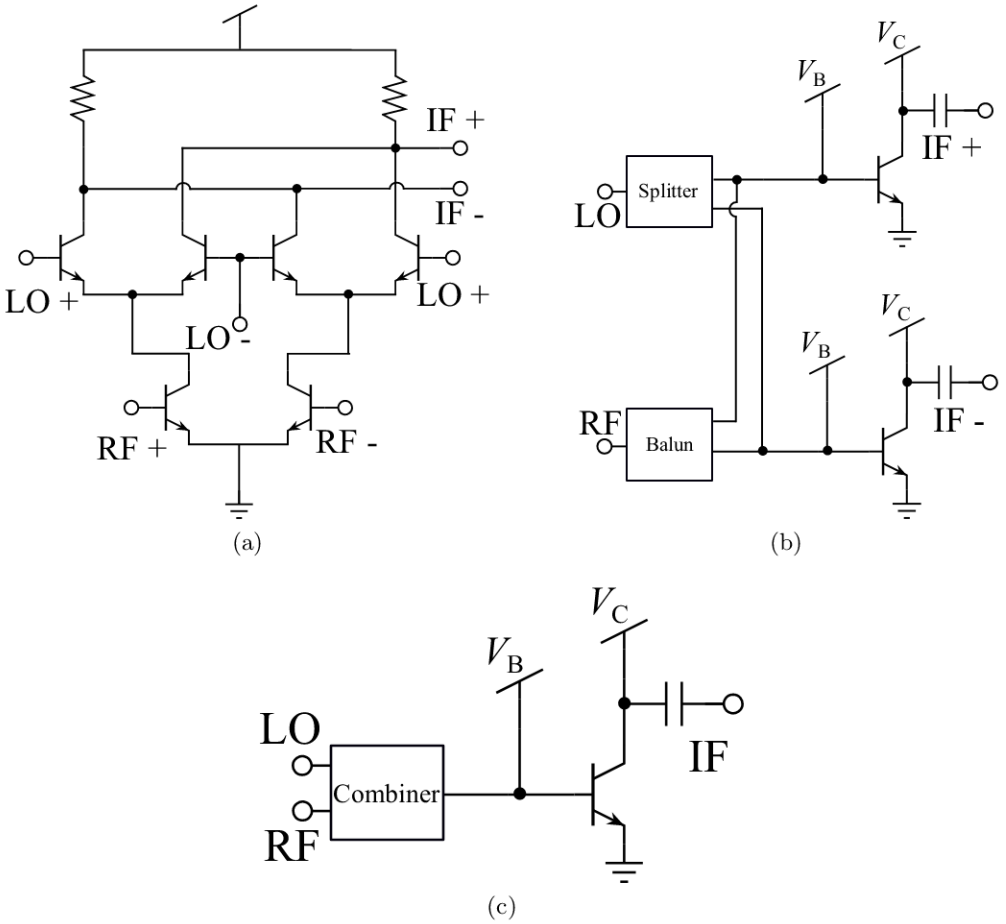


Figure 4.1: Simplified diagram of (a) gilbert-cell-based and (b) single-balanced, (c) single-ended transconductance-based mixer using bipolar technologies. Bias networks are omitted here.

the expense of relatively low port isolation and CG. Meanwhile, the integration with differential topology requires extra components for signal conversion, such as the balun or transformer. Gilbert-cell-based mixer has been an attractive solution at mm-wave frequencies since it offers high CG [117–119]. Also, the virtual ground generated by the differential pairs of the Gilbert-cell leads to much higher port isolation, further beneficial to prevent crosstalk and leakage between circuit blocks in the receiver. However, a higher P_{dc}, NF, and LO power are the compromise. Notice that the higher NF and LO power is mainly due to the loss of the passive balun at the front of RF and LO ports. At the mm-wave frequencies, higher CG becomes the primary consideration, while the higher NF can be partly compensated by LNAs as the front stage. Therefore, the Gilbert-cell-based configuration is usually selected in LNA-first receivers.

However, due to the stacked configuration requiring higher V_{supply} and more devices (cf. Fig. 4.1a), the gilbert-cell-based mixers typically consume more DC power. Fortunately, the P_{dc} of the gilbert-cell-based mixer can be optimized by topology enhancement methods, which will be discussed below.

Assuming a sinusoidal LO waveform, the CG of the gilbert-cell-based mixer is roughly described as [123]

$$\mathrm{CG} \cong \frac{2}{\pi}\frac{\sin(\mathrm{c})}{\mathrm{c}} \cdot g_{\mathrm{m,\ T1,2}}. \tag{4.2}$$

The term $\sin(\mathrm{c})/\mathrm{c}$ is contributed by the SQ stage, and the term $g_{\mathrm{m,\ T1,2}}$ is the transconductance

of two transistors at the operation point in the TC stage. Factor c is given as

$$c = \arcsin(\frac{V_x}{V_{LO,peak}}). \tag{4.3}$$

Here, $V_{LO,peak}$ is the peak amplitude of LO pumping power, and V_x is the ON-OFF switch voltage of the transistors in the SQ stage. Similar to the g_m-based mixer, the signal in the gilbert-cell is mixed in the SQ stage by the time-varying non-linear g_m of each device. As seen in Fig. 4.1a, each differential pair is pumped by the differential LO signal at the base, with which the two devices switch on and off alternately within one LO period. Fig. 4.2 demonstrates the simplified graphical evaluation of the time-varying g_m of one pair of HBTs in the SQ stage. Notice that the relatively large LO power is superimposed on the base bias $V_{B,SQ}$. Also notice that the time-varying g_m waveform is approximated as a square wave for simplification, which is reasonable under the condition of large LO power [121, 124]. As presented, V_x is defined as a

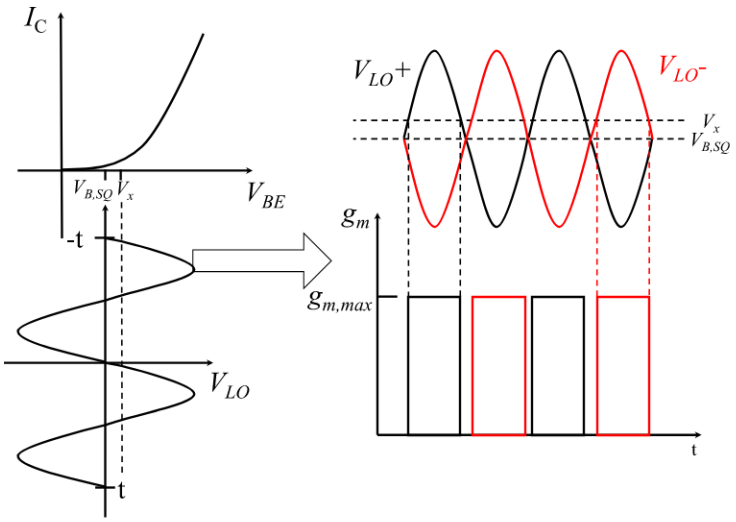


Figure 4.2: Evaluation of time-varying g_m of one differential pair of SQ stage, with black and red representing different devices.

particular value of the base voltage for a device to switch on, i.e., when $V_{LO}(t)+V_{B,SQ}$ is larger than V_x, the device operates for signal mixing and vice versa. V_x controls the duty cycle of each device in the SQ stage and thus should be carefully selected. Typically, a 50% duty cycle indicates a perfect switch between two devices in the differential pairs, which is beneficial to maximize the mixing performance of the SQ stage. V_x can be approximately expressed as

$$V_x \propto \frac{1}{\theta}(\frac{J_C}{2} + \sqrt{\frac{J_C^2}{4} + J_C}), \tag{4.4}$$

where θ is a parameter related to technology and device dimension (emitter area) [123].

Based on the above three equations, the contribution of the SQ and TC stages can be analyzed separately. Firstly, the contribution of $g_{m,T1,2}$ from the TC stage has a more substantial impact and thus dominates the CG. Also can be seen that the two devices in the TC stage act as a CE amplifier. As discussed in Chapter 3, the gain of the CE amplifier is dominated by g_m. Therefore, for the HBTs in the TC stage with given device dimension, biasing with larger J_C close to peak g_m is the key to improve its CG contribution. On the other hand, the SQ stage influences the mixer's CG by the sinc function sin(c)/c ($\leq$1). To maximize SQ's contribution, sin(c)/c close to 1 is required, which in turn requires c ($V_x/V_{LO,peak}$) close to 0. Therefore, a large LO pumping power (large $V_{LO,peak}$)and a small V_x (and thus small threshold J_C) are both

recommended.

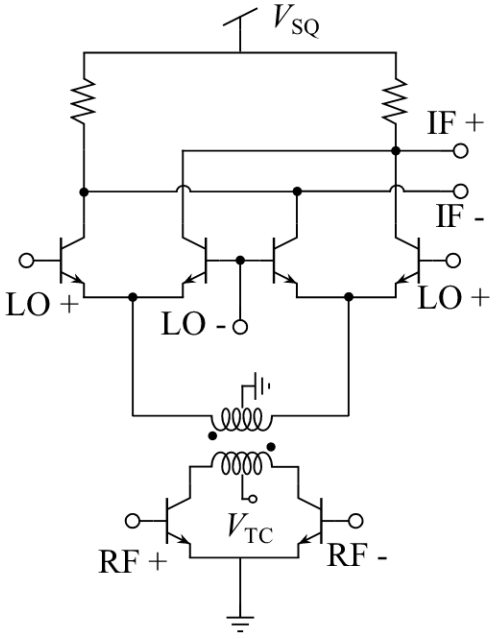


Figure 4.3: Simplified schematic of the low-power gilbert-cell-based mixer in this work.

To conclude, to maximize the CG performance, a large J_C in the TC stage and a small J_C in the SQ stage is the best. However, for the conventional gilbert-cell-based mixer shown in Fig. 4.1a, the above-suggested J_C bias can not be realized simultaneously due to the TC-SQ-stack. Because of the much more significant impact of the TC stage on CG than the SQ stage, a large J_C is usually selected to bias the overall gilbert cell. For the SQ stage, the larger J_C and larger V_x can be somewhat compensated by further enlarging LO pumping power (i.e., $V_{LO,peak}$ in the equation. 4.3), but at the expense of extra design difficulty and consumed P_{dc} of the LO chain. Additionally, the accurate selection of voltage bias is also tricky because the V_{supply} of standard gilbert-cell is not equally distributed to the two stages.

Fig. 4.3 displays the schematic of the proposed gilbert-cell-based mixer in this work. Instead of the stacked configuration, an on-chip transformer is implemented to couple the RF signal between the two stages, and also to provide an extra port for V_{supply} and DC ground for TC and SQ stage, respectively. With this topology, the optimum J_C, i.e., large J_C for TC and small J_C for SQ, can be achieved at the same time to obtain the maximal CG. More importantly, this topology requires only half of V_{supply} with only around 10% increase of total current since the SQ stage will be biased at very small J_C, leading to a nearly 40% reduction of overall P_{dc} of the gilbert cell. Meanwhile, less LO pumping power is required for this topology since $\sin(c)/c \approx 1$ can be realized by small V_x of the SQ stage, which in turn relaxes the design effort in the LO chain design.

4.1.1.2 Bias Selection and Device Sizing

In addition to the topology enhancement technique, a careful bias selection and device sizing are also essential for further P_{dc} reduction and performance optimization of the mixing core, based on the accurate compact model HICUM/L2 with the geometry scalable capability.

As discussed in Section 3.1.2.2, the biased g_m is determined by V_{BC} and J_C. Fig. 4.4a presents the simulated g_m versus J_C with varied V_{BC}. Similar to the LNA designs introduced before, biasing two transistors in the TC stage of the mixer with a moderately forward-biased V_{BC} does not necessarily lead to a significant speed degradation of HBTs. Also, the peak g_m causes J_C to shift towards a lower value with increasing V_{BC}, which is a further benefit for saving

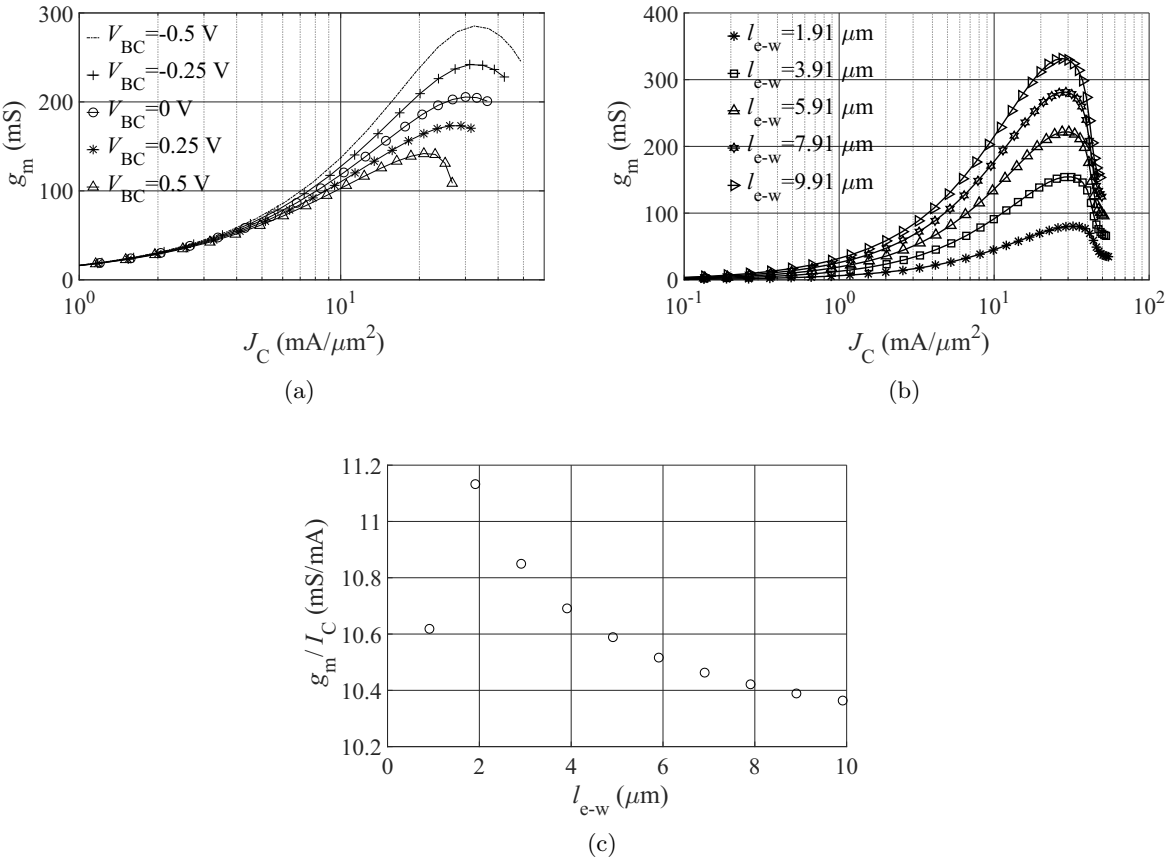


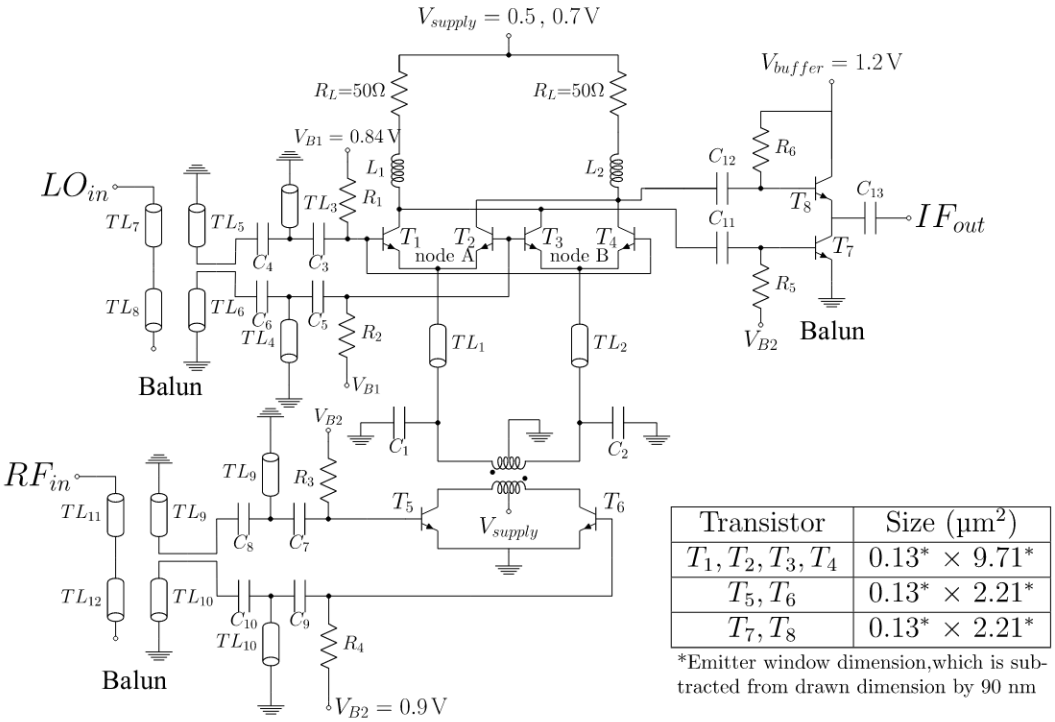
Figure 4.4: Simulated g_m versus J_C with (a) varied V_{BC} of the BEC transistor with $A_{e\text{-}w}$≈0.13 μm×4.91 μm, (b) varied $l_{e\text{-}w}$ and (c) peak g_m normalized by I_C of BEC transistor with V_{BC} of 0.2 V.

P_{dc}. As shown, more than 2/3 of the g_m value remains when biasing the TC stage with V_{BC} of 0.25 V instead of -0.5 V, while reducesP_{dc} by more than half. Therefore, a positive V_{BC} of 0.25 V is selected for the two HBTs in the TC stage, with the biased J_C close to the peak g_m position (with 0.9 V base voltage).

Because of the increased I_C with emitter length at the same J_C, larger available g_m can also be obtained by selecting larger HBTs, as illustrated in Fig. 4.4b. Doubling $l_{e\text{-}w}$ does not necessarily mean twice available g_m, while consuming twice P_{dc} (with the same V_{BC} and V_{supply}). Thus, a small device ($l_{e\text{-}w}$≈2 μm) is recommended due to the better trade-off between CG (g_m) and P_{dc}, as indicated by the simulated peak g_m normalized by I_C presented in Fig. 4.4c. This also agrees reasonably with the device sizing of amplifiers analyzed in Section 3.1.3.1 because the TC stage acts as CE amplifier. As a result, BEC transistors with $l_{e\text{-}w}$ of 2.21 μm are finally selected in the TC stage. In contrast, the SQ stage should be biased with a small J_C in order to minimize V_x. Also, from equation 4.4 with certain LO pumping power and bias, choosing a large device will helps the further reduction of V_x (by the parameter θ). As a result, the transistor with large size but not reaching the upper limit, i.e., $l_{e\text{-}w}$ of 9.71 μm is eventually chosen. Here, increasing $l_{e\text{-}w}$ directly leads to the increased I_C with the same J_C. However, since the biased J_C is small, the overall increased I_C is somewhat acceptable. Nevertheless, a positive V_{BC} is also selected for the SQ stage for P_{dc} reduction. Meanwhile, the V_{supply} of the SQ stage can be combined with the TC stage, which in turn saves the effort for DC bias network design.

4.1.1.3 Mixer Implementation

Fig. 4.5 shows the schematic of the designed low-power down-conversion mixer. The mixer is designed based on gilbert-cell, with an on-chip transformer coupling between SQ (T1-T4) and TC (T5-T6) stage. Two broadband low-loss spiral baluns are designed and implemented at the LO and RF ports for single-to-differential signal conversion. As discussed in Chapter 2, at the IF output frequency (7 GHz), an on-chip passive balun based on a quarter wavelength structure consumes a large space with limited bandwidth. Instead, an active inverse balun (T7-T8) is implemented to convert the IF signal from differential back to single-ended. Consuming extra P_{dc} of around 1.3 mW, this balun offers approximately 2 dB amplification, and more importantly, obviates the need for an extra IF passive balun with its large size.



Transistor	Size (µm²)
T_1, T_2, T_3, T_4	0.13* × 9.71*
T_5, T_6	0.13* × 2.21*
T_7, T_8	0.13* × 2.21*

*Emitter window dimension,which is subtracted from drawn dimension by 90 nm

Figure 4.5: Schematic of the designed low-power down-conversion mixer.

The value of the load impedance R_{L} also requires a careful selection. The aforementioned CG of the gilbert-cell-based mixer in equation 4.2 describes the conversion capabilities of the cell itself without considering loads. For the standard mixer design, the power delivery (and power CG) can be boosted by selecting a large R_{L}, if DC power consumption is not the priority [121, 124]. In contrast, for a certain V_{supply}, R_{L} increases the actual V_{BC} of the device in the SQ stage due to the voltage division, and thus needs to be minimized. Instead of resistive load, an inductive load without supply voltage drop would be another option to generate the large Z_{L}, but at the expense of extra chip area due to the required large inductance value in (nH level).6 As a result, resistive load with 50 Ω is selected as a compromise.

In order to obtain the desired broadband and low-loss properties, both the LO and RF baluns are implemented by two pairs of $\lambda/4$ transmission lines (TL5-TL8 and TL9-TL12) located at the topmost metal layer M6. They are interleaved in a multi-turn spiral configuration, and by comparison, the on-chip transformer is designed in a single-turn completely overlapped broadside coupling configuration, as shown in Fig. 4.6. Keysight ADS Momentum is used for the balun and transformer design and optimization. The EM-simulated S-parameters of the balun and transformer, and the phase and amplitude imbalance of the balun are shown in Fig. 4.7. The results of the balun predict an insertion loss of around 4.1 dB with wide-band performance

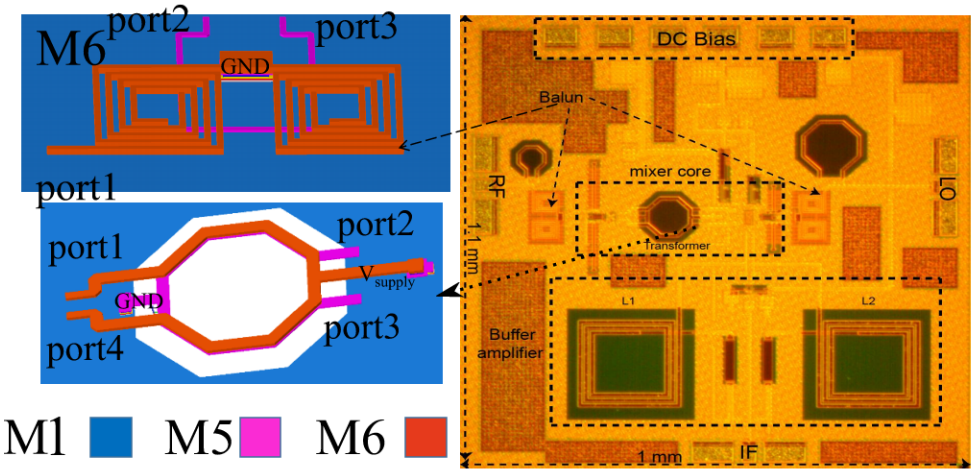


Figure 4.6: Chip micrograph and 3-D views of balun and transformer, with the total chip area of 1 mm×1.1 mm.

covering the entire W-band from 75 GHz to 110 GHz. Approximately 0.15 dB and 5° amplitude and phase difference of the two output ports indicate the generation of relatively good differential signal. Only the EM simulation result of port 1 is shown here, due to the symmetry of the transformer. A 0.9 dB insertion loss and 15 dB port isolation are obtained over the W-band. Between balun and mixing core (at LO and RF ports), the T-type inter-matching network is implemented, consisting of two MIM capacitors with one shunt stub shorted to ground in the middle, as can be seen in Fig. 4.6. Including pad structures, the total chip area of this mixer is 1 mm×1.1 mm=1.1 mm^2.

4.1.2 Results and Discussion

This mixer was measured on Wafer. The LO pumping power was generated externally by Tactron Elektronik ×6 multiplier. RF test signal was automatically controlled by VNA (Keysight PNA E8361C) with the W-band T/R module (N5260A). A VDI Erickson PM5 power meter was utilized for power calibration. A spectrum analyzer (Keysight PSA E4440A) monitored the IF signal power. An accurate on-chip power level was obtained by subtracting Probe loss from the LO and RF ports.

4.1.2.1 Measurement Results

Fig. 4.8 demonstrates the impact of LO pumping power on the mixer's CG. With the relatively low P_{LO}, the P_{LO} increase directly contributes to higher CG, but the further enhancement becomes much less after LO power reaching -3 dBm. Therefore, -5 dBm is selected and fixed in this mixer measurement below.

The comparison of simulated and measured upper side-band (USB) and lower side-band (LSB) CG is shown in Fig. 4.9a. With a 0.7 V V_{supply} and a -5 dBm LO signal at 90 GHz (USB) case and 103 GHz (LSB case), the peak USB and LSB CG of this mixer are measured to be 9.6 and 9 dB at 97 and 96 GHz, respectively. From 91 to 99 GHz, both the measured LSB and USB CG are higher than 4 dB. The USB NF is simulated to be below 14.5 dB from 91 to 101 GHz, with the minimum point of 13.6 dB at 96 GHz. The overall static P_{dc} is measured to be 12 mW, of which 8.5 mW is consumed by the mixer core and 2.5 mW by the active inverse balun. With a further reduced V_{supply} of 0.5 V, the measured maximum CG of this circuit is still observed to be 5.2 dB, dissipating an extremely low P_{dc} of 8 mW only. Fig. 4.9b presents the simulated and measured P_{IF} versus P_{RF} at the peak CG point (97 GHz) of the USB case. The measured iP_{1dB} is -20 and -16 dBm with 0.7 and 0.5 V V_{supply}, respectively, with the corresponding oP_{1dB} of

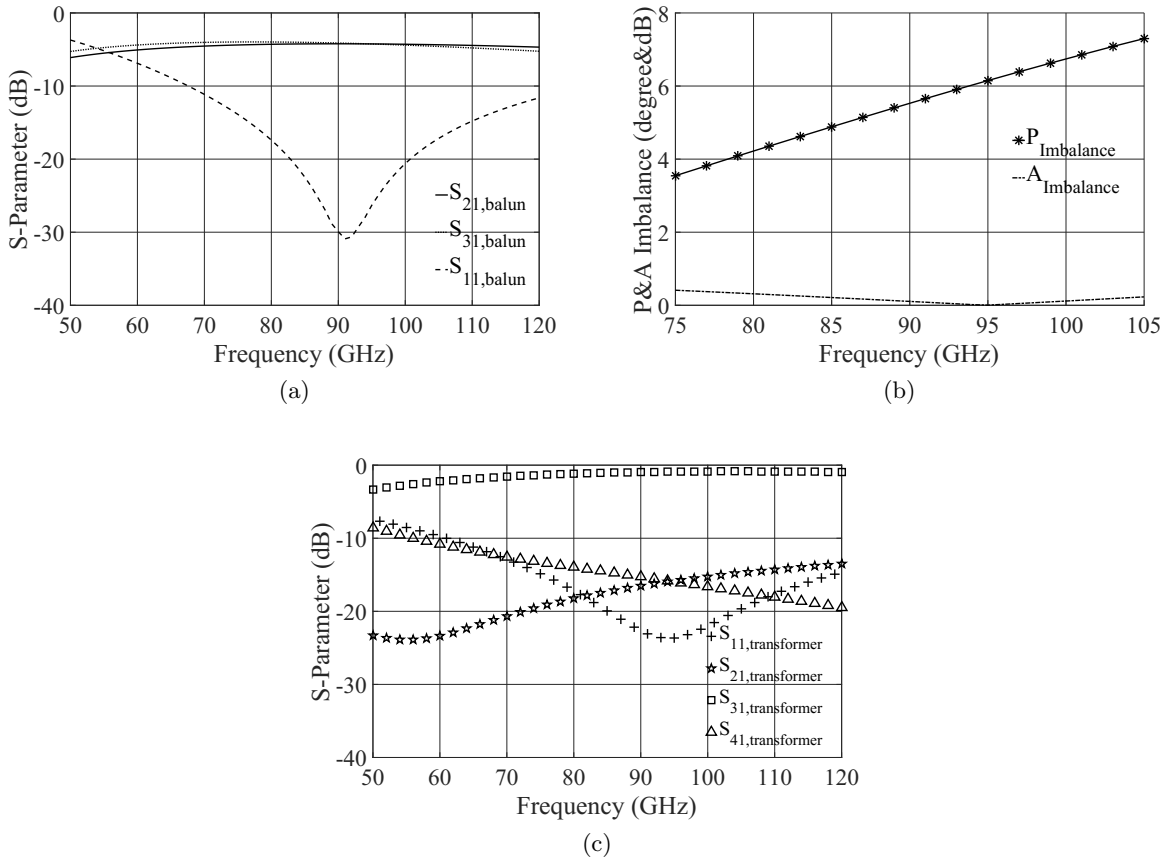


Figure 4.7: Simulated S-parameters of balun and transformer and the phase, and the simulated amplitude imbalance of the balun.

-11.4 and -11.8 dBm, respectively. As can be seen, a reasonable agreement is observed between simulation and measurement, thanks to the accurate compact HICUM model.

The measured reflection coefficients and the LO-to-RF port isolation are compared with the simulation in Fig. 4.10. Higher than -12 dB return loss is observed for RF and LO ports from 80 to 110 GHz, indicting the good power injection at these two ports. Additionally, 30 dB isolation between LO and RF port is measured.

Based on the method in [125], the large-signal stability of this mixer is analyzed. By introducing a small independent auxiliary signal at node A as shown in Fig. 4.6, the node admittance Y(f) is calculated using the harmonic balance simulator with the LO pump. As presented in Fig. 4.10, the negative Im{Y(f)} is mainly due to the capacitive components of the device, and the positive Re{Y(f)} predicts in-band stability of this circuit.

The performance of this work is summarized in Table 4.2, and compared to the previously reported W-band down-conversion mixer using SiGe technology as well as other technologies. The SiGe-based mixers reported in [117, 126, 127] are all designed using a gilbert-cell but with transistors operating still in the forward-active region, leading to a higher consumed P_{dc}. [117] realizes the highest CG of SiGe-based work in the table, yet dissipating much higher P_{dc} of around 100 mW. The mixer presented in this work consumes only 12 mW P_{dc}, which is the lowest value among SiGe-based W-band down-conversion mixers listed in the table. [128] uses the same technology (B11HFC) and V_{supply} with this design but achieves lower CG and requires higher P_{LO} and P_{dc}. Compared to the state-of-the-art low-power CMOS-based down-conversion mixer in [130], the performance of this mixer shows that SiGe-HBT-based technology with relaxed lithography (130 nm) can well compete with significantly more expensive CMOS technology in

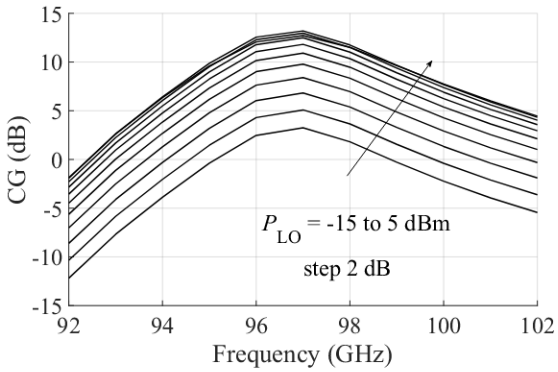


Figure 4.8: Simulated USB CG of the designed mixer with 0.7 V V_{supply} and varied P_{LO} from -15 to 5 dBm.

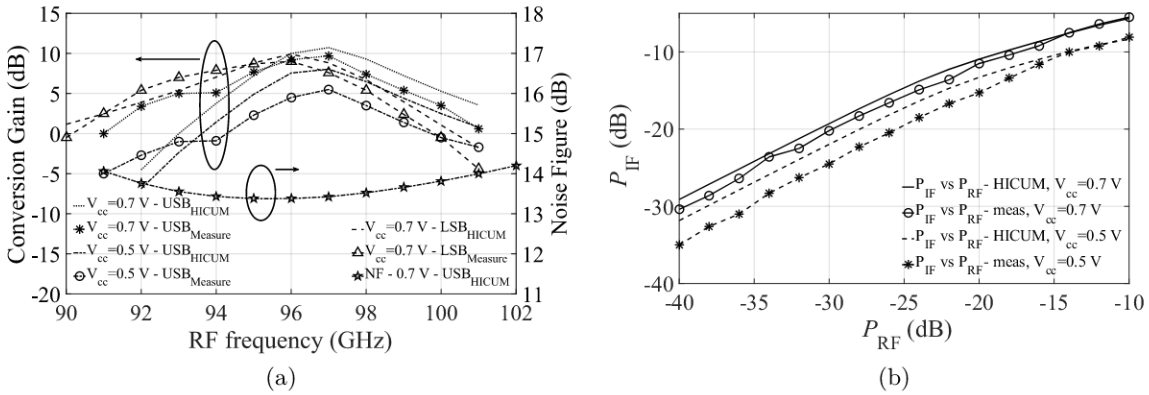


Figure 4.9: (a) Simulated and measured USB and LSB CG and the simulated USB NF of this mixer. (b) Simulated and measured results of USB P_{IF} versus P_{RF}, -5 dBm LO signal at 90 GHz.

W-band circuit performance.

4.1.2.2 Analysis

Thanks to the observed reasonable agreement between simulation and measurement, the impact of physical effects on important mixer performance parameters is analyzed in this section.

Firstly, considering the mismatch effect and process variation, a statistical analysis of this mixer is obtained. Such analysis is enabled by varying the most relevant device parameters (resulting in ±7 % change in f_{max} of the mixing core), and the external sensitive passive components in the circuit networks (such as R_{L} and R_1-R_6, ±12.5 %). The Monte Carlo method is suitable here because all the varied parameters are linearly independent. The analysis shown in Fig. 4.11 demonstrates a probability of >65 % for the realization of ± 1 dB CG variation for the three biases (V_{supply}/V = (0.3, 0.5, 0.7)).

The large-signal sensitivity for the CG of the mixer is analyzed by varying the model parameters by ±40 %. The corresponding parameters include internal and external series resistive components and parasitic capacitive components. As shown in Fig. 4.12, the external base and emitter resistances, R_{bx} and R_{e}, show a more significant impact by 36 % and 26 % CG variation, respectively. Additionally, higher than 10 % variation is also observed from external collector resistance R_{cx} and B-C parasitic capacitance C_{bcpar}.

Then, the impact of the forward-bias-related parameters dt0h, tvbl, and tef0, on the mixer's

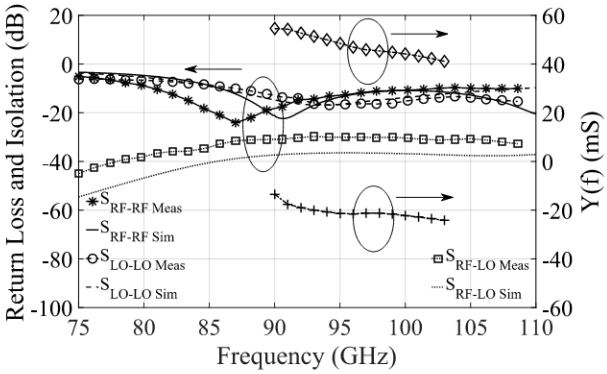


Figure 4.10: Simulation and measurement of the reflection coefficients at RF, LO port, LO-to-RF isolation, and the simulated real & imaginary part of node admittance Y(f) at node A (cf. Fig. 4.6).

Table 4.2: Comparison with published W-band down-conversion mixers

Ref.	Tech.	Topology	f_T (GHz)	f_{RF} (GHz)	CG (dB)	P_{LO} (dBm)	P_{dc} (mW)	NF (dB)	V_{supply} (V)
117	130 nm SiGe	gilbert-cell	200	95	14.4	3	92.4	19.5 (SSB)	3.3
126	90 nm SiGe	gilbert-cell	300	95	-6	0	19.7	-	-
127	130 nm SiGe	differential	210	85	10.8	-3	57	20.5* (SSB)	3.5
128	130 nm SiGe	gilbert-cell	270	94	7	0	21.8	-	0.7
This	**130 nm SiGe**	**gilbert-cell**	**270**	**97**	**9.6**	**-5**	**12**	**13.5***	**0.7**
129	65 nm CMOS	gilbert-cell	150	76	-8	-2	6	17.8 (SSB)	1.2
130	90 nm CMOS	gilbert-cell	~140	94	11.6	0	6.3	15.8 (SSB)	1
131	150 nm GaAs pHEMT	triple cascode	~100	95	-9	5	24	15 (SSB)	3

- not shown; * simulated.

CG is checked by switching on/off in the HICUM model, as presented in Fig. 4.13a, Fig. 4.13b, and Fig. 4.13c. Around 0.5-1.3 dB deviation is observed, which corresponds to around 12 % to 30% variation of the peak CG. Varying ± 20 % introduces 0.9-1 dB CG change, which transfers to around 25 % variation.

Finally, the substrate coupling effect is checked for this mixer. Unlike the small-signal impact shown in Section 3.2.4.2, the substrate coupling effect shows a smaller impact on the large-signal CG. With the same value change of Rsu and Csu, only up to 3.5 % CG change is obtained. Besides, by totally turning on/off Cjs0, a 1.3 dB (35 %) difference is observed, and the impact becomes increasingly larger with frequencies, as presented in Fig. 4.13e.

4.2 Conclusion

A W-band low-power down conversion mixer has been introduced in detail. The design process has been discussed, including topology selection and performance enhancement technique, bias selection and device sizing. In terms of CG, NF, and port isolation, highly competitive performance has been achieved simultaneously with extremely low DC power consumption, thanks to operating transistors in the moderate saturation region and careful circuit design and optimization. Additionally, first-pass success has been achieved supported by the compact model HICUM/L2. Finally, the physical-effects-related impacts on mixer performance have been ana-

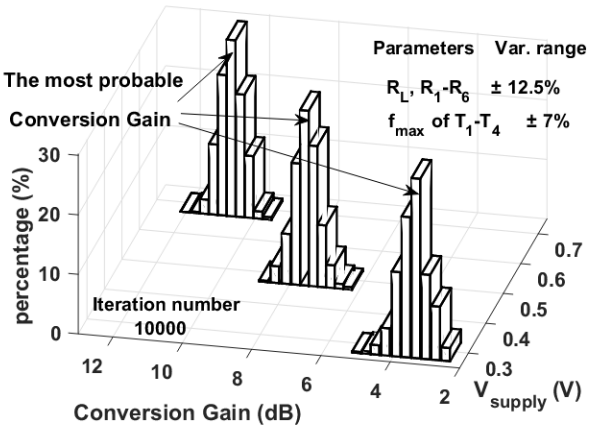


Figure 4.11: Simulated statistical analysis of the USB CG with $V_{\text{supply}}/\text{V} = (0.3, 0.5, 0.7)$.

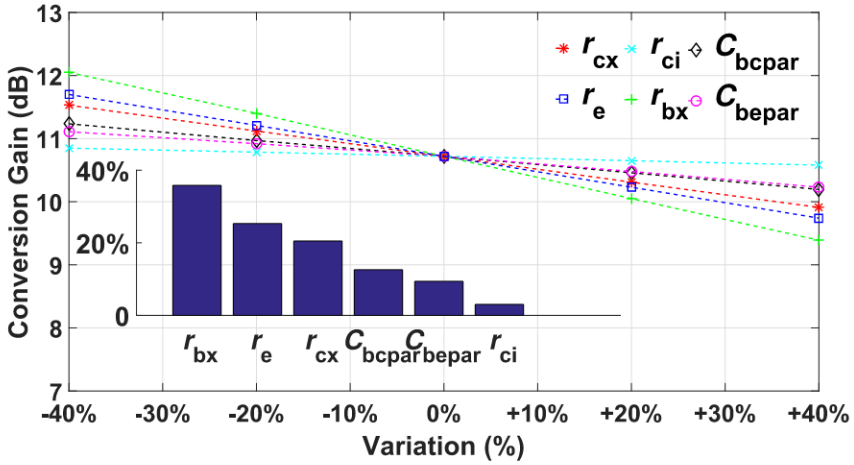


Figure 4.12: Large-signal sensitivity analysis for the peak CG of the mixer at 97 GHz with the parameter variation of ±40. The varied parameter includes internal and external series resistances and parasitic capacitances.

lyzed based on the reasonable agreement between simulation and measurement.

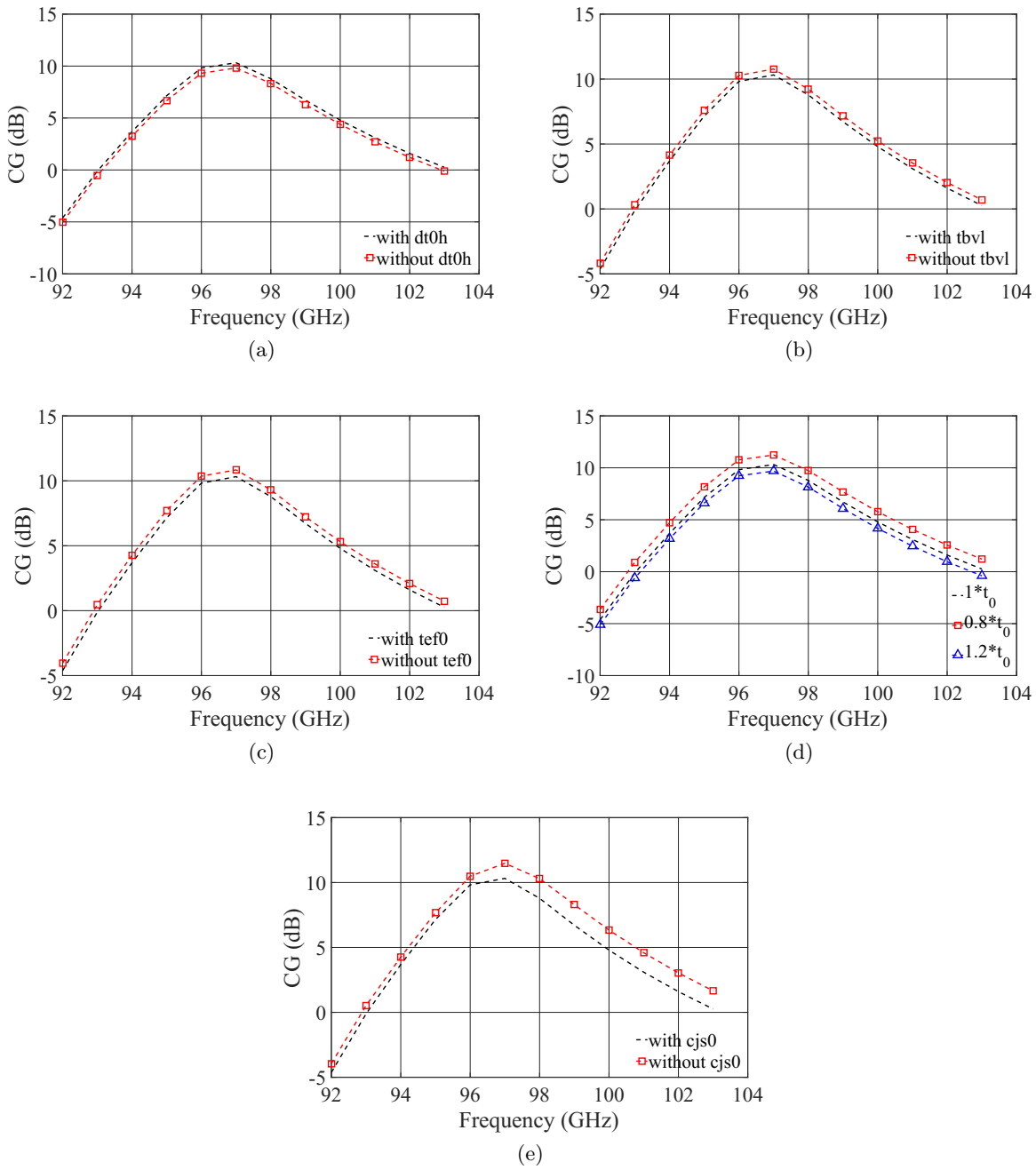


Figure 4.13: Simulated CG of this mixer with/without (a) dt0h, (b) tbvl, (c) tef0, (d) ±20 % varied t0, and (e) Cjs0.

5 Low-power Multipliers

When the frequency of operation goes up to mm-wave and sub-mm-wave region, the signal source realization with high power, stability, and low noise becomes tricky. Instead, multiplying the signal from the local oscillator at a low frequency with a particular multiplication factor is a popular solution for signal generation. Similar to the mixer, the multiplier is designed also based on the nonlinear characteristics of the devices. With one frequency component as input, the nonlinear devices generate different frequency harmonics at the output, and the crucial FoMs of multipliers are conversion gain, maximum P_{out} , and harmonic rejection.

Based on the approximate Fourier series analysis of a single HBT multiplier with the input signal of frequency ω_0 at the base in [38], the output collector current I_{n} of the harmonic frequency nω_0 can be expressed as

$$I_{\text{n}} = I_{\text{max}} \frac{4\tau}{\pi T} \frac{cos(n\pi\tau/T)}{1-(2n\tau/T)^2}. \tag{5.1}$$

Here, τ is the duration of the collector current pulse, which is controlled by the base bias, and I_{max} is the maximum available collector current of the HBT, which corresponds to the device size, T is the waveform period, and n is the order of harmonics. Assuming a perfect matching both at input and output, the P_{out} at harmonic nω_0 becomes [38]

$$P_{\text{n}} = \frac{1}{2}|I_{\text{n}}|^2 R_{\text{L}}, \tag{5.2}$$

where R_{L} is the load impedance, and the conversion gain becomes

$$CG = \frac{P_{\text{n}}}{P_{\text{in}}}. \tag{5.3}$$

Fig 5.1 presents the simulated harmonic current elements as a function of τ/T with different n based on equation 5.1. In order to improve the CG as well as the efficiency of the multiplier, I_{n} needs to be maximized. As shown, since the I_{n} decreases with n, the performance of multiplication generally decreases with n. Meanwhile, $I_{\text{n}}/I_{\text{max}}$ is determined by the ratio τ/T, and the optimum τ differs with different n.

Apart from P_{out} and CG, harmonic rejection is another essential performance parameter of a multiplier. The fundamental frequency and all undesired harmonics need to be shorted at the output, which can be realized by filters or circuit topology. As shown in Fig. 5.2a, the single-ended topology with a single device requires a passive bandpass filter at the output to filter out unwanted frequency components, and because of the relatively poor isolation, a low-pass filter is also necessary at the input. As a comparison, the differential or balanced configuration offers automatic cancellation of half of the unwanted harmonics, but at the expense of more complicated schematics and doubled P_{dc}. For the differential topology, the suppression of either even or odd harmonics depends on the multiplication factor. As presented in Fig. 5.2b, for doublers and other even-order multipliers, the differential output is connected directly (like push-

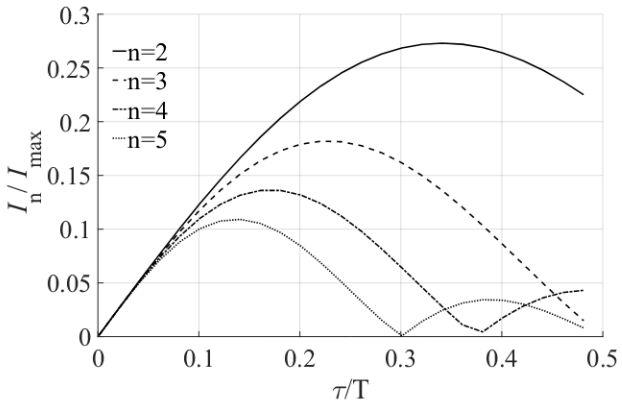


Figure 5.1: Harmonic current elements as a function of τ/T with different n.

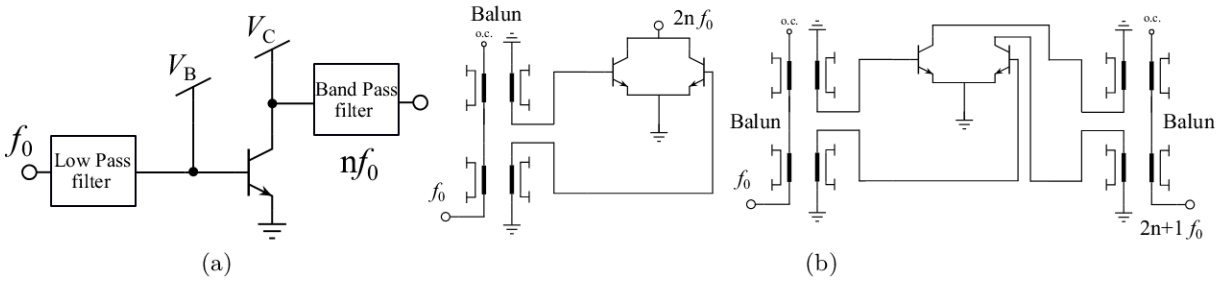


Figure 5.2: Simplified schematic (a) single-ended and (b) balanced topology of the multiplier.

push topology) so that odd harmonics are canceled automatically. For triplers and other odd-order multipliers, however, an output balun is required, and the even harmonics are canceled.

There have been several SiGe-based multipliers reported in different frequency bands. In V-band (50-75 GHz), a ×8 multiplier and a quadrupler were realized with a high harmonic rejection of 40 dBc [132]; a quadrupler was designed with 12 dB CG [133]; a tripler was designed with conversion loss but with ultra-broadband performance [134]. In E-band (60-90 GHz) and W-band (75-110 GHz), an 80 GHz tripler was designed aiming to realize a higher efficiency [135]; A 96 GHz frequency tripler was achieved with ultra-low P_{dc} of 4.7 mW [136]. In the higher frequency band up to H-band (220-325 GHz), several high-order up to ×8 multipliers were reported [137–142]. Apart from those FoMs such as CG, P_{out}, and harmonic rejection, the low DC power consumption demand is also common to most applications. The high performance of HBTs makes the operation with moderate saturation appealing for reducing the P_{dc} without significantly sacrificing circuit performance. Unfortunately, all multipliers listed above were designed with negative BC voltage of the HBT operating with relatively high P_{dc}, except [136]. Overall, the multiplier design with particular focus on low DC power dissipation are still limited.

In this chapter, a 56-66 GHz low-power frequency quadrupler and a 190 GHz G-band tripler are introduced, aiming to realize a better trade-off between performance and DC power consumption. Consequently, a G-band ×12 multiplier with two cascaded blocks is demonstrated. To the best of the author's knowledge, this is the first reported G-band multiplier chain with forward-biased V_{BC}.

5.1 General Design Flow

The general design flow of the frequency multiplier is summarized as follows:

- Base bias (J_C) selection. Since the I_n/I_{max} and the ratio τ/T shown in Fig. 5.2 are

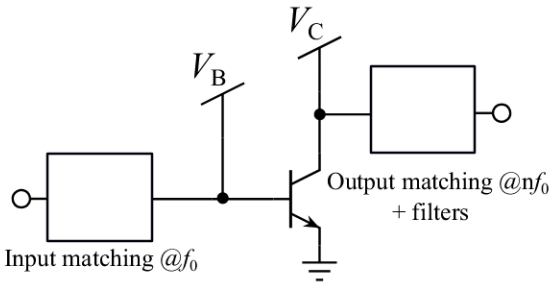


Figure 5.3: Block diagram example of the general frequency multiplier (the single-ended configuration as an example).

determined by the base bias, the biased J_C needs to be selected and optimized based on n so that I_C has the desired period. Typically, the final optimized value is slightly larger than the theoretical calculation due to the trade-off between higher maximum P_{out} and efficiency (similar to class C PA).

- Topology selection. The differential configuration helps in simplifying filter network design by automatic cancellation of half of the unwanted harmonics and provides ideally doubled P_{out} by power combination but at the expense of doubled P_{dc} and extra design effort for differential generation, like baluns or hybrid coupler.

- Device sizing and V_{supply} selection. The trade-off that needs to be considered here is the maximum P_{out} and P_{dc}. P_{out} can be improved by enlarging device size with a larger I_C and V_{supply} with higher available voltage swing, but with a larger P_{dc} as a compromise.

- Passive components design, including matching network, filter, and balun. The input network requires a perfect match at f_0, while the output should be matched at the target nf_0 (cf. 5.3). As shown in Fig. 5.1, at the optimum ratio τ/T of a quadrupler (n=4), the second harmonic I_2 is around 1.5 times larger than I_4. However, the second harmonics can not be automatically filtered out by differential topology. Hence, for the frequency multiplier with the order higher than 2, an extra filter at the output may still be required even with differential configuration.

- Layout optimization based on EM-simulation.

Following these steps, several mm-wave frequency multipliers were designed and are shown below.

5.2 56-66 GHz Low-power Frequency Quadrupler

As mentioned before, the forward-active region with negative V_{BC} is commonly utilized in most circuits to maximize the performance of the HBT. However, a better trade-off with P_{dc} requires a substantial reduction of P_{dc} while keeping performance parameters still competitive. For the multiplier with a given multiplication factor n, τ is determined by the base bias. Thus, the degree of freedom of biased J_C selection is very limited. Nevertheless, a moderately forward-biased V_{BC} with a soft reduction of V_{supply} is necessary still to save P_{dc}.

The schematic diagram of the designed V-band quadrupler is illustrated in Fig. 5.4. This circuit was realized by a single-ended configuration using a single HBT as the harmonic generation core in order to analyze the device nonlinear characterizes accurately. This quadrupler was fabricated using the 130 nm SiGe BiCMOS technology SG13G2 from IHP with high-speed HBTs of f_T/f_{max} of 300/500 GHz at V_{BC} of -0.5 V, and the details of the process were presented in Section 2.1.3. At the time of design, SG13G2 offered a SiGe device with just a single emitter

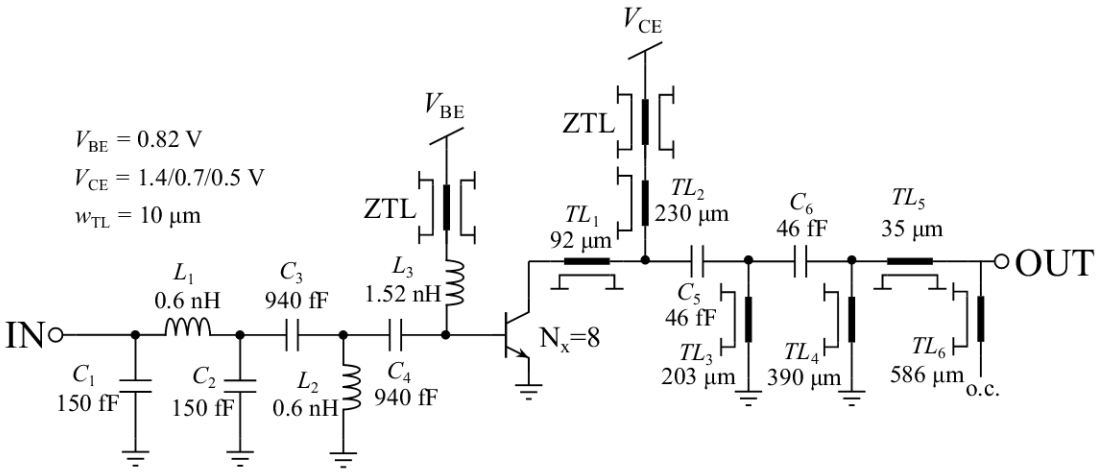


Figure 5.4: Schematic diagram of this designed quadrupler.

area but with the capability of extension to larger transistors by emitter layout duplication by N_x times up to eight. As shown in equation 5.2, increasing transistor size will directly enlarge I_n by I_{max}, which in turn enhances the P_{out} but with a higher P_{dc} as a compromise. Sufficient P_{out} is beneficial to pump the following stage if this quadrupler is placed as the front-stage in a multiplier chain with a high order number. As a result, a large device with the N_x of 8 is selected, with the emitter area A_{E0}=8×70 nm×900 nm.

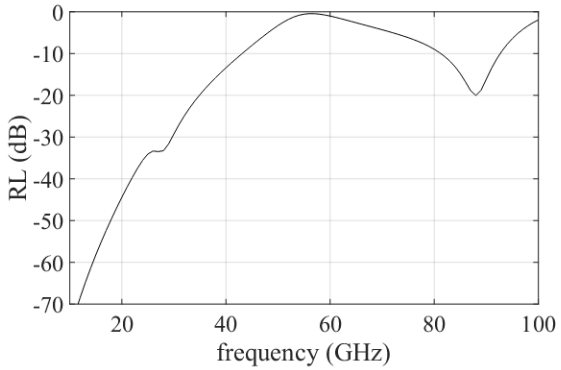


Figure 5.5: EM simulated return loss of the output filter.

The base bias V_{BE} of 0.82 V is chosen to realize the optimum τ with n close to 4, as shown in Fig. 5.1. The input part of this circuit consists of a π-type low-pass filter (C_1, L_1, C_2) together with a T-type matching network (C_3, L_2, C_4). The low-pass filter here filters out the inverse leakage from output to input, especially for high-order harmonic components. An RF choke (L_3) is used in the input DC bias network because of its lower loss at the input frequency than a resistor. At the output of this circuit, an L-type impedance matching network (TL_1 and TL_2) together with a band-pass filter ($TL_{3\text{-}6}$, $C_{5\text{-}6}$) is used to improve the harmonic rejection of this circuit. The band-pass filter contains a third-order high-pass filter ($TL_{3\text{-}5}$, $C_{5\text{-}6}$) to filter out the harmonic frequencies up to 3^{rd} order, as well as an additional $\lambda/4$ open-stub at around 87 GHz (TL_6) to further improve the rejection of 5^{th} and 6^{th} harmonic. The EM simulated return loss of the designed output filter is presented in Fig. 5.5. Around 1-2 dB insertion loss is observed for the target passband at 4^{th} from around 56 to 66 GHz. Harmonics lower than 43 GHz are filtered out by more than 15 dB loss. Thanks to the extra $\lambda/4$ open-stub, 5^{th} and 6^{th} harmonics at around 80-95 GHz are shorted with 10-15 dB attenuation. ZTLs discussed in Section 2.2.2 are used in the DC bias network, acting as AC ground with impedance close to 0 Ω, to decouple

the parasitics introduced by connection lines, DC pads, and probes.

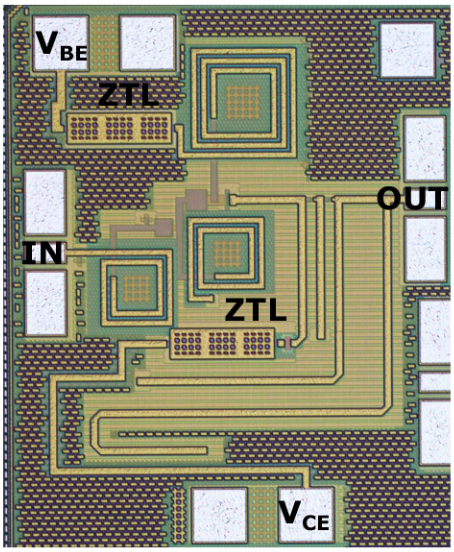


Figure 5.6: Micrograph of the designed frequency quadrupler.

The chip photo is presented in Fig. 5.6. The total chip size is 0.6 mm×0.7 mm=0.42mm^2, including all pad structures.

This circuit was measured on-wafer. The input power is generated by a signal generator (Keysight E8257D). The P_{out} was measured by a power sensor (U8488A). Spectrum analyzer (Keysight E4448A) and W-band harmonic mixer (Keysight 11970W) were used to measure the harmonic components up to 50 GHz and 75-110 GHz. Return loss was measured by a vector network analyzer (Keysight E8361C).

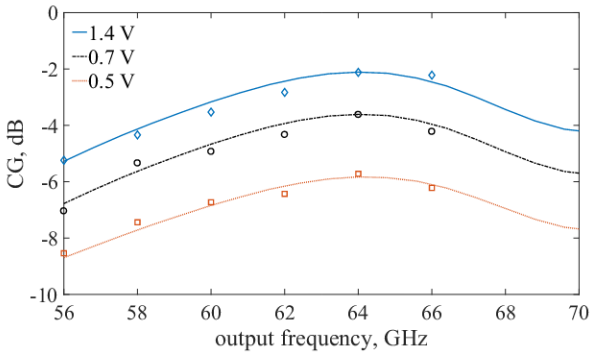


Figure 5.7: Measured (symbols) and simulated (lines) CG of this frequency quadrupler with different V_{supply}/V=1.4, 0.7, 0.5.

Fig. 5.7 presents the measured and simulated CG of this quadrupler with a -1 dBm input signal from 14 to 16.5 GHz. Firstly, this circuit is biased with a V_{supply} of 1.4 V (V_{BC}≈-0.5 V). A peak CG of -2 dB at 64 GHz is observed, consuming 2.7 mW and 25 mW P_{dc}, respectively, without and with the input signal. Keeping V_{BE} the same and Reducing V_{supply} to 0.7 V (V_{BC}≈0.1 V) leads to a slightly lower peak CG of -3.6 dB but with a significantly decreased P_{dc} of 1.35 mW and 12 mW without and with the input signal. Besides, with a further reduced V_{supply} of 0.5 V (V_{BC}≈0.3 V), this circuit still operated with a peak CG of -6.6 dB, consuming an extremely low DC power of 0.96 mW 8.2 mW without/with input power. The simulation results show an excellent agreement with the measurement, resulting in the first pass success of this circuit.

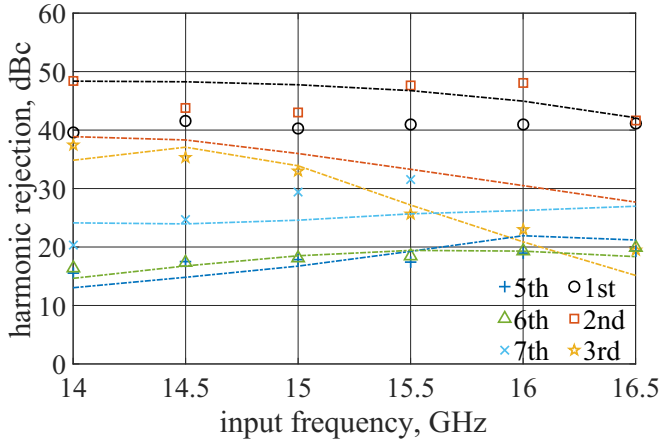


Figure 5.8: Measured and simulated harmonic rejection from 1^{st} to 7^{th} with V_{supply}=0.7 V.

The measured rejection from 1^{st} to 7^{th} harmonics of this quadrupler is shown in Fig. 5.8. As can be seen, the in-band overall unwanted harmonic leakages are higher than 15 dBc with respect to the fourth harmonics, which indicates a good spectral purity. Meanwhile, the measurement results are predicted by simulation with reasonable well agreement.

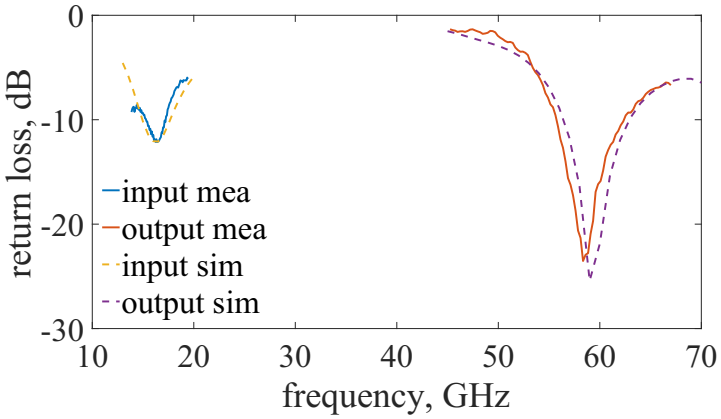


Figure 5.9: Measured and simulated return loss of the input and output port of the designed quadrupler with V_{supply}=0.7 V.

The measured input and output return loss at V_{supply} of 0.7 V is compared with the simulation in Fig. 5.9. The overall in-band return loss of the input and output port is below 10 dB, indicating a good power injection. Excellent agreement between measurement and simulation is also observed, thanks to the accurate HICUM model.

According to the good simulation-measurement agreement of this quadrupler, the impacts of several physical effects on quadrupler performance are analyzed by tuning on/off the corresponding model parameters, and the comparisons are presented in Fig. 5.10. As can be seen, the high-current effect shows a strong influence on P_{out} with more than 3 dB overestimation. Furthermore, a remarkable impact with around 1.3 dB higher P_{out} is observed by switching off the vertical non-quasi-static effect. Since this quadrupler is operating with low P_{dc}, the self-heating effect demonstrates a relatively small impact of 0.4 dB. Moreover, the substrate-coupling effect (rsu=value or 0) is also checked but with very limited impact (less than 0.1 dB), and hence is not shown in the figure.

The key FoMs of this quadrupler are summarized in Table 5.1 and compared to previously reported frequency multipliers operating at around 60 GHz using SiGe and CMOS technologies.

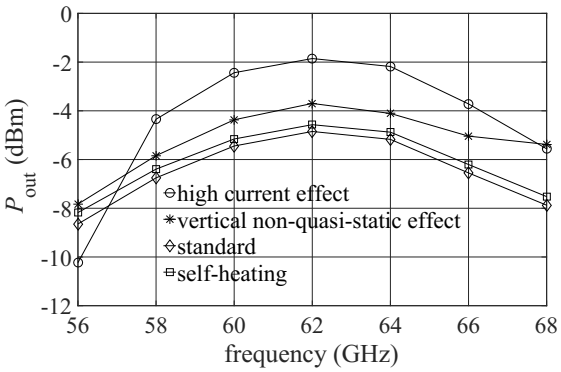


Figure 5.10: Impact of Physical effect on quadrupler P_{out}: high-current effect (tef0 and thcs=value or 0), self-heating effect (flsh=1 or 0), and vertical non-quasi-static effect (flnqs=1 or 0).

Table 5.1: Comparison with published multipliers operating at around 60 GHz

Ref.	Tech.	Topology	f_{out} (GHz)	CG (dB)	P_{dc} (mW)	HR (dBc)	BW (GHz)
APMC20 [143]	130 nm SiGe	×2+buffer+×2+buffer	46	3.2*	38*	-	10*
SiRF14 [133]	130 nm SiGe	active balun+×2+×2	67	10	92	29	25
EuMIC15 [132]	130 nm SiGe	×2+buffer+×2+buffer	68	19	350	40[1]	24
IMS15 [144]	130 nm SiGe	×3	50	-4.4	62	30[1]	8
MWCL14 [134]	130 nm SiGe	×3	61	-19	220	10	36
This work(0.7 V)	**130 nm SiGe**	**×4**	**64**	**-3.6**	**12**	**15**	**12**
Section 6.2.3.3(3 V)	**130 nm SiGe**	**active balun+×4**	**64**	**24**	**93**	**25**	**16**
MWCL19 [145]	65 nm CMOS	×2	62	0.8	14	30[1]	22
MWCL16 [146]	65 nm CMOS	×2	76	-5.5	14	20[1]	28
MWCL15 [147]	65 nm CMOS	×2	80	-4	14	19[1]	15

- not shown, * simulation; [1] fundamental rejection

As shown, the achieved -3.6 dB CG is comparable to those multipliers without integrating buffer amplifiers [144], and the higher CG realized in [132,133,143] is mainly due to the extra amplifier stages. With other competitive performance, the consumed P_{dc} of 12 mW of this quadrupler is the lowest listed value indicating the good trade-off of the multiplier design with forward-biased V_{BC}. In addition, compared to state-of-the-art CMOS-based multipliers [145–147], the result of this circuit shows that the SiGe HBTs with relaxed lithography of 130 nm can compete well with more advanced and in turn costly CMOS technologies in multiplier design. The first-pass success design was realized thanks to the compact model HICUM/L2.

Apart from the low-power quadrupler shown in this section, another V-band quadrupler with a particular focus on high CG listed here was designed as part of the LO chain in the receiver system, which will be discussed later in Section 6.2.3.3.

5.3 172-201 GHz Low-power Frequency Tripler

The schematic of the designed G-band frequency tripler is shown in Fig. 5.11, consisting of two cascaded stages. The first CE stage (T1 and T2) acts as the third harmonic generator, while the second stage (T3 and T4) is used as the buffer amplifier stage of the third harmonics. Instead of the single-ended configuration used in [148], the differential topology is chosen in this design

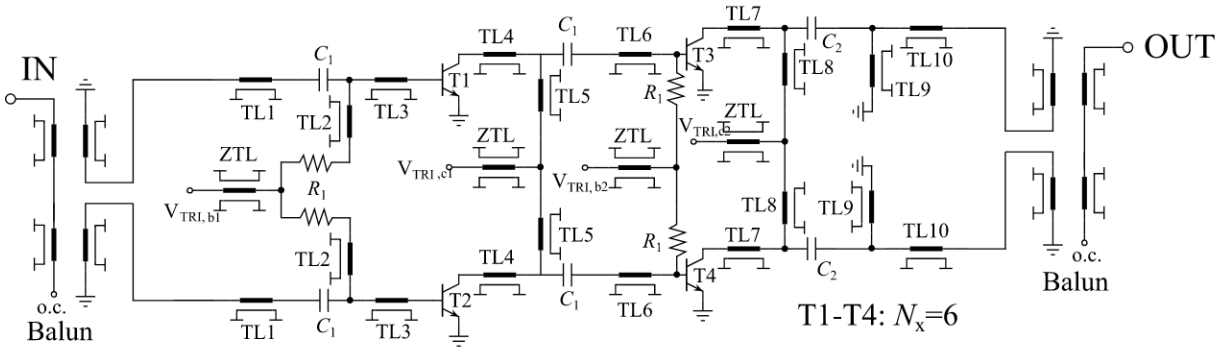


Figure 5.11: Schematic diagram of this designed G-band tripler.

in order to automatically cancel the second harmonics, obviating an extra filter (for the second harmonics) but at the expense of doubled P_{dc}. A relatively large device with N_x of 6 is selected in two stages as a trade-off between P_{out} and P_{dc}. The G-band balun introduced in Section 2.2.3.2 is implemented at the output, and a V-band balun with the same topology but operating at lower frequency is used at the input. The purpose of two baluns is the signal conversion between differential and single-ended. Fig. 5.12 shows the EM-simulated S-parameters and output phase difference of this 60 GHz input balun. From 50 to 70 GHz, this balun offers 1-2 dB insertion loss, with a minimum value of 1 dB at 58 GHz. The overall return loss of the input port is below 10 dB at 50-70 GHz, which indicates a good power injection. Meanwhile, the simulated amplitude and phase imbalance of this balun is less than 0.2 dB and 4°, respectively, indicating a good differential signal conversion. A T-type network ($TL_{1\text{-}3}$, $TL_{4\text{-}6}$, and $TL_{7\text{-}9}$) are used as

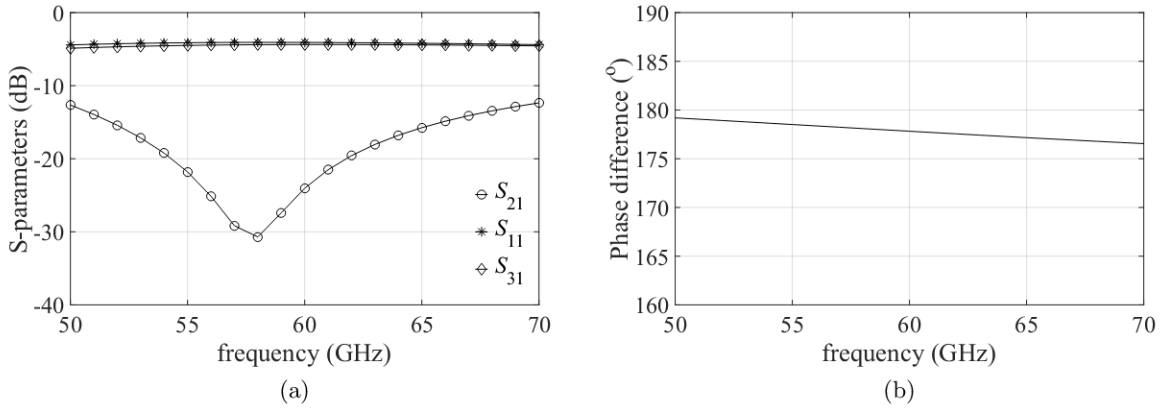


Figure 5.12: EM-simulated (a) S-parameters and (b) output phase difference of the input 60 GHz balun.

the input, interstage, and output matching, but with different frequencies: input matching at the first harmonics, and interstage and output matching at third harmonics. The resistor R_1 with 10 kΩ acts as RF open instead of RF short (of the ZTL) and is implemented at the end of TL2, because with the same realized admittance, the open-ended TL2 has a much shorter length than a short-ended line.

For base bias, 0.86 V is chosen for the first CE stage to obtain a better τ value for third harmonic generation, while 0.94 V for the second CE stage is used for power amplification. To explore the best trade-off between G-band circuit performance and P_{dc}, the supply voltage is selected as 0.7 V, with V_{BC} of 0.15 V and 0.25 V for the two stages, respectively. The chip micrograph of the designed G-band frequency tripler is illustrated in Fig. 5.13. This tripler

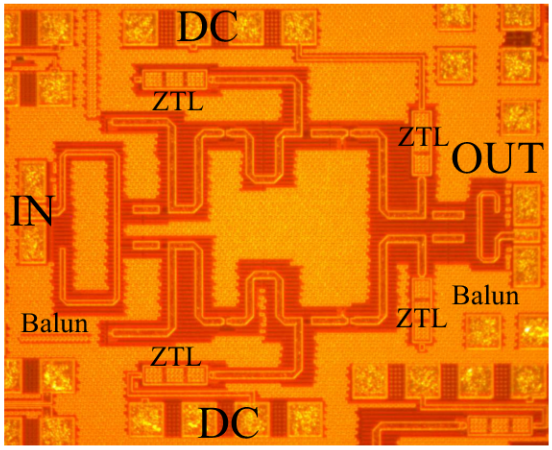


Figure 5.13: Micrograph of the designed frequency tripler.

was fabricated using the 130 nm SiGe BiCMOS technology from IHP, SG13G2, as presented in Section 2.1.3. The total size of the circuit is 1.1 mm×1 mm=1.1mm^2, including all pad structures.

The circuit was measured on-wafer. The input signal was given by the Keysight signal generator N8257D. The output signal was measured using OML WR-05 subharmonic mixer M05GWD together with the Keysight spectrum analyzer E4448A. Probe and cable losses are subtracted for accurately determining the on-chip RF power level. The input and output return losses are calibrated using a Keysight PNA-X N5247A with OML G-band VNA extender.

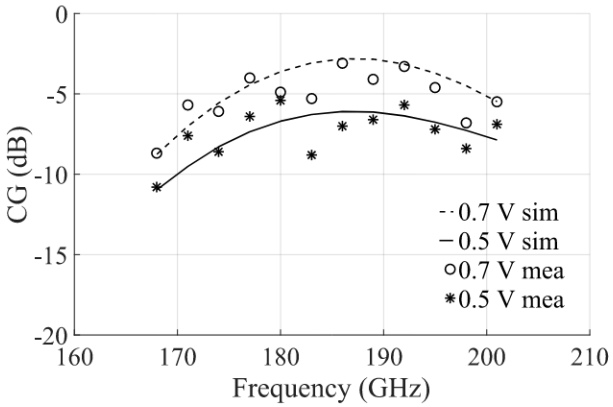


Figure 5.14: Measured (symbols) and simulated (lines) CG of the tripler with P_{in} of around -9 to -10 dBm for the supply voltage of 0.7 and 0.5 V, respectively.

Because of the limitation of the source, the available input power level is limited to around -9 to -10 dBm. With this input signal, Fig. 5.14 presents the measured CG of the designed tripler with simulation by comparison. Firstly, with 0.7 V V_{supply} , a peak CG of -4 dB is obtained at 192 GHz by this circuit with the 3 dB bandwidth of 29 GHz from 172 to 201 GHz, consuming a low DC power of 10.5 mW with the peak P_{out} of -13.5 dBm. Furthermore, reducing the V_{supply} to 0.5 V decreases P_{dc} to 7 mW and yields a slightly low peak CG of -5.5 dB at 180 GHz with 3 dB bandwidth of 29 GHz in the same frequencies. The peak P_{out} with this bias is slightly reduced to -15 dBm. Additionally, a reasonable agreement between measurement and simulation indicates the high accuracy of the HICUM model for nonlinear performance simulation in G-band.

The measured and simulated return loss of the input and output port of this circuit is presented in Fig. 5.15. The overall return loss is below -10 and -15 dB, respectively, for input and output port, which indicates the good power injection. In addition, reasonable agreement be-

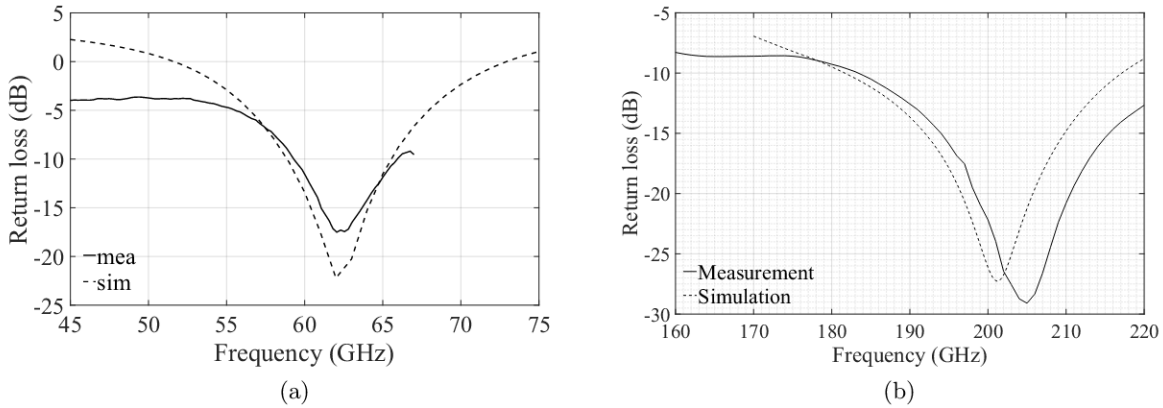


Figure 5.15: Measurement and simulated return loss of (a) input and (b) output of this tripler.

tween measurement and simulation is shown. The observed deviation may due to the inaccurate EM simulation of the passive structures and components.

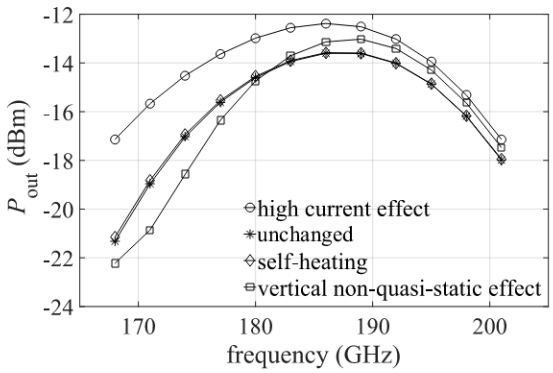


Figure 5.16: Impact of physical effect on tripler P_{out}: high-current effect (tef0 and thcs=value or 0), self-heating effect (flsh=1 or 0), and vertical NQS effect (flnqs=1 or 0).

The first-pass success design was enabled thanks to the accurate model HICUM/L2 and careful design. Based on the good simulation-measurement agreement, the impacts of physical effects on tripler P_{out} are analyzed, and the results are presented in Fig. 5.16. Since this tripler also works with low P_{dc}, the impact level of physical effects are quite similar: strong impact by high-current effect, remarkable impact by NQS effect, relatively small impact by self-heating effect, and very limited impact by substrate coupling effect (not shown in Fig. 5.16).

The performance of this tripler is summarized in Table 5.2 and compared with recently reported triplers and quadruplers operating at similar frequencies and using SiGe and other technologies. This design achieves the lowest value of P_{dc} of 10.5 mW with the input pumping power, thanks to the forward-biased V_{BC} reduced V_{supply}, with comparable RF performance in terms of CG and BW. Furthermore, the achievements of this circuit present the suitability of SiGe-based technology for high-frequency (G-band) circuit design with relaxed technology nodes compared with advanced CMOS [152].

5.4 176-193 GHz Low-power ×12 Frequency Multiplier

This ×12 multiplier chain consisting of the quadrupler and tripler introduced before was fabricated in the 130 nm SiGe BiCMOS SG13G2 technology from IHP Microelectronics. The chip

Table 5.2: Comparison with published G-band triplers and quadruplers

Ref.	Tech.	Topology	f_{out} (GHz)	CG (dB)	P_{dc} (mW)	HR (dBc)	BW (GHz)
RFIC20 [142]	130 nm SiGe	×2+×2	186	0	45	52	68
TMTT19 [139]	130 nm SiGe	×4	195	6	63	40	37
EuMIC16 [149]	90 nm SiGe	×2+PA+×2	230	-3	200	-	31
JSSC18 [141]	130 nm SiGe	×4	150	5	100	20	42
This work(0.7 V)	**130 nm SiGe**	**×3**	**188**	**-4**	**10.5**	**25***	**29**
IMWS-AMP16 [150]	100 nm GaAs	×3	190	-11	150	10	65
MWCL14 [148]	250 nm InP DHBT	×3	120	7	45	30	16
CSICS16 [151]	250 nm InP DHBT	×3	175	-1	26	20	27
RFIC15 [152]	32 nm CMOS	×4	140	-21	32	-	24

- not shown, * simulation 2^{nd};

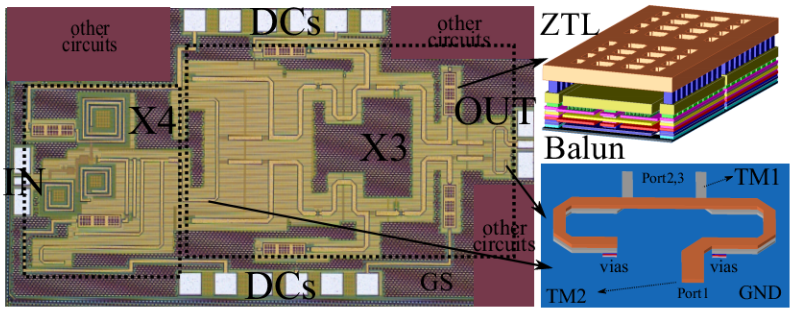


Figure 5.17: Micrograph of the fabricated ×12 frequency multiplier with the 3D and layout view of the designed ZTL and baluns, respectively.

micrograph is shown in Fig. 5.17, with the total chip size of 1.8 mm×0.9 mm=1.62 mm^2, including all pads. ZTLs and grounded sidewalls are implemented as the AC ground and to prevent crosstalk between different structures and components, respectively.

This multiplier was measured on-wafer. The input signal is generated by Keysight signal generator N8257D. The output signal and G-band harmonics were measured using OML WR-05 harmonic mixer M05GWD together with the keysight spectrum analyzer E4448A. Probe, waveguide, and cable losses are subtracted for accurately determining the on-chip power level. The return loss of input and output port are calibrated using Keysight PNA-X N5247A (input) with OML G-band VNA extender (output).

With the input pumping power injection, the total P_{dc} of the multiplier is 26 mW. The quadrupler consumes 12 mW with 0.7 V V_{supply} (V_{BC}≈0.15 V), and the tripler dissipates 14 mW with 0.8 V V_{supply} (V_{BC}≈0.1 V). Compared to the single tripler shown before (0.7 V V_{supply}), a slightly higher V_{supply} of 0.8 V is used here in this multiplier to achieve higher P_{out}. Fig. 5.18 presents the measured and simulated P_{out} and CG of this circuit with the calibrated on-chip P_{in} as a function of output frequency f_{out}. The accurate on-chip P_{in} varies slightly from -3 to -4 dBm, due to the varied losses of the probe and cable with frequencies. As shown in the figure, a peak P_{out} of -11 dBm at both 183.5 and 184.5 GHz, with a 3 dB bandwidth of 17 GHz from 176 to 193 GHz is realized, with the corresponding peak CG of -8.5 dB at two frequency points of peak P_{out}. Overall good agreement between simulation and measurement is observed. A presented 2-3 GHz frequency shift towards lower frequency may be due to the inaccurate EM simulation of the passive structures and components.

The close-by harmonics (11^{th} and 13^{th}) were measured using the same setup, and the har-

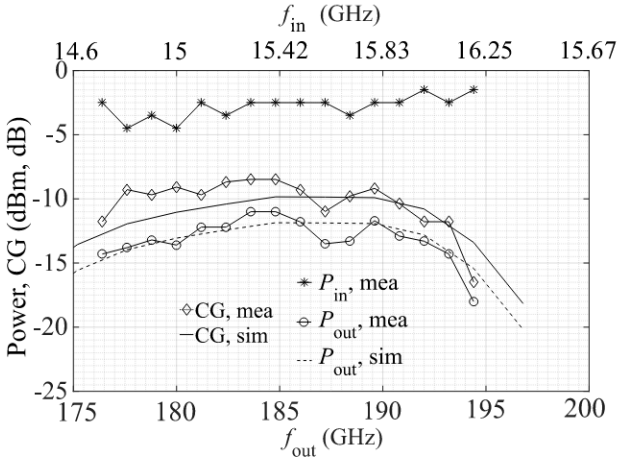


Figure 5.18: Measured and simulated P_{out} and CG of the designed ×12 multiplier, as well as P_{in} used in the measurement. Notice that the input frequency is 1/12 of the shown output frequency.

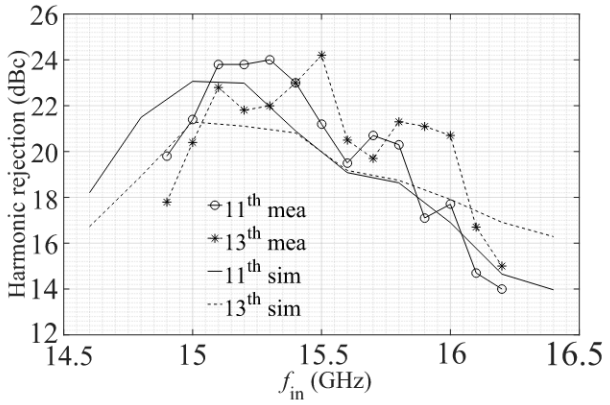


Figure 5.19: Measured and simulated close by 11^{th} and 13^{th} harmonic rejection of this circuit.

monic rejections are calculated and presented in Fig. 5.19 with the simulation as a comparison. As shown, the in-band harmonic rejections are higher than 15 dBc. The other harmonics are far away from the operating frequency, and thus will be attenuated by passive components such as the output balun. The measured harmonic rejections are well predicted by simulation, with around a 2 dB deviation.

The measured and simulated return losses of the input and output port of this circuit are illustrated in Fig. 5.20. As presented, the in-band return loss is below -10 dB and -15 dB for input and output, respectively, indicating a good impedance match of the two ports, and the measurement results are well approximated by simulation, with only 5 GHz frequency shift, which may caused by an imperfect probe contact or inaccurate EM simulation and passive component models.

The observed agreement between simulation and measurement enables the sensitivity analysis of the circuit to demonstrate the influence of physical effects on circuit performance and thus find the most critical technology-related parameters. HICUM/L2 parameters were varied by 20%, and the impact was recorded in Fig. 5.21 for P_{out}. Transistor parameters are ranked by relevance. As can be seen, the transistor parasitics (i.e., series resistances and parasitic capacitances) and the internal base-collector depletion capacitance have the most significant impact.

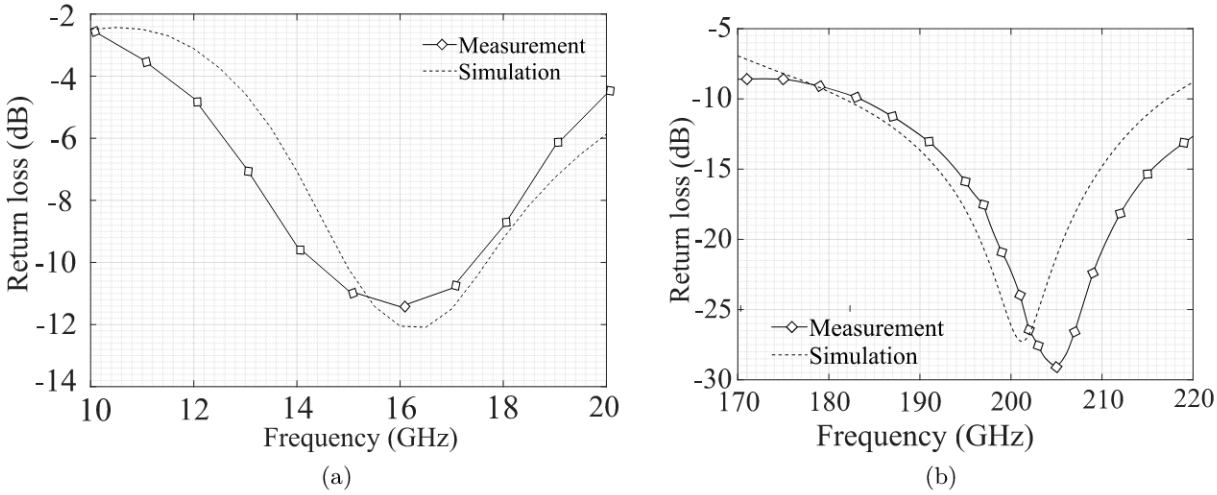


Figure 5.20: Measurement and simulated return loss of (a) input and (b) output of this multiplier.

Table 5.3: Comparison with SiGe-based multipliers with n>4 operating close to G-band

Ref.	153	154	155	156	**This work**	**LO in receiver**
f_t (GHz)	250	300	300	300	**300**	**300**
Topology	dou.×3	qua.+PA+dou.	tri.+dou.	dou.×4	**qua.+tri.**	**act.+qua.+tri.**
f_{out} (GHz)	240	240	240	240	**190**	**190**
P_{out} (dBm)	-7.7	-8	-4	-8.5	**-11**	**-6**
CG (dB)	-13.7	-12	-4	-13	**-8.5**	**23**
HR (dBc)	29	25	18-30	-	**15-24**	**35**
BW (GHz)	81	30	15	40	**17**	**34**
rel.BW (%)	32.3	12.5	6.5	15.6	**9.2**	**18**
P_{dc} (mW)	240	150	900	300	**26**	**164**
FoM	229	132	23	223	**281**	**276**

-: not available; rel. BW= $\frac{BW}{f_{out}}$.

The comparison of the designed multiplier with previously reported state-of-the-art SiGe-based multipliers with similar multiplication factors (n>4) operating at around 200 GHz is shown in Table 5.3. The data for all multipliers listed in the table do not include the end-stage power amplifier. As presented, the consumed P_{dc} of 26 mW of this design is the lowest value listed in the Table, with nearly six times lower compared to 154 which achieves only 3 dB higher P_{out}. Taking P_{dc}, P_{out}, and relative Bandwidth into consideration, a suitable FoM defined as

$$\text{FoM} = \frac{P_{out}(\text{mW}) \cdot \text{rel. BW}(\%)}{P_{dc}(\text{mW})} \cdot 10^6, \tag{5.4}$$

is used for comparison. This design yields the highest FoM value, indicating a better trade-off between P_{dc} and other key performance parameters. This circuit demonstrates the potential of G-band SiGe-based multipliers with HBTs operating in saturation region for a significant reduction of P_{dc}.

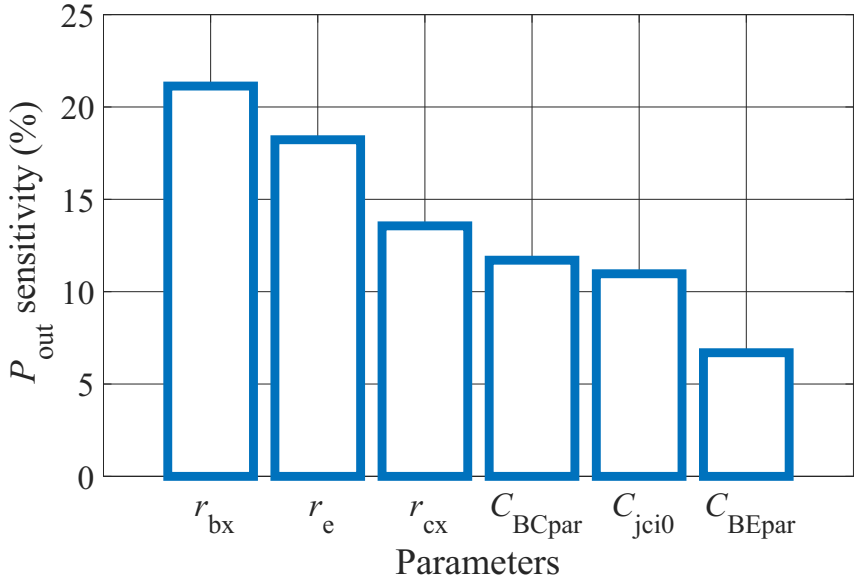


Figure 5.21: Sensitivity of peak P_{out} at 190 GHz w.r.t. important HBT parameters.

5.5 Conclusion

The low-power design approach has been applied in this Chapter to three multiplier circuits at different frequencies. The extremely low DC power consumption has been realized with other competitive multiplier performances, due to a significant decrease in supply voltage by operating the HBTs in saturation. First-pass success with good agreement between simulation and measurement have been realized thanks to the accurate modeling and careful circuit optimization, allowing a sensitivity analysis for the deeper insight of the impact of physical-effects.

6 Low-power Receivers

The receiver is a core component for mm-wave and sub-mm-wave applications. As one critical demand, reducing the DC power dissipation while keeping other key FoMs of the receiver still competitive is challenging. Since the LNA and mixer are two commonly used blocks in the receiver chain, the low-power design method introduced in the former chapters becomes good guidance in low-power receiver design. However, those discussions were mainly focused on the device and circuit level, and the further decrease of P_{dc} of the entire receiver chain requires extra measures at the system level, like topology selection, performance distribution and optimization.

In this chapter, the design and analysis of a 190 GHz low-power SiGe-based receiver with $\times 12$ LO cfhain integration is presented with as an example. This receiver is designed as a receiving channel of a G-band frequency extender specifically for a VNA-based measurement system, but is suitable for general applications with a wide LO sweeping range.

6.1 Receiver Performance

In principle, the basic functionality of the receiver is similar to the down-conversion mixer, which converts the RF signal at high frequency to IF at low frequency with the LO pumping power. Thus, the down-conversion mixer is the core block, and the significant receiver FoMs also include CG, NF, and linearity. To further enhance the receiver performance, several circuit blocks are also essential: LNA for lower NF and higher CG; IF buffer amplifiers for higher CG and linearity; IF VGA for CG tunability; on-chip LO Chain for multiplying frequency and boosting power required by mixer core.

Depending on applications, different SNR of the output IF signal of the receiver (SNR_{IF}) are required for reliable signal processing. For example, imaging, RADAR and material test need at least 10 dB SNR_{IF} [157]; high-speed wireless communication requires at least 10-20 dB SNR_{IF}, depending on modulation level, such as on-off keying (OOK) [158, 159], binary phase shift keying (BPSK) [160, 161], and quadrature phase shift keying (QPSK) [162, 163].

The thermal-related noise level of the RF signal can be expressed as

$$NF_{\mathrm{RF}} = 10\log_{10}\left(\frac{N_0 \times \mathrm{BW}}{1\ \mathrm{mW}}\right), \tag{6.1}$$

where N_0 is the noise spectral density, which is described as

$$N_0 = k_{\mathrm{b}} \times T. \tag{6.2}$$

NF_{RF} is determined by the RF noise BW and temperature. Fig 6.1 shows the NF_{RF} as the function of RF noise BW. The RF power level P_{RF}, IF noise level NF_{IF} and IF signal power P_{IF} are also displayed. As can be seen, the receiver converts the RF signal to IF with the gain of CG_{rx}, while NF_{RF} is also converted to NF_{IF} by the receiver with the same gain but adding

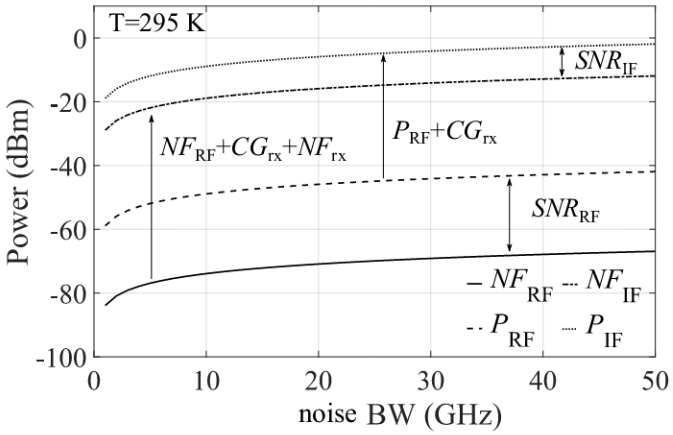


Figure 6.1: Thermal noise power of RF and IF signal as a function of the RF noise BW.

extra noise NF_{rx} introduced by the receiver itself. Therefore,

$$SNR_{\mathrm{IF,min}} = SNR_{\mathrm{RF,min}} - NF_{\mathrm{rx}}, \tag{6.3}$$

and $SNR_{\mathrm{RF,min}}$ defines the minimum detectable power of the RF signal at a certain BW of a receiver, and the required BW depends on applications. For instance, a large BW up to the range of tens of GHz is recommended in high-speed wireless links as it improves the data rates at high carrier frequencies, while in other applications such as imaging, the BW does not necessarily have to be very large (several hundreds of MHz). Common to application is the demand for lower NF_{rx} to improve SNR. On the other hand, at least several hundred mV voltage swings are desired at the IF output of the receiver for the direct interface to the analog-to-digital converter (ADC), which translates to P_{IF} higher than about -10 dBm. Sufficient IF power level helps to avoid supplementary on-chip power amplification networks. Since the value of -10 dBm is fairly large compared to the RF signal in transmission, a higher CG_{rx} and also higher output 1 dB compression point are typically advantageous as long as the input 1 dB compression point does not fall under the minimum detectable power of RF signal required for $SNR_{\mathrm{RF,min}}$.

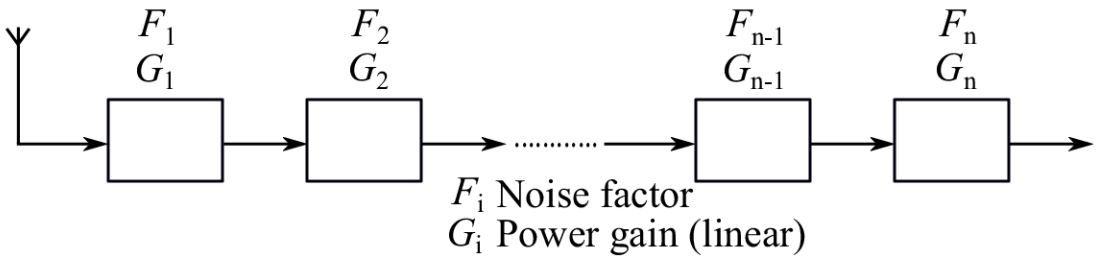


Figure 6.2: Block diagram example of a cascaded receiver for performance analysis.

For the general receiver chain with several cascaded components, the contribution of each block to the overall receiver performance should be analyzed to realize better efficiency in system performance distribution. Fig. 6.2 demonstrates the block diagram example of a receiver with n cascaded components. Notice here that the blocks include both the active circuits, like amplifiers and mixers with positive G (in dB scale), and the passive components, such as filters and balun with loss (or negative G in dB scale). Assuming all blocks in the receiver are operating linearly, the overall G in linear scale should be the product of the linear G of each block, as

$$CG_{\mathrm{rx}} = G_1 \times G_2 ... \times G_{\mathrm{n\text{-}1}} \times G_{\mathrm{n}}, \tag{6.4}$$

By the Friis formula [48], the entire noise factor of the receiver is:

$$F_{\mathrm{rx}} = F_1 + \frac{F_2 - 1}{G_1} + ... + \frac{F_{\mathrm{n}} - 1}{G_1 G_2 ... G_{\mathrm{n\text{-}1}}}. \tag{6.5}$$

As shown in equation 6.4, the overall CG_{rx} of the receiver can be boosted either by the RF LNA and mixer or by the IF blocks at the end. Generally, the CG realization at IF is much easier than at RF stages because of the design difficulty and device capability. If simply evaluating the amplification efficiency by linear gain relative to the DC power consumption ($\mathrm{G}/P_{\mathrm{dc}}$), IF circuits provide higher value. In other words, fewer stages and\or P_{dc} are required for the IF amplifier to achieve the same gain as RF blocks. However, as seen from equation 6.5, the noise contribution from the first stage of the receiver (usually are RF circuits) dominates the overall noise of the chain, and the noise from the following stages will be compensated by the front-stage gain. As a result, a relatively high gain from the LNA is critical to reducing the overall receiver noise performance.

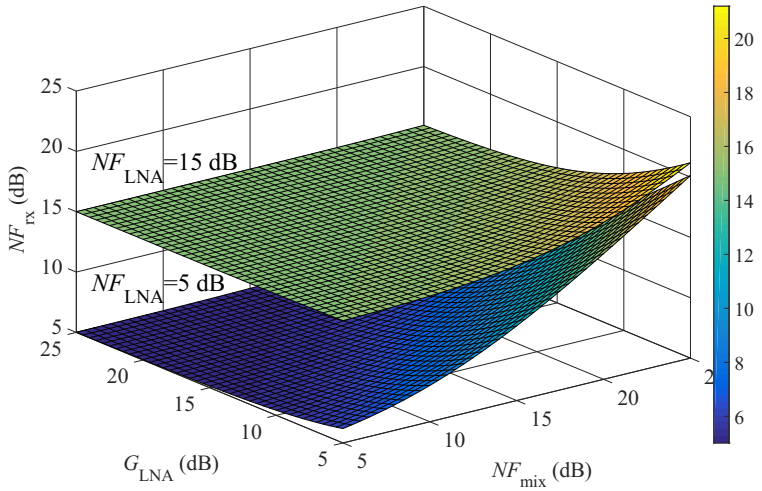


Figure 6.3: Calculated NF_{rx} of a two-stage receiver consisting of a LNA and a mixer, as a function of LNA's gain G_{LNA} and mixer's noise figure NF_{mix}, with a fixed noise figure of LNA NF_{LNA} at 5 and 15 dB.

Considering a receiver with only two cascaded stages in Fig. 6.2 with a LNA as the first block and mixer as the second for simplification, Fig. 6.3 calculates the NF_{rx} of this receiver as a function of LNA gain G_{LNA} and mixer noise figure NF_{mix}. The noise figure of LNA NF_{LNA} is fixed at 5 and 15 dB in the calculation. As shown, $NF_{\mathrm{LNA}} \approx NF_{\mathrm{rx}}$ after G_{LNA} is higher than 15 dB, even if the second-stage mixer offers a much worse NF_{mix} of 25 dB. Also, if NF_{LNA} is comparable to NF_{mix}, implementing an extra LNA only improves CG_{rx} and is no longer advantageous for NF_{rx} reduction. As a result, an LNA is preferable as the first stage as long as the good noise performance is still achievable. A reasonable rule of thumb for the operation frequency is around half of f_{max} after considering the impact of relevant parasitics in the mm-wave and sub-mm-wave range [73].

The output 1 dB compression point of this receiver $oP_{\mathrm{1dB,rx}}$ in the linear scale can be roughly expressed as

$$\frac{1}{oP_{\mathrm{1dB,rx}}} \approx \frac{1}{oP_{\mathrm{1dB,LNA}} CG_{\mathrm{mix}} G_{\mathrm{IF}}} + \frac{1}{oP_{\mathrm{1dB,mix}} G_{\mathrm{IF}}} + \frac{1}{oP_{\mathrm{1dB,IF}}}. \tag{6.6}$$

The detailed derivation of the above equation can be found in Appendix D. The overall $oP_{\mathrm{1dB,rx}}$ is determined by the smallest term among the denominators on the right of the above equation.

The oP_{1dB} requirement of the front stages can be relaxed by the gain of the following stages. Therefore, the oP_{1dB} with gain of the last stage has the most significant impact on the linearity performance of the receiver chain.

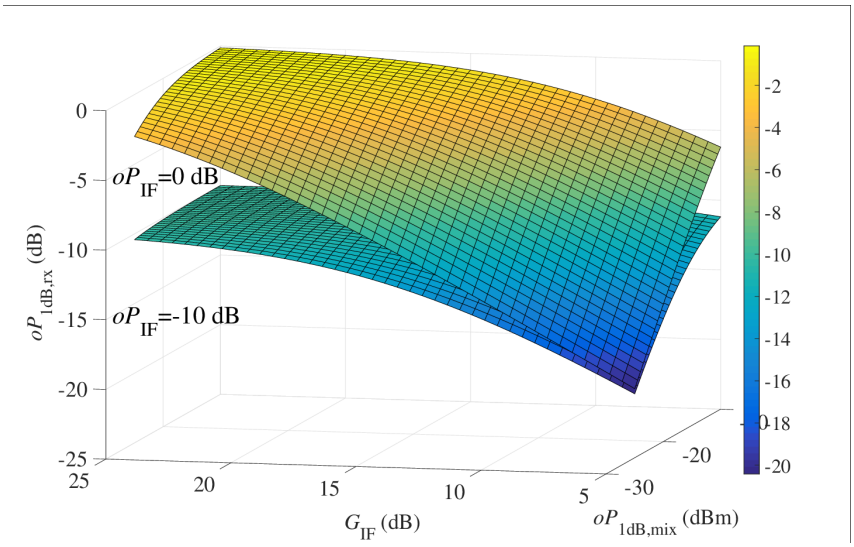


Figure 6.4: Calculated $oP_{1dB,rx}$ of a two-stage receiver consisting of a mixer and an IF buffer amplifier, as a function of IF buffer amplifier gain G_{IF} and mixer's output 1 dB compression point $oP_{1dB,mix}$, with fixed $oP_{1dB,IF}$ at 0 and -10 dB.

Now considering a two-stage receiver containing a down-conversion mixer as the front-stage and an IF buffer amplifier as the end-stage (cf. Fig. 6.2), Fig. 6.4 presents the calculated $oP_{1dB,rx}$ as the function of IF buffer amplifier gain G_{IF} and mixer's output 1 dB compression point $oP_{1dB,mix}$. $oP_{1dB,IF}$ is fixed at 0 and -10 dB. To minimize the impact of $oP_{1dB,mix}$, at least 15 dB G_{IF} is required, then $oP_{1dB,rx} \approx oP_{1dB,IF}$. Thus, high G_{IF} is favorable only if $oP_{1dB,IF}$ is higher than $oP_{1dB,mix}$.

Apart from the above FoMs, CG_{rx} tuning range and wide-band tunable LO source are two additional recommended performance parameters. The possibility of CG_{rx} tuning increases the dynamic range in receiver utilization for various applications requiring different RF BW. Additionally, a wide-band LO source is required in applications such as imaging, automotive radar with fixed IF but swept RF and LO simultaneously.

To conclude, some key points should be considered to design a receiver:

- Definition of the $oP_{1dB,rx}$, CG_{rx}, and NF_{rx}, $\triangle CG_{rx}$ based on the potential applications and utilized technology.
- Topology selection and optimization. For instance, if the device enables the design of LNA with good noise and gain performance at the frequency of operation, the LNA-first receiver topology is better for selection in terms of NF reduction. On the contrary, mixer-first topology does not have to be limited by the transistor amplification ability and thus can operate even above f_{max}, but with the compromise of less gain and worse NF.
- System performance distribution and analysis to define the priority of the design goal for each circuit.

6.2 LO Chain (×12) Integrated 190 GHz Low-Power Receiver

Various receiver works have been presented in recent years. Based on 65 nm and 40 nm CMOS technologies, a 240 GHz and a 260 GHz receiver were reported in [164], and [165]. Nevertheless,

due to the limited device speed mentioned in Section 1.1, the realized CG_{rx} is only 25 dB and 2 dB, respectively. As a comparison, SiGe-BiCMOS-technology-based receivers demonstrated better gain performance. For instance, a 47 dB CG_{rx} 190 GHz receiver [166], and three 240 GHz receivers with up to 44 dB CG_{rx} were achieved [167–169]. However, all SiGe-based receivers listed above consume more than 100 mW P_{dc} in their receiver cores and 250 mW if including a complete LO chain.

In this section, a 190 GHz down-conversion-mixer-based low-power receiver system with LO ×12 chain integration is introduced. This receiver is realized in the 130 nm SiGe BiCMOS SG13G2 technology from IHP, featuring high-speed npn HBTs with $f_{\mathrm{T}}/f_{\mathrm{max}}$ of 300/500 GHz. The details of this technology were shown in Section 2.1.3.

6.2.1 Receiver Architecture

This receiver has two goals. The first one is to explore the best possible trade-off between key performance parameters and P_{dc} for mm-wave and sub-mm-wave SiGe-based receivers. The second target for this receiver is to be used as one receiving channel of a G-band frequency extender for on-wafer device characterization utilizing a commercial vector network analyzer (VNA). A simplified block diagram in Fig. 6.5 shows the operation principle of this receiver

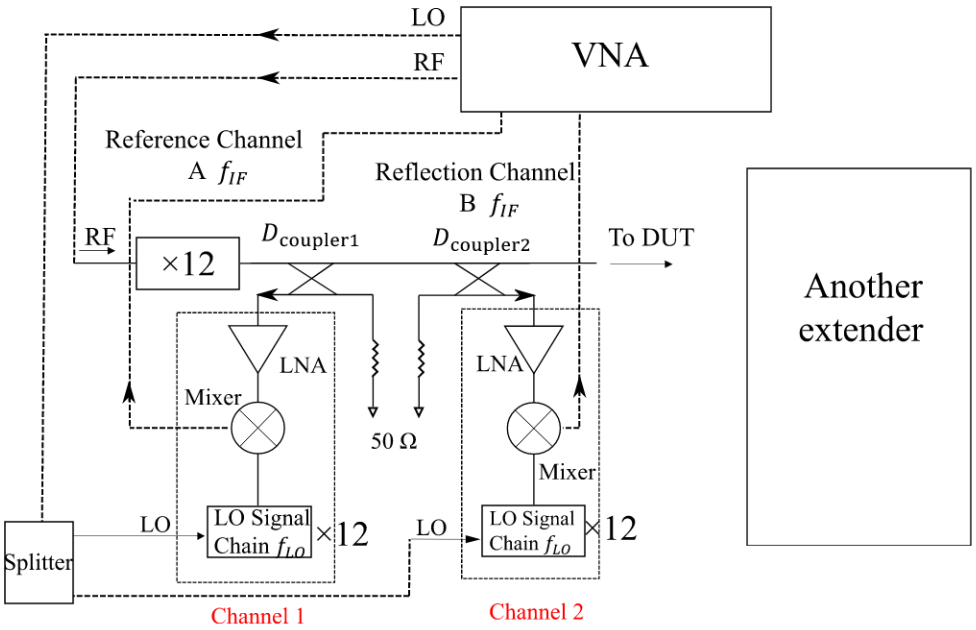


Figure 6.5: Simplified block diagram of this receiver working as one channel of a frequency extender controlled by VNA for on-wafer S-parameter characterization.

channel in a VNA-based frequency extender system. As shown, since the LO signal at around 15 GHz is externally controlled by the VNA, a LO chain with a multiplication factor of 12 is required on-chip. Besides, the IF frequency should be fixed at around 0.5 to 1 GHz to directly communicate with the VNA. Hence, both the RF and LO signals are swept during the characterization over a wide range covering the overall G-band. Additionally, to alleviate the power requirements of the LO control signals from the VNA especially when a power splitter has been used to pump several receiving channels simultaneously (cf. Fig. 6.5), a high CG becomes another design target for this LO chain.

To conclude, the main FoMs is summarized here to finalize the receiver architecture. Because a low DC power dissipation is a general target, the specific FoMs are evaluated by the second goal of this receiver, which are

- At least 10 dB SNR_{IF};

- The frequency extenders for S-parameter characterization operate with BW of up to several hundred MHz typically, and thus a bit critical value, 1 GHz RF BW, is reasonable to be used here for evaluation of receiver architecture.
- Higher than -10 dBm IF output power is required for several hundreds of mV voltage swing to direct interface with the VNA;
- Low NF and high CG_{rx}, together with a certain level of $\triangle CG_{\mathrm{rx}}$ (usually 15 dB);
- $\times$12 LO chain with high gain and enough output power to pump the down-conversion mixer.
- Both the RF and LO circuit require a large BW for G-band device characterization.

Assuming T=22 °C (295.1 K), which is a typical room temperature for circuit operation, the calculated RF noise floor is -84 dBm with 1 GHz RF BW based on equation 6.1. If NF_{rx} is around 15 dB, $SNR_{\mathrm{RF,min}}$ turn out to be 25 dB based on equation 6.3 with the corresponding minimum detectable RF power of around -59 dBm. Therefore, a maximum CG_{rx} of around 50 dB is desired. Meanwhile, to improve the signal detection dynamic range as well as make this receiver also suitable for other applications requiring higher RF BW up to 15-20 GHz, a $\triangle CG_{\mathrm{rx}}$ of around 15 GHz is recommended.

Choosing a suitable receiver topology and circuit blocks is the next step. Fig. 6.6 presents

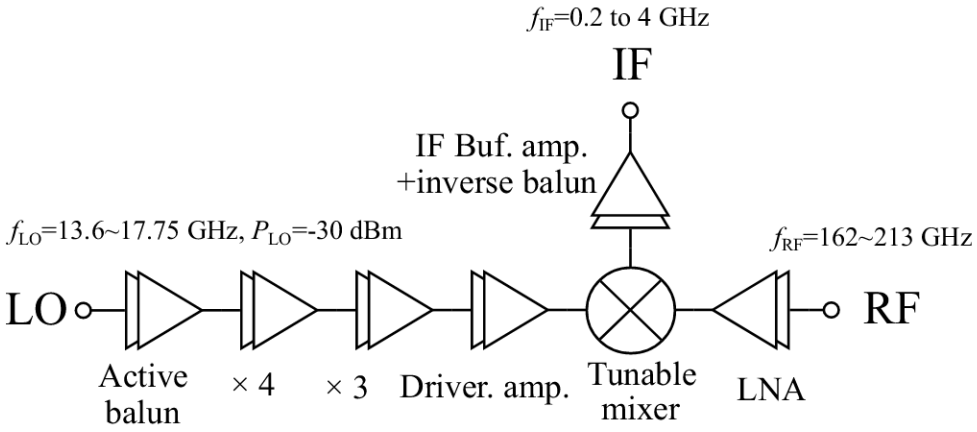


Figure 6.6: Block diagram of the implemented receiver.

the block diagram of the proposed receiver. At around 200 GHz, several G-band SiGe LNAs using the same technology (SG13G2) have been reported with a good noise performance of around 8 dB [64, 65, 74, 76]. As a comparison, the G-band down-conversion mixer provides much worse noise performance above 16 dB (SSB NF) [119, 170]. On the other hand, the listed G-band LNAs provide around 8 dB gain per stage, which is also much higher than that of the mixer, and according to equation 6.5, a higher front-stage gain is beneficial to reduce the noise contribution from the following stage. As a result, a G-band LNA is finally selected as the first stage at RF. Then, an active down-conversion mixer is utilized as the mixing core. Here, the fundamental mixer is used instead of higher-order because of two reasons. Firstly, the fundamental mixer offers higher CG and lower NF. Additionally, the on-chip $\times$12 LO chain (without driver amplifier) can be directly used to generate the G-band test signal of the frequency extender, as shown in Fig. 6.5, which significantly reduces the design effort. At IF, an additional IF buffer amplifier (BA) is implemented to provide sufficient IF output power as well as CG_{rx}. An active inverse balun is used at the end of IF to convert the IF signal from the differential to single-ended for on-chip verification before packaging.

The on-chip ×12 LO chain is integrated with the receiver. It consists of a ×12 multiplier followed by a LO driver amplifier (DA). The multiplier contains a quadrupler together with a tripler to realize the multiplication factor of 12, as well as a high CG for the sake of relaxing the frequency demand by the direct LO control signal and also the power level by the common LO pumping signal for the multi-channel system after off-chip power splitting. The DA at the end aims at further boosting the output power for the mixer. Since the multiplier is differentially operated, an active balun is placed as the first stage to generate the differential signal at around 15 GHz.

6.2.2 Low-power Considerations

Exploring the best trade-off between performance and P_{dc} is another goal of this receiver. Among all general critical points for receivers listed before, several additional considerations should be taken concerning P_{dc} reduction while keeping good receiver performance.

To begin with, achieving those FoMs of the receiver but using fewer circuit blocks is the key. Typically, the mixer core of the receiver is designed with certain CG, and CG tunability is realized by a variable gain amplifier (VGA) at IF [166–169]. However, due to the stacked configuration, an IF VGA usually requires high V_{supply}, which results in at least 50 mW P_{dc} even with the smallest device size [166]. In this design, the $\triangle CG_{\mathrm{rx}}$ is obtained directly by the down-conversion mixer instead of an extra IF VGA, which significantly saves overall P_{dc} of the receiver.

Secondly, a careful FoM distribution and operation analysis for each circuit block is desired to finalize each design goal. Since the maximum output power level of a circuit is positively correlated to the bias voltage and current (and in turn P_{dc}), the P_{dc} reduction methods more or less decrease the output power level as a compromise. However, as demonstrated in equation 6.6, the last stages, i.e., the IF circuities of this receiver, dominate the overall linearity and $oP_{\mathrm{1dB,rx}}$ as long as G_{IF} is high enough to compensate the relatively low oP_{1dB} of the front stages. Thus, the LNA and mixer of a low-power receiver do not necessarily offer very high output power by consuming high P_{dc}. On the other hand, Fig. 6.3 indicates that around 15 dB gain is required by the LNA to minimize the noise contribution of the following stage. A higher gain by cascading more gain stages in the LNA would only be beneficial to enhance the overall CG_{rx} while sacrificing more P_{dc} than the IF BA. In summary, for this low-power receiver, the design goals of each block are:

- LNA: The lowest possible NF, high enough gain (of around 15 dB), wideband performance;
- Down-conversion mixer: high CG with a certain level of CG tunability, wideband performance;
- IF circuities: enough oP_{1dB} and high gain to achieve the overall CG_{rx}, and differential to single-ended conversion.

By careful analyzing of the dynamic range of each circuit block and FoM distribution, overall DC power consumption will be indeed saved.

In addition, low-power considerations at circuit level are also recommended, especially for the output power relaxed LNA and mixer. The first step is the careful choice of the device dimension. As long as the emitter is long enough, f_{T} as a function of J_{C} is independent of emitter length. Hence, selecting a transistor with a shorter emitter length results in a direct reduction of I_{C} and in turn P_{dc} if V_{supply} stays the same. Meanwhile, further P_{dc} reduction requires a different bias selection with reduced V_{supply}, and the low-power LNA and mixer design with forward biased V_{BC} introduced in previous chapters are suitable candidates. For this technology, the operation of HBTs with moderately forward-biased V_{BC} also offer an acceptable speed. As shown in the comparison between simulated and measured f_{T} and f_{max} of the device in SG13G2

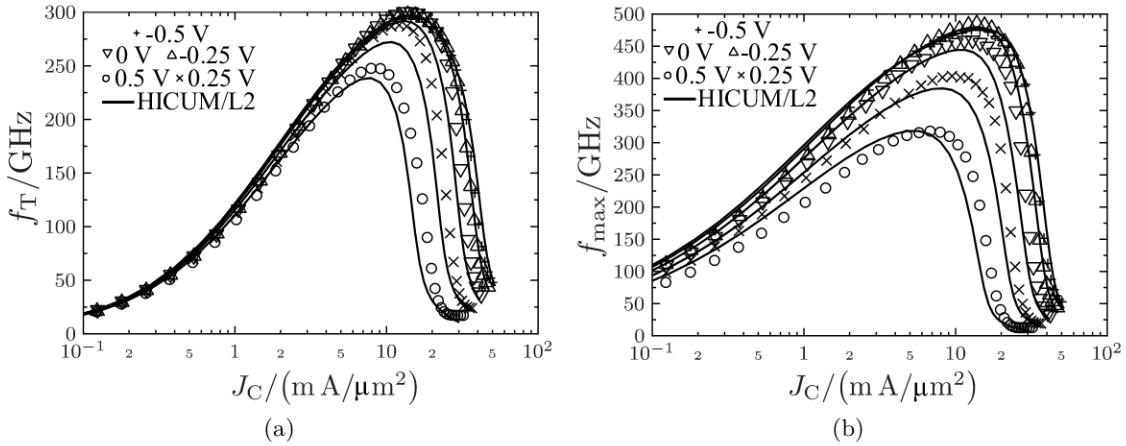


Figure 6.7: Measured (symbols) and simulated (lines) (a) f_T and (b) f_{max} as a function of J_C with various V_{BC} of an HBT with an emitter window area A_{E0}=8 ×70 nm×900 nm [36].

technology in Fig. 6.7, at least 250 GHz f_T and 300 GHz f_{max} can still be realized even with an aggressively forward biased V_{BC} of 0.5 V, which makes a substantial reduction of P_{dc} feasible while maintaining small-signal performance. On the other hand, the relatively low linearity and output power level of the LNA and mixer can be compensated by the high-gain IF BA as the final stage and thus have a limited impact on the overall large-signal performance of this receiver. Therefore, the operation of RF front stages in moderate saturation is promising for low-power receiver design.

6.2.3 Building Blocks

6.2.3.1 LNA and LO DA

As discussed before, a LNA and a LO DA are required as the first stage of RF and final stage of LO, but with different design goals. Low NF and around 15 dB gain are desired for the LNA, while reaching enough output power to pump the mixer is the primary goal of the LO DA. The amplifier topology needs to be chosen firstly. Based on the comparison shown in Section 3.1.1, the cascode configuration offers higher available gain per stage with similar NF performance and output power level than the CE and CB configuration, with the best output-to-input isolation, which is especially beneficial in the receiver system design. Hence, both LNA and LO DA are designed with cascode configuration.

As the first stage operating at a relatively low power level, the LNA is designed with the transistor operating in saturation, and the design process has been described in Chapter 3. The device with an N_x of 2 is selected due to its shown good trade-off between small-signal performance and P_{dc}, as well as the good impedance response for noise matching.

Using the relationship expressed in equation 3.3 and setting the same actual V_{BC} for the upper CB and bottom CE device, the simulated MSG/MAG and NF_{min} of an ideal cascode stage (N_x=2) as a function of J_C at 190 GHz is presented in Fig. 6.8. As shown, if selecting the minimum NF_{min} at J_C of around 6 mA/µm^2, the available MSG/MAG is more than 3 dB lower than the peak value. In contrast, NF_{min} increases rapidly by 4 dB if J_C with peak MSG/MAG is chosen. As a compromise, V_{BC}=0.2 V and J_C=12 mA/µm^2 are selected. Compared to V_{BC} of -0.4 V, this bias selection significantly decreases V_{supply} from 2.6 to 1.4 V with nearly half of P_{dc} (if biased with same J_C) but with around 3 dB lower available MSG/MAG (also a reduction with a factor of 2), due to the selected positive V_{BC}. Gratefully, such gain degradation can be compensated by the G_m-boosting technology shown in Section 3.1.4.1, by implementing two

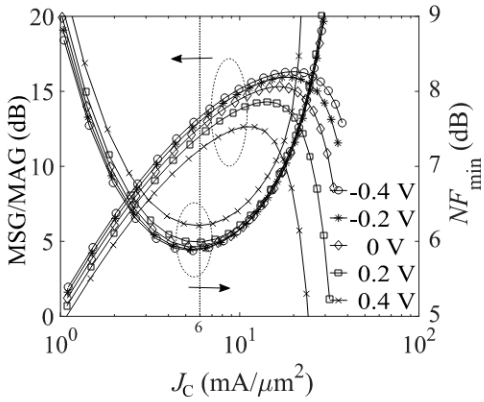


Figure 6.8: Simulated MSG/MAG and $NF_{\min}$ as a function of J_C at 190 GHz for the ideal cascode stage with N_x of 2 with various V_{BC}. Here V_{BC} of CB and CE devices are the same.

small inductors into the cascode stage, as shown in Fig. 6.9a.

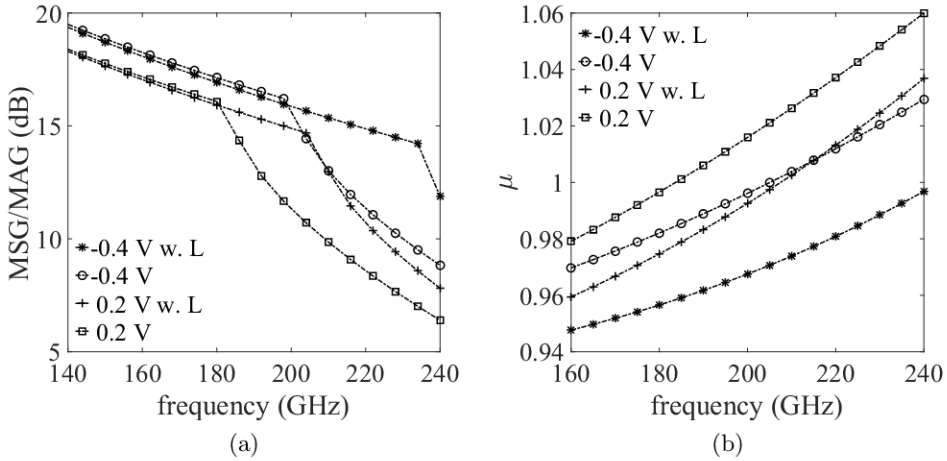


Figure 6.9: Simulated (a) MSG/MAG and (b) μ factor versus frequency of the ideal cascode stage for V_{BC} of -0.4 V and 0.2 V with and without 5 pH small inductors. An ideal cascode stage with the device of N_x=2 with J_C=12 mA/µm^2 is used.

Additionally, the stability factor μ is simulated as a function of frequency in Fig. 6.9b. Compared to V_{BC}=-0.4 V, a similar μ value at V_{BC}=0.2 V with inductors indicates no additional instability risk introduced by forwarded-bias operation with G_m-boosting inductors.

Fig. 6.10 shows the simulated output power of the ideal cascode stage as a function of J_C at also 190 GHz, with devices of N_x=2. As presented, the observed 2 dBm is sufficient to reach the LO pumping power requirement of the gilbert-cell-based down-conversion mixer as described in Section 4.1.2. Therefore, N_x of 2 is also selected for LO DA. However, V_{BC} of -0.4 V and J_C of 22 mA/µm^2 are chosen for the LO DA for higher output power.

The schematic of the designed LNA and LO DA is presented in Fig. 6.11. As mentioned before, around 15 dB gain is required for the first-stage LNA, and thus two stages are selected for LNA due to the approximately 8 dB gain per stage. Notice that the LO DA is also designed with two stages of similar gain, although the gain is not the primary goal. The main concern here is to reserve a certain budget during the LO chain so that the entire chain can still work even if the multiplier does not offer enough output as expected. Besides, the LO chain as mixer

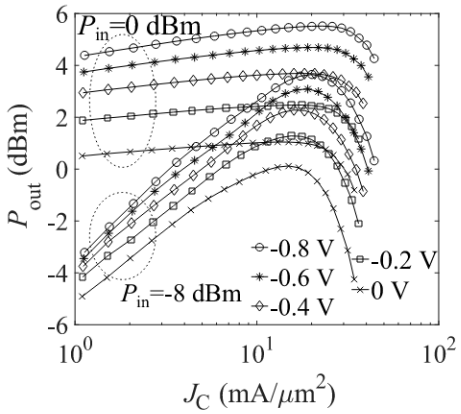


Figure 6.10: Load-pull simulated output power as a function of J_C at 190 GHz for the ideal cascode stage with N_x of 2 with various V_{BC}. Here V_{BC} of CB and CE devices is the same.

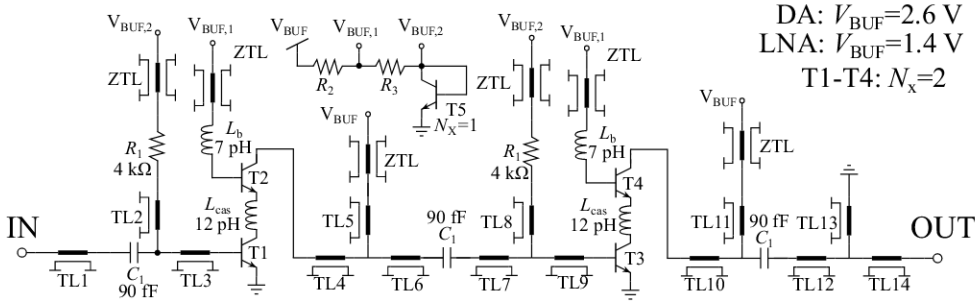


Figure 6.11: Schematic of the designed LNA and LO DA. The two inductors are not used for LO DA due to stability reason.

pumping does not necessarily operate in the highly linear region if the harmonic rejection is high enough, and thus the over pump of the LO DA is acceptable. Also notice that the two G_m-boosting inductors are not implemented in the the LO DA. One reason is that, with negative V_{BC}, the gain per stage is already enough, especially when the gain is not the most critical target. Another reason is the stability issue. As shown in Fig. 6.9b, adding two inductors reduces μ factor to a value smaller than one at 200 GHz with the negative V_{BC}.

Typically, the differential configuration provides theoretically doubled output power and virtual ground nodes, which help stabilize the circuit but at the expense of doubled P_{dc}. In this work, the output power is not the primary goal of the LNA, and the single-ended operation already provides enough power for the LO DA. Meanwhile, the stability issue can be overcome by implementing ZTLs as discussed in Section 2.2.2. As a consequence, both the LO DA and LNA are designed with a single-ended configuration. The T-type matching network is used at the input, and the dual-band matching network is used both as interstage and output for wide-band performance. Details have been discussed in Section 3.1.5.3.

The simulated small-signal performance of the complete LNA and LO DA is presented in Fig. 6.12. The LNA and LO DA offer a similar simulated gain of around 18 dB, with a 3 dB BW of 32 and 35 GHz, respectively. The in-band S_{11} and S_{22} of the two amplifiers are lower than -6 dB, which indicates a good match both at the input and output ports. The simulated NF of the LNA is around 9 dB, as shown in Fig. 6.12a.

Fig 6.13 shows the large-signal performance of the two amplifiers. The in-band oP_{1dB} of the LNA is simulated to be around -19 to -13 dBm, with the corresponding iP_{1dB} of around -35 to -22 dBm. This value is enough for the front stage of this receiver, as discussed before. The

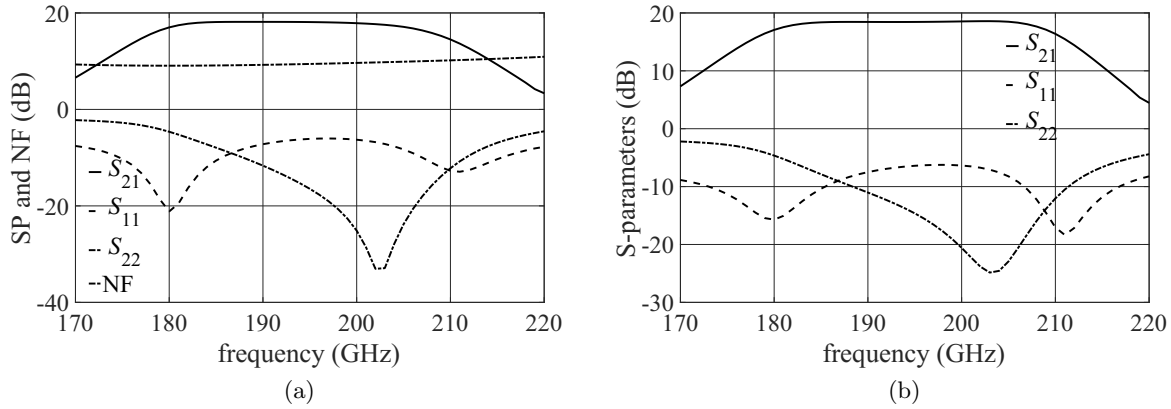


Figure 6.12: Simulated S-parameters and NF of (a) LNA, and S-parameters of (b) LO DA.

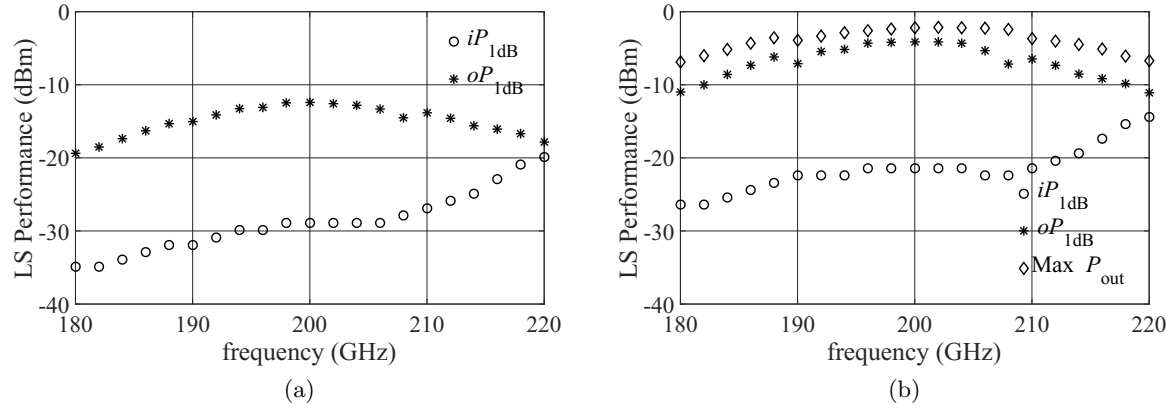


Figure 6.13: Simulated oP_{1dB} and iP_{1dB} of two amplifiers, as well as the maximum output power of LO DA.

maximum output power of the LO DA is -6 to -3 dBm, which is sufficient for the LO pump of the mixer core. Including the voltage distribution networks (T5 in Fig. 6.11), the consumed P_{dc} of LNA and LO DA are 9 and 25 mW, respectively. If comparing with the previously reported LNA designs operating at around 200 GHz using the same technology (SG13G2), the LNA designed in this work achieves a higher ratio of linear gain divided by P_{dc} (gain(1)/P_{dc}) of 8.22/mW than 7.87/mW in [66] and 2.72/mW in [65].

6.2.3.2 Tunable Mixer and IF BA

The schematic of the designed tunable mixer with IF BA and active inverse balun is presented in Fig. 6.14. The main design process and analysis have been introduced in Chapter 4. This tunable mixer is also based on the gilbert-cell topology, with T1-T2 as the TC stage and T3-T6 as the SQ stage. T7-T8 are the differential IF buffer amplifier pair, and T9-T10 are the active inverse balun converting balanced signal back to single-ended.

Based on equation 4.2, the g_m of the TC stage (T1 and T2) is the main contributor of the mixer CG. Therefore, CG can be varied by tuning the biased g_m of the two transistors in the TC stage. As shown in Fig. 4.4a, the g_m of the TC stage is varied with different V_{BC}, and thus, can be tuned by V_{MIX}. However, the accurate choice of the actual V_{BC} of the TC stage is tricky in the traditional gilbert-cell-based mixer since the SQ stage and TC stage are stacked on top of each other and thus, the supply voltage is not equally distributed to the two stages. Similar to

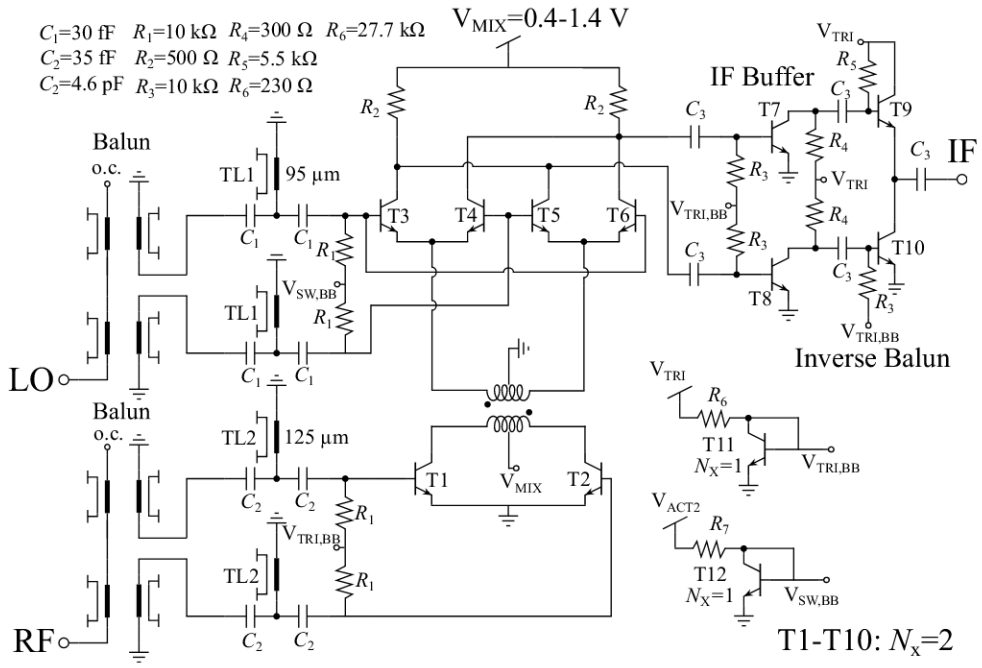


Figure 6.14: Schematic of the designed tunable mixer, IF BA, and active inverse balun.

the mixer design in Chapter 4, an on-chip transformer is implemented to couple the two stages, as shown in Fig. 6.14. Apart from the P_{dc} reduction discussed in Chapter 4, the transformer implementation also offers the separate (and hence accurate) biases of the two stages, enabling the accurate control of the mixer CG. Additionally, the V_{MIX} of the SQ stage is also tuned together with the TC stage for two reasons. First, V_{BC} of the SQ stage influences the biased J_C and thus changes the SQ contribution to the mixer CG with the same trend as the TC stage. Therefore, tuning the V_{MIX} of SQ together enlarges the overall CG tuning range. Secondly, the DC distribution networks can be combined if the V_{MIX} of the two stages can be tuned together. Eventually, the SQ and TC stages of this mixer are biased with 3 and 23 mA/µm^2, respectively, with the V_{MIX} tuning from 0.3 to 1.4 V.

The G-band broadband low-loss balun shown in Section 2.2.3.2 is implemented both at LO and RF ports to convert the single-ended LO and RF signal to the differential required by the gilbert-cell. The on-chip transformer is designed by two topmost layers, i.e., TM1 and TM2, with virtually coupled configuration, similar to the one shown in Fig. 4.6 but operating at higher frequencies at around 190 GHz. Based on EM simulation, this transformer provides around 1 dB in-band insertion loss and port isolation higher than 15 dB. T-type networks consisting of two capacitors at both sides with a shunt TL in between are implemented for impedance matching between the balun and gilbert-cell at RF and LO (TL1 and C_1, TL2 and C_2). At the IF output, an active inverse balun (T9 and T10) transfers the differential IF back to a single-ended signal to characterize it on-chip and provide an extra 2-3 dB gain. An additional differential CE amplifier is inserted between active inverse balun and gilbert-cell to further enhance CG_{rx} with around 17 dB gain at around 1 GHz. As shown in equation 6.4 and equation 6.6, the high gain of the IF BA significantly relaxes the demand of LNA and mixer in terms of gain and oP_{1dB}. The transistors in the mixer core, IF BA, and active inverse balun are chosen with N_x of 2. The smaller size of devices in the mixer core is due to the further reduction of their P_{dc}, and N_x of 2 at IF (around 1 GHz) offers sufficient output power of the receiver.

Fig. 6.15 shows the simulated USB CG of the complete mixer core together with the active inverse balun with swept LO pumping power P_{LO}. LO and RF are selected at 192 and 193 GHz. As clearly shown, CG increases with P_{LO}, and the improvement becomes less after around -5 dBm. Therefore, the desired operation of this mixer can be realized by the LO DA with

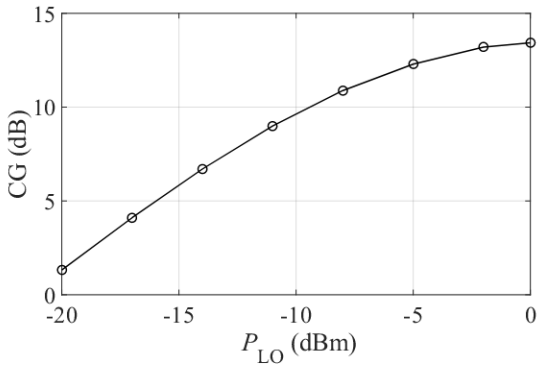


Figure 6.15: Simulated USB CG of the complete mixer core with only the active inverse balun as a function of LO pumping power P_{LO} with LO and RF at 192 and 193 GHz, respectively.

around -5 dBm output pumping power.

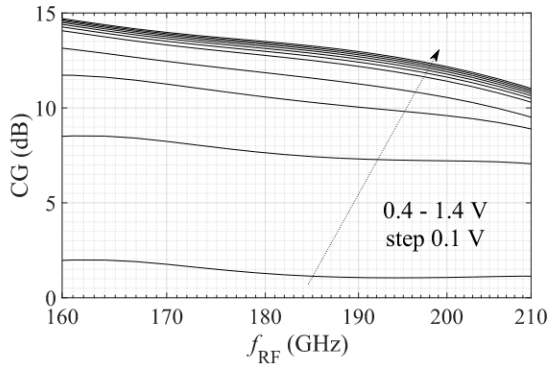


Figure 6.16: Simulated USB CG of the complete mixer core with only the active inverse balun with V_{MIX} tuned from 0.4 to 1.4 V, fixed f_{IF} at 1 GHz, and P_{LO}=-14 dBm.

The simulated USB CG of the mixer with active inverse balun is shown in Fig. 6.16, with V_{MIX} tuned from 0.4 to 1.4 V and fixed f_{IF} at 1 GHz. P_{LO}=-5 dBm is used in this simulation. By tuning V_{MIX} from 0.4 to 1.4 V, the CG of this mixer is varied from 1 to 14 dB. The iP_{1dB} stays at around -21 dBm during the bias tuning, with the corresponding oP_{1dB} varying from -21 to -8 dBm. Based on the simulation, P_{dc} of 11.2 mW is consumed by the mixer core with maximum CG bias (1.4 V), and the IF buffer amplifier and active inverse balun dissipate 8.5 mW totally, including all voltage distribution networks (T11-T12).

To verify the performance of the mixer core, a single block of the mixer with active inverse balun was fabricated, and the photograph is presented in Fig. 6.17. The total chip area is 720 μm×720 μm=0.49 mm^2, including all DC and RF pad structures.

This mixer block was measured on-wafer. The LO signal was externally generated by an R&S ZVA G-band converter together with a Keysight signal generator N8257D. The RF signal was generated by an OML G-band VNA extender (V05VNA2) fed by a Keysight PNA E8361C. The IF signal was measured using a Keysight Spectrum analyzer (E4448A). A VDI Erickson PM5 power meter was employed to carefully level the output power of the extender together with a waveguide bend. Probe and cable losses were subtracted to calculate the power on-chip accurately. Return loss was measured by a vector network analyzer (Keysight E8361C) with OML G-band VNA extender (V05VNA2).

Due to the equipment limitation, the mixer was characterized with a fixed LO at 192 GHz,

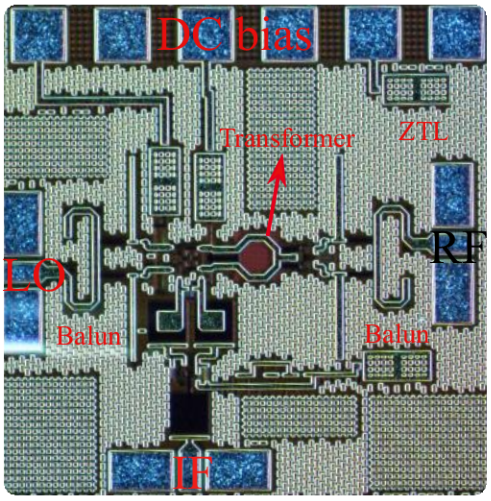


Figure 6.17: Photograph of the fabricated mixer block. The total chip area is 720 μm×720 μm, including all pad structures.

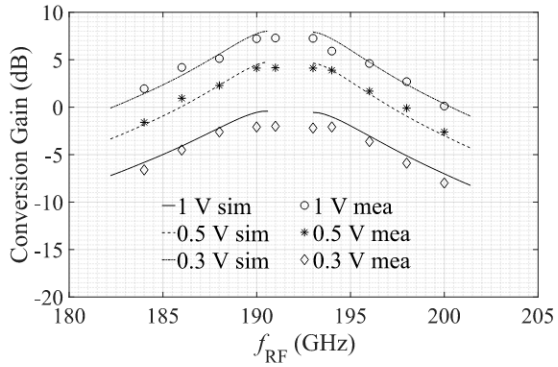


Figure 6.18: Measured and simulated LSB and USB with -14 dBm fixed LO at 192 GHz, for V_{MIX}/V=1,0.5,0.3.

and the P_{LO} was limited to -14 dBm on-chip, which is much less than -5 dBm in the receiver system (provided by LO chain) but still enables a proper mixer operation. Unless otherwise noted, all results shown here are measured using this 192 GHz LO with -14 dBm power. Fig. 6.18 illustrates the comparison between measured and simulated LSB and USB CG for different V_{MIX} (0.3,0.5 and 1 V). The peak CG of this mixer can be tuned from -2 to 7 dB at 191 GHz (LSB) and 193 GHz (USB), with the 3 dB RF BW of 11 GHz from 186 to 197 GHz. With various V_{MIX}, this circuit consumes a total P_{dc} of 10, 6.8, and 5.1 mW, respectively, including 3.5 mW P_{dc} from the active inverse balun. As shown, an overall good agreement between simulation and measurement is observed only with around 1 dB deviation between 190 and 194 GHz, which might due to the inaccurate EM-simulation of the TLs and passive components. Such good agreements indicate a good prediction of the simulation shown in Fig. 6.15 and Fig. 6.16 with higher P_{LO}.

Fig. 6.19 shows the P_{IF} as a function of P_{RF} at 193 GHz with different V_{MIX}. During the CG tuning, the iP_{1dB} of this mixer stays at a similar value at around -21 dBm, while the corresponding oP_{1dB} varies from -24 dBm to -14.9 dBm. Also, the measurement is well approximated by the simulation, and the observed deviation is due to the above-mentioned 1 dB lower measured CG at 193 GHz. Based on equation 6.6, the oP_{1dB} variation of the mixer can be compensated by the IF buffer amplifier with 17 dB gain, which will not influence the final $oP_{1dB,rx}$ of the receiver.

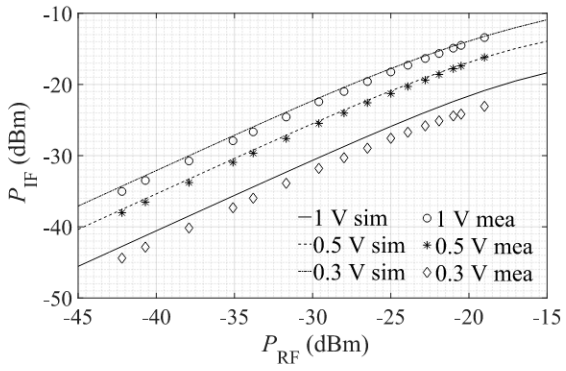


Figure 6.19: Measured and simulated P_{IF}versus P_{RF}at f_{RF}=193 GHz for V_{MIX}/V=1,0.5,0.3.

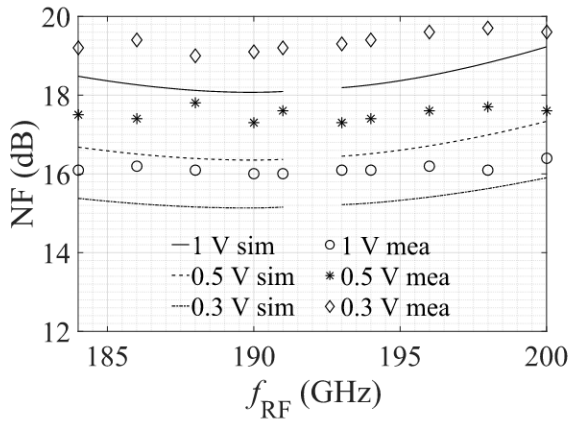


Figure 6.20: Measured and simulated NF versus f_{RF} for V_{MIX}/V=1,0.5,0.3.

The NF of this mixer is measured based on the method in [85, 166] and is presented in Fig. 6.20. As shown, the minimum SSB NF of around 16 dB is observed with V_{MIX}=1 V, and the value increases to 17.5 and 19 dB with lower CG bias (V_{MIX} of 0.5 and 0.3 V), mainly due to the CG reduction. Realizing the CG tunability directly by the mixer itself lead to noticeable NF variation, which in turn varies the overall NF of the receiver if such mixer is placed as the front stage (mixer-first topology). Nevertheless, such impact can be minimized in the receiver of this work due to high-gain LNA as the first stage.

The LO and RF port return loss and the LO-to-RF isolation were also measured as presented in Fig. 6.21. The overall in-band return loss is lower than 9 dB for the RF and 11 dB for the LO port, which indicates a good power injection at these two ports. The measured LO-to-RF isolation is better than 30 dB, which predicts good isolation between the two ports. The simulations agree mostly well with the measurements, and the observed derivation at higher frequencies may due to the imperfect probe contact or inaccurate EM simulation and passive components.

The performance summary of this mixer building block is presented in Table 6.1 and is compared with previously reported SiGe-based down-conversion mixers operating at around 200 GHz. As shown, this design achieves the highest CG of 7.2 dB while consuming the lowest P_{dc} of maximal 10 mW. [119] uses the same technology with a LO driver amplifier with around 17 dB gain integrated with the mixer, which reduces the requirement of the off-chip P_{LO} from -3 dBm to -20 dBm, but at the expense of 22 mW more P_{dc} (20 mW by mixer and 42 mW in total). As a comparison, the mixer described in this work realizes higher CG, lower NF but consuming only half of P_{dc}. More importantly, the direct CG tunability is also realized with

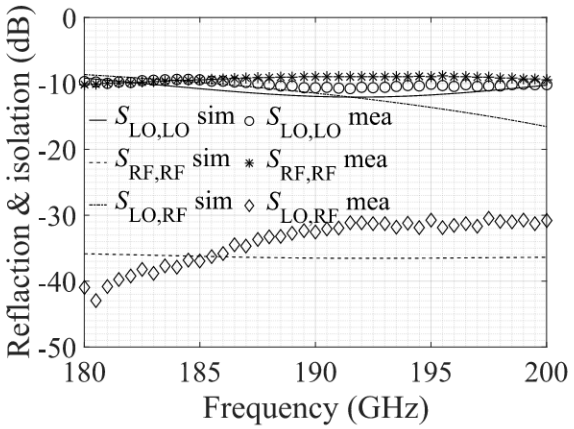


Figure 6.21: Measured and simulated reflection coefficients of RF and LO port and the LO-to-RF isolation with V_{MIX} of 1 V.

Table 6.1: Comparison with reported down-conversion mixers operating at around 200 GHz

Ref.	Tech.	Topology	f_T (GHz)	f_{RF} (GHz)	CG (dB)	P_{LO} (dBm)	P_{dc} (mW)	NF (dB)	ΔCG (dB)	BW (GHz)
[119]	130 nm SiGe	G.mixer+LO driver	300	200	5.5	-20	40	16^{ds}	-	30
[171]	90 nm SiGe	G.mixer+IF VGA	300	155	1...7	3	136	9.5^{ss}	6	30
[170]	130 nm SiGe	G.mixer	300	180	-8	-6	18	21^{ss}	-	30
This	**130 nm SiGe**	**G.mixer**	**300**	**190**	**7.2**	**-14**	**10**	$\mathbf{19^{ss}}$	9	11

- not shown; ^{ds} DSB; ^{ss} SSB

highly competitive NF performance. Notice that this mixer was designed with fixed IF but was verified with fixed LO due to the limited available external LO source for measurement. A much wider available bandwidth is predicted with fixed IF (and swept LO and RF), as shown in Fig. 6.16. The overall observed good agreement between simulation and measurement of the single-block mixer indicates the proper operation of this mixer in the receiver system.

6.2.3.3 65 GHz (V-band) Quadrupler

The ×12 multiplier chain is designed with a V-band quadrupler and a G-band tripler. The differential configuration is chosen due to the automatic cancellation of unwanted harmonics, especially beneficial for the high-order multiplier chain [137, 138]. Because of the smaller size, wider bandwidth and possibly an insertion gain, the active balun is chosen as the first stage of the LO chain. Details have been described in Section 2.2.3.1, and hence are not shown here.

Typically, the single-stage multiplication is not recommended for quadruplers due to the relatively poor performance and difficulties in filtering out all unwanted harmonic components, especially for those low-order harmonics with stronger powers. Instead, cascading two doublers is a popular solution [45, 137]. The push-push doubler [139, 140] is one of the commonly used topologies. However, due to the direct differential to single-ended transformation, the push-push doubler is usually placed as the final-stage but not encouraged as the front- or middle-stage. By comparison, the gilbert-cell-based topology is a suitable candidate as it offers differential outputs, which can be directly implemented into the differential chain without extra balun or transformer.

Fig. 6.22 illustrates the schematic of the designed V-band quadrupler, with the target output signal at around 60 GHz. Instead of the cascaded topology, the stack topology is selected due

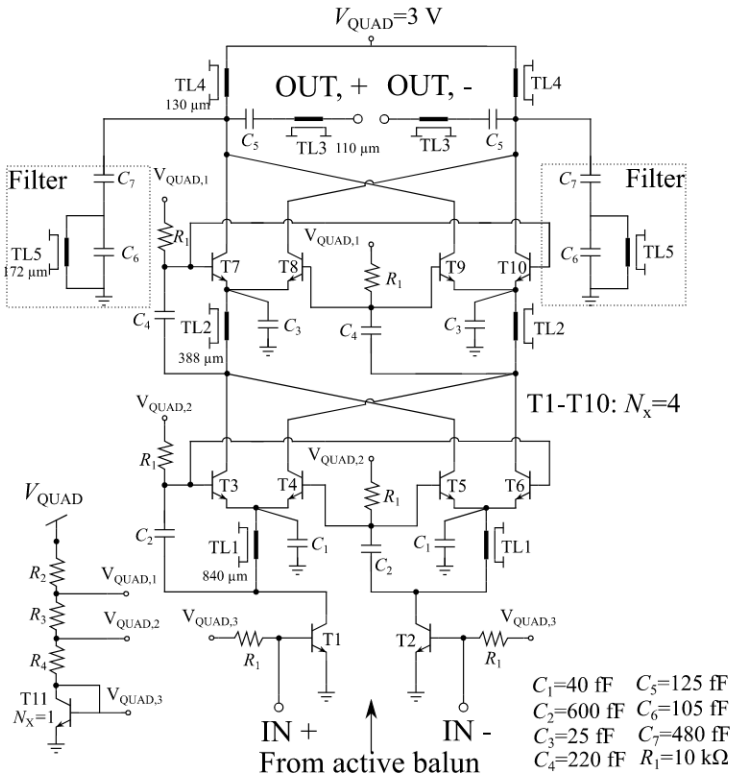


Figure 6.22: Schematic of the designed quadrupler.

to the wider bandwidth and compactness of chip area but at the expense of higher V_{supply}. The stacked topology obviates the complicated interstage matching network, which consumes larger chip area, limits the bandwidth, and introduces extra losses. Similar to the gilbert-cell-based mixer, the circuit consists of an input TC stage with a pair of transistor (T1-T2) and two stacked gilbert-cells (T3-T10). Compared to the traditional gilbert-cell-based quadrupler, two extra TLs are inserted between TC and the first SQ stage, and between two SQ stages (TL1 and TL2). By adding an additional phase shift (theoretically 90° [172]), the CG of the quadrupler can be significantly improved. Based on the analysis in [141] using the same technology, the highest simulated RF-to-DC efficiency is achieved with HBTs with N_x of 4, and thus this size is used in this quadrupler.

For a multiplier chain with high multiplication order, the signal purity becomes a critical FoM, especially when integrating the chain with receiving circuits. As mentioned, the odd harmonics are canceled automatically by the differential configuration. However, the even harmonics (for instance, the 2^{nd} and 6^{th} harmonics of this quadrupler) still exist in the differential operation, due to either the front stage leakage or the self-mixing. In [141], a tail resistor under T1 and T2 was implemented to enhance the harmonic rejection of the 2^{nd} and 6^{th} harmonics by around 10 dB, but with more than 20% consumed P_{dc} because the tail resistor increases the overall supply voltage of the quadrupler core. To further improve the harmonic rejection, a compact zero-pole filter is utilized at the output of the quadrupler [173]. Such filter consists of two capacitors (C_6, C_7), together with a piece of TL (TL5) shorted at the end. By carefully selecting the proper value of the elements, the filter offers a low impedance (shorted to the ground) at 2^{nd} and 6^{th} harmonics but a high impedance at the target 4^{th} frequency (open). The EM-simulated return loss of the designed zero-pole filter is shown in Fig. 6.23. It offers 20 dB and 30 dB attenuation at 2^{nd} and 6^{th} harmonics, respectively, with 0.8 dB insertion loss at 4^{th} harmonic frequency. Apart from that, two small extra shunt capacitors (C_2, C_4) are implemented for the further enhancement of the harmonic rejection of 6^{th} harmonics and higher [141].

To verify the performance of the quadrupler, a single test block was fabricated. The chip

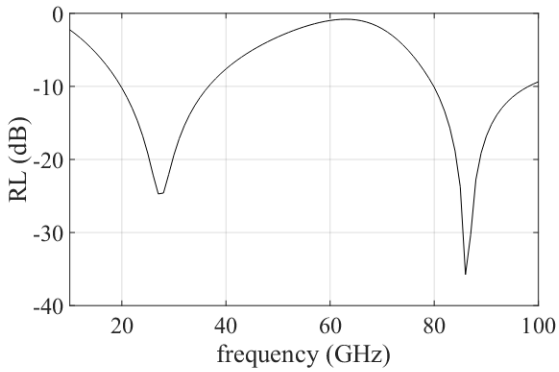


Figure 6.23: EM simulated return loss of the designed output zero-pole filter of the quadrupler.

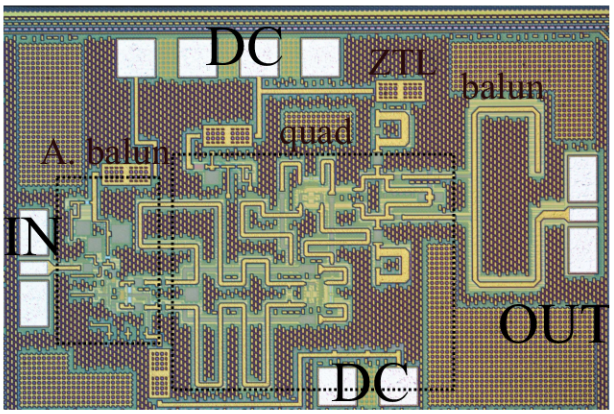


Figure 6.24: Chip photograph of the the fabricated test quadrupler with active balun as the first stage. The total chip size is 1.1 mm×0.7 mm, including output balun (which is used for single block test only) and all DC and RF pad structures.

photograph is illustrated in Fig. 6.24. This quadrupler was fabricated with the front-stage active balun used in the LO chain. A V-band (50-75 GHz) balun is implemented at the output for on-wafer characterization. The total chip size is 1.1 mm×0.7 mm=0.77 mm^2, including the output balun and all DC and RF pad structures. The output passive balun is designed using the same configuration as discussed in Section 2.2.3.2 but is operating in V-band (50-75 GHz). With a size of 0.3 mm×0.6 mm, this balun offers broadband performance over V-band with around 1 dB EM-simulated insertion loss.

This quadrupler was measured on-wafer. The input power was generated by the signal generator (Keysight E8257D). The output power was measured by the Keysight power sensor (U8488A). Spectrum analyzer (Keysight E4448A) and W-band harmonic mixer (Keysight 11970) were used to measure the harmonic components up to 50 GHz and 75-110 GHz. Return loss was measured by a vector network analyzer (Keysight E8361C). The loss of probes, cables, and connectors were subtracted for the accurate power level on-chip.

The measured CG of this quadrupler together with the active balun compared to simulation is presented in Fig. 6.25. With a higher V_{QUAD} of 4 V, this circuit offers a peak CG of 28.5 dB at 64 GHz with -30 dBm P_{in}, consuming around 110 mW DC power. The 3 dB BW is estimated to be 16 GHz from 56 to 72 GHz, a relative BW of 25%. With a lower V_{QUAD} of 3 V, the consumed P_{dc} reduces to 69 mW, but still provides 24 dB CG at 64 GHz with -28 dBm P_{in}. The 3-dB BW for this bias is predicted to be 14 GHz from 58 to 72 GHz, a relative BW of 22%. V_{QUAD}=3 V is selected for the quadrupler in the LO chain with a bit lower CG but with nearly half of less consumed P_{dc}. As presented, good agreement between measurement and simulation

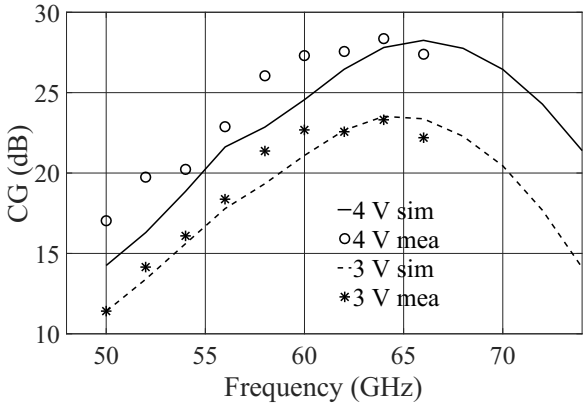


Figure 6.25: measured and simulated CG versus output frequencies with two different supply voltages (V_{QUAD}). Input power is fixed to -30 and -28 dBm for two bias cases.

is observed, with a slight band shift of around 2.5 GHz towards lower frequency, which may be caused by inaccurate EM simulation and passive components.

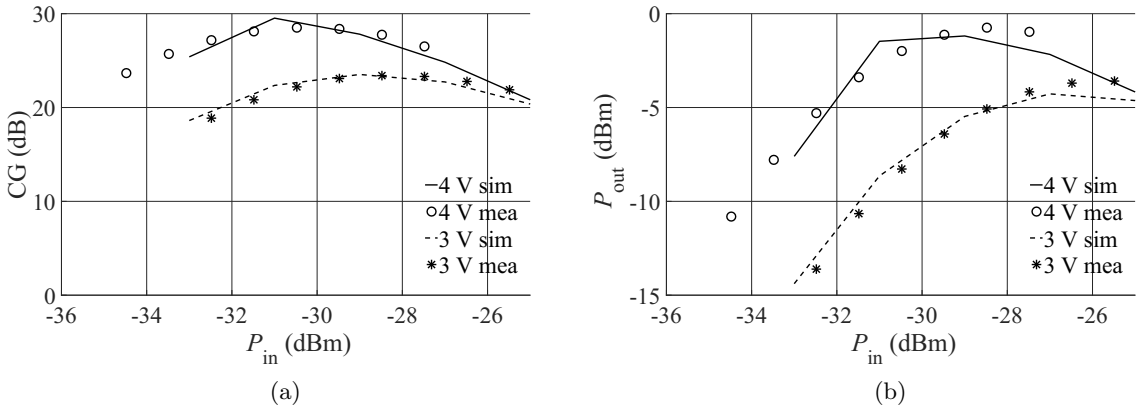


Figure 6.26: Measured and simulated (a) CG, (b) P_{out} vs P_{in} with different V_{QUAD} at 64 GHz.

At 64 GHz, the simulated and measured CG and P_{out} as a function of P_{in} are presented in Fig. 6.26. The peak P_{out} of -1.5 dB and -4 dB are observed for V_{QUAD} of 4 V and 3 V, respectively. As shown, the measurements are well predicted by the simulation, with a slightly higher measured P_{out} than expected, which might be due to the inaccurate EM simulation of matching networks. The measured harmonic rejection of this quadrupler with V_{QUAD}=4 V compared to simulation results is shown in Fig. 6.27a. The measured in-band harmonic rejection (input frequency of 14-18 GHz) is higher than 20 dBc for all harmonic components from 1^{st} to 7^{th}, which indicates a good signal purity. The observed reduced harmonic rejection for 5^{th} and 6^{th} at the input frequency of 13 GHz is mainly due to the off-band input frequency, which makes 5^{th} and 6^{th} falls in the designed frequency band of 4^{th} harmonics at around 65 GHz. These input frequencies do not fall in the interesting operation region of this circuit. Similarly, the simulated in-band harmonic rejection of V_{QUAD}=3 V is also higher than 20 dBc, as shown in Fig. 6.27b. The observed excellent agreement between measurement and simulation for V_{QUAD}=4 V indicates the high accuracy of the simulation results for V_{QUAD}=3 V. Also notice that tuning V_{QUAD} does not necessarily lead to the degradation of harmonic rejection, thanks to the careful design of filter and topology.

The measured and simulated output return loss of the quadrupler is shown in Fig. 6.28. Less

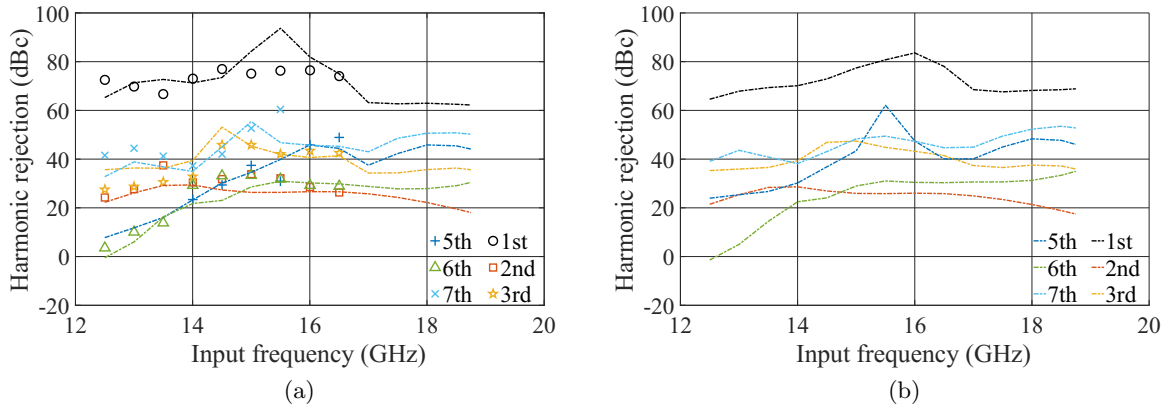


Figure 6.27: Measured (symbols) and simulated (lines) harmonic rejection of (a) V_{QUAD}=4 V, and simulated harmonic rejection of (b) V_{QUAD}=3 V.

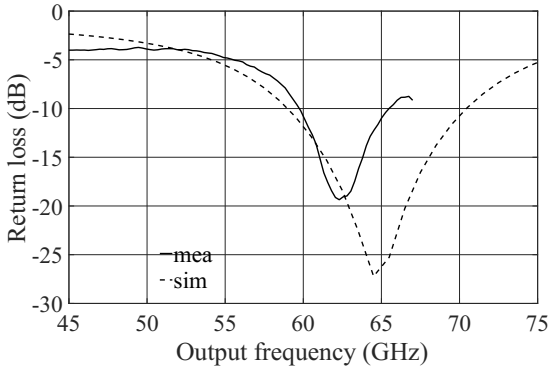


Figure 6.28: measured and simulated output return loss for V_{QUAD}=3 V. The result of V_{QUAD}=4 V is almost the same as for 3 V and thus is not shown in the plot.

than -10 dB in-band return loss indicates a good match of the output port. The input return loss is lower than -8 dB, which will be shown in the receiver results later. The overall good agreement between measurement and simulation is observed, with a 2.5 GHz frequency shift towards lower frequency, which might be the main reason for the shift of CG shown before and maybe mainly due to inaccurate EM-simulation. The slightly higher measured return loss maybe caused by the non-perfect probe contact.

The key performance of this designed quadrupler was summarized in Table 5.1 and compared with state-of-the-art reported multipliers using different SiGe and CMOS technologies. With a relatively low consumed P_{dc} of 69 mW, this circuit realizes the highest CG listed in the table with highly competitive performance in terms of bandwidth and harmonic rejections.

Based on the excellent agreement between simulation and measurement, the influence of the physical effects on P_{out} are analyzed, as shown in Fig. 6.29. The high-current effect has a significant impact on P_{out}. Differently, the self-heating effect in this circuit presents a comparable influence with the NQS effect, mainly due to higher biased J_{C} and V_{supply} of this circuit than the low-power designs in Chapter 5.

6.2.3.4 G-band Tripler

This G-band tripler is realized based on the design shown in Section 5.3, but with some improvements. First, due to the limited number of DC pads for on-wafer characterization, a DC voltage distributor (T5 and R_2) is implemented for DC combination. Secondly, a slightly higher V_{supply}

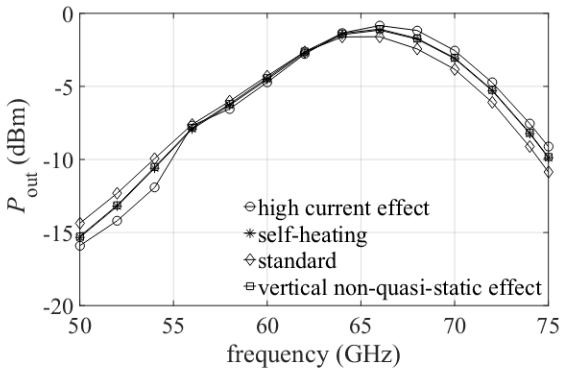


Figure 6.29: Impact of physical effects on the P_{out} of the quadrupler with V_{QUAD}=4 V: high-current effect (tef0 and thcs=value or 0), self-heating effect (flsh=1 or 0), and vertical NQS effect (flnqs=1 or 0).

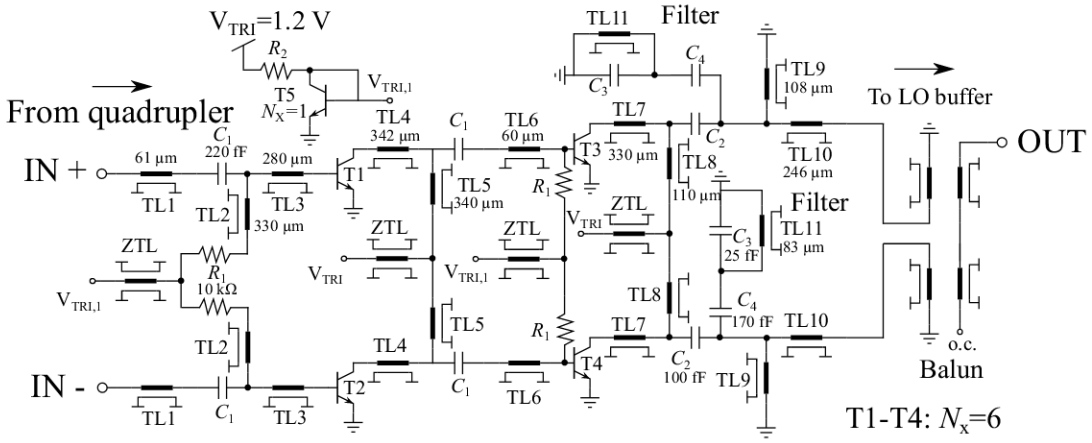


Figure 6.30: Schematic of the designed tripler.

of 1.2 V is selected in order to realize a higher output power, but at the expense of a higher consumed P_{dc} of 24 mW. Furthermore, the performance of input and output matching networks is optimized. Moreover, an extra zero-pole shunt filter with a similar topology as the one used in the quadrupler in Section 6.2.3.3 is utilized at the output to filter out the leakage from the quadrupler and thus improve the harmonic rejection of 4^{th} harmonic of the entire multiplier chain. Fig. 6.31 shows the EM simulation result of the designed zero-pole output filter of this tripler, offering an -25 dB attenuation at 4^{th} harmonic (60 GHz) and 1 dB insertion loss at 12^{th} (180 GHz).

The ×12 signal generation chain (active balun+quadrupler+tripler) was fabricated and measured on-wafer. The total size of the test ×12 multiplier chain is 1.8 mm×0.9 mm=1.7 mm^2, including all pad structures, as shown in Fig. 6.32. For measurement, the input signal was generated by a Keysight signal generator N8257D. A 20 dB fixed attenuator was added during the measurement due to the low required input power level. The output signal and G-band harmonics were measured using OML WR-05 harmonic mixer M05GWD together with Keysight spectrum analyzer E4448A. A G-band waveguide-based tunable attenuator was added at the output to reduce the output power level and thus to avoid the harmonic mixer from falling into the saturation region. Probe and waveguide and cable losses were subtracted to determine the power on-chip accurately.

This ×12 multiplier chain consumes 164 mW in total: 24 mW in the active balun, 110 mW in the quadrupler (4 V), and 30 mW in the tripler (1.4 V). Fig. 6.33 shows the simulated and

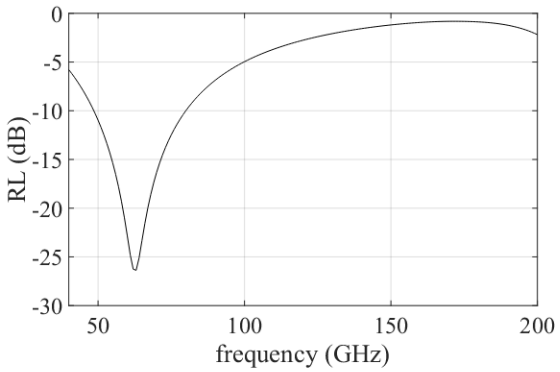


Figure 6.31: EM simulated return loss of the designed output zero-pole filter of the tripler.

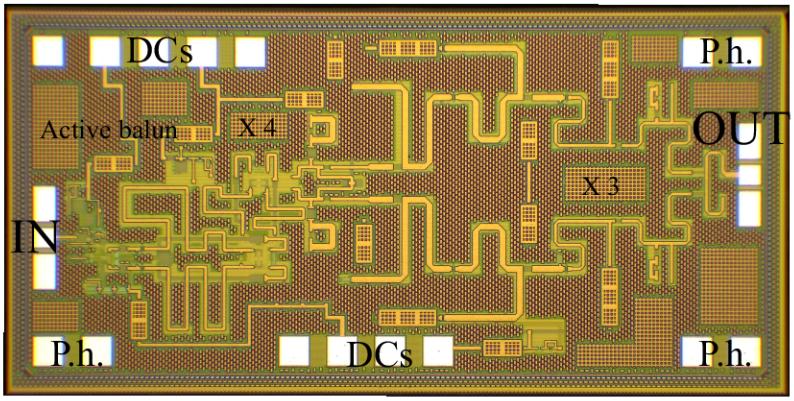


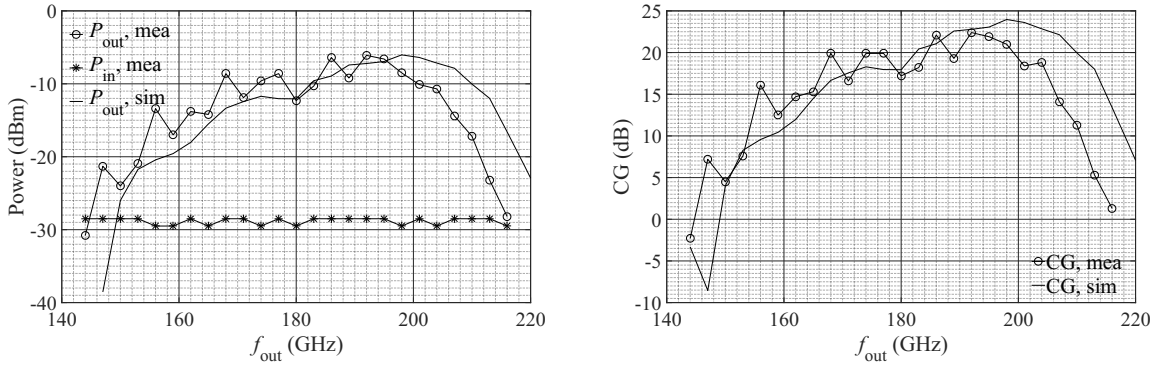
Figure 6.32: Chip micrograph of the test block of this designed ×12 multiplier chain including active balun, quadrupler, and tripler. The total size is 1.8 mm×0.9 mm=1.7 mm^2, including all pad structures.

measured P_{out} and CG versus f_{out}. With around -28 dBm P_{in}, a peak P_{out} of -6 dBm is achieved at 192 GHz, with the 3 dB BW of 34 GHz from 168 to 202 GHz, and the corresponding peak CG is 22 dB at 192 GHz. The overall measurement is well predicted by simulation. Compared to the measurement, the simulation exhibits a band shift of around 7-10 GHz towards higher frequency, which might be due to inaccurate EM-simulation of the TLs or the passive components.

The harmonic rejection of the close-by frequency components is vital because they are in-band of the end-stage amplifier and thus are hard to filter out, especially for a high-order multiplier chain for which the harmonics are close to each other. The 11^{th} and 13^{th} harmonic rejection is measured, and the results are presented in Fig. 6.34 compared with simulation. As shown, the in-band harmonic rejections from 168 to 202 GHz (input 14-17 GHz) are higher than 30 dBc, thanks to the proper operation of on-chip filters and the circuit topologies. Also, the simulation agrees well with measurement.

The measurement and simulation of the return losses of input and output of this designed multiplier are shown in Fig. 6.35. Lower than -8 dB both for input and output return loss is obtained, which indicates a good impedance match of the two ports. Besides, the good agreement between simulation and measurement indicates the proper operation of the designed matching network. may due to the imperfect probe contact or inaccurate EM simulation and passive components.

The performance of this designed test ×12 multiplier chain was summarized in Table 5.3 with state-of-the-art reported multipliers as comparisons. As shown, this design achieves the highest CG and harmonic rejection listed in the table, with highly competitive performance in terms of P_{out}, bandwidth, and a relatively lower P_{dc}. If considering the FoM using the equation 5.4, the



(a) (b)

Figure 6.33: Measured and simulated (a)P_{out} and (b) CG as a function of f_{out} of this test ×12 multiplier chain. The calibrated on-chip input power is shown in (a), and the input frequency is 1/12 of f_{out}.

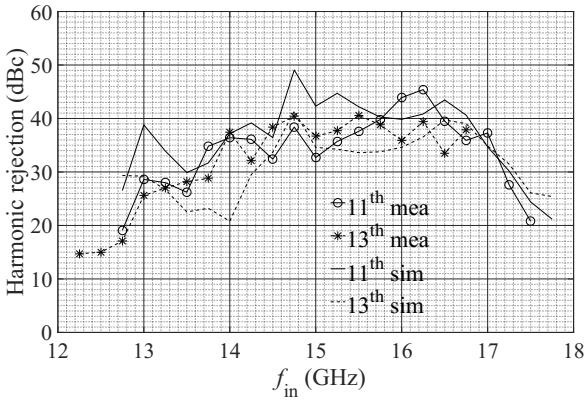


Figure 6.34: Measured and simulated in-band harmonic rejections of 11^{th} and 13^{th} frequency components.

achieved value of 276 is the second-highest one close to 281 of the low-power design introduced in Section 5.4, but with 30 dB higher CG and 10 dB higher harmonic rejection, which is not included in FoM calculation.

The presented good simulation-measurement agreement enables a sensitivity analysis of this ×12 multiplier chain. With a 20% variation of the uncorrelated HICUM/L2 parameters, the impact of the parameter-related physical effect on P_{out} is checked, and those parameters with top five impact are ranked and shown in Fig. 6.36. The transistor parasitics (i.e. series resistances and parasitic capacitances) and the internal base-collector depletion capacitance have the most significant impact.

6.2.4 Receiver Results and Discussion

Fig. 6.37 illustrates the micrograph of the fabricated receiver chip. The total area of this chip is 3600 μm× 1000 μm=3.6 mm^2, containing all pads and packaging holders (p.h.). Because of the further packaging requirement, reducing the number of DC pads is required, and thus the voltage distributors (transistor plus resistors) are used in all circuit blocks (see all schematics). The smallest possible size was chosen for all transistors with N_{x} of 1 to minimize its P_{dc}. The p.h. and TL test structures were placed at the chip edges for mechanical purposes and for verifying

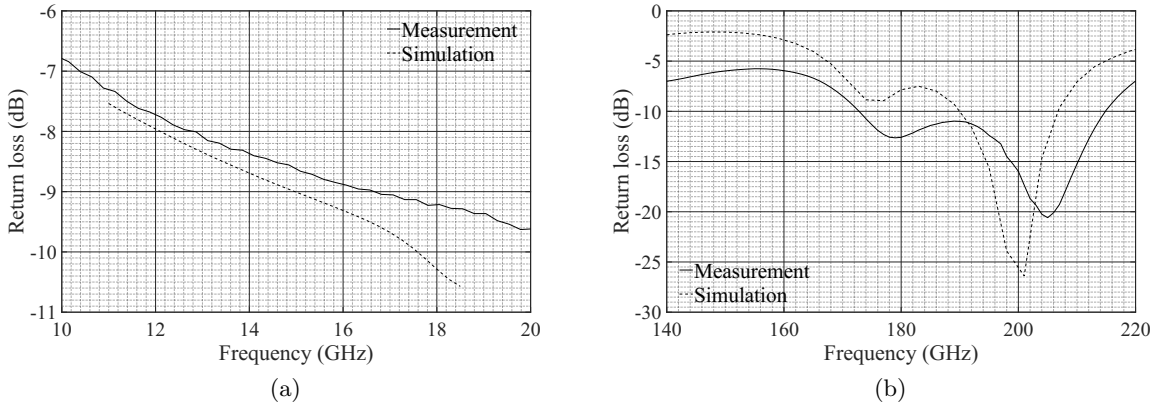


Figure 6.35: Measurement and simulation of the return loss of (a) input and (b) output of this chain.

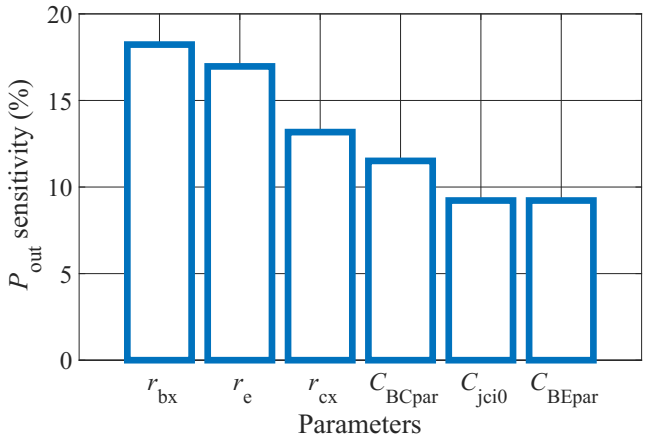


Figure 6.36: Sensitivity w.r.t. import HBT parameters of peak P_{out} at 185 GHz of the ×12 multiplier chain.

packaging quality. ZTLs were used for the DC supply connection in all circuit blocks, and grounded sidewalls were implemented in the chip margin area to prevent the crosstalk between adjacent stages and circuit blocks. Details have been described in Chapter 2.

6.2.5 Measurement Setup

Fig. 6.38 describes the measurement setup of this receiver. The circuit was measured on-wafer. The Keysight signal generator (N8257D) with a 20 dB fixed attenuator was used to generate the LO signal. The OML G-band VNA extender following a Keysight PNA-X (N5247A) was utilized to create the RF test signal and also to verify the return loss of the RF port. The Keysight spectrum analyzer (E4448A) was used to monitor the IF signal. A VDI Erickson PM5 power meter was employed to carefully level the output power of the extender together with a waveguide bend. Probe and waveguide, cable losses were subtracted to obtain the power on-chip accurately. IF and LO return losses were measured by Keysight PNA-X (N5247A).

6.2.6 Results

The receiver consumes 171 mW with 142 mW from the LO chain and 29 mW from the receiver core part (LNA + mixer + IF BA + inverse balun), including all voltage distribution networks,

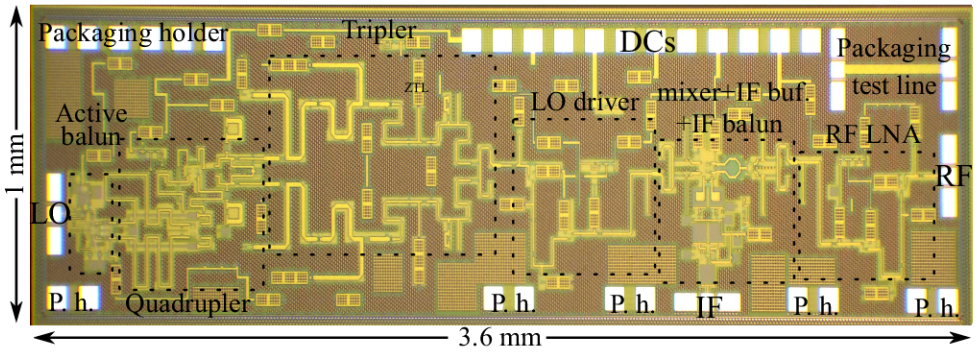


Figure 6.37: Photograph of the fabricate receiver chip, with total chip size of 3.6 mm×1 mm=3.6 mm^2, including all pads and packaging holders.

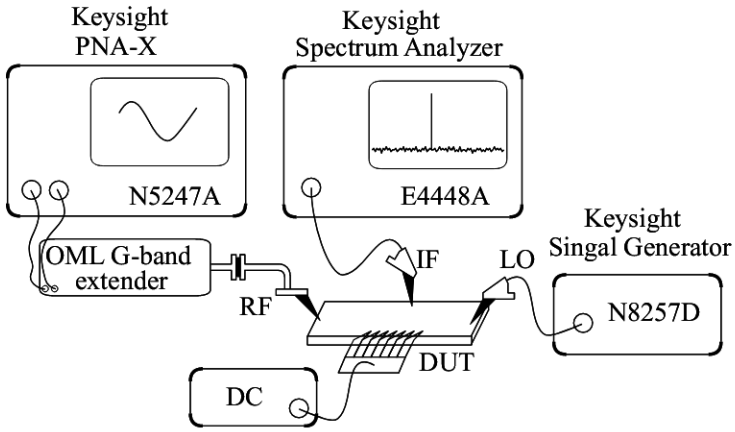


Figure 6.38: Receiver measurement setup.

operating with the maximum CG bias condition. Unless otherwise noted, the f_{IF} is fixed at 1 GHz and P_{LO} is -30 dBm for all presented results below.

Fig. 6.39 presents the measured USB and LSB CG of the receiver with the maximum (1.4 V) and minimum (0.4 V) CG bias compared with simulation. As displayed, a maximum USB/LSB CG of 48.3 and 49 dB is measured at the RF frequency (f_{RF}) of 193 and 191 GHz, respectively. With the maximum CG bias of 1.4 V, the obtained RF 6-dB BW is 27 and 23 GHz, respectively, for USB and LSB cases. Around 14 dB CG tuning range is obtained by biasing the down-conversion mixer to 0.4 V. With this minimum CG bias, the USB and LSB CG of 35.2 and 34.5 dB at f_{RF} of 193 and 191 GHz are realized. The RF 6-dB BW becomes slightly higher to 32 and 33 GHz at low CG bias, respectively, at two frequency points. The figure shows the overall good agreement between measurement and simulation with an approximate 3-5 GHz shift towards the higher frequency.

Fig. 6.40 shows the measured and simulated P_{IF} as the function of P_{RF} with f_{RF} of 193 and 191 GHz at two CG biases. The measured USB/LSB oP_{1dB} with the maximum CG bias is -8.5/-8.1 dBm at iP_{1dB} of -55.5/-56 dBm, respectively; P_{RF} is saturated at around -1 dBm. With the minimum CG bias, the measured USB/LSB oP_{1dB} remains a similar value of -8.8/-8.9 dBm, with a higher iP_{1dB} of -42.2/-43 dBm and a slightly lower IF saturation power of -3 dBm. The achieved oP_{1dB} fulfills the requirement for direct communication with a VNA since the corresponding iP_{1dB} will not fall below the detection limit. As shown, simulation and measurement agree quite well for two bias conditions.

In practice, the receiver channel does not necessarily operate in a very linear region because the accurate LO pumping power level is difficult to control within a wide frequency range. Instead, the commercial VNA usually gives over-pumped LO power, leading to the saturation

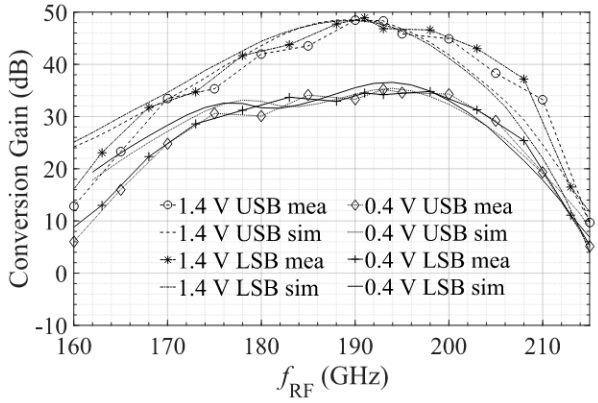


Figure 6.39: Measured (symbols) and simulated (lines) USB and LSB CG of the fabricated receiver biased for maximum and minimum CGs.

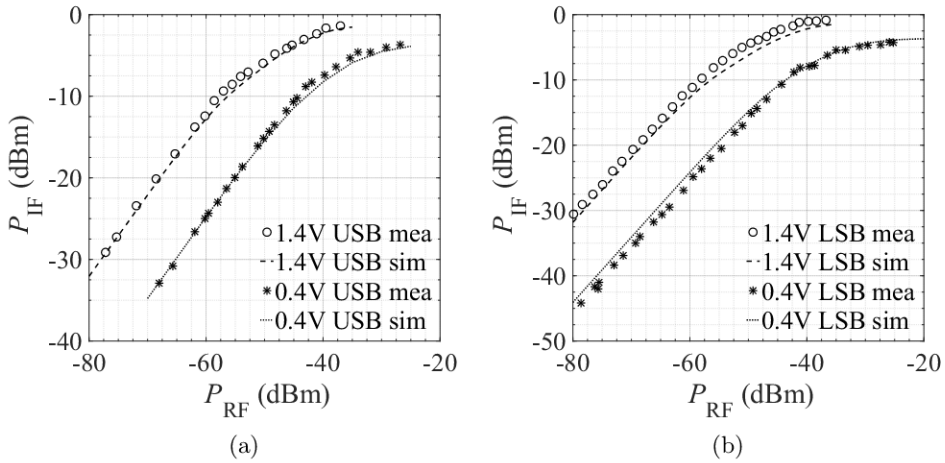


Figure 6.40: Measured (symbols) and simulated (lines) (a) USB and (b) LSB P_{IF} as a function of P_{RF} of this receiver at maximum and minimum CG biases with f_{RF} of 193 and 191 GHz, respectively.

operation of the receiver channel. Such saturation operation is reasonable as long as the harmonic rejection is still high enough. Fig. 6.41 shows the simulated and measured saturation power P_{sat} as a function of f_{rf} for USB and LSB case of this receiver with fixed f_{if} at the maximum CG bias. The IF power is saturated from -5 to -1 dBm from 163 to 213 GHz, with around 50 GHz saturation bandwidth, both for USB and LSB. Simulation and measurement agree well, and the measurement shifts around 3 GHz to a higher frequency.

Fig. 6.42 presents the measured USB and LSB IF spectrum at the 1 dB compression and saturation point with maximum CG bias. The resolution BW of the spectrum analyzer is 500 kHz. As shown, at 2 GHz, 29 and 25 dB lower power than that of the fundamental tone are observed for USB and LSB, respectively. In the saturation region, the measured harmonic rejection is still higher than 22 dBc, which indicates a good signal purity of this design. For minimum CG bias, similar values of 28 and 26 dBc at 1 dB compression and 23 and 22 dBc at saturation point are measured, and the data is not shown in the above figure.

Based on the NF measurement method described in [85, 166], the NF of this receiver was measured, and the result is shown in Fig. 6.43. As presented, the minimum measured USB/LSB NF with maximum CG bias is 16.5/16.6 dB at 180/184 GHz, and the value increases slightly

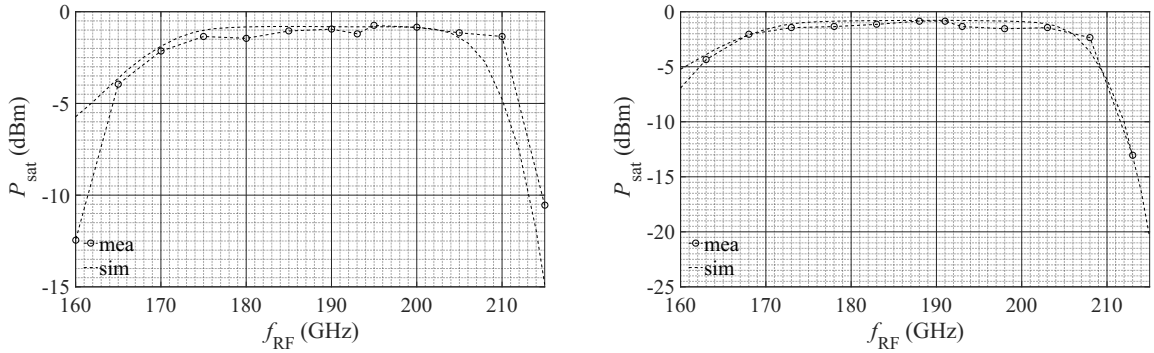


Figure 6.41: Simulated (line) and measured (symbols) (a) USB and (b) LSB P_{sat} of the receiver with fixed f_{IF} at 1 GHz and maximum CG bias.

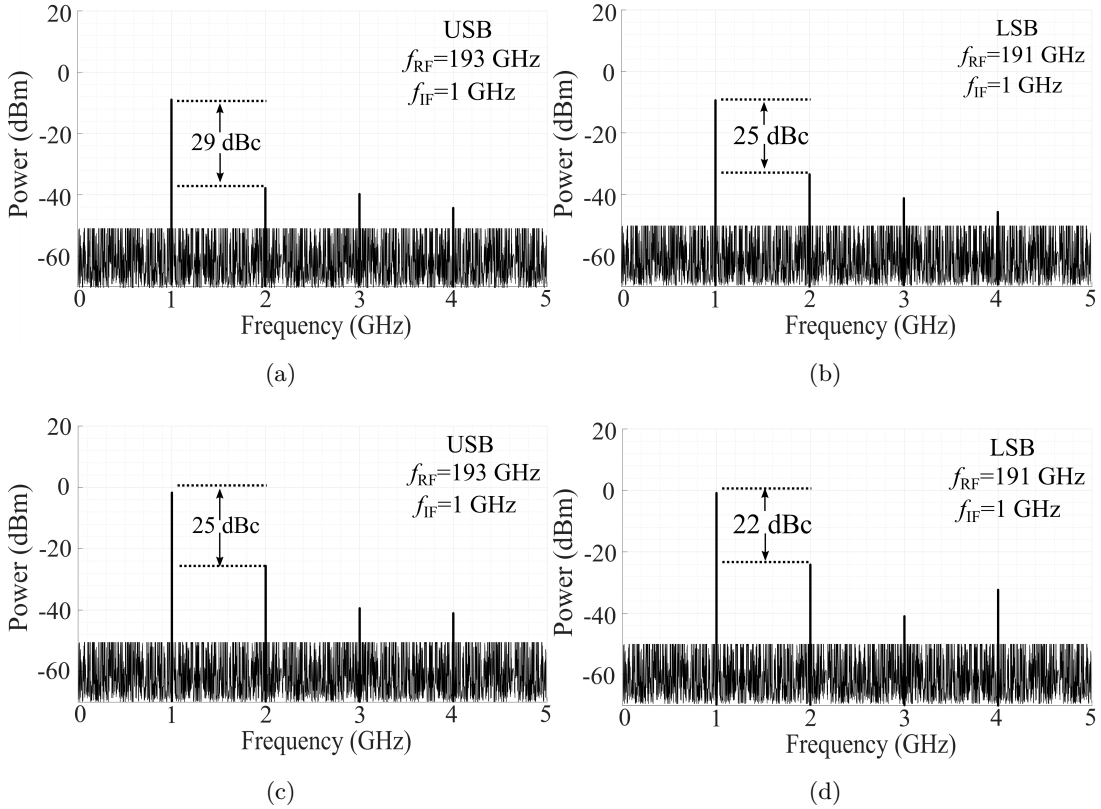


Figure 6.42: Measured (a), (c) USB and (b), (d) LSB IF power at (a), (b) 1-dB compression point and at (c), (d) saturation point with maximum CG bias at 193 and 191 GHz, respectively. The resolution BW of the spectrum analyzer is 500 kHz.

to 17 dB with minimum CG bias. As discussed before, because the first-stage LNA dominates the overall noise performance of the receiver as long as the LNA gain is higher than 15 dB, the overall receiver NF remains similar during the CG tuning. Notice that the overall measured NF is approximately 1-2 dB higher than the simulated one. Such deviation might come from larger losses and mismatches due to inaccurate EM simulation of the TLs and passive components, especially in the LNA.

Fig. 6.44 shows the measured and simulated return loss for the three ports of the receiver.

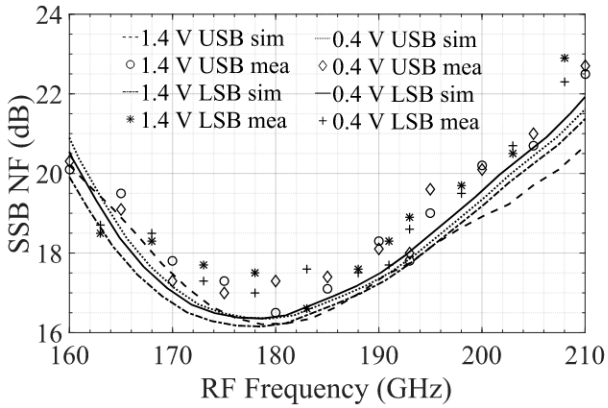


Figure 6.43: Measured (symbols) and simulated (lines) USB and LSB NF of the fabricated receiver biased for maximum and minimum CGs.

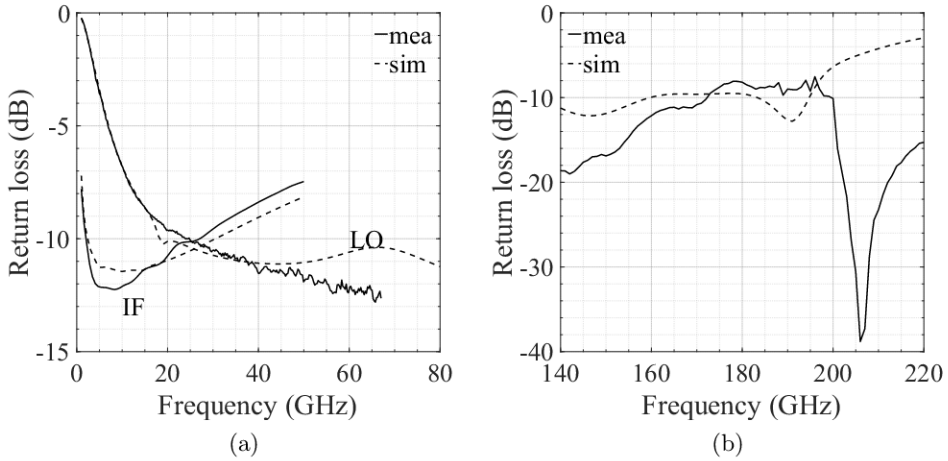


Figure 6.44: Measured and simulated (a) IF and LO, and (b) RF return loss.

As shown, below -10, -7, and -9 dB in-band return loss is observed or IF, LO, and RF port, respectively. The slightly higher return loss at the LO port is due to the active (transistor) matching at the input port of the active balun, which provides a noticeable inductive mismatch but significantly saves chip area by getting rid of the large on-chip inductor at this low frequency. For the LO and IF cases, simulation agrees reasonably well with measurement. The deviation observed for the RF return loss at high frequencies might be due to a non-perfect probe contact and inaccuracies in EM simulation.

Fig. 6.45 shows the measured CG for four different chips with maximum CG bias and fixed LO at 192 GHz (16 GHz off-chip) compared to simulation with typical parameters. The obtained CG is higher than 40 dB with a selectable IF frequency from 0.2 to 4 GHz. For four different chips, the measured CG shows a slight variation of less than 2 dB and good agreement with the simulation using typical parameters.

Table 6.2 demonstrates a summary of this work compared to the state-of-the-art mixer-based receivers having a CG higher than 10 dB and operating at and above 190 GHz, which were fulfilled in different technologies. As shown, the fundamental mixer was implemented in most of the receivers, except for [85, 174], in which the subharmonic mixer is implemented. The SiGe-HBT-based receivers provide a better performance, especially for the CG, compared to the CMOS-based receiver [164], mainly due to the higher RF speed. The mixer-first architecture was

Table 6.2: Comparison with stage-of-the-art mixer-based receivers at frequencies higher than 160 GHz

Ref.	[164]	[174]	[160]	[167]	[168]	[169]	[85]	[175]	**This work**
Tech.	65 nm CMOS	25 nm InP HEMT	130 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe	250 nm InP	**130 nm SiGe**
f_T/f_{max} (GHz)	≈130/200	610/1500	300/500	300/500	300/500	300/500	280/435	370/650	**300/500**
Archt.	antenna, IQ mixer, IF buf., LO mult.	LNA, sub. mixer, IF buf., LO mult.	LNA, mixer, IF VGA+buf., LO driver	antenna, LNA, IQ mixer, LO mult.	antenna, mixer, VGA, IF buf., LO mult., DC. loop	mixer, VGA, IF buf., LO mult., DC. loop, 3-ch FI	LNA, sub. mixer	LNA, mixer, IF buf., VCO, LO driver	**LNA, mixer, LO mult., LO driver**
LO type	x2+x3 +ILO+PA +x3	x3 +x3 +x2	LO driver	act. balun+x2 +x2+x2 +x2+PA	x4+amp +x2 +amp	3 channels x2, x4, x8	external	VCO +LO driver	**act. balun +x4+x3 LO driver**
f_{RF} (GHz)	240	670	190	240	240	240	220	300	**192**
f_{LO} (GHz)	13.3	326	190	15	30	22-30	110	300	**13.6-17.75**
CG (dB)	25	27.5	47	11	32	44	16	26	**49**
ΔCG (dB)	0	0	20	0	25	25	0	0	**14**
BW (GHz)	14^1	25^2	35^1	17^2	55^1	55^1	28^1	20^2	**16-23^1 27-32^2**
NF_{min} (dB)	15	10	10.7^D	15^S	13.4^S	14	15^D	12^D	**16.5^S**
P_{LO} (dBm)	0	0	-20	0	4	-10	0	N/A	**-30**
iP_{1dB} (dBm)	N/A	N/A	-45 to -28	-18	-28.5^3	N/A	N/A	-30	**-55 to -42**
oP_{1dB} (dBm)	N/A	N/A	-2	-8	-4	N/A	N/A	-5	**-8.1**
P_{dc} (mW)	80^r 260^w	630^r 1800^w	100^r 122^l	144^r 866^w	325^r 575^w	1435^w	216^w	202^r 482^w	**29^r 171^w**
Area (mm^2)	2	0.8	1.24	1.57	4.5	6.05	0.66	1.32	**3.6**
FoM	0.6	1	640	0.05	7.3	40	0.08	0.4	**213**

N/A: no information available; [1] 3 dB BW; [2] 6 dB BW; [D] DSB; [S] SSB; [w] with LO Chain; [l] with LO driver amplifier only; [r] receiver core; [3] At maximum gain setting.

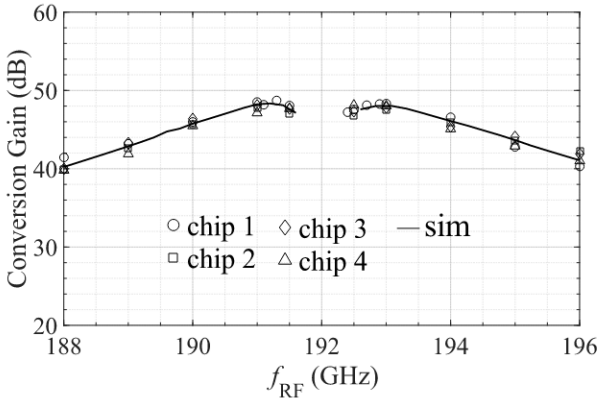


Figure 6.45: Measured (symbols) and simulated (lines) USB and LSB CG for four chips with maximum CG bias and fixed LO at 16×12=192 GHz.

used in [164, 168, 169], whereas the LNA-first architecture was used is in other listed receivers. The on-chip LO chain was used in [167–169] to relax the demand of LO frequency, while the additional voltage-controlled oscillators are used as the start stage in [164, 175]. In contrast, [160] just includes an LO driver on-chip, resulting in lowering on-chip P_{dc} but requiring an off-chip LO source in G-band. The high-frequency external source also applies to [85]. In [160, 168, 169], an IF VGA is implemented to obtain the CG tunability, which comes at the expense of a significant P_{dc} consumption in the receiver core.

As shown, the receiver achieved in this thesis achieves the highest listed CG of 49 dB, while the total consumed P_{dc} of 171 mW is the lowest reported value among those receivers with an on-chip LO chain. Due to the careful design of the LNA and mixer with HBTs operating with forward-biased V_{BC} and the achievement of direct CG tunability in the mixer, the P_{dc} of the receiver core has been significantly reduced to 29 mW, which is only around 1/3 of the lowest reported value in CMOS [164] and SiGe HBTs [160]. Furthermore, highly competitive performance in terms of RF bandwidth, CG tuning range, and NF have also been realized, making this receiver suitable for numerous applications. Taking into consideration the 3-dB BW, linear CG (gain), SSB noise (F), and P_{dc}, a suitable FoM can be defined as

$$\text{FoM} = \frac{\text{gain(1)} \cdot \text{BW(GHz)}}{\text{(F(1)-1)} \cdot P_{dc}\text{(mW)}}, \tag{6.7}$$

where F is the SSB noise factor. A high FoM indicates a better trade-off between DC power consumption and other essential performance. This work achieves the highest FoM value among receivers with LO chain, and the second-highest value among all receivers, while the top FoM in [160] was achieved by using just an on-chip LO driver amplifier without a G-band signal source, and thus requiring an additional high-frequency source externally. Furthermore, thanks to the ×12 LO chain with high CG, only -30 dBm LO power at around 15 GHz is required for this design. This is the lowest value listed in the table and significantly reduces the demand for the external LO source, allowing the implementation of a lossy off-chip power distribution network at the LO port for the multi-channel system with the common LO source. Moreover, for other applications requiring higher oP_{1dB}, the value could be further improved by around 4 dB by selecting larger devices (N_x=5) in the IF buffer amplifier and the active inverse balun stage. The corresponding simulation yields the same CG but around 12 mW higher P_{dc} in the receiver core.

6.3 Conclusion

In this chapter, the design method of a low-power receiver has been introduced. Aiming at realizing a better trade-off between key performance parameters and DC power consumption, the discussion contains the analysis of the receiver performance, the receiver topology optimization and FoMs distribution of each circuit block. Along this line, a G-band low-power receiver has been presented. Thanks to transistor operation in saturation which enables a significant decrease in supply voltage for the LNA and mixer, as well as the optimization of every circuit block with respect to performance and DC power, Highly competitive performance in terms of NF, RF BW, and CG tuning range, have been obtained simultaneously with the highest reported CG and the lowest reported DC power dissipation among receivers with LO chain have been achieved. First-pass success and good agreement between simulation and measurement have been enabled by accurate modeling and careful design.

7 Conclusions

7.1 Summaries

In this thesis work, the main objectives are to design, characterize and analyze low-power mm-wave circuits and systems based on the SiGe BiCMOS technology, aiming to realize a better trade-off between DC power dissipation and other key RF performance parameters. To this end, several low-power designs operating in different mm-wave frequency bands have been described in detail.

First, three 130 nm SiGe BiCMOS technologies have been introduced in Chapter 2, with the device feature and back-end process information. Besides, various circuit components and structures have been described in this Chapter, which are are utilized in this thesis to improve the design performance. For instance, the grounded-sidewall-shielded microstrip line for low-loss and cross-talk reduction, the zero-impedance line for DC distribution and circuit stabilization and the active/passive balun for differential to single-end signal conversion.

In Chapter 2-5, various mm-wave low-power circuits have been presented. The observed extremely low DC power dissipation has been realized by a drastic reduction in the supply voltage and collector current, forcing all transistors in the circuits to operate in saturation. Highly competitive performance in terms of gain, NF, and 3-dB BW has been simultaneously realized.

- A 173-207 GHz low-power amplifier has been designed with 23 dB gain and 3.2 mW P_{dc}. Excellent performance has been realized simultaneously with the lowest reported DC power consumption and an up to ten times improvement of the gain to DC power ratio.

- A 72-108 GHz low-power tunable amplifier has been presented with 10-23 dB gain and 4-21 mW P_{dc}. An additional tunability has been enabled with outstanding RF performance and extremely low DC power consumption. Thanks to the novel regional matching network design method, the wide 3-dB BW has been maintained within a large bias tuning range.

- A 97 GHz low-power down-conversion mixer was presented with 9.6 dB CG and 12 mW P_{dc}. Using the on-chip transformer coupled gilbert-cell, competitive performance in terms of CG and required LO power along with signal injection has been achieved simultaneously with very low-power dissipation.

- For multipliers, a 56-66 GHz low-power quadrupler with -3.6 dB peak CG and 12 mW P_{dc}, and a 172-201 GHz low-power tripler with -4 dB peak CG and 10.5 mW P_{dc} have been designed. By cascading these two circuits, also a 176-193 GHz low-power $\times$12 multiplier have been realized with -11 dBm output power and only 26 mW P_{dc}.

Moreover, the design and analysis of a 190 GHz ultra-low-power receiver have been introduced in Chapter 6. This receiver is designed as one receiving channel of a frequency extender specifically for a VNA-based measurement system but is also suitable for general applications

requiring a wide LO tuning range. A ×12 LO chain with high CG has been integrated on-chip. The obtained extremely low DC power consumption has been realized not only by the low-power design methods of LNA and mixer but also by optimizing every circuit block concerning performance and DC power. CG tunability has been directly attained by the mixer, obviating the need for an IF VGA. In terms of NF, RF BW, and CG tuning range, highly competitive performance parameters have been obtained simultaneously with the highest reported CG and the lowest reported DC power consumption among receivers with LO chain.

First-pass success has been achieved for all designs in this thesis, thanks in part to the compact model HICUM/L2. The overall simulation results demonstrate mostly excellent agreement with measurements. The sensitivity analysis of each design proceeds a deeper insight into the impact of transistor-related physical effects on critical circuit performance parameters. Such studies do provide meaningful feedback for process improvement and modeling development has been obtained based on the observed excellent agreement,

7.2 Outlook

At the time of thesis writing, the investigation of G-band VNA extender integrated active probe has still been in process. Hence, future work will cover the packaging design and verification for the chip of the G-band receiver channel and signal chain (presented in Chapter 6). The receiver chip and signal chain chip will be packaged into a waveguide environment and then connected with the 3D printed probe for the small-signal network measurement. Additonally, the H-band (220-325 GHz) frequency extender related designs would be a future goal.

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A | Derivation of the G_{m}

This appendix demonstrates the derivation of G_{m} of the standard cascode stage, cascode stage with L_{b}, and with L_{cas} presented in Section 3.1.4.1.

A.1 G_{m} of standard cascode stage

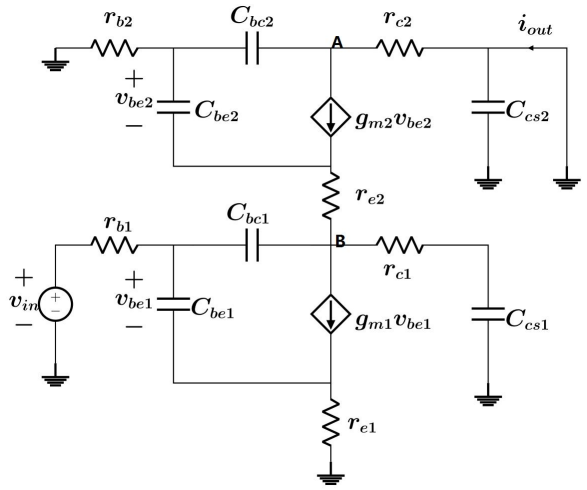

Figure A.1: Simplified small-signal equivalent circuit of standard cascode stage.

Neglecting all the resistance elements,setting k=jω, and using Kirchhoff's current law (KCL) at point A

$$i_{\mathrm{out}} = i_{\mathrm{cbc2}} + i_{\mathrm{ccs2}} + i_{\mathrm{gm2vbe2}} = 0 + 0 + g_{\mathrm{m2}}V_{\mathrm{be2}}, \tag{A.1}$$

where i_{cbc2}, i_{ccs2}, i_{gm2vbe2} are the current of C_{bc2}, C_{cs2}, and the voltage-controlled current source 2, respectively. Here, i_{out} flows towards point A, whereas the others are with the opposite directions, i.e., flow out from point A. Using KCL at point B

$$\begin{aligned} g_{\mathrm{m2}}V_{\mathrm{be2}} &= i_{\mathrm{gm1vbe1}} + i_{\mathrm{cbe2}} + i_{\mathrm{cbc1}} + i_{\mathrm{ccs1}} \\ &= g_{\mathrm{m1}}V_{\mathrm{be1}} + V_{\mathrm{b}}k(C_{\mathrm{cs1}} + C_{\mathrm{be2}}) + (V_{\mathrm{b}} - V_{\mathrm{be1}})kC_{\mathrm{bc1}}, \end{aligned} \tag{A.2}$$

where i_{cbe2}, i_{cbc1}, i_{ccs1}, and i_{gm1vbe1} are the current of C_{be2}, C_{bc1}, C_{cs1}, and the voltage-controlled current source 1, respectively. Similarly, i_{gm2vbe2} flows into A, whereas others flow out. V_{b} is the voltage at point b for calculation. Since

$$V_{\mathrm{b}} = -V_{\mathrm{be2}}, \tag{A.3a}$$

$$V_{\mathrm{in}} = -V_{\mathrm{be1}}, \tag{A.3b}$$

the input voltage V_{in} becomes

$$V_{in} = \frac{g_{m2} + k(C_{cs1} + C_{be2} + C_{bc1})V_b}{kC_{bc1} - g_{m1}}, \tag{A.4}$$

Then,

$$\begin{aligned} G_m &= \frac{i_{out}}{V_{in}}, \\ &= \frac{g_{m2}(g_{m1} - j\omega C_{bc1})}{g_{m2} + j\omega(C_{bc1} + C_{be2} + C_{cs1})}. \end{aligned} \tag{A.5}$$

A.2 G_m of cascode stage with L_{cas}

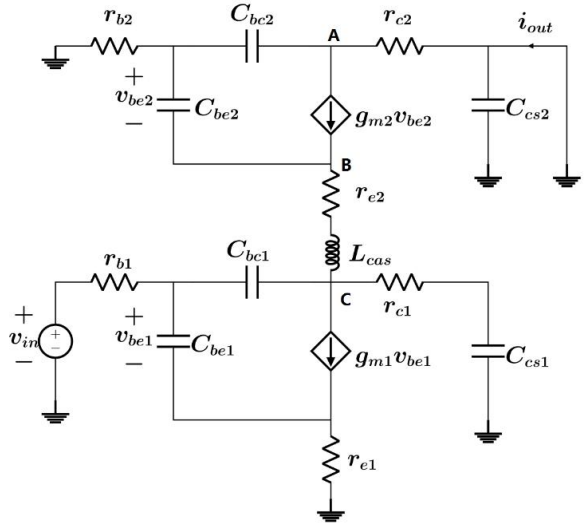

Figure A.2: Simplified small-signal equivalent circuit of cascode stage with L_{cas}.

Also neglecting all resistance elements and using KCL at point A,

$$i_{out} = -g_{m2}V_b. \tag{A.6}$$

Using KCL at point B,

$$-g_{m2}V_b = V_b kC_{be2} + \frac{V_b - V_c}{kL_{cas}}. \tag{A.7}$$

Using KCL at point C,

$$\frac{V_b - V_c}{kL_{cas}} = (V_b - V_c)kC_{bc1} + V_c kC_{cs1} + g_{m1}V_{in}. \tag{A.8}$$

From equation A.7,

$$V_c = kL_{cas}(g_{m2} + kC_{be2} + \frac{1}{kL_{cas}}). \tag{A.9}$$

Substitude equation A.9 from equation A.8,

$$V_{in} = \frac{V_b[(kC_{be2} + g_{m2}) + k^2 L_{cas}(C_{bc1} + C_{cs1})(g_{m2} + kC_{be2} + \frac{1}{kL_{cas}})]}{kC_{be1} - g_{m1}}. \tag{A.10}$$

Finally,

$$G_{\mathrm{m}} = \frac{g_{\mathrm{m2}}(g_{\mathrm{m1}} - j\omega C_{\mathrm{bc1}})}{g_{\mathrm{m2}}[1 - (\frac{\omega}{\omega_{\mathrm{r1}}})^2] + j\omega[C_{\mathrm{bc1}} + C_{\mathrm{cs1}} + C_{\mathrm{be2}}[1 - (\frac{\omega}{\omega_{\mathrm{r1}}})^2]]}, \tag{A.11}$$

with

$$\omega_{\mathrm{r1}} = \frac{1}{\sqrt{L_{\mathrm{cas}}(C_{\mathrm{cs1}} + C_{\mathrm{bc1}})}}. \tag{A.12}$$

A.3 G_{m} of cascode stage with L_{b}

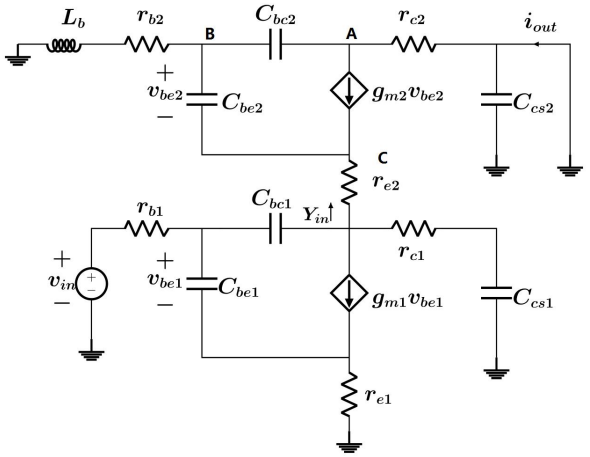

Figure A.3: Simplified small-signal equivalent circuit of cascode stage with L_{b}.

Neglecting all resistance elements and using KCL at point A,

$$i_{\mathrm{out}} = -[V_{\mathrm{b}} k C_{\mathrm{bc2}} + g_{\mathrm{m2}}(V_{\mathrm{c}} - V_{\mathrm{b}})]. \tag{A.13}$$

Using KCL at point B,

$$kC_{\mathrm{be2}}(V_{\mathrm{c}} - V_{\mathrm{b}}) = V_{\mathrm{b}}(kC_{\mathrm{bc2}} + \frac{1}{kL_{\mathrm{b}}}). \tag{A.14}$$

Using KCL at point C,

$$(g_{\mathrm{m2}} + kC_{\mathrm{be2}})(V_{\mathrm{b}} - V_{\mathrm{c}}) = V_{\mathrm{c}} k(C_{\mathrm{cs1}} + C_{\mathrm{bc1}}) + (g_{\mathrm{m1}} - kC_{\mathrm{bc1}})V_{\mathrm{in}}. \tag{A.15}$$

Then,

$$V_{\mathrm{c}} - V_{\mathrm{b}} = \frac{kC_{\mathrm{bc2}} + \frac{1}{kL_{\mathrm{b}}}}{kC_{\mathrm{be2}}} V_{\mathrm{b}}, \tag{A.16}$$

and,

$$V_{\mathrm{c}} = \frac{k(C_{\mathrm{bc2}} + C_{\mathrm{be2}}) + \frac{1}{kL_{\mathrm{b}}}}{kC_{\mathrm{be2}}} V_{\mathrm{b}}, \tag{A.17}$$

Then V_{in} turn out to be

$$V_{\mathrm{in}} = -\frac{[(g_{\mathrm{m2}} + kC_{\mathrm{be2}})(V_{\mathrm{c}} - V_{\mathrm{b}}) + V_{\mathrm{c}} k(C_{\mathrm{cs1}} + C_{\mathrm{bc1}})]}{g_{\mathrm{m1}} - kC_{\mathrm{bc1}}}. \tag{A.18}$$

Thus, G_m becomes

$$G_\mathrm{m} = \frac{[g_\mathrm{m2}(1+k^2C_\mathrm{bc2}L_\mathrm{b}) + k^3C_\mathrm{be2}C_\mathrm{bc2}L_\mathrm{b}](g_\mathrm{m1} - kC_\mathrm{bc1})}{g_\mathrm{m2}(1+k^2C_\mathrm{bc2}L_\mathrm{b}) + k[C_\mathrm{be2}(1+k^2C_\mathrm{bc2}L_\mathrm{b}) + C_\mathrm{bc1} + C_\mathrm{cs1} + k^2(C_\mathrm{be2}+C_\mathrm{bc2})(C_\mathrm{bc1}+C_\mathrm{cs1})L_\mathrm{b}]}. \tag{A.19}$$

Finally, G_m can be simplified by dividing $(1+k^2C_\mathrm{bc2}L_\mathrm{b})$, as

$$G_\mathrm{m} = \frac{(g_\mathrm{m2} + j\omega\frac{C_\mathrm{be2}}{1-(\omega_\mathrm{r3}/\omega)^2})(g_\mathrm{m1} - j\omega C_\mathrm{bc1})}{g_\mathrm{m2} + j\omega[C_\mathrm{be2} + \frac{C_\mathrm{bc1}+C_\mathrm{cs1}-(\omega/\omega_\mathrm{r2})^2}{1-(\omega/\omega_\mathrm{r3})^2}]}, \tag{A.20}$$

with

$$\omega_\mathrm{r2} = \frac{1}{\sqrt{L_\mathrm{b}(C_\mathrm{be2}+C_\mathrm{bc2})(C_\mathrm{bc1}+C_\mathrm{cs1})}}, \tag{A.21a}$$

$$\omega_\mathrm{r3} = \frac{1}{\sqrt{L_\mathrm{b}C_\mathrm{bc2}}}. \tag{A.21b}$$

B Derivation of Y_{in} in the stability analysis

This appendix demonstrates the derivation of Y_{in} in the stability analysis presented in Section 3.1.4.2.

Recalling Fig. A.3 by neglecting all the resistive elements and L_{cas} in Fig. 3.18, the input current I_{in} from the collector of CE device to emitter of CB device can be expressed using KCL at point c as

$$I_{\text{in}} = (V_{\text{c}} - V_{\text{b}})(kC_{\text{be2}} + g_{\text{m2}}), \tag{B.1}$$

where V_{c} and V_{b} are the voltages at point b and point c, respectively. Using KCL at point b,

$$(V_{\text{c}} - V_{\text{b}})(kC_{\text{be2}}) = V_{\text{b}}(kC_{\text{bc2}} + \frac{1}{kL_{\text{b}}}). \tag{B.2}$$

Then,

$$\begin{aligned} V_{\text{c}} - V_{\text{b}} &= \frac{V_{\text{b}}(kC_{\text{bc2}} + \frac{1}{kL_{\text{b}}})}{kC_{\text{be2}}}, \\ V_{\text{c}} &= \frac{V_{\text{b}}(k(C_{\text{bc2}} + C_{\text{be2}}) + \frac{1}{kL_{\text{b}}})}{kC_{\text{be2}}}. \end{aligned} \tag{B.3}$$

Hence,

$$Y_{\text{in}} = \frac{I_{\text{in}}}{V_{\text{c}}} = \frac{(g_{\text{m2}} + j\omega C_{\text{be2}})[1 - (\omega/\omega_{\text{r3}})^2]}{[1 - (\omega/\omega_{\text{r4}})^2]}, \tag{B.4}$$

and

$$\omega_{r4} = \frac{1}{\sqrt{L_b(C_{be2} + C_{bc2})}}. \tag{B.5}$$

The boundary condition of the real part of Y_{in} can be written as

$$\begin{cases} Re\{Y_{\text{in}}\} \geqslant 0, & \omega_{\text{r3}} \geqslant \omega_{\text{r4}} \geqslant \omega \\ Re\{Y_{\text{in}}\} \leqslant 0, & \omega_{\text{r3}} \geqslant \omega \geqslant \omega_{\text{r4}} \\ Re\{Y_{\text{in}}\} \geqslant 0, & \omega \geqslant \omega_{\text{r3}} \geqslant \omega_{\text{r4}} \end{cases} \tag{B.6}$$

C | Derivation of Z_{in} and Z_{out}

This appendix demonstrates the derivation of Z_{in} and Z_{out} presented in Section 3.2.2.1.

C.1 Z_{in}

The voltage gain A_v is defined as the ratio of output and input voltages, as

$$A_v = \frac{v_{out}}{v_{in}}. \tag{C.1}$$

Based on Fig. 3.32a and Fig. C.1, and focusing on the bottom CE transistor of the cascode

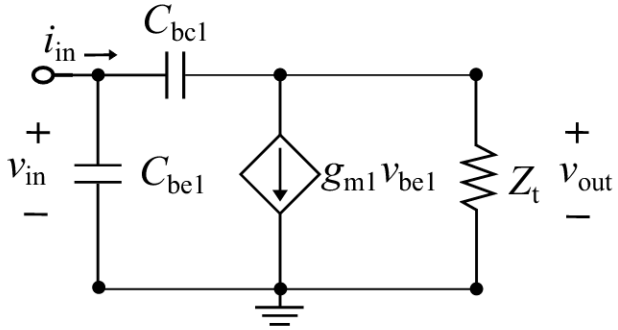

Figure C.1: Simplified small-signal equivalent circuit of bottom CE device of the cascode stage.

stage at first, the equivalent circuit of the bottom CE transistor of the cascode stage is simplified as Fig. C.1. Here, Z_t is the equivalent load impedance of CE transistor (cf. Fig. C.1). According to Fig. C.1, we have

$$(v_{in} - v_{out})j\omega C_{bc1} = g_{m1}v_{in} + \frac{v_{out}}{Z_t}. \tag{C.2}$$

Then, the A_v of CE device becomes

$$A_{v,CE} = \frac{(j\omega C_{bc1} - g_{m1})Z_t}{j\omega C_{bc1}Z_t + 1}, \tag{C.3}$$

where Z_t is the equivalent load impedance, which consists of r_{01}, C_{cs1}, and the input impedance of the upper CB transistor $Z_{in,\,CB}$. Then the input impedance Z_{in} of the cascode stage can be written as

$$\begin{aligned} Z_{in} &= \frac{v_{in}}{j\omega C_{bc1}(v_{in} - v_{out}) + j\omega C_{be1}v_{in}}, \\ &= \frac{1}{j\omega[C_{bc1}(1 - A_{v,CE}) + C_{be1}]}. \end{aligned} \tag{C.4}$$

Under the condition of zero output voltage v_{out} (shorted) of the cascode stage, the simplified small-signal equivalent circuit of the upper CB transistor is shown in the left of Fig. C.2. As

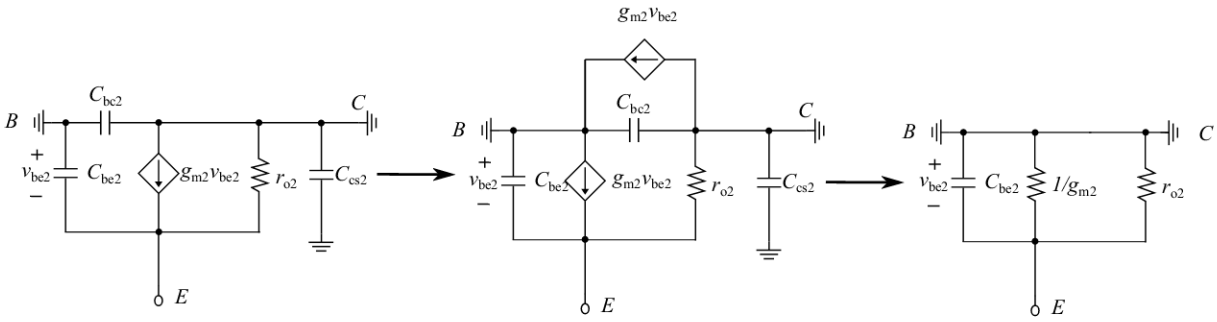

Figure C.2: Simplified small-signal equivalent circuit of the upper CB device with zero v_{out} (shorted) in the cascode stage.

seen, the current source is located between nodes C and E. This current source can be split into two series current sources with the same current value ($g_{m2}V_{be2}$) and with the shared node B (cf. Fig. C.2). Then, the current source between B and E can be replaced by a resistor (R=V/I=$1/g_{m2}$). Besides, the current source between C and B, C_{bc2}, and C_{cs2} are shorted. Finally, the simplified small-signal equivalent circuit can be transferred to the right of Fig. C.2, and $Z_{in,\,CB}$ saw from node E can be written as

$$Z_{in,CB} = \frac{1}{g_{m2} + j\omega C_{be2} + \frac{1}{r_{02}}}. \tag{C.5}$$

Z_t can be described as

$$Z_t = \frac{1}{j\omega[C_{be2} + C_{cs1}] + g_{m2} + \frac{1}{r_{01}} + \frac{1}{r_{02}}}, \tag{C.6}$$

and Fig. C.1 becomes Fig. 3.32b. To further simplify $A_{v,CE}$ and Z_{in}, the numerical check based on extracted parameters the operation point simulation of HICUM/L2 model at 100 GHz, are listed in Table C.1, for the four bias examples covering the entire tunning range shown in Section 3.2.2.1. As can be seen, at 100 GHz, $|j\omega C_{bc1}Z_t| \ll 1$, and $|j\omega C_{bc1}| < g_{m1}/6$ (minimum

Table C.1: Numerical check of $A_{v,CE}$ based on operation point simulation at 100 GHz

	Case 1	Case 2	Case 3	Case 4
$j\omega C_{bc1}Z_t$	0.0058+0.0255j	0.0082+0.0335j	0.0099+0.0414j	0.0107+0.055j
$j\omega C_{bc1}$	0.0046j	0.0048j	0.005j	0.0056j

g_{m1} of 0.033 S within the tunning range), therefore these two terms are neglectable, and the voltage gain of CE transistor can be then written as

$$A_{v,CE} \approx -g_{m1}Z_t, \tag{C.7}$$

and the input impedance Z_{in} of the cascode stage can be then written as

$$Z_{in} \approx \frac{1}{j\omega[C_{be1} + (1 + g_{m1}Z_t)C_{bc1}]}. \tag{C.8}$$

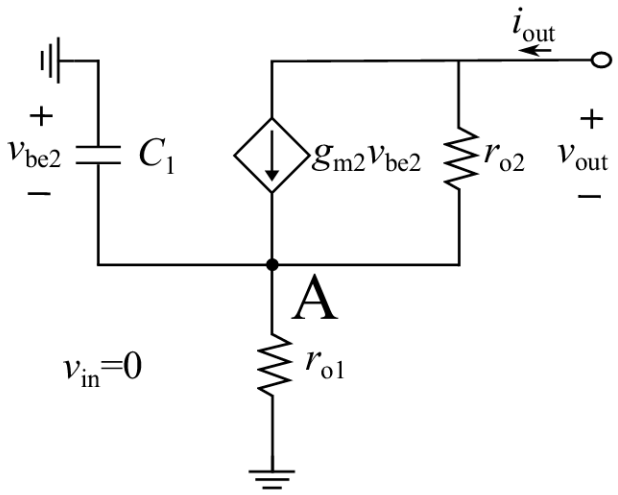

Figure C.3: First part of the simplified small-signal equivalent circuit for Z_{out} analysis.

C.2 Z_{out}

Under the condition of zero input voltage (input shorted), the simplified small-signal equivalent circuit shown in Fig. 3.32c can be separated into two parallel parts. The first part is shown in Fig. C.3, and the second part contains two shunt capacitances (C_{bc2} and C_{cs2}) at the collect note of the upper CB device. Naming the black node A, the voltage at this node is v_A, setting k=jω, and using KCL at the output port yields

$$i_{out} = \frac{v_{out} - v_A}{r_{02}} + g_{m2}v_{be2}, \tag{C.9a}$$

$$v_{be2} = -v_A. \tag{C.9b}$$

Thus,

$$i_{out}r_{02} = v_{out} - (1 + g_{m2}r_{02})v_A, v_{out} = i_{out}r_{02} + (1 + g_{m2}r_{02})v_A. \tag{C.10}$$

and

$$v_{out} = i_{out}r_{02} + (1 + g_{m2}r_{02})v_A. \tag{C.11}$$

Using KCL at node A,

$$i_{out} = (kC_1 + \frac{1}{r_{01}})v_A. \tag{C.12}$$

Thus,

$$Z_{out,1} = \frac{v_{out}}{i_{out}}|_{v_{in}=0} \tag{C.13a}$$

$$= \frac{(kC_1 + \frac{1}{r_{01}})v_A r_{02} + (1 + g_{m2}r_{02})v_A}{(kC_1 + \frac{1}{r_{01}})v_A} \tag{C.13b}$$

$$= r_{02} + \frac{g_{m2}r_{02} + 1}{\frac{1}{r_{01}} + j\omega C_1}. \tag{C.13c}$$

Then, considering the second part of the shunt capacitances, the total Z_{out} becomes

$$Z_{out} = (r_{02} + \frac{g_{m2}r_{02} + 1}{\frac{1}{r_{01}} + j\omega C_1})||\frac{1}{j\omega C_2}. \tag{C.14}$$

with

$$C_1 = C_{\text{bc1}} + C_{\text{cs1}} + C_{\text{bc2}}, \tag{C.15a}$$

$$C_2 = C_{\text{bc2}} + C_{\text{cs2}}. \tag{C.15b}$$

D | Derivation of the cascaded oP_{1dB}

This appendix demonstrates the derivation of the cascaded oP_{1dB} presented in Section 6.1, equation 6.6.

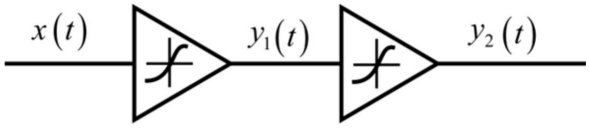

Figure D.1: Simplified block diagram of the cascaded two-satge nonlinear circuit [176].

Considering a two-stage nonlinear circuit, as shown in Fig. D.1. With the input voltage x(t), the output voltage y_1(t) of the first stage can be expressed as

$$y_1(t) = a_1x(t) + a_2x^2(t) + a_3x^3(t). \tag{D.1}$$

Here, we assume that the harmonic components with the order higher than 3 are small enough and thus are neglected for easier calculation, and a_1, a_2, a_3 are the unknown constants. Additionally, due to the most RF circuits and systems of interest are compressive, the second-order term in the output can also be neglected here due to its expansive characteristic [176]. Therefore, we have

$$y_1(t) \approx a_1x(t) + a_3x^3(t). \tag{D.2}$$

Setting x(t)=Acos(ωt),

$$y_1(t) \approx (a_1 + \frac{3a_3A^2}{4})Acos(\omega t) + \frac{a_3A^3}{4}cos(3\omega t). \tag{D.3}$$

To calculate the input 1 dB compression, we equate the compressed voltage gain to 1 dB less than the ideal voltage gain of the fundamental harmonics a_1,

$$20log|a_1 + \frac{3a_3A^2}{4}| = 20log|a_1| - 1, \tag{D.4}$$

Then we have

$$A_{\text{in,1dB,1}} = \sqrt{0.145|\frac{a_1}{a_3}|} \tag{D.5}$$

Similarly for the second stage, we have

$$y_2(t) \approx b_1y_1(t) + b_3y_1^3(t), \tag{D.6}$$

and

$$A_{\text{in,1dB,2}} = \sqrt{0.145|\frac{b_1}{b_3}|}. \tag{D.7}$$

Combining equation D.2 and equation D.6 for the cascaded two-stage nonlinear circuit, we have

$$y_2(t) = b_1[a_1x(t) + a_3x^3(t)] + b_3[a_1x(t) + a_3x^3(t)]^2 \tag{D.8}$$

Here, we also keep the first and third order terms and neglect the second and higher-order terms which lead to expansive characteristics, then we get

$$y_2(t) \approx b_1a_1x(t) + (a_3b_1 + a_1^3b_3)x^3(t). \tag{D.9}$$

Similarly, the input 1 dB compression of the two-stage circuit can be calculated as

$$\begin{aligned} A_{\text{in,1dB,total}} &= \sqrt{0.145|\frac{a_1b_1}{a_3b_1 + a_1^3b_3}|}, \\ \frac{1}{A^2_{\text{in,1dB,total}}} &= \frac{a_3}{0.145a_1} + \frac{a_1^2b_3}{0.145b_1}, \\ \frac{1}{A^2_{\text{in,1dB,total}}} &= \frac{1}{A^2_{\text{in,1dB,1}}} + \frac{a_1^2}{A^2_{\text{in,1dB,2}}}. \end{aligned} \tag{D.10}$$

Since the 1 dB compression leads to only around 10% lower than the ideal gain, it is reasonable to use the overall ideal voltage gain of two-stage circuit a1*b1 to evaluate the output 1 dB compression point and simplify the equation

$$\begin{aligned} A_{\text{out,1dB,total}} &\approx A_{\text{in,1dB,total}}a_1b_1, \\ A_{\text{out,1dB,1}} &\approx A_{\text{in,1dB,1}}a_1, \\ A_{\text{out,1dB,2}} &\approx A_{\text{in,1dB,2}}b_1. \end{aligned} \tag{D.11}$$

For the system with the same input and output impedance, the relation between voltage gain G_{v} and power gain G_{p} in linear scale is

$$G_{\text{p}} = G_{\text{v}}^2, \tag{D.12}$$

hence the output power 1 dB compression in linear scale becomes

$$\frac{1}{oP_{\text{1dB, total}}} = \frac{1}{oP_{\text{1dB, 1}}G_{\text{p,2}}} + \frac{1}{oP_{\text{1dB, 2}}}. \tag{D.13}$$

E Table of element values for the designed circuits

Table E.1: Value of important parameters for the 15 GHz actie baun in Section 2.2.3.1

R_1	R_2	R_3	R_4	R_5	R_6	R_7
200 Ω	10 kΩ	500 Ω	450 Ω	1.5 kΩ	1.5 kΩ	3.5 kΩ
C_1	C_2	T1,T8	T2-T7			
500 fF	3 pF	N_x=1	N_x=2			

Table E.2: Value of important parameters for the 173-297 GHz LNA in Section 3.1

L_{cas}	L_b	R_{bs}	T1-T6	C_{block}	V_{supply}	V_{BB}	V_{UB}
21 pH	10 pH	4 Ω	N_x=2	30 fF	1.3 V	0.84 V	1.5 V

Table E.3: Value of important parameters for the 72-108 GHz LNA in Section 3.2

L_{cas}	L_b	R_{bs}	$A_{e\text{-}W,\ T1\text{-}T6}$	C_{block}	R_{bb}	V_{supply}	V_{BB}	V_{UB}
15 pH	13 pH	15 Ω	0.13 μm×4.91 μm	90 fF	4 kΩ	0.9-1.6 V	0.84-0.9 V	1.3-1.7 V

Table E.4: Value of important parameters for the 97 GHz mixer in Section 4.1

L_1	L_2	R_L	$R_{1\text{-}5}$	R_6	$A_{\text{e-W, T1-T4}}$	$A_{\text{e-W, T5-T8}}$
1.2 nH	0.8 nH	50 Ω	2.5 kΩ	350 Ω	0.13 μm×9.71 μm	0.13 μm×2.21 μm
$C_{1,2}$	$C_{3\text{-}6}$	$C_{7\text{-}10}$	$C_{11\text{-}13}$	V_{supply}	V_{B1}	V_{B2}
400 fF	90 fF	96 fF	500 fF	0.7/0.5 V	0.84 V	0.9 V
V_{buffer}						
1.2 V						

Table E.5: Value of important parameters for the 66 GHz frequency quadrupler in Section 5.2

L_1	L_2	L_3	$C_{1\text{-}2}$	$C_{3\text{-}4}$	$C_{5\text{-}6}$	T1
0.6 nH	0.6 nH	1.52 nH	150 fF	940 fF	46 fF	N_x=8
w_{TL}	V_{CE}	V_{BE}				
10 μm	1.4/0.7/0.5 V	0.82 V				

Table E.6: Value of important parameters for the 172-201 GHz tripler in Section 5.3

R_1	C_1	C_2	T1-T4	w_{TL}	$V_{TRI,b1}$	$V_{TRI,b2}$
3 kΩ	150 fF	80 fF	N_x=6	12 μm	0.86 V	0.94 V
$V_{TRI,c1}$						
0.7/0.5 V						

Table E.7: Value of important parameters for the G-band LNA/DA in Section 6.2.3.1

R_1	C_1	$L_{b,\text{ LNA}}$	$L_{cas,\text{ LNA}}$	w_{TL}	T1-T4	V_{BC} (DA/LNA)
4 kΩ	90 fF	7 pH	12 pH	10 μm	N_x=2	-0.4/0.2 V
J_C (DA/LNA)						
22/12 μ^2						

Table E.8: Value of important parameters for the G-band mixer in Section 6.2.3.2

C_1	C_2	C_3	R_1	R_2	R_3	R_4
30 fF	35 fF	4.6 pF	10 kΩ	500 Ω	10 kΩ	300 Ω
R_5	R_6	R_7	T1-T10	V_{MIX}	V_{BC}	
5.5 kΩ	230 Ω	27.7 kΩ	N_x=2	0.4-1.4 V	-0.5-0.5 V	

Yaxin Zhang

INFORMATION

Birth: 16/10/1991 *Gender*: Male *Nationality*: Chinese *Work permit*: **Unlimited (Niederlassungserlaubnis)**
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EXPERIENCE

Scientific Researcher (Wissenschaftlicher Mitarbeiter) at Technische Universität Dresden 08/2017-Now
Chair for Electron Devices and Integrated Circuits (5G Lab Germany), Dresden, Germany

- Design and characterization of **millimeter-wave circuits and receiver systems** based on **SiGe BiCMOS** and **InP (III-V) HBTs** up to 325 GHz, and benchmark circuit design for **HICUM model** verification

Guest Researcher at Ferdinand-Braun-Institut 08/2016-05/2017
III-V Electronics Department, Berlin, Germany

Research Fellow at Technical University of Denmark
Electromagnetic Systems Group, Lyngby, Denmark

- Design of **millimeter-wave nonlinear circuits** based on **Transfer-Substrate InP (III-V) HBTs** up to 325 GHz

Research Assistant at Chalmers University of Technology 02/2015-07/2016
Terahertz and Millimetre Wave Laboratory, MC2, Gothenburg, Sweden

- Design, fabrication, and characterization of **Graphane-FET (G-FET)** device and **G-FET** based **millimeter-wave circuits and receiver systems** up to 220 GHz

PROJECTS

HBT modeling and circuit design for low-power mm-wave applications (DFG, Germany)

- Design and characterization of **SiGe** and **InP (III-V) HBT** based low-power circuits: 97 GHz **mixer**s, 160 and 200 GHz **LNA**s, 200 GHz **×12 multiplier chain**
- **Responsible person** of chip-assembly, measurement, and communication with foundries

TowARds Advanced bicmos NanoTechnology platforms for rf and thz applicatiOns (ECSEL, Europe)

- Design and characterization of **SiGe** and **InP (III-V) HBT** based circuits: 80-190 GHz **ultra-broadband PAs**, 200 GHz **frequency doubler**, and device HICUM modeling related **benchmark circuit blocks**
- **Responsible person** of work package 3, task 1.1, chip-assembly, and verification

Active Probe for On-Wafer SiGe HBT Device Characterization up 750 GHz (APSICA, DFG, Germany)

- Independent design and on-chip verification of **SiGe** based **×12 LO chain integrated 190 GHz low-power receiver system** (mixer+LNA+IF buffers+×12 LO multiplier+LO driver amplifier)
- **Project responsible person** and coordination of packaging process and system verification

Carbon Based High-Speed 3D GaN Electronics System (Swedish Foundation for Strategic Research, Sweden)

- Design, fabrication, and characterization of in-house **G-FET** device and 200 GHz **receiver**
- Full-time participation in cleanroom fabrication and verification of device and chip

EDUCATION

Doctor of Philosophy (pending graduation) 2017-2021
Microelectronics, Technische Universität Dresden, Dresden, Germany

Master of Science (GPA: 4.625/5, Ranking: 1/22) 2014-2016
Wireless Photonics and Space Engineering, Chalmers University of Technology, Gothenburg, Sweden

Bachelor of Engineering (GPA: 83.6/100, Ranking: 26/147) 2010-2014
Optoelectronic Technology, University of Electronic Science and Technology of China, Chengdu, China

AWARDS

- 2014 The IPOET Scholarships (Master tuition fee waivers), Sweden
- 2015 Adlerbert 60th Anniversary Scholarships (GPA **Top 10** international students), Sweden

SKILLS

Fabrication technologies: **Infineon AG** B11HFC, B12HFC; **IHP** SG13G2, SG13D7 (G3), **Teledyne** TD250, TD130
Tools: Keysight ADS, Cadence Virtuoso, CST Microwave Studio, Ansys HFSS, Matlab
Equipment: Vector network analyzers, spectrum analyzers, signal generators, power meters, and Suss/Cascade probe stations setup up to 325 GHz
Languages: English (Articulate, technically very proficient), Chinese (mother language), German (A1-A2)

PUBLICATIONS

Top journals with the **first authorship** in ***IEEE JSSC, T-MTT, MWCL***, please find attached "List of Publications"

List of Publications

[1] **Y. Zhang**, W.Liang, X. Jin, M. Krattenmacher, S. Falk, P. Sakalas, B. Heinemann and M. Schröter, "3.2-mW Ultra-Low-Power 173–207-GHz Amplifier With 130-nm SiGe HBTs Operating in Saturation," ***IEEE Journal of Solid-State Circuits***, vol. 55, no. 6, pp. 1471-1481, Jun. 2020.

[2] **Y. Zhang**, W.Liang, C. Esposito, X. Jin, P. Sakalas and M. Schröter, "LO Chain (×12) Integrated Low-power SiGe 190 GHz Receiver With 49 dB Conversion Gain and 171 mW DC Power Consumption," ***IEEE Transactions on Microwave Theory and Techniques***, vol. 69, no. 3, pp. 1943-1954, Mar. 2021.

[3] **Y. Zhang**, W. Liang, P. Sakalas, A. Mukherjee, X. Jin, J. Krause and M. Schröter, "12-mW 97-GHz Low-Power Downconversion Mixer With 0.7-V Supply Voltage," ***IEEE Microwave and Wireless Components Letters***, vol. 29, no. 4, pp. 279-281, Apr. 2019.

[4] M. A. Andersson, **Y. Zhang** and J. Stake, "A 185–215-GHz Subharmonic Resistive Graphene FET Integrated Mixer on Silicon," ***IEEE Transactions on Microwave Theory and Techniques***, vol. 65, no. 1, pp. 165-172, Jan. 2017.

[5] X. Jin, M. Müller, P. Sakalas, A. Mukherjee, **Y. Zhang** and M. Schröter, "Advanced SiGe:C HBTs at cryogenic temperatures and their compact modeling with temperature scaling," ***IEEE Journal on Exploratory Solid-State Computational Devices and Circuits***, doi: 10.1109/JXCDC.2021.3130041.

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[8] M. Bonmann, M. A. Andersson, **Y. Zhang**, X. Yang, A. Vorobiev and J. Stake, "An Integrated 200-GHz Graphene FET Based Receiver," *43rd International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)*, Nagoya, 2018, pp. 1-3.

[9] A. Omar, A. Mukherjee, W. Liang, **Y. Zhang**, P. Sakalas and M. Schröter, "82 GHz Direct Up-converter Mixer using Double-Balanced Gilbert Cell with Sensitivity Analysis at Mm-wave Frequency," *IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Nashville, TN, USA, 2019, pp. 1-4.

[10] X. Jin, C. Weimer**, Y. Zhang** and M. Schröter, "Modeling the Temperature Dependence of Sheet Resistances in SiGe:C HBTs from 4.3 to 423 K," *IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2020, pp. 1-4.

[11] W Liang, A. Mukherjee **Y. Zhang** and M Schröter, "Circuit activities for compact model verification at mm-wave frequency," *HICUM Workshop*, Rohde & Schwarz, Munich, Jun. 2019.

[12] **Y. Zhang**, W.Liang, C. Esposito, X. Jin, P. Sakalas and M. Schröter, "26 mW 190 GHz Low-power Frequency Multiplier (×12) in 130 nm BiCMOS," manuscript submission in preparation to *IEEE Radio and Wireless Symposium (RWS 2022)*.

[13] **Y. Zhang**, W.Liang, C. Esposito, X. Jin, P. Sakalas and M. Schröter, "10 mW 190 GHz Low-Power Down-Conversion Mixer with -2 to 7 dB Tunable Conversion Gain in 130 nm SiGe BiCMOS," manuscript submission in preparation to *IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)*.

[14] **Y. Zhang**, W.Liang, C. Esposito, X. Jin, P. Sakalas and M. Schröter, "162–202 GHz Broadband (×12) Multiplier Chain with 22 dB Conversion Gain in 130 nm SiGe BiCMOS," manuscript in preparation.

[15] **Y. Zhang**, W.Liang, X. Jin, P. Sakalas and M. Schröter, "72-108 GHz SiGe Low-Power Tunable Amplifier with 10-23 dB Gain and 3.8-21 mW DC power," manuscript in preparation.

[16] **Y. Zhang**, W.Liang, X. Jin, P. Sakalas and M. Schröter, "85-195 GHz ultra-Broadband Amplifier with 20 dB Gain in 130 nm SiGe BiCMOS," manuscript in preparation.