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Erstveröffentlichung in / First published in:

49th European Solid-State Device Research Conference (ESSDERC). Cracow, 23.-26.09.2019. IEEE, S. 118–121. ISBN 978-1-7281-1539-9

DOI: https://doi.org/10.1109/ESSDERC.2019.8901735

Final edited form was published in "49th European Solid-State Device Research Conference (ESSDERC). Cracow, 2019". S. 118–121.
ISBN 978-1-7281-1539-9
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Ultra-dense co-integration of FeFETs and CMOS logic enabling very-fine grained Logic-in-Memory

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***Abstract*— Ferroelectric field-effect transistors (FeFET) based on hafnium oxide offer great opportunities for Logic-in-Memory applications, due to their natural ability to combine logic (transistor) and memory (ferroelectric material), their low-power operation, and CMOS compatible integration. Besides aggressive scaling, dense integration of FeFETs is necessary to make electronic circuits more area-efficient. This paper investigates the impact of ultra-dense co-integration of a FeFET and an n-type selector FET, sharing the same active area, arranged in a 2TNOR memory array. The examined FeFETs exhibit a very similar switching behavior as FeFETs arranged in a standard AND-type array, indicating that the ultra-dense co-integration does not degrade the FeFET performance, and thus, paves the path to a very fine-grained, ultra-dense Logic-in-Memory implementation. Based on this densely integrated 2TNOR array we propose a very compact design of a 4-to-1 multiplexer with a build-in look-up table, thus directly merging logic and memory.**

Keywords*— *active area sharing, ferroelectric FET (FeFET), hafnium oxide, look-up table (LUT), Logic-in-Memory (LiM), multiplexer (MUX), ultra-dense integration

I. Introduction

Ferroelectric field-effect transistors (FeFETs) utilizing ferroelectric hafnium oxide (HfO_2) instead of conventional gate dielectric materials do not only exhibit nonvolatile behavior, they are likewise scalable and can be integrated close-by with conventional CMOS devices [1]. Beyond being a promising candidate for embedded nonvolatile memory [2], several novel applications have been proposed recently. Besides the memory functionality of the ferroelectric material, these concepts exploit the logic functionality of the underlying transistor. Proposals include neuromorphic applications (synapses [3,4], artificial neurons [5,6]), Logic-in-Memory (LiM) devices [7-9], random number generators [10], ferroelectric oscillators [11], content addressable memories [12], and look-up tables (LUTs) [13,14]. To accomplish a very fine-grained combination of logic and memory devices, a very dense integration of the aforementioned elements is required. Despite aggressively scaling the nonvolatile devices [15], other approaches, like 3D stacking [16], were pursued in order to increase integration density.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 780302.
This work is funded by the German Bundesministerium für Wirtschaft (BMWI) and by the State of Saxony in the frame of the "Important Project of Common European Interest (IPCEI)."

In this paper, we investigate the impact of an ultra-dense co-integration of an n-type FeFET and a serially connected n-type FET (selector device) within a 2TNOR memory array (Fig 1a). In this structure, a nonvolatile FeFET and a selector n-FET share the same active area. In addition, we explored a FeFET-only AND memory array that serves as comparison. Measurements reveal a very similar switching behavior for FeFETs in both arrays, indicating that the co-integration process does not degrade the performance of the FeFET, and thus guiding a new way to a very-fine grained co-integration of logic and memory transistors in direct spatial proximity. As a proof of concept, a 4-to-1 multiplexer (MUX) with integrated nonvolatile look-up table (LUT), capable of realizing the 16 two-input-one-output logic functions, is proposed. Transient logic measurements of the LUT multiplexer within the 2TNOR

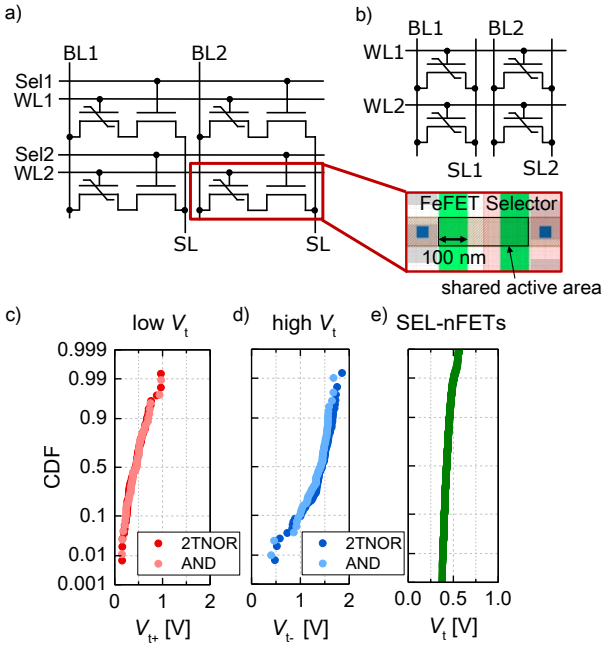

Fig. 1. Structure of the 2TNOR memory array with an n-type FeFET and selector n-FET (SEL-nFET) (a) and the FeFET-only AND memory array (b). The inset in (a) reveals the layout view of one 2TNOR array cell. BL, WL, SL and Sel denote the bit, word, source and select word lines. The distribution of threshold voltages (V_t) of the low V_t (c) and high V_t state (d) is depicted for FeFETs programmed/ erased at a write pulse of V_P = 4.5 V/ -3.5 V, while the pulse width was kept at t_P = 10 µs. (e) V_t distribution of the selector n-FETs (2TNOR array). The CDF is centered around 0.43 V.

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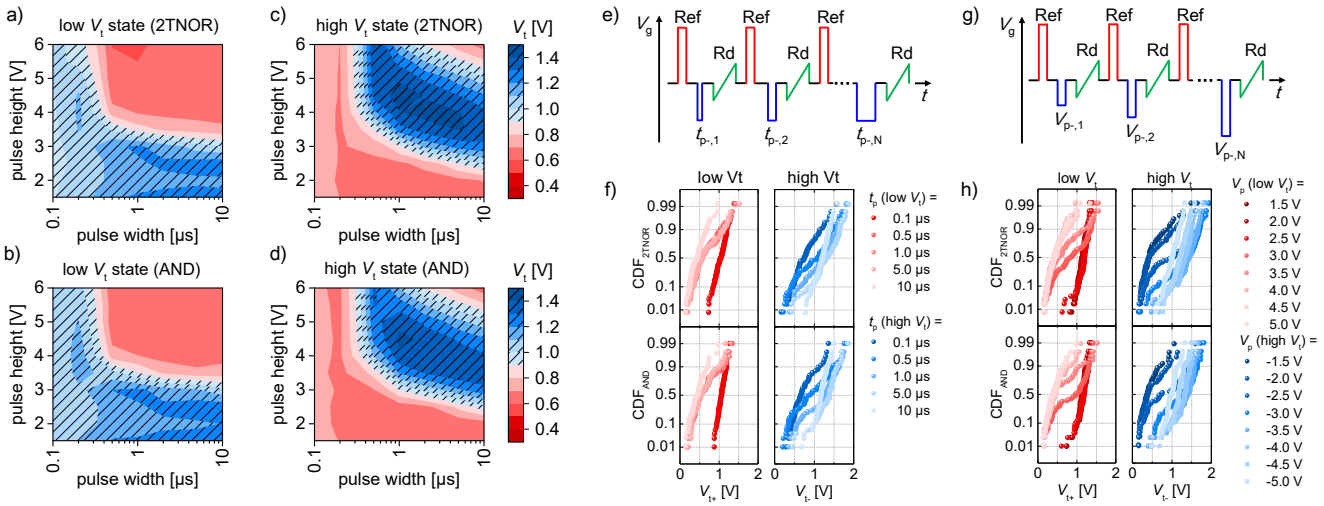

Fig. 2. Maps of the median value of the low V_t (a,b) and high V_t (c,d) as a function of the pulse width (t_p) and height (V_p) of the applied voltage pulse during write operation, for 2TNOR (90 devices, in (a) and (c)) and for AND memory arrays (63 devices, in (b) and (d)). The pulse schemes for the variation of voltage pulse width (e) and pulse height (g) during write operation are shown for the example of the erased state. "Rd" denotes the readout phase. (f) and (h) illustrate the distribution of measured V_t at V_p = 4.5 V (low V_t state) and V_p = -3.5 V (high V_t state) with varied t_p, and at t_p = 10 µs with varied V_p, respectively. The switching dynamics with respect to t_p and V_p is nearly the same for FeFETs of both arrays.

memory array emphasize the potential of the densely integrated structure for possible LiM applications. Realistic SPICE simulations of the LUT/MUX structure not only reveal a low energy consumption of the structure during read and write in case no RC delays of the measurement setup are present, but also indicate a high readout frequency of 1 GHz.

II. Experimental Results

A. FeFET switching behavior

Measurements were performed on transistors within a 2TNOR memory array, one array cell embedding an n-type FeFET with serially connected n-type selector FET fabricated in a 28 nm high-k metal gate (HKMG) process flow, and an AND memory array of FeFETs fabricated in the same manner [2]. The 2TNOR (Fig. 1a) and AND memory arrays (Fig. 1b) comprised 90 and 63 FeFETs, respectively. The FeFETs feature 10nm thick Si:HfO_2 and a 1.2nm thick SiON interface layer. Channel width and length are both 100 nm (inset in Fig. 1a). Keithley 4225PMU pulsed measurement units (PMUs) applied a chosen voltage to the terminals of an array cell and measured the output currents. To write a state into a specific FeFET, a voltage pulse of height V_p and width t_p was applied to its gate at a selected word line (WL), while the other word lines were sufficiently inhibited to avoid unintentional write processes of neighboring FeFETs. During the write phase, bit line (BL) and source line (SL) remained grounded. Applying a negative voltage pulse at the gate sets the n-type FeFET into a high threshold voltage state, called erased state, while a positive pulse entails the FeFET to be in the low threshold voltage state, called programmed state. In accordance to the JEDEC constant current criterion [17] the threshold voltage (V_t) was extracted from the transfer curves (I_d-V_g curves), which were collected after each write pulse.

Fig. 1c and Fig. 1d show the cumulative distribution function (CDF) of the low V_t (programmed state) and high V_t state (erased state) of FeFETs in the 2TNOR and the AND memory array, which are obtained by programming/ erasing at V_P = 4.5V/ -3.5V for t_p = 10µs, respectively. While both V_t distributions are steep and clearly separated, they also contain a tail. This is attributed to the channel size (100nm x 100nm), as it was also shown in [15] that FeFETs of smaller dimensions tend to have a larger V_t variability. The median memory window – the voltage difference between high V_t and low V_t – is up to 0.94 V (2TNOR) and 0.88 V (AND). The V_t distribution of the n-type selector FETs (Fig. 1e) is centered on a median V_t of 0.43 V, indicating that voltages as low as 0.5 V are sufficient to operate the selector n-FET.

To map the FeFET switching behavior, V_p and t_p were varied from ± 1.5V to ± 6 V and from 0.1 µs to 10 µs, respectively. A reference voltage pulse of 5V/ -5V, applied to the gate of the FeFET for 10 µs, sets the FeFETs in a uniform reference state just before the write operation (erase/ program). For FeFETs in both array types (2TNOR and AND), the median threshold voltages indicate the formation of a memory window with a distinct voltage and time dependence of the polarization switching (low V_t state in Fig. 2a and 2b, high V_t state in Fig. 2c and 2d), as it was also observed for larger devices in [18]. Nonetheless, the threshold voltages of the high V_t state (Fig. 2c and 2d) decrease significantly with higher V_p and t_p. A process overlaying the effect of the ferroelectric polarization switching might be the injection of holes from the substrate into the gate stack, which effectively reduces the V_t by screening the ferroelectric polarization [19][20]. The corresponding cumulative distribution function of threshold voltages for a fixed voltage pulse height V_p = 4.5 V/-3.5V (Fig. 2f) or width t_p = 10 µs (Fig. 2h) confirms the trend of the median V_t values, with FeFETs embedded within the 2TNOR or AND array showing a very similar behavior. The slope of high and low V_t CDFs decreases during transition from low to high V_t or vice versa, revealing a nonuniform switching of different devices within the FeFET memory array. When the polarization reversal process of all FeFETs is completed, the slope increases again, indicating a more uniform distribution of threshold voltages of the FeFETs. Voltage pulse heights less than -3.5V

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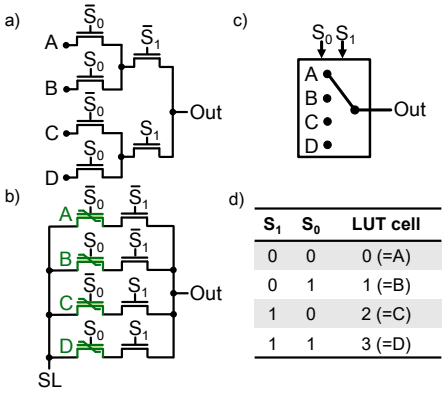
(t_p = 10 µs fixed) result in a steep CDF of threshold voltages (high V_t state) that exhibits a shift to smaller threshold voltages with increasing voltage pulse height. It indicates that all FeFETs are switched, but suffer from hole trapping, which screens the ferroelectric polarization and reduces the memory window.

B. Multiplexer with directly embedded look-up table

The specific structure of the 2TNOR memory array does not only raise interest for memory applications, but also for Logic-in-Memory and routing concepts. As shown in Fig. 3, this structure naturally comprises a look-up table – in this case a simple 4-bit LUT – whose values (A, B, C, D) are stored within the polarization state of the FeFETs, similar to the look-up table proposed in [14]. A logic "0" is stored by setting the FeFET into the high V_t state, while the low V_t state represents a logic "1". Thus, the logic output function of the LUT is defined by setting the polarization state of the four FeFETs. By applying the selector signals S_0 and S_1 to the gate of the FeFETs and selector FETs, respectively, a 4-to-1 multiplexer structure (MUX) for the aforementioned LUT is built. As proposed in our previous work [7], the FeFET operates as an AND gate between the applied input signal S_0 and its internal polarization state (A, B, C, or D). Different from other volatile [21] and nonvolatile [14][22] 4-to-1 MUX implementations for LUTs (Fig. 3a), the proposed 4-bit LUT is directly merged with the MUX (Fig. 3b and 3c, truth table in 3d). Thus, the proposed structure saves at least the first selection stage of the MUX, which due to the FeFET's CMOS compatibility will result in a significant area advantage for larger LUTs. Moreover, the values of the LUT are stored in a nonvolatile manner.

In our measurements, S_i = 0 corresponds to a voltage of V_{si} = 0 V, applied to the gate of the FeFET and selector FET. In case of S_i = 1, the voltage V_{si} was fixed at 0.9V (= V_{dd}), where the high and the low V_t state of the FeFETs can be clearly distinguished (vertical line in Fig. 4a). The FeFETs were erased or programmed by 10µs wide voltage pulses with heights of -3.5V or 4.5V, respectively. FeFETs with slightly different



S_1	S_0	LUT cell
0	0	0 (=A)
0	1	1 (=B)
1	0	2 (=C)
1	1	3 (=D)

Fig. 3. (a) Conventional multiplexer structure. The selector signals S_0 and S_1 specify which input is passed to the output terminal. (b) Proposed MUX/LUT structure with selector signals as before. A nonvolatile look-up table consisting of four n-FeFETs, each storing one binary "input" state (A, B, C, or D), is directly integrated into the first stage of selector FETs. (c) Schematic of the operation principle of the MUX/LUT structure. (d) Corresponding to the applied S_0 and S_1, one cell of the LUT is selected and read out, corresponding to an output of A (cell 0), B (cell 1), C (cell 2) or D (cell 3).

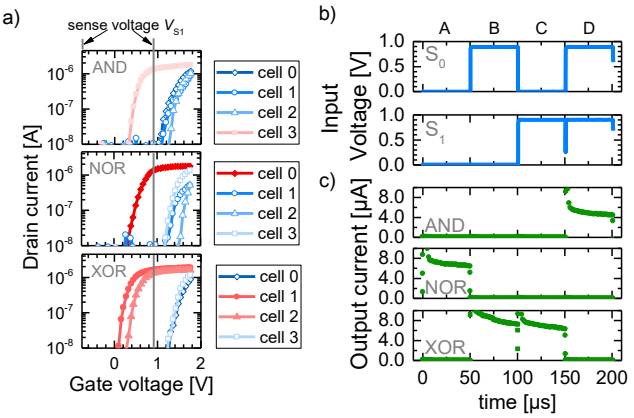


Fig. 4. (a) shows the I_d-V_g curves of four n-FeFETs, that constitute the storage cells of the proposed LUT, in case of AND, NOR, and XOR output functions, respectively. (b) By applying the selector signals S_0 and S_1 to the MUX, represented by the input voltage V_{sj}, one specific storage cell is read out. (c) The value, which is stored in the selected cell, is reflected in the measured output drain current I_d. The output functions AND, NOR, and XOR are chosen as examples of the 16 possible 2-input 1-output logic functions.

threshold voltages (variations up to 0.2V) emulate a realistic situation. In the transient measurement, this variation in threshold voltages results in a difference of output current levels up to a factor of two, especially for the low V_t state (filled symbols in Fig. 4a). Compared to the on/off ratio of at least two orders of magnitude between the low V_t and the high V_t state of the FeFET, this variation is negligible. Note that due to the current compliance of the used PMUs, values less than 10^{-8} A are overlaid by measurement noise. By using a sense amplifier or dynamic (clocked) logic circuit, a voltage can be outputted. From the 16 two-input-one-output logic functions a 4-bit LUT is able to implement, AND, NOR, and XOR were chosen, since these functions exhibit the low and high V_t state of every LUT storage cell at least once (input selector signals S_0 and S_1 in Fig. 4b, output currents in Fig. 4c). Compared to CMOS or MTJ implementations of 4-bit LUTs [14] [21] [22], the number of routing transistors is reduced by at least two devices since the FeFET performs not only the storage task of the LUT but also acts as a routing transistor with respect to passing the stored LUT values to the output terminal. In the case of cells 0 and 1 (stored values: A/ B) as well as cells 3 and 4 (stored values C/ D) sharing the same selector FET, the number of routing transistors is even reduced by four devices (40 %).

To further confirm the experimental results, SPICE simulations were carried out. The behavioral FeFET model comprises a ferroelectric capacitor (FeCap), based on the time-dependent Preisach model [23][24], which is connected to the gate of a high-V_t n-FET, originating from a 28nm process design kit (PDK). The supply voltage was V_{dd} = 0.9 V. Here, the full potential of the FeFET is exploited, as setup RC delays present in measurements are avoided. Thus, time delays are solely based on FeFET switching and internal circuit delays. Moreover, the full drain current span of the FeFET ranges over six orders of magnitude from 10^{-12} A to 10^{-6} A. To model the output voltage, a clocked pull-up transistor is placed between the output node ("Out" in Fig. 3b) and V_{dd}. LUT cells 0, 1, 2, and 3 are written to represent the AND, NOR, and XOR logic with respect to the output current as used in the transient measurement. Due to the

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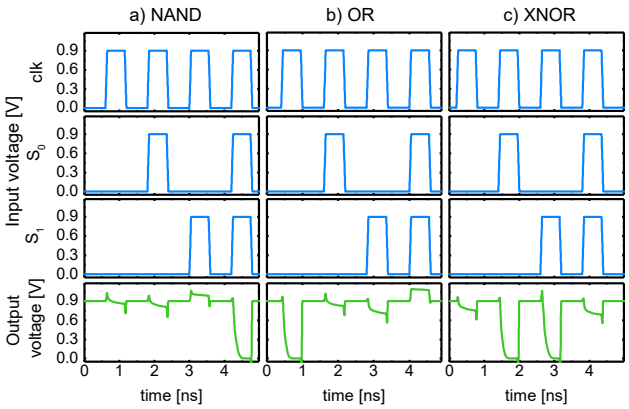

Fig. 5. Simulation of the proposed MUX/ LUT structure. A dynamic readout scheme with a clock frequency around 1 GHz was used. S_0 and S_1 are the selector signals of the multiplexer. "clk" denotes the clock. As in the measurements, AND, NOR, and XOR were chosen for the output current, which transform into NAND (a), OR (b), and XNOR (c) regarding the output voltage.

pull-up device, the output voltage results in a NAND (Fig. 5a), OR (Fig. 5b), and XNOR function (Fig. 5c). In the simulation, the frequency of the inputs during the readout was as high as 1 GHz. The largest dynamic energy consumption is as low as 0.271 fJ for the readout of one LUT cell and 1.36 fJ for the writing of the cells.

III. Conclusion

In this paper, we highlighted that FeFETs are suitable to share the same active area with serially connected FETs within a 2TNOR memory array framework. The impact of the co-integration onto the switching behavior of the FeFETs is low. The median threshold voltages and the cumulative distribution of the threshold voltages with and without varied write voltage pulse height and width are very comparable to FeFETs of the same specifications arranged in an AND memory array without any selector FETs. The feasibility of the ultra-dense co-integration for very fine-grained Logic-in-Memory applications was confirmed by demonstrating a new FeFET-based 4-to-1 multiplexer concept with embedded, nonvolatile look-up table, wherein all 16 Boolean 2in-1out functions are realizable. Dense co-integration and the shown functional merging of logic (multiplexer) and memory (LUT) promise significant area and delay time savings. Simulations verified the functionality of the new concept with readout frequencies as high as 1 GHz.

Acknowledgment

The authors would like to thank GlobalFoundries Dresden, Germany, for experimental samples and support.

References

[1] J. Müller *et al.*, "Ferroelectric hafnium oxide: A CMOS-compatible and highly scalable approach to future ferroelectric memories," in *IEDM Tech. Dig.*, pp. 10.8.1-10.8.4, Dec. 2013.

[2] M. Trentzsch *et al.*, "A 28nm HKMG super low power embedded NVM technology based on ferroelectric FETs," in *IEDM Tech. Dig.*, pp. 11.5.1-11.5.4, Dec. 2016.

[3] H. Mulaosmanovic *et al.*, "Novel ferroelectric FET based synapse for neuromorphic systems," in *Proc. Symposium on VLSI Technology (VLSIT)*, Jun. 2017, pp. T176-T177.

[4] Y. Nishitani, Y. Kaneko, M. Ueda, T. Morie, and E. Fujii, "Three-terminal ferroelectric synapse device with concurrent learning function for artificial neural networks," *J. Appl. Phys.*, vol. 111, pp. 124108-1 – 6, Jun. 2012.

[5] H. Mulaosmanovic, E. Chicca, M. Bertele, T. Mikolajick, and S. Slesazeck, "Mimicking biological neurons with a nanoscale ferroelectric transistor," *Nanoscale*, vol. 10, pp. 21755-21763, Nov. 2018.

[6] H. Ishiwara, "Proposal of Adaptive-Learning Neuron Circuits with Ferroelectric Analog-Memory Weights", *Jap. J. Appl. Phys.*, vol. 32, part 1, no.1B, pp. 442-446, 1993.

[7] E. T. Breyer, H. Mulaosmanovic, T. Mikolajick, S. Slesazeck, "Reconfigurable NAND/NOR logic gates in 28 nm HKMG and 22 nm FD-SOI FeFET technology," in *IEDM Tech. Dig.*, pp. 28.5.1-28.5.4, Dec. 2017.

[8] E. T. Breyer, H. Mulaosmanovic, S. Slesazeck, T. Mikolajick, "Demonstration of versatile nonvolatile logic gates in 28nm HKMG FeFET technology," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1-5.

[9] X. Yin *et al.*, "Exploiting ferroelectric FETs for low-power non-volatile logic-in-memory circuits," in *Proceedings of the 35th International Conference on Computer-Aided Design (ICCAD '16)*, Article No. 121, Nov. 2016, pp. 121:1 – 121:8.

[10] H. Mulaosmanovic, T. Mikolajick, and S. Slesazeck, "Random Number Generation Based on Ferroelectric Switching," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 135-138, Jan. 2018.

[11] Z. Wang, S. Khandelwal, and A. I. Khan, "Ferroelectric oscillators and their coupled networks," *IEEE Electron Device Lett.*, vol. 38, no. 11, pp. 1614-1617, Nov. 2017.

[12] T. Hanyu, H. Kimura and M. Kameyama, "Multiple-valued content-addressable memory using metal-ferroelectric-semiconductor FETs," in *Proceedings of the 29th IEEE International Symposium on Multiple-Valued Logic,* May 1999, pp. 30-35.

[13] K. Li, Y. Xiong, M. Tang, Y. Qin, Z. Li and Y. Zhou, "Design and implementation of fefet-based lookup table," in *12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Oct. 2014, pp. 1-3.

[14] X. Chen, M. Niemier and X. S. Hu, "Nonvolatile Lookup Table Design Based on Ferroelectric Field-Effect Transistors," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1-5.

[15] S. Dünkel *et al.*, "A FeFET based super-low-power ultra-fast embedded NVM technology for 22 nm FDSOI and beyond," in *IEDM Tech. Dig.*, pp. 19.7.1–19.7.4, Dec. 2017.

[16] J. Van Houdt, "3D Memories and Ferroelectrics,", in *2017 IEEE International Memory Workshop (IMW)*, May 2017, pp. 1-3.

[17] JEDEC-Standard, JESD28-A, "Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation under DC Stress," Dec. 2001.

[18] J. Müller, T. S. Böscke, U. Schröder, R. Hoffmann, T. Mikolajick, L. Frey, "Nanosecond Polarization Switching and Long Retention in a Novel MFIS-FET Based on Feroelectric HfO_2," *IEEE Electron Device Lett.,* vol. 33, no. 2, pp. 185-187, Feb. 2012.

[19] W.-T. Lu *et al.*, "The Characteristics of hole trapping in HfO_2/ SiO_2 gate dielectrics with TiN gate electrode," *Appl. Phys. Lett.*, vol. 85, no. 16, pp. 3525-3527, Oct. 2014.

[20] E. Yurchuk *et al.*, "Charge-Trapping Phenomena in HfO_2-Based FeFET-type Nonvolatile Memories," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3501-3507, Sep. 2016.

[21] R. J. Baker, "CMOS: Circuit Design, Layout, and Simulation", 3rd edition, Hoboken, NJ, USA: John Wiley & Sons, 2011, p. 381.

[22] J. Yang *et al.*, "Exploiting Spin-Orbit Torque Devices as Reconfigurable Logic for Circuit Obfuscation," *IEEE Trans. Comput-Aided Des. Integr. Circuits Syst.*, vol. 38, no. 1, pp. 57-69, Jan. 2019.

[23] B. Jiang, P. Zurcher, R. E. Jones, S. J. Gillespie, and J. C. Lee, "Computationally Efficient Ferroelectric Capacitor Model for Circuit Simulation," in *Proc. Symposium on VLSI Technology (VLSIT)*, Jun. 1997, pp. 141-142.

[24] K. Dragosits, R. Hagenbeck, and S. Selberherr, "Transient Simulation of Ferroelectric Hysteresis," in *Technical Proceedings of the 2000 International Conference on Modeling and Simulation of Microsystems*, Mar. 2000, pp. 433-436.