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Eliminating Charge Sharing in Clocked Logic Gates on the Device Level Employing Transistors with Multiple Independent Inputs

Jens Trommer *Member IEEE*, Maik Simon, Stefan Slesazeck, Walter M. Weber *Member IEEE* and Thomas Mikolajick *Senior Member IEEE*

***Abstract* — Charge sharing poses a fundamental problem in the design of dynamic logic gates, which is nearly as old as digital circuit design itself. Although, many solutions are known, up to now most of them add additional complexity to a given system and require careful optimization of device sizes. Here we propose a simple CMOS-technology compatible transistor level solution to the charge sharing problem, employing a new class of field effect transistors with multiple independent gates (MIGFETs). Based on mixed-mode simulations in a coordinated device-circuit co-design framework, we show that their underlying device physics provides an inherent suppression of the charge sharing effect. Exemplary circuit layouts as well as discussion on the switching performance are given.**

Index Terms* — *dynamic logic gates; charge sharing, domino logic; reconfigurable transistor; Schottky transistors; multi-gate

I. Introduction

DYNAMIC logic is a design methodology widely used in modern microprocessors, due to their benefits in terms of area, performance and power consumption over other logic families, such as static logic, pseudo-NMOS logic and complementary pass transistor logic (CPL) [1]. In order to build any N-input function only $N + 2$ transistors are needed in dynamic logic, while $2 \cdot N$ transistors are needed in complementary static CMOS design [2]. While both static and dynamic logic can eliminate static power dissipation by design, dynamic logic gates can be up to twice as fast as their static counterparts. This is especially important for logic functions with many inputs, such as 4-NAND or 4-NOR logic gates.

On the other hand, dynamic logic gates suffer from a number of reliability problems and circuit design constraints [3], [4]. First of all, dynamic gates facilitate a two-step operation scheme, which is controlled by an external clock. During a *pre-charge* phase, the output of a gate is temporarily charged. Then, during *evaluation* the capacitance is discharged depending on the conditions of logic inputs of the gate. As the evaluation step is non-reversible dynamic gates require monotonically rising inputs during evaluation. Contrariwise, dynamic gates produce monotonically falling outputs. As a result, it is illegal for one dynamic gate to drive another one. This typically inflicts issues with clock synchronization and timing. Further stability problems can be caused if the volatile charge is lost during the evaluation process either by leakage across the channel or through the reverse-biased diode of the diffusion area.

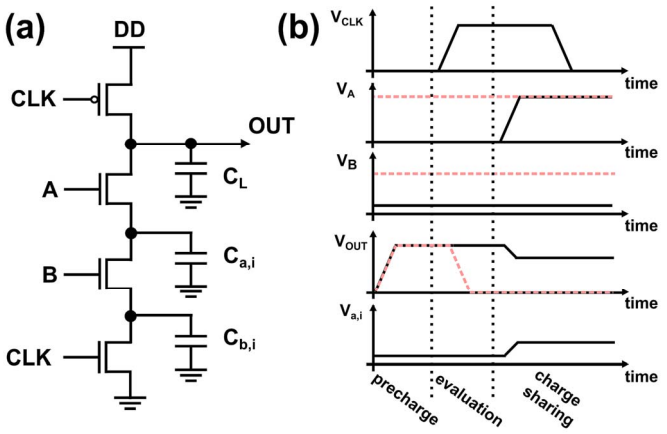

Figure 1. The charge sharing problem in a dynamic logic gate. (a) Circuit shematic of a footed dynamic 2-NAND logic gate. (b) Shematic waveforms during operation. While the clock singal (CLK) is 0, the output node C_L is pre-charged. During, evaluation (V_{CLK}=1) the output node is discharged, if A and B are at 1 (dashed red lines). The output node will stay charged, if at least A or B is at 0 and the pull-down-network is off (solid lines). If signal A is switched during evaluation charge will be redistributed from the output node C_L to the internal node $C_{a,i}$. This charge sharing effect can disturb the readout of the logic gate.

Another very specific issue to dynamic gates is the so-called *charge sharing problem*. This is a signal integrity phenomena where the charge stored at the output node is redistributed during the pre-charge phase towards the internal junction capacitances of the network which is in the evaluation phase [5]. Similar to charge leakage, charge sharing can degrade the output voltage level and thus cause an erroneous output value. As device geometries are scaled down, leakage currents and charge sharing become increasingly critical problems, especially in full-custom circuit designs [6]. As a result the signal integrity of the circuit is at risk, especially when the design does not account for possible charge sharing.

In this paper we will demonstrate how a new class of transistors, the so called multiple independent gate field effect transistors

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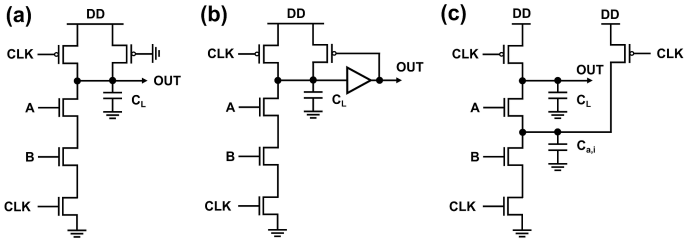

Figure 2. Known circuit level solutions for the charge sharing problem. (a) Static bleeder circuit at the output, (b) week keeper circuit, (c) additional pre-charge of the internal node $C_{a,i}$.

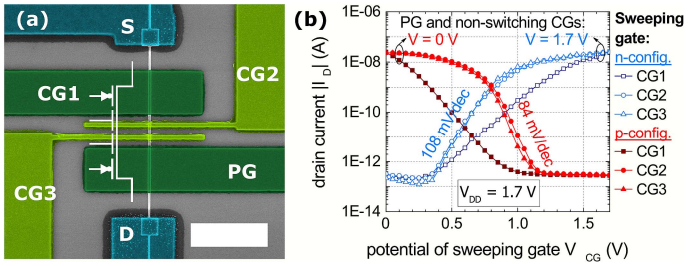

Figure 3. Multiple independent gate field effect transistor (MIGFET). (a) Colored top view SEM image of a fabricated and measured device based on a FD-SOI channel. The lables mark source (S), drain (D), control gate one to three (CG1, CG2, CG3) and program gate (PG) contacts. Scale bar is 2 µm. Used circuit symbol is given. (b) All transfer characteristics for one measured device. Depending on the applied voltage at the program gate, the transistor exhibits either p-type configuration (red, V_{PG} = 0 V) or n-type configuration (blue, V_{PG} = 1.7 V). A steeper subtreshold slope is achieved if the transistor is operated using the inner gates CG2 or CG3 (light color) as compared to CG1 (dark color). All transfer characteristics achieve an identical current in the on-state.

(MIGFETs), can be employed to eliminate the charge sharing problem without the need for any additional circuitry. This paper thereby is organized as follows. In section II the charge sharing problem as well as some known circuit-level solutions will be introduced in detail. In section III multiple independent gate field effect transistors (MIGFETs) based on gated nanoscale Schottky junctions are reviewed briefly. Demonstrator devices utilizing fully-depleted silicon-on-insulator (FD-SOI) channels are discussed. In section IV, it will be explained how the underlying operation principle of these devices can be used to eliminate the charge sharing issue on the device level. Possible performance enhancements will be discussed on section V. A conclusion is drawn in section VI.

II. The Charge Sharing Problem

Figure 1 illustrates the operation principle of a simple dynamic 2-NAND logic gate including the charge sharing problem. During the pre-charge phase, the clock-controlled pull up network (PUN) is opened and the output node C_L is charged. During the evaluation phase, C_L will either be discharged, if the inputs A and B are both at high level or it will retain its value if one of the input signals is low. The charge sharing effect only becomes relevant, when the last stage of the pull down network (PDN) alters its state during the evaluation phase. In this case, charge is redistributed from the output to the internal node $C_{a,i}$. The effect becomes severe, if the induced voltage drop reaches below the threshold voltage of the p-type transistor. As a rule of thumb, the capacitance of the internal node $C_{a,i}$ has to be smaller than 1/5 of output capacitance C_L to be uncritical. However, if the number of series FETs in the PDN increases, i.e. the number of inputs increases, charge sharing becomes a more severe problem, because the number of internal capacitances that potentially can share charge increases. Therefore, charge sharing is one of the factors that limit the stack height of dynamic logic gates.

As dynamic logic is a major part of modern microprocessors, there are several known solutions that can be used to minimize charge sharing with the help of additional circuitry as shown in Figure 2. Using so called keeper or bleeder circuits [7], [8], the charge lost at the output is restored via a weak transistor directly connected to the supply line. Careful sizing of those devices is needed so that they do not override the PDN in case of a switching event. Another option is to pre-charge the internal node $C_{a,i}$ so that it will have the same potential as the output node [4]. Unfortunately, all these solutions not only require additional transistors, but also add an additional source for power dissipation to the system. Thus, a solution without the need for additional circuitry would be desirable. We will show that such a solution can be provided by MIGFETs.

III. Schottky Barrier Based Transistors with Multiple Independent Gates

MIGFETs are a relatively novel class of emerging devices that are based on gated low-dimensional semiconductor Schottky junctions. They are extensions of the more-well known polarity-controllable or reconfigurable field effect transistors (RFETs) and thus are able to offer multiple operation states [9]–[11]. Exploiting the plurality of gate electrodes REFTs merge unipolar p- and n-type conduction into a single device. The desired device operation type is programmed by an electric signal. Different to conventional complementary metal oxide semiconductor circuits, no doping is generally required. All materials and process steps needed are compatible with standard CMOS fabrication. It has been demonstrated that the programmable nature of those devices can be exploited on the circuit level to build complex logic gates with a reduced amount of transistors [12]–[14].

However, in order to deal with the charge sharing problem, we will exploit a completely different feature of those transistors. It has been shown, both by simulations [15] and measurements [10], [11] that MIGFETs support an internal wired-AND functionality, i.e. a single transistor can be described as an equivalent circuit of several MOSFETs in series. The transistors thereby will only pass a current, if all gates are in the on-state at the same time. A fabricated and measured nanowire device demonstrating this functionality is shown in Figure 3. The channel was formed on a FD-SOI substrate. After gate oxide formation by rapid thermal annealing, sharp $NiSi_2$ source and drain contacts were formed. The program gate (PG), which is aligned atop of the drain sided Schottky junction, thereby blocks the undesired carrier type. In addition three independent control gates (CG) are used for operation. Although the devices exhibit a reduced subthreshold slope and a lower V_{TH} when steered at a control gate aligned in the middle of the channel (CG2, CG3), the on-current is the same for all three inputs as demonstrated in the measured subthreshold characteristics (Figure 3b). More detailed insights into the device operation principle are given in Ref. [10].

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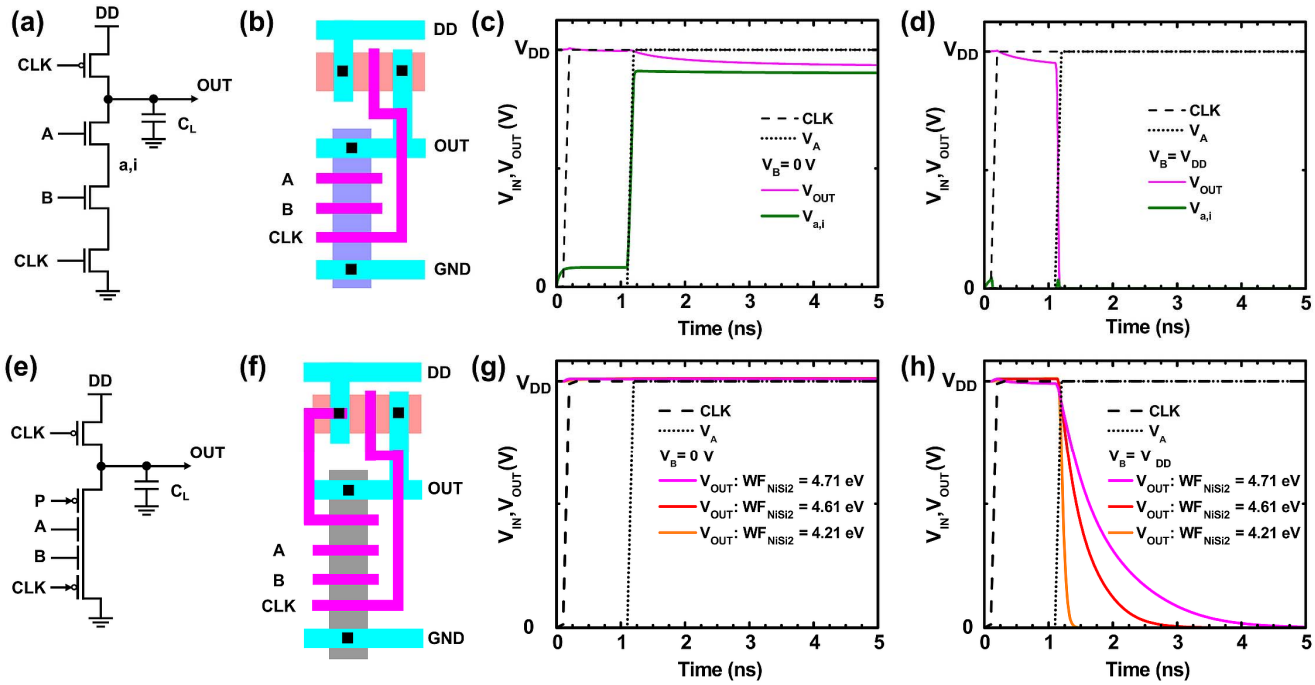

Figure 4. Circuit shematics, layouts and transient simulations for dynamic 2-NAND gate variants. (a) simple footed CMOS realization, (b) corresponding circuit layout, (c) circuit behavior in the charge sharing case (d) circuit behavior with an open pull down network. (e) Realization using a single MIGFET with four independent gates, (f) corresponding circuit layout, (g) circuit behavior in the charge sharing case and (h) circuit behavior with an open pull down network. Increased switching speed is achieved with a reduced work function of the $NiSi_2$ contacts.

Circuit analysis in this work was carried out by mixed-mode TCAD simulations using a similar MIGFET layout with scaled geometries that can be patterned in a 25 nm technology (128 nm channel lengths, 4 individual gates of 24 nm lengths each, 6 nm silicon channel diameter, 5.6 nm HfO_2 dielectric, corresponding to 1 nm EOT). TaN electrodes with 4.62 eV work function are used. Typically a $NiSi_2$ Schottky contact having a work function of 4.71 eV near midgap band alignment is used to realize symmetric p- and n-functionality [16]. More details about the simulation setup and considered transport models can be found in Ref. [13], [15].

IV. Elimination of Charge Sharing on the Device Level

Circuit schematics, layouts and mixed-mode simulation results of two dynamic 2-NAND gate versions are shown in Figure 4. First, a CMOS reference design in FDSOI technology is analyzed. In accordance with the theory explained in section II, the drain sided junction region is charged during the charge sharing event. As a result, the output capacitance C_L is partially discharged and the electrical potential of the intermediate node a,i and the output equalize (Fig. 4(c)). This effect can be prevented if the PDN is replaced by a single MIGFET with four individual gates. Here, both inputs A and B are connected to the channel gates CG2 and CG3 while the clock signal is connected to the CG1 above the Schottky junction. The program gate is used to set the polarity of the MIGFET to an n-type operation and to block parasitic charge leakage via the drain sided Schottky barrier. In addition, the unique multi-gate device layout inherently suppresses charge sharing. As opposed to a normal CMOS design, the ungated area between each of the gates is a part of the channel. Consequently, in MIGFETs there is no internal junction depletion region to be charged. Both

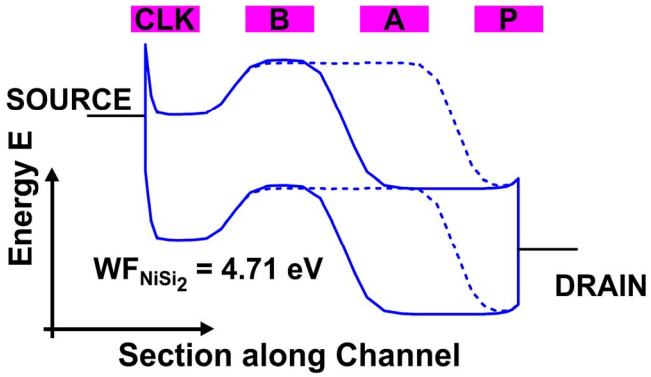

Figure 5. Band diagram of a the n-programmed MIGFET with four gates in Figure 4(e) before (dash lines) and after (solid lines) the charge sharing event. No potential well for charge storage is present within band structure between both control gates in the middle of the channel. Electron current is blocked by the potential barrier of CG2 (input B).

control gates CG2 and CG3 exhibit a strong coupling to the ungated area between them. As the device operation is purely diffusion driven, no charge is stored within the channel before the charge sharing event. The strong local electric field induced by the blocking signal B counteracts any attempt of charge redistribution from the source side (Figure 5). As a result, there is negligible charge loss at the output C_L during a potential charge sharing event, as shown in Figure 4(g).

Comparing the layouts of both CMOS and MIGFET realizations it is obvious that the MIGFET version requires slightly more area, to accommodate the additional gate needed to set the polarity. However, this gate can be conveniently hard-wired to the supply lines as shown in Figure 4(f). Overall, the space needed for the MIGFET solution will therefore be lower than for conventional circuit based solutions requiring substantial overhead as discussed earlier in Fig. 2.

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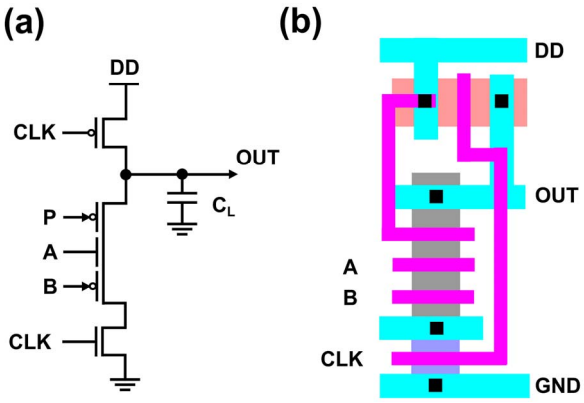

Figure 6. (a) Circuit shematic and (b) layout for a dynamic 2-NAND gate with mixed CMOS-MIGFET pull down network design for improved performance.

V. Discussion on Performance Enhancements

The main application for dynamic logic gates are high performance circuits. Thus, it is important to also consider the switching speed within the operation case in order to evaluate the applicability of the new device level approach. Comparing the magenta lines in Figures 4(d) and (g) it is evident, that the CMOS circuit responds much faster in the operation case. This is a result of a relatively high Schottky barrier of 0.64 eV present at the $NiSi_2$ to the intrinsic Si interface of the MIGFET. Typically, such a midgap barrier is used to optimize the devices for reconfigurable operation. This means in effect, that n-type program and p-type program are equally strong [16]. However, in the present case, where the MIGFETs are used to suppress the charge sharing effect, the feature of reconfigurability is not needed. In turn, it is possible to increase the performance of the n-type program at expense of the p-type performance. The most straightforward way of doing this is by lowering the Schottky barrier height of the drain contact, either through work function engineering of the silicide or through doping at the contact region. For instance, Zhang et al. and recently Mauersberger et al. have shown that a segregation of dopants near the Schottky barrier interface can be used to reduce the barrier and increase the output current [17], [18]. Corresponding mixed-mode simulations are shown in Figure 4(h). For a $NiSi_2$ work function exemplary lowered to 4.2 eV, the resulting fall time is in the range of the CMOS reference design. Simultaneously, charge sharing is still well suppressed. Beyond this, it has been demonstrated that germanium and silicon-germanium channel materials further reduce V_{TH} and increase the on-currents of the shown multi/gate transistors [19]. Another very straightforward improvement is to connect the clock signal not to a gate aligned on-top of the Schottky barrier, but to one of the channel gates. Although all three CGs deliver the same maximum current, a lower V_{TH} and higher subthreshold slope is achieved with the inner gates. Ultimately, even a mixed PDN is possible, where the clock is steered by a conventional n-type MOSFET, while the charge sharing effect is prevented by a MIGFET (Fig. 6).

VI. Conclusion

To summarize, we have shown that field effect transistors with multiple independent gates (MIGFETs) provide a simple and CMOS compatible yet powerful solution to mitigate the charge sharing problem in clocked logic gates. The unique operation principle of those devices enables to eliminate charge sharing without the need for additional circuitry. It allows for larger stacking height of the PDN and reduced charge leakage. Exemplary circuit layouts and mixed-mode simulations of a dynamic 2-NAND gate have been discussed. Work function tuning has been shown among other options to be an efficient method for increasing the switching performance.

References

[1] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.

[2] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low-power CMOS digital design," *IEEE J. Solid-State Circuits*, vol. 27, 4, 1992.

[3] R. H. Krambeck, C. M. Lee, and H.-S. Law, "High-speed compact circuits with CMOS," *IEEE J. Solid-State Circuits*, vol. 17, no. 3, 1982.

[4] P. Srivastava, A. Pua, and L. Welch, "Issues in the design of domino logic circuits," in *Proceedings of the 8th Great Lakes Symposium on VLSI (Cat. No.98TB100222)*, 1998, pp. 108–112.

[5] L. Lavagno, L. Scheffer, G. Martin, L. Scheffer, and G. Martin, *EDA for IC Implementation, Circuit Design, and Process Technology*. CRC Press, 2006.

[6] R. I. Bahar, H.-Y. Song, K. Nepal, and J. Grodstein, "Symbolic failure analysis of complex CMOS circuits due to excessive leakage current and charge sharing," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 24, no. 4, pp. 502–515, Apr. 2005.

[7] V. Kursun and E. G. Friedman, "Domino logic with variable threshold voltage keeper," *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 11, no. 6, pp. 1080–1093, Dec. 2003.

[8] V. G. Oklobdzija and R. K. Montoye, "Design-performance trade-offs in CMOS-domino logic," *IEEE J. Solid-State Circuits*, vol. 21, no. 2, pp. 304–306, Apr. 1986.

[9] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, and W. M. Weber, "Reconfigurable Silicon Nanowire Transistors," *Nano Lett.*, vol. 12, (1) 2012.

[10] M. Simon *et al.*, "A wired-AND transistor: Polarity controllable FET with multiple inputs," in *2018 76th Device Research Conference (DRC)*, 2018, pp. 1–2.

[11] J. Zhang, M. De Marchi, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici, and G. De Micheli, "Polarity-Controllable Silicon Nanowire Transistors With Dual Threshold Voltages," *IEEE Trans. Electron Devices*, vol. 61, no. (11), pp. 3654–3660, 2014.

[12] M. De Marchi *et al.*, "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, p. 8.4.1-8.4.4.

[13] J. Trommer, A. Heinzig, T. Baldauf, S. Slesazeck, T. Mikolajick, and W. M. Weber, "Functionality-Enhanced Logic Gate Design Enabled by Symmetrical Reconfigurable Silicon Nanowire Transistors," *IEEE Trans. Nanotechnol.*, vol. 14, no. 4, pp. 689–698, Jul. 2015.

[14] M. Raitza *et al.*, "Exploiting Transistor-Level Reconfiguration to Optimize Combinational Circuits," *Proc. Des. Autom. Test Eur.*, 2017.

[15] J. Trommer *et al.*, "Reconfigurable nanowire transistors with multiple independent gates for efficient and programmable combinational circuits," in *2016 Design, Automation Test in Europe Conference Exhibition (DATE)*, 2016, pp. 169–174.

[16] A. Heinzig, T. Mikolajick, J. Trommer, D. Grimm, and W. M. Weber, "Dually Active Silicon Nanowire Transistors and Circuits with Equal Electron and Hole Transport," *Nano Lett.*, vol. 13, no. 9, 2013.

[17] M. Zhang, J. Knoch, Q. T. Zhao, S. Lenk, U. Breuer, and S. Mantl, "Schottky barrier height modulation using dopant segregation in Schottky-barrier SOI-MOSFETs," in *Solid-State Device Research Conference, 2005. ESSDERC 2005. Proc of 35th*, 2005, pp. 457–460.

[18] T. Mauersberger, I. Ibrahim, A. Heinzig, T. Mikolajick, and W. M. Weber, "Electrical characterization and size effect of highly arsenic-doped silicon nanowires," *IEEE Conf. Proc. ULIS-EUROSOI* 2019.

[19] J. Trommer *et al.*, "Enabling Energy Efficiency and Polarity Control in Germanium Nanowire Transistors by Individually Gated Nanojunctions," *ACS Nano*, Jan. 2017.