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# Scaling Aspects of Nanowire Schottky Junction based Reconfigurable Field Effect Transistors

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***Abstract*—This contribution discusses scaling aspects of individually gated nanowire Schottky junctions which are essential parts of reconfigurable field effect transistors (RFETs). The applicability of the screening (or natural) length theory in relation to the carrier transport is discussed first. Various geometrical parameters of the device were investigated to find the optimal structure in terms of performance. For this purpose, electrostatic properties and the dynamic behavior of the RFET were studied. Finally the increase in performance due to an additional substitution of the silicon by germanium is analyzed.**

***Keywords: scaling, screening length, nanowire, Schottky junction, SBFET, reconfigurable logic, RFET, tunneling, simulation, TCAD***

## I. Introduction

Due to physical limits like tunneling between source and drain, field-effect transistors cannot be scaled down to arbitrary low channel lengths [1]. For performance enhancement beyond that limit, alternative approaches providing more functionality of highly scaled integrated circuits are under investigation [2]. Reconfigurable field effect transistors (RFETs) represent a basic element of such functionality-enhanced logic gate designs [3], [4], where the circuit function can be reconfigured at runtime. By adjusting an external input voltage, the same nanowire Schottky barrier based RFET is able to operate as n- or p-type transistor [5]. A detailed description of the functionality and how to use the device in circuits can be found in [5]-[7]. Important aspects are the enhancement of the RFET performance by elaborating an optimal structure and the demonstration of the compatibility to existing semiconductor technologies or those currently under development by investigating the scaling behavior. In this paper we first discuss the applicability of the screening (or natural) length theory to describe scaling aspects related to the geometry of nanowire RFETs. Shrinking the cross-section of the active area ensures an increase in device performance which is inter alia demonstrated by the power consumption of a ring oscillator (RO) in comparison to its resonant frequency.

The presented data are mainly based on TCAD simulations (SYNOPSYS, Sentaurus) previously calibrated by experimental data [8]. Drift-diffusion with modified local-density approximation was used to calculate the carrier transport and the quantum-mechanical confinement occurring at Si-$SiO_2$ interface near the gate contacts [9]. A nonlocal tunneling model based on a Wentzel-Kramers-Brillouin approximation for finite-elemente-methode simulations computed the injection of carriers at the Schottky barrier. Also charge carrier mobility degradation by high-field saturation and surface scattering were taken into account. As shown in previous studies, a symmetrical I-V behavior between n- and p-configuration from the same device could be achieved by the impact of mechanical stress on the injection at the junctions [8].

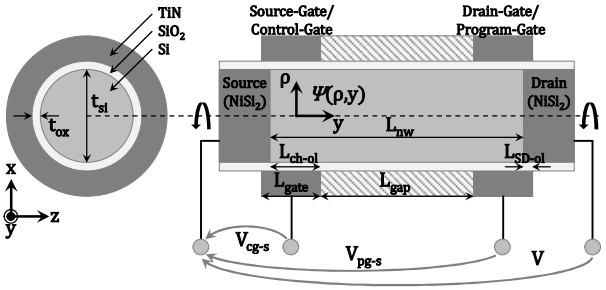


Figure 1. Schematic view of a cylindrical reconfigurable silicon nanowire RFET with two independent Schottky junctions at source and drain covered by surrounding gates.

## II. Scaling Aspects

The RFET structure of choice in this study is a cylindrical and lowly doped (Boron 1e15) or intrinsic semiconductor nanowire body with intruded metal silicide source/drain contacts that provide abrupt and flat Schottky junctions [10][11] for charge carrier injection as shown in Figure 1. In the simplest RFET implementation, each junction is controlled by an individual gate, labeled as control and program gate. Through the applied band bending n- and p-type behavior is programmed, see Figure 3a. The surround gate geometry is advantageous for the enhancement of the electrostatic impact of the gate potential on the junctions. Decisive for the electrostatic properties of the device are the longitudinal and the radial sizes, such as nanowire diameter $t_{si}$, gate oxide thickness $t_{ox}$ and the length of the gate electrodes $L_{gate}$. To relate the geometric properties on the potential distribution within the wire, the screening or natural length is a suitable indicator. Indeed it is in the focus of scaling theories of modern MOSFET geometries [12]. For the screening length to be applicable it must be determined in the region where electronic transport is bound to [13]. In the case of partially depleted (and inversion mode) devices like planar SOI-MOSFETs the screening length is thus derived at the

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surface of the active region. I.e. at the interface to the gate oxide. Differently, the screening length of fully depleted devices like nanowire MOSFETs with surround gate is derived at the center of the channel. In the case of nanowire RFETs with Schottky junctions both solutions at the nanowire center $\lambda_c$ and surface $\lambda_{if}$ are necessary to be considered. Note that different analytic expressions are obtained for the solutions of the Poisson equation at the center and surface (Figure 2). The ON-currents and higher current part of the sub-threshold region that are mainly given by Fowler-Nordheim tunneling at the Schottky junctions are primarily located near the gate oxide interface (Figure 2b) because the band bending caused by the gate potential at the S/D contact region is stronger at the nanowire surface compared to the nanowire center. In contrast, the OFF-currents including the lower current parts of the sub-threshold region are being dominated by thermionic emission. There charge carriers are located within the nanowire center where the blocking potential barrier (Figure 2a) also caused by the gate potential is lower compared to the region near the gate oxide interface. Both charge carrier transport mechanisms and the corresponding subthreshold swing can be observed at an exemplary transfer characteristic of an n-type nanowire RFET in Figure 3a. Thus, the transfer curve of the RFET is subdivided into two regions, $SS_{TE}$ (thermionic emission) and $SS_{TU}$ (tunneling). Plotting both subthreshold swings as function of $\lambda_c$ as well as $\lambda_{if}$ demonstrates the correlation with the corresponding screening length location (Figure 3c,d). $t_{si}$ and $t_{ox}$ were varied in the range from 6 nm to 20 nm and from 1 nm to 5 nm, respectively. This analysis of the corresponding screening or natural lengths allows a simple estimation of the scaling rules.

Following the general scaling rules for conventional MOSFETs, the minimum channel lengths should correspond to approximately ten times the screening length (nanowire center) of the whole nanowire ($L_{NW} > 10 \cdot \lambda_c$) or five times per junction [12] in order to make short channel effects negligible [14]. For short RFET channel lengths both barriers interfere with one another, especially in the OFF-state. We have verified that for $L_{NW} < 8 \cdot \lambda_c$ the potential barriers for the charge carriers is lowered, the OFF-current is increased and $|V_{th}|$ is reduced. This effect is analog to the drain-induced barrier

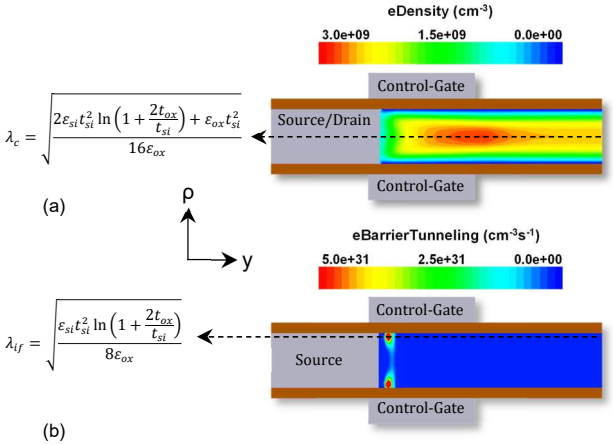


Figure 2. Comparison of relevant screening length locations: (a) screening length along the nanowire center $\lambda_c$ is most relevant in the off-state as seen in the distribution of electron density (2D slice) with a maximum also along the nanowire center. (b) screening length along the interface to the gate oxide $\lambda_{if}$ is most relevant in the on and threshold regions as the electron tunneling rate is maximum near this interface.

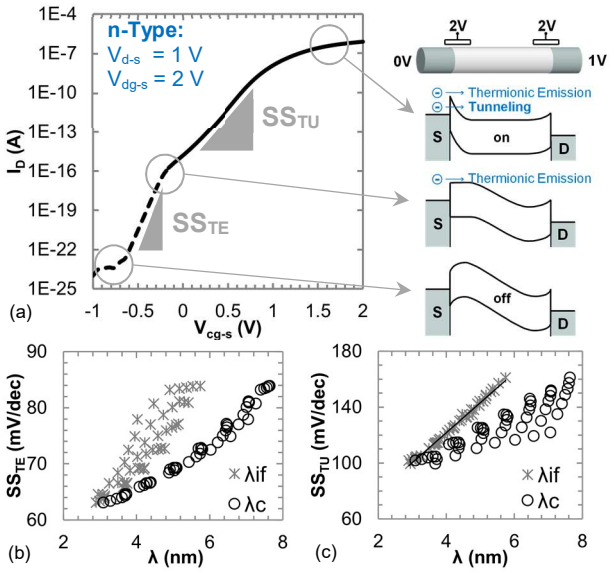


Figure 3. n-type transfer characteristic: (a) transfer curve with a schematic view of the band structure of the respective n-RFET operating points. (b) and (c) show the subthreshold swing of the thermionic emission and the tunneling dominated section respectively, vs. the (simulated) screening length at the channel center $\lambda_c$ (Figure 2a) and at the interface to the gate oxide $\lambda_{if}$ (Figure 3b). The thermionic emission behavior is described in more accuracy by the natural length located in the nanowire center, whereas the tunneling regime is better and linearly described by the surface screening length.

lowering in conventional MOSFETs. Based on $\lambda_c$ we can thus define the minimal channel length for proper OFF-state and $V_{th}$ stability of the RFET, when $L_{NW} > 8 \cdot \lambda_c$. However, an aggressive channel length scaling for higher ON-currents is primarily not required due to a Schottky junction dominated resistance. Only for significantly longer RFETs, the series channel resistance as a result of phonon scattering and surface roughness becomes relevant. The ON-state resistance (p-type RFET, $V_{d-s}$ = -1 V, $V_{pg-s}$ = -2 V, $V_{cg-s}$ = -2 V.) of a thinner RFET structure with $t_{si}$ = 10 nm and $t_{ox}$ = 2 nm can be described by a linear function $R_{on} = a \cdot L_{NW} + b$ with a slope $a = 516.1\ k\Omega/\mu m$ and an offset of $b = 162.6\ k\Omega$ (combined resistivity of both Schottky junctions). Consequently, only from 315 nm channel length upwards the channel resistance of the 10 nm thin RFET becomes larger than the contact resistance. In conventional MOSFET technologies, the gate pitch describes the spacing between the gates of two adjacent transistors. In regard to a simple integration of REFTs into existing technologies, the distance between the program and the control gates should correspond to this gate pitch. Thus, assuming the current set of design rules as for a process optimized for conventional MOSFET fabrication, a RFET may occupy twice the length of a conventional MOSFET but provides an additional functionality. Should RFETs become mainstream devices, the process and the corresponding design rules need to be optimized to the device architecture and self-aligning techniques may be used to reduce the gate spacing below what is possible in conventional CMOS processes.

To optimize both the ON- and OFF-states, the optimal gate length $L_{gate}$ is determined by the sum of the overlap to the source or drain contact $L_{SD\text{-}ol}$ and the overlap to the channel region $L_{ch\text{-}ol}$. A larger overlap to the channel region improves the controllability of the channel by the gate potential and thus the ON-current of the device

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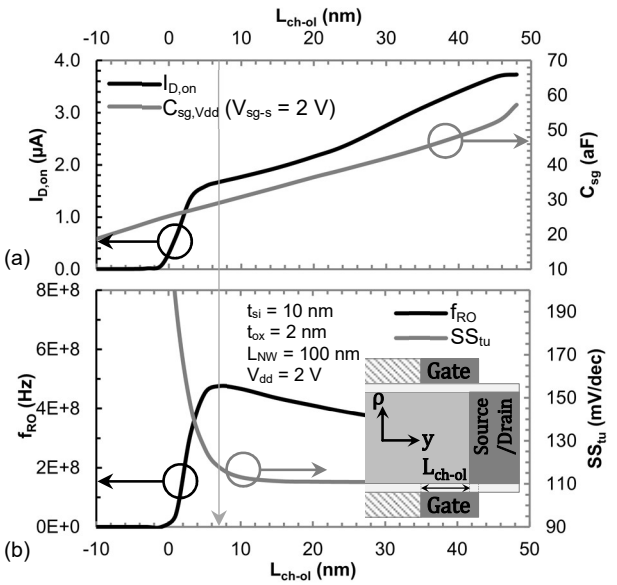


Figure. 4. RFET characteristics represented as functions of the overlap of the gate contacts and the channel region $L_{ch-ol}$. The upper part (a) shows the on-current (only n-type, p-type behaves similar) and the on-state-capacitance of the control-gate. The lower part (b) shows the ring oscillator frequency and the subthreshold swing of the tunneling dominated part of the transfer characteristic. The overlap of the gate contacts to the source or drain region of an RFET structure was always set to $L_{SD-ol}$ = 20 nm.

(Figure 4a). But it also increases the Miller capacity of the gate contact which has to be charged or discharged during the switching process of a circuit. As a figure of merit we analyze the ring-oscillator (RO) frequency which considers the interplay of current, subthreshold swing and capacity to find an optimal value for the overlap to the channel region. This mixed-mode simulated RO was a simplified circuit of five inverter stages (sketch as shown by the insert of Figure 7) made up of ten RFETs with symmetric transfer characteristics of n- and p-type for a supply voltage of $V_{dd}$ = 2 V. The best performance of a RO was observed for a gate overlap to the channel region of $L_{ch-ol}$ = 7 nm (Figure 4b) amounting to approximately twice the screening length along the channel surface ($L_{ch-ol} \approx 2 \cdot \lambda_{if}$). Note also, that the subthreshold swing in the Fowler-Nordheim Tunneling region is severely degraded for $L_{ch-ol} < 7$ nm.

The gate overlap to the source or drain contacts $L_{SD-ol}$ should be as short as possible to avoid a large capacitance between the gate contacts and the source/drain regions. Because of these parasitic capacitances, the RO frequency decreases for larger values of $L_{SD-ol}$ (Figure 5). In the case of missing overlap (negative value) the ON-current is degraded due to the reduced controllability of the Schottky junction. Already a small overlap is sufficient even if the gate oxide is not aggressively scaled. Ideally, an overlap of $L_{SD-ol} \approx 2$ nm is beneficial for performance. Of course, this process accuracy is difficult to control.

The reduction of the channel thickness $t_{si}$ and the oxide thickness $t_{ox}$ reduces the screening length especially at the nanowire surface and improves the controllability of the channel. The result is a stronger bending of conduction as well as valence bands at the Schottky junction providing an increased total tunneling current at the ON-state (Figure 6). Also the channel overlap to the gates has been reduced to the same extent while the overlap to the source or drain contacts remains unchanged. However, when

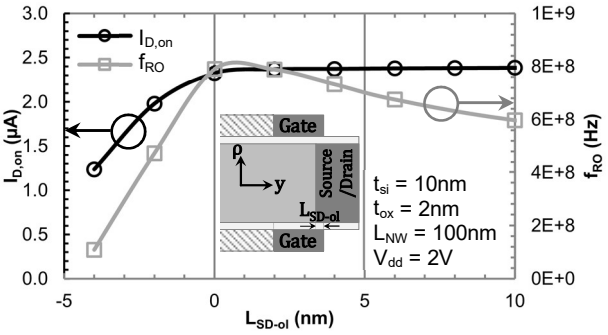


Figure 5. On-current (only n-type, p-type behaves similar) and ring oscillator frequency as function of the overlap of the gate contacts to the source or drain region of an RFET structure $L_{SD-ol}$. A negative value denotes a missing overlap between these two regions. The overlap to the channel region was constant at 20 nm.

reducing $t_{si}$ to values comparable to the Fermi wavelength (< 4 nm in Si) quantum confinement effects should be considered [15]. Bandgap widening can lead to higher barrier heights and thus to lower ON-currents. Additionally, the reduced density of states at the band edges, quantum capacitance behavior [16] and possible alterations of the band structure depending on the wire orientation can strongly impact charge carrier transport. The performance improvement of a RFET structures with scaled cross-section can also be demonstrated with mixed-mode RO simulations. Figure 7 shows the RO (five RFET inverter stages) power consumption normalized to the nanowire diameter $t_{si}$ of two different scaling nodes as a function of the resonant frequency. The channel thickness was scaled from 20 nm to 10 nm and the oxide thickness form 4 nm to 2 nm as well. In this example the ring oscillator frequency at equal power consumption has doubled by halving the channel thickness as well as the oxide thickness. As a result of the improved controllability of the channel and the steeper subthreshold swing, the supply voltage could be reduced by a factor of 0.7 (in the case of Figure 7).

## III. GERMANIUM CHANNEL

Another way to enhance the RFET performance is the replacement of silicon by germanium as channel material [17]. Besides the mentioned higher carrier mobility, germanium also offers a smaller bandgap compared to silicon. As a result, the barrier heights for the n- and

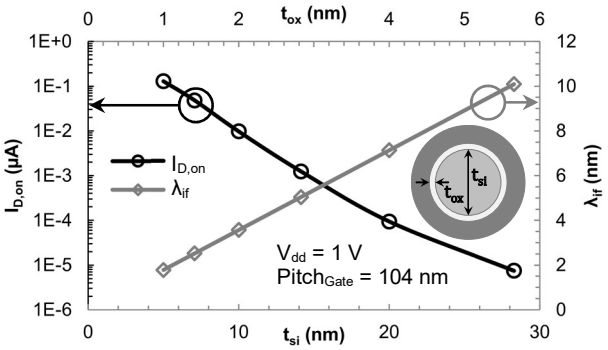


Figure 6. On-current $I_{D,on}$ (only n-type, p-type behaves similar) and screening length at the interface to the gate oxide $\lambda_{if}$ as function of channel thickness as well as oxide thickness $t_{ox}$ (scaled at the same time and by the same factor $k = 1/\sqrt{2}$) of an RFET structure. The supply voltage and the gate pitch are constant 1V and 104 nm, respectively.

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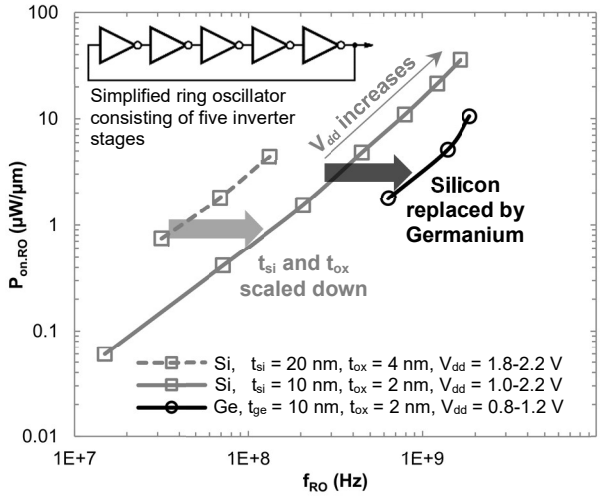


Figure 7. Simulated ring oscillator performance demonstrated by the dynamic power consumption normalized to the nanowire diameter vs. the frequency of ring oscillators consisting of five RFET inverter stages. The gray lines show the increased frequency by down scaled channel thickness as well as oxide thickness. The black lines show the increased frequency of a germanium channel instead of a silicon channel with the same dimensions. Note the dependence on supply voltages.

p-configuration are significantly reduced and higher ON-currents at a lower threshold voltage are to be expected. This is also reflected in an increased RO frequency at equivalent power consumption as seen in Figure 7. In turn the static leakage increases due to the smaller bandgap, nevertheless the dual gating structure of the RFET helps in reducing this effect compared to conventional MOSFETs because the blocking barrier is enlarged by electrostatic tuning of the program gate.

## IV. CONCLUSION

For increasing the complexity as well as functionality of highly scaled integrated circuits, Reconfigurable field effect transistors offer an alternative path to pure scaling. However, the device dimensions still need to stay small enough to utilize an economic benefit. The presented scaling dependencies and rules are especially relevant to enhance performance. An analysis of the screening length theory exhibits its applicability for the thermionic as well as the tunneling dominated part of the charge carrier transport. It has to be emphasized that the RFET performance can be increased by the shrinking of its cross-section. Additionally, the use of germanium as channel material offers an additional increase in performance even at lower supply voltages. The scaling of the RFET length towards larger values, specially relevant when applying large gate pitches between program and control gates has a negligible effect on the RFET performance. As long as the nanowire length is $L_{NW} > 8 \cdot \lambda_c$, proper OFF-state operation and $V_{th}$ stability of the RFET could be observed. The gate contacts should have the corresponding overlaps to the channel region ($L_{ch\text{-}ol} \approx 2 \cdot \lambda_{if}$) as well as a minimal overlap to source or drain. With these results we could show the scaling behavior of nanowire RFET structures and their compatibility with the scaling of conventional technology nodes.

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