Uwe Schroeder, Kyuho Cho, Stefan Slesazeck

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Erstveröffentlichung in / First published in:

Vijay Narayanan, Martin M. Frank, Alexander A Demkov, Hrsg. *Thin Films on Silicon : Electronic and Photonic Applications*. 2016. Singapur: World Scientific, S. 369-401. ISBN 978-981-4740-47-0

DOI: https://doi.org/10.1142/9789814740487_0008

Chapter 8

Materials for DRAM Memory Cell Applications

Uwe Schroeder
NaMLab gGmbH/TU Dresden, Germany

Kyuho Cho
Samsung Electronics, Semiconductor Research Center, Hwasung, Korea

Stefan Slesazeck
NaMLab gGmbH/TU Dresden, Germany

Semiconductor memory is one of the key technologies driving the success of Si-based information technology within the last five decades. The most prominent representative memory type, the dynamic random access memory (DRAM) was patented in 1967[1] and was introduced into the market by Intel Corporation in 1972. Until the year 2001 and the realization of the 110 nm technology node, DRAM was the driving force on the lithography shrink roadmap, before NAND FLASH took over that role. Hence, the development of the DRAM technology was long time the forerunner for the exponentially growing large-scale integration and promoted similar advances in logic chips. One of the reasons of the success of the DRAM is its simple cell structure, which consists of only one transistor (1T) and one capacitor (1C), where the information is stored in form of a charge.

1. DRAM Operation

1.1. *Basic operation*

Figure 1 depicts the comparatively simple structure of a 1T-1C DRAM cell. In this cell, the information is stored as electrical charge on the storage capacitor C. C can be electrically connected to the bitline (BL) via the access transistor T. This means T acts as a switch and its gate is controlled by the wordline (WL), which is arranged perpendicular orientated to the BL. Hence, each individual DRAM cell can be addressed by one WL and one BL. The information is written to the capacitor C by switching on the access transistor T when applying a high voltage V_{WLH} to WL. C is then charged or discharged, applying a bitline voltage V_{BLH} or V_{BLL} to the BL, respectively. When C becomes disconnected from the BL when forcing a low voltage V_{WLL} to the gate of transistor T the remaining charge on the capacitor C represents then the binary information. A charged capacitor denotes a logical '1', whereas a discharged capacitor represents a logical '0'.

The memory state is read using an external circuit — the so called sense amplifier SA, which is connected to each of the bitlines. This SA commonly consists of a cross-coupled inverter circuitry (flip flop) to translate the charge back into digital information. Typically, two bitlines are connected to the two terminals of the SA in order to maximize the signal to noise margin during read operation.

For reading out the information from the DRAM cell, first an equalizing signal of $V_{BLH}/2$ is applied to these two differential inputs. The operation voltage as well as the ground terminal of the sense amplifier

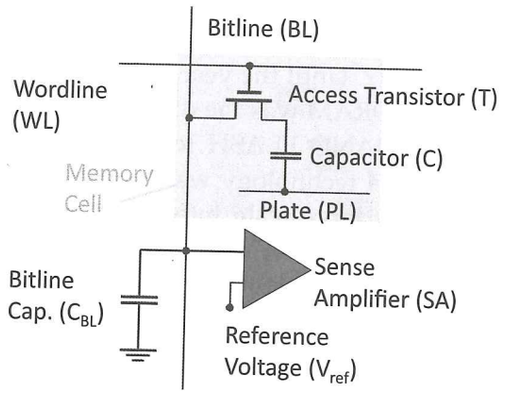

Fig. 1. DRAM memory cell within a memory array.

are disconnected. The flip flop is now in an instable state. Subsequently, the selected WL is activated by applying V_{WLH} so that cell capacitor C and corresponding BL are connected via the access devices. The stored charge on the corresponding capacitor C is redistributed between the cell capacitance, C, and the bitline capacitance C_{BL}. This leads to a voltage change on the active BL, whereas the voltage on the passive BL stays at the pre-charge level of $V_{BLH}/2$. When the sense-amplifier becomes activated by connecting the operation voltage and ground terminal, the flip flop swings into the stable state according to the sign of the voltage change at the active BL. If the capacitor was empty, the voltage on the active BL drops to a lower values than $V_{BLH}/2$ ending in the flip flop reaching the stable state '0'. If the capacitor was charged, the bitline becomes more positive and the flip flop falls into the '1' state. The state of the flip flop can be read by additional digital logic. The subsequent use of the read information is described in section 1.2. The read operation of the DRAM cell is called 'destructive' readout, since the information which was stored in the DRAM cell is destroyed. Hence, after each readout, the information has to be restored for a subsequent read operation. The refresh operation is performed by keeping the WL activated during the whole readout process. With the flip flop swinging to a stable state, the information in the cell can be rewritten. If the capacitor was uncharged, the flip flop moves to the '0' state by pulling the bitline with the activated cell to 0 V. If the capacitor was charged, i.e. in '1' state, the bitline is pulled to V_{BLH}. This means the capacitor is recharged according to its previous state. When turning off the access transistor, the information is restored in the cell as it was before the read operation. In order to reduce the electrical stress over the capacitors dielectric and to minimize the leakage currents, the plateline (PL) is always kept at $V_{BLH}/2$. Hence, the effective voltage over the capacitor is switched between $\pm V_{BLH}/2$ instead of switching between 0 V and full level V_{BLH}.

Unfortunately, leakage paths exist through the capacitors dielectric as well through the non-ideal transistor. The most prominent leakage mechanisms in the transistor are the junction leakage at the so called node side of the transistor (the terminal where the capacitor is connected to) and the channel leakage. Those leakage currents might charge or discharge C over time. In order to prevent the complete loss of the information, a certain charge on C and a corresponding minimum voltage change of the BL has to be guaranteed, which is still detectable by the sense amplifier during the read operation. Therefore, the charge of each memory capacitor has to be

refreshed periodically. For the 16 Gb generation, the refresh time is at 64 or 32 ms depending on the DRAM type.[2] A special built-in counter takes care of the refresh for those rows that are not selected by the working program during the given refresh period. In case of cutting the operation voltage of the DRAM, the information is lost. Therefore, the DRAM is a volatile memory component.

In general, by selecting a WL, all the select-transistors in this row are active so that all cells in this row (1024 or 2048, depending on the chip design) can be read simultaneously. So, each BL has to be connected to one sense amplifier at the array edge. This is the reason why sense amplifier layouts have to be optimized to fit into the very dense pitch which is given by the BLs. The number of cells which can be connected to one BL depends mainly on the available cell capacitance C, BL capacitance per cell and the minimum signal on the BL which can be detected by the sense amplifier.

1.2. *Access transistor*

The planar devices with symmetric junctions used since the beginning of DRAM were not shrinkable below 120 nm without modification. In order to switch off the array devices sufficiently to guarantee a channel leakage well below 1 fA, a negative V_{WLL} was mandatory (see section 1.1). The resulting high electrical fields in the gate-to-junction overlap region lead to an increased junction leakage, the so called gate-induced drain leakage (GIDL). In order to minimize that leakage current, the pn-junctions had to be designed very soft and the boron channel doping concentration of the devices had to be kept below $\approx 2 \cdot 10^{17}/\mathrm{cm}^3$. Low channel doping in turn decreases the threshold voltage of the access devices, resulting in even more negative gate voltages. Hence in order to minimize the leakage currents, a well-balanced dopant profile was mandatory. Further constraints were given by the performance of the access devices. These have to drive a current in the range of $\approx 20\ \mu$A when switched on, allowing to read and rewrite the DRAM cells in an access time well below 10 ns. In order to improve the device performance, the more uncritical pn-junction with respect to leakage currents at the BL-side was doped more heavily and a single-sided so called halo implant was used to increase the BL-sided channel doping. The result was an unsymmetrical device design.

For groundrules below the 70 nm generation, the channel length of the access devices reached a distance at which the potential drop between source and drain lead to an unacceptably high electrical field at the capacitor-side

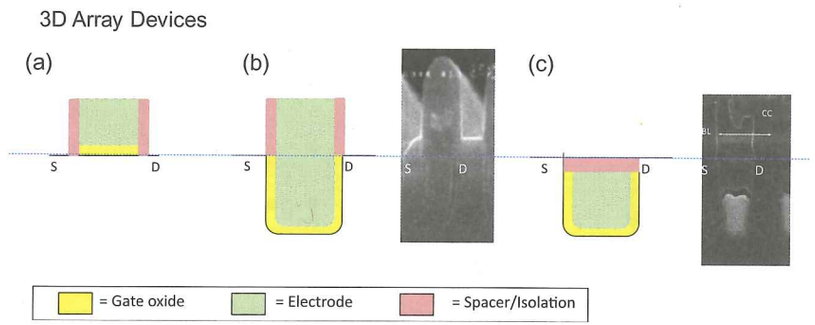

Fig. 2. Access transistor overview for different DRAM technology nodes. (a) Schematic view of a planar transistor in comparison to 3D array devices: (b) recessed channel device and (c) buried word line (BWL) device. For the BWL device, even the electrode is buried in the Si substrate.[71] The dotted line is the wafer surface.[3,4]

pn-junction. Therefore, the so-called 3D devices had to be introduced. In contrast to planar devices, the 3D devices are either formed with a vertical channel [3] or a recess channel [4] as shown in Figure 2(b). Up to that time, the WL typically was integrated in the gate stack module. This means, it ran as poly-gate with tungsten cap over the array. Now additional processing steps had to be introduced for the formation of the 3D devices. Furthermore, with the introduction of the so called "buried wordline" concept, the wordline was shifted below the silicon surface and the gate stack layer[71] was used to integrate the BL (Figure 2(c)). In order to guarantee a fast array access and sufficiently low RC-delay on the WL, a metal-gate had to be introduced. The main advantages of the curved channel below the silicon surface were the spatial separation of both source drain junctions, the possibility to locally increase the channel doping (no increasing electric field at capacitor-sided junction) and the threshold voltage increase due to the concave channel shape. As a result, further margin was yielded for the device design in the attempt to find the best compromise between junction leakage and sub-threshold channel leakage.

1.3. *Capacitor specifications*

The cell charge must be sufficiently high to compensate for leakage in the memory cell. Accordingly, the storage capacitance C needed to be kept constant and could only be slowly decreased during DRAM scaling when other factors were improved e.g. the sensitivity of the sense amplifier (Figure 3). For the 8 Gb chip, C is approx. 20 fF per capacitor. C can be

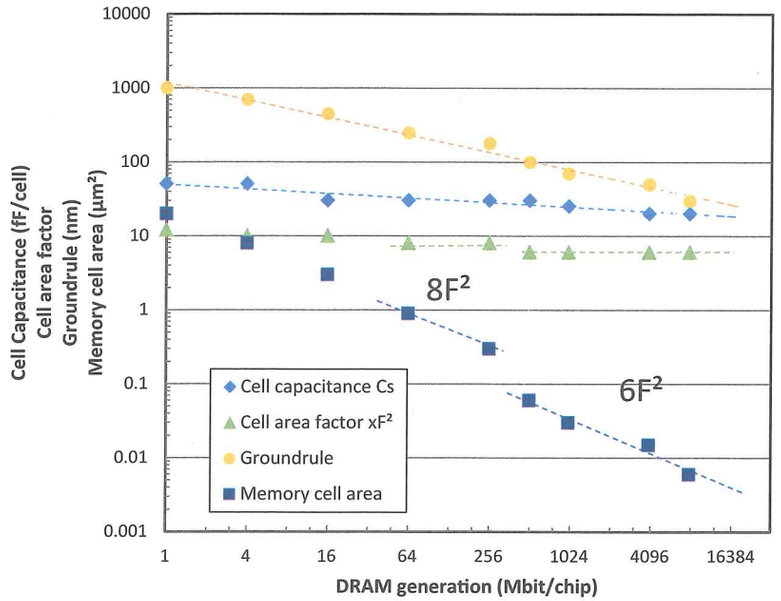

Fig. 3. DRAM roadmap trends during the last 30 years for cell storage capacitance, memory cell area, cell area factor and groundrule.[5,6,8]

calculated by the simple equation (Eq. 1)

$$C = \varepsilon_0 \cdot \varepsilon_{r\,SiO_2} \cdot \frac{A}{CET} \; with \; CET = \frac{\varepsilon_{r\,SiO_2}}{\varepsilon_r} \cdot d \; and \; \varepsilon_{r\,SiO_2} = 3.9 \qquad (1)$$

Here, ε_r is the relative permittivity, ε_0 is the vacuum permittivity, A is the capacitor area (here the average surface area of top and bottom electrode), and d is the physical thickness of the dielectric. Eq. 1 also defines the capacitance equivalent thickness (CET) with respect to the relative permittivity of SiO_2, ($\varepsilon_{r,SiO2} = 3.9$) — the dielectric, which was used for the first DRAM capacitors. Accordingly, the cell capacitance is determined by two main parameters: the cell capacitor area and the capacitance equivalent thickness. As can be seen from eq. 1, for high density DRAM with smaller and smaller cell area (Figure 3), there are only a few options to keep C constant when the cell area decreases:

- reduce CET by enhancing the ε_r-value of the dielectric or by shrinking of the physical thickness d.
- keep A constant by increasing the aspect ratio of the structure with decreasing cell area.

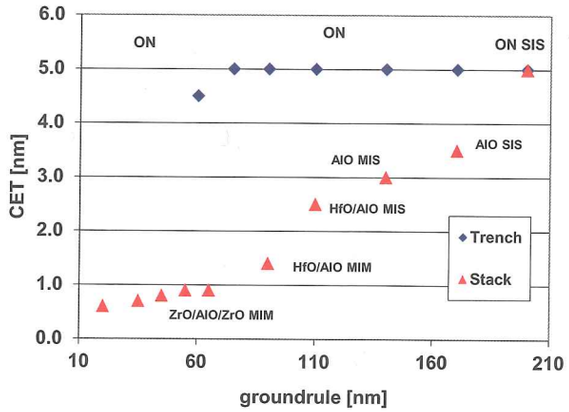

Fig. 4. CET values of capacitor dielectric for trench and stack capacitors for different technology nodes.[8–17]

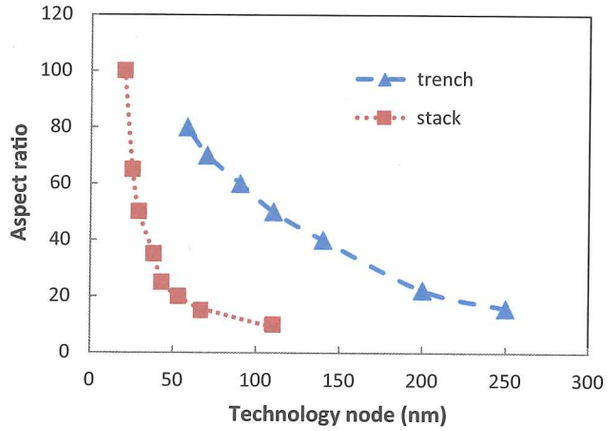

Fig. 5. Aspect ratio of capacitor structure vs. technology node.[7,17]

During the evolution of capacitors in the past DRAM generations, both options have been exercised (see Figures 4 and 5).

SiO_2 with a dielectric constant of 3.9 was used as the capacitor dielectric material for the first DRAM generations. With higher integration density, the dielectric was replaced by a mixture of Si oxide and nitride layers with higher effective dielectric constant ($\varepsilon_r \approx 7$), the so-called ON dielectric.[8] Below the 200 nm groundrule, stack capacitor technology in this conventional design approached its limits: the thickness of the (Si) oxide/nitride (ON) compound layer allowed no further thinning beyond ≈5 nm because

of unacceptably high tunneling leakage currents (see section 2.3). A search for new materials started and industry followed in general the same trend. As a first replacement dielectric material Al_2O_3 was introduced by most of the companies (see Figure 4).[9–11] There are three factors favoring the material, namely its higher dielectric constant ($\varepsilon_r \approx 11$) compared to ON, low leakage current density i.e. high band gap, and also the availability of atomic layer deposition (ALD) processes, along with the ALD equipment suitable for a manufacturing environment. A first fully functional MIS (metal-insulator-semiconductor structure) 1 Gb DRAM chip using Al_2O_3 deposited by ALD on hemispherical Si grains (HSG, for surface area enhancement) with TiN top electrodes[10] was demonstrated. The typical capacitance increase compared to SIS ON (CET $\approx$ 5 nm) was in the order of 200% altogether for HSG introduction, 30% for Al_2O_3 dielectric (CET $\approx$ 3.5 nm), and 10% for depletion reduction by a change from doped poly-Si to TiN top electrode.

As a next step, DRAM manufacturers developed layered or "laminate" dielectrics, in order to gain maximum advantage from each of the two different dielectric materials used in these laminates. For example, amorphous Al_2O_3/HfO_2 structures have been demonstrated by Samsung.[12] The apparent advantage is that Al_2O_3 has a high band gap of $\approx$8 eV, while amorphous HfO_2 has a higher dielectric constant ($\varepsilon_r \approx 22$) at a lower band gap of $\approx$6 eV.[13] MIS Al_2O_3/HfO_2 capacitors showed CET values of $\approx$2.5 nm, which compensated the area loss due to the fact that hemispherical grains for surface area enhancement were no longer feasible in conjunction with this dielectric as ALD HfAlO showed no conformal growth on the grains in a high aspect ratio structure. Further capacitance gain was achieved by introducing a TiN bottom electrode, which reduced the CET value down to $\approx$1.2 nm for a TiN/HfAlO/TiN metal-insulator-metal (MIM) capacitor.

For most of the stack capacitor companies the HfAlO was the last amorphous dielectric. In 2006 the introduction of crystalline tetragonal ZrO_2 (CET $\approx$ 0.8 nm, $\varepsilon_r \approx 40$) with an amorphous Al_2O_3 layer in the center of the ZrO_2 film (ZAZ) to optimize breakdown behavior and reliability was announced (Figure 6).[14,15] In parallel to stack capacitor based DRAM, also memory cells with capacitor underneath the select transistor (trench capacitor) was developed.[16] The main advantage was that the surface area of the capacitor could be easier increased by etching the structure deeper into the Si-substrate. Accordingly, the ON based dielectric material could be used down to 70 nm technology node.[7] However, below the 58 nm node, the trench technology could not be extended because it was difficult to keep

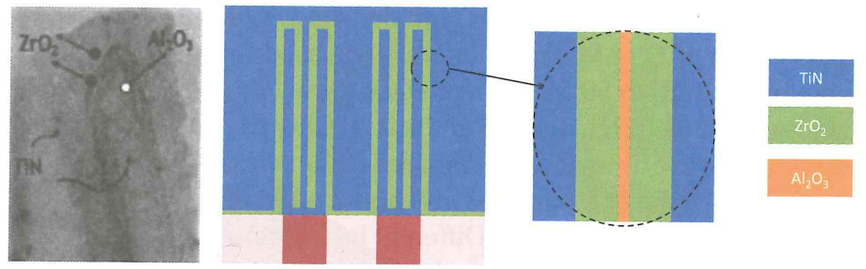

Fig. 6. DRAM capacitor with TIT ZAZ structure: (left) SEM image of typical top layer stack (©2006 IEEE. Reprinted, with permission, from Ref. 14) (middle) schematic overview of capacitor structure (right) detailed overview of MIM structure.

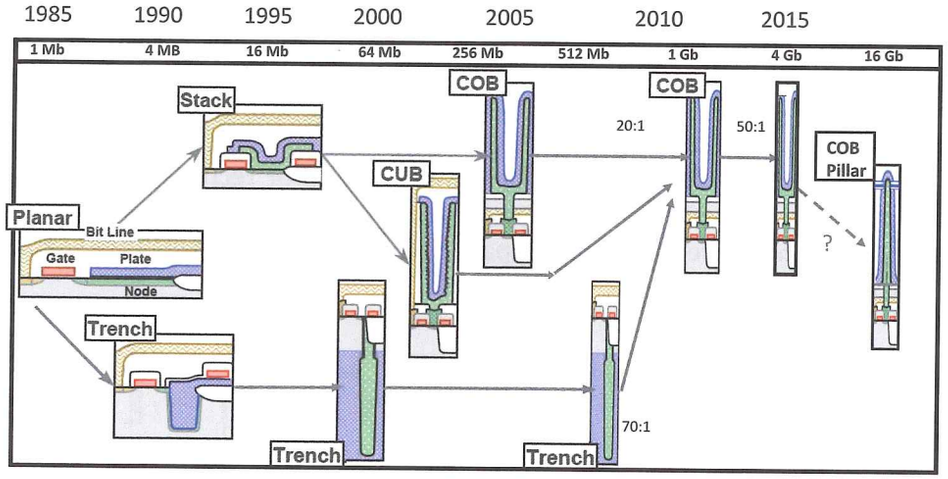

Fig. 7. Schematic overview of different cell concepts.[18]

the capacitor area A_s constant. High-ε_r dielectric materials were difficult to implement due to the high thermal budget of subsequent processing steps (e.g. transistor dopant activation anneals). Accordingly, only stack capacitors with ZAZ dielectric were used up to current 18 nm technology nodes (Figures 4 and 6).[17]

In the beginning of DRAM fabrication, only planar capacitors were processed (see Figure 7). Starting with the 4 Mb generation, the required capacitor area (A_S) was too large for the available cell area (A_{cell}) and the cell capacitance could not be achieved by a planar geometry. Consequently, the third dimension had to be used in the form of trenches and later also of posts in a stacked geometry (see Figure 7). An increasing height of the cell capacitor was maintained the capacitor area, although the area of the DRAM

cell was continuously decreased in high density DRAM. As a consequence, the aspect ratio of DRAM capacitor was increased up to 80 for the trench technology[7] and up to 50 for current stack capacitor devices below 30 nm technology node (see Figure 4).[17] For the last 58 nm trench technology, the ε_r value was about five times lower compared to the stack case and accordingly, the aspect ratio of the structure was also about a factor of five higher than in the stack structure (see Figure 5). Different integration concepts, having the capacitor under (CUB: capacitor under bitline) and over the bitline (COB: capacitor over bitline) of the memory array, were verified. Below 18 nm technology the current capacitor integration concept (cylinder structure, see section 2.3) might be too large for the remaining cell area and pillar concepts might be the only feasible way to form the capacitor. Overall, high aspect ratio capacitor structures require a deep contact hole etch as well as conformal dielectric and electrode depositions (see section 2.6). ALD processes enable the required conformal deposition. In addition, the prevention of leaning and bending is critical when the storage node height is increased. Therefore, below 50 nm stack capacitor technology node, a support structure was successfully adapted to high aspect ratio storage node to stabilize the movement of the capacitor top region[19,20] (see Figure 16.5 in comparison to Figure 16.6).

2. Materials for Capacitor Stacks

2.1. *High-permittivity dielectrics*

As discussed in section 1, a dielectric material with dielectric constant ε_r and a high band gap E_g is required to fabricate a capacitor with sufficient capacitance and minimal charge loss due to leakage current. Looking at published data of oxides for most elements of the periodic table,[13] only a small number of binary oxides have a dielectric constant above 20 (see Figure 8). Since a plot of the dielectric constant versus the band gap follows a hyperbolic behavior (see Figure 12) an even smaller number of materials exhibit a band gap close to or beyond 4 eV: Al doped TiO_2, ZrO_2, and HfO_2. In addition, perovskite type dielectrics like $SrTiO_3$ (STO) show even better dielectric constants and low CET values at target leakage current (see Figure 9).

For other binary dielectrics like Nb_2O_5 and Ta_2O_5 the crystallization temperature is higher than 550°C to reach the reported dielectric constants larger than 40. This temperature is too high to be integrated in a typical DRAM process flow. Here, values below 500°C would be feasible.

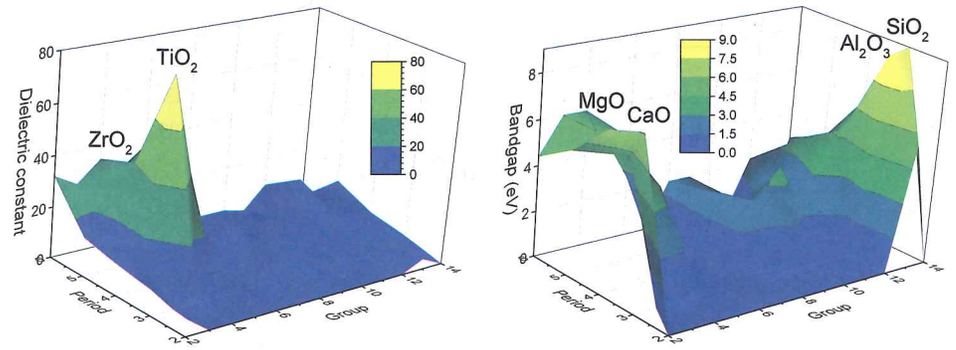

Fig. 8. Overview of dielectric constant and band gap for oxide materials of the periodic table [values mainly from Robertson *et al.*[13]]

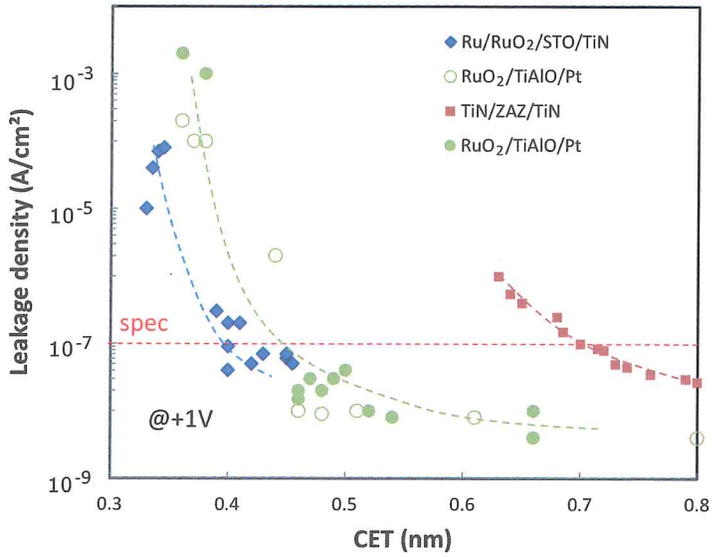

Fig. 9. Leakage current density versus CET value for DRAM capacitor dielectrics as reported in literature for the dielectric materials: doped TiO_2,[22,24] ZrO_2[23] and STO.[21] The leakage current specification limit for DRAM applications is at $1 \cdot 10^{-7}$ A/cm^2.

Having a closer look at the reported literature values for CET plotted as a function of leakage current density (see Figure 9), STO[21] shows the best CET results at target leakage specification ($1 \cdot 10^{-7}$ A/cm^2). These results indicate a slight improvement for $SrRuO_3$ compared to pure Ru electrodes. For $SrRuO_3$ the lattice constants are very similar to STO which reduced dead layer effects.[5,21] The good results of a STO dielectric are followed by Al doped TiO_2[22] and ZrO_2 with Al_2O_3[23] or SrO_2[53] interlayer.

Table 1. Material properties of high work function electrodes.

	TiN	Ru	Ir	Pt
Effective Work Function ϕ [eV]	4.2–4.7[25,26]	4.8[27]	5.6[28]	5.7[33]
Resistivity ρ [$\mu\Omega$.cm][29]	21.7	7.1	4.7	10.5

For a decision on a new dielectric for future DRAM generations important parameters are:

- STO and Al doped TiO_2 would require cost intensive noble metal electrodes with higher work function values (see section 2.2).
- In addition, the physical thickness of the overall MIM capacitor is critical. Due to the lower E_g values of STO and Al doped TiO_2 the overall physical thickness of the dielectric has to be higher than for ZrO_2. This could be critical for future scaled capacitors structures and development is ongoing to reduce the stack height.

2.2. *High work function electrodes*

Different electrode materials could be used for a DRAM capacitor. For best capacitor performance a material with low resistivity, high work function, and high conduction band offset to the adjacent dielectric would be beneficial. In addition, the electrode should be semiconductor compatible, cheap, and a deposition into high aspect ratio structures needs to be possible. Typical material properties of different reported electrodes are summarized in Table 1. For many years, TiN was the material of choice due to the high work function, high thermal stability and good reliability performance. In addition, the process of TiN is relatively inexpensive due to the low precursor cost ($TiCl_4$ and NH_3). For future DRAM capacitors also noble metal electrodes are of interest due to their high work function, high conduction band offset values, and low resistivity. But here, a conformal deposition in high aspect ratio structures and capacitor reliability still need to be proven. Furthermore, the high cost of current noble metal precursors needs to be reduced.

With shrinking capacitor dimensions, the dielectric thickness becomes thinner and electrode effects on the leakage currents become more and more important since the leakage current of the capacitor becomes mainly determined by the dielectric/electrode interface. In addition, the resistance of the electrode is important considering the high operating speed of

DRAMs. These two important properties of the electrode material (Table 1) are briefly discussed below.

2.2.1. *Work function*

According to the Schottky-Mott rule, the conduction band offset *CBO* of a metal insulator contact is determined by the electron affinity χ of the dielectric material and the work function ϕ of the electrode material (Eq. 2) (see Figure 11).

$$CBO = \phi - \chi \tag{2}$$

The Schottky-Mott rule does not consider the interface reaction between electrode and dielectric. Therefore, the observed conduction band offset value of the metal/dielectric contact is usually different from calculated material parameters. Considering an interface formation, the Schottky-Mott rule can be modified as:

$$CBO = \phi - \chi + e \cdot D_{int} \tag{3}$$

(with $e \cdot D_{\text{int}}$: term induced by the interface dipole)

There have been several approaches to determine the interface dipole value systematically. A pinning factor S and the addition of a density of interface state N were suggested to calculate the conduction band offset.[31,32]

$$CBO = S(\phi - \phi_s) + (\phi_s - \chi)$$
$$S = [1 + (e^2 N\delta/\varepsilon_{int}\varepsilon_0)]^{-1} \tag{4}$$

(with e: elemental charge, N: density of interface states, δ: interface thickness, ε_{int}: relative permittivity of the interface, ε_0: permittivity of free space, ϕ_s: interface energy level of the dielectric).

It was also found that higher- ε_r dielectric materials showed a larger deviation from Schottky-Mott rule due to a small S value (see Figure 10). However, no universal formula has been suggested to successfully calculate the conduction band offset yet.

Regardless of such a deviation, high work function electrode materials increase the *CBO* of the metal insulator contact which results in a lower capacitor leakage current. Replacing the low-ε_r SiON ($\varepsilon_r \approx 7$) to the higher-ε_r ZrO_2 dielectric ($\varepsilon_r \approx 40$) at 80 nm technology node decreased the barrier height of the capacitor inevitably since the electron affinity of ZrO_2 ($\chi \approx 2.2$ eV) is higher than the one of SiON ($\chi \approx 1.5$). Therefore, TiN was chosen as a higher work function material ($\phi \approx 4.7$ eV) to replace the doped

Si ($\phi \approx 4.0$ eV) electrode to maintain the barrier height. The usage of TiN as an electrode has been successfully extended for 10 years to the current 18 nm technology node. Further scaling of the DRAM capacitor requires higher ($\varepsilon_r > 40$) dielectric constant materials. Unfortunately, the electron affinity of higher dielectric constant materials is higher than ZrO_2 (e.g TiO_2: 3.3 eV[34]). Therefore, higher work function electrode materials are necessary to maintain the barrier height. There has been tremendous research effort to integrate an noble metal based electrode such as Ru ($\phi \approx 4.8$ eV), RuO_2 ($\phi \approx 5.0$ eV[35]), Ir ($\phi \approx 5.6$ eV), Pt ($\phi \approx 5.7$ eV)[72] into DRAM capacitors. Ru and RuO_2 were most intensively studied because Ru is relatively easy to etch and the cost of Ru precursors is relatively low among the noble metal electrode materials.

Even though the work function of the noble metal is higher than the one of TiN, which is an advantage for further scaling of the dielectric, several technical issues remain to be solved. First, a conformal deposition process for the thin noble metal is one of the major challenges for integrating the material into the capacitor. Unlike oxide and nitride materials a pure metal deposition process does not have a self-limiting surface reaction. Conformal thin inert noble metal films in high aspect ratio capacitor require appropriate ALD precursors and processes. Considering the high cost of the noble metals, process cost should be minimized by development of a low cost precursors and a fast deposition process.

In addition, the *CBO* does not improve as expected because of two reasons: As described in Eq. 3 pinning due to interface dipoles is lowering the *CBO*.[36] Furthermore, noble metal atoms can easily diffuse into the dielectric material, which causes traps at the interface and degrades the barrier height of the capacitor[37] (see Figure 11). Accordingly, new integration schemes are necessary to prevent these effects. The experimental determination of the work function and the *CBO* is described in section 2.4.

2.2.2. *Resistance*

To store information in a DRAM capacitor the charge needs to be transferred within the electrode to the dielectric layer interface. Possible write and read times are determined by the RC-delay of the cell (see section 1). If the resistance of the electrode is too high, the RC-delay reduces the charge transport within the electrode material, which lowers the effective cell capacitance. During capacitor scaling the thickness of the capacitor electrodes was continuously decreased, which causes a higher RC-delay since the resistivity of the thin film electrode is higher than the one of

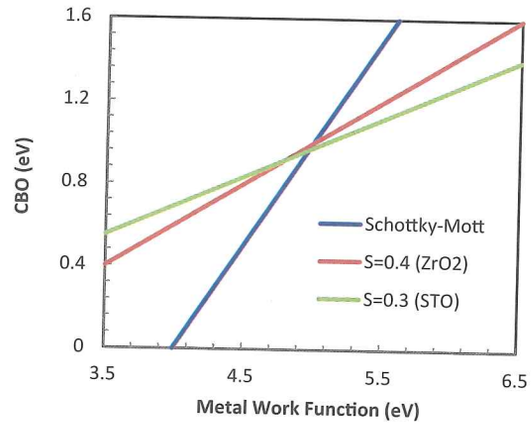

Fig. 10. Metal work function vs. barrier height: prediction from CBO models that assume a fixed separation between interface states and metal.[30]

the bulk material.[38] In addition, the top electrode is thinner than the bottom electrode, which further impacts the RC-delay. The main reason for this difference in electrode thickness is the integration flow described in section 2.6 (see Figure 16). Here, a certain thickness is required for the bottom electrode to guarantee the stability of the whole structure and the top electrode only fills remaining gaps in the structure.

$$R = \rho \cdot \frac{l}{A} \tag{5}$$

The resistance R of a thin TiN wire depends on the resistivity ρ, the length l and area A of a wire (Eq. 5). The resistivity of a film can be reduced by increasing the film density and improving the conformality of the film. The resistivity of inert noble metal electrodes is several times lower than that of TiN (Table 1.) Therefore, applying inert metal electrodes to DRAM capacitors can effectively reduce the electrode resistance.[72]

2.3. *Leakage mechanisms and traps*

The charge on the storage capacitor is decreased by leakage currents. Therefore, DRAM capacitors need to be recharged periodically, which is called "refresh". Typical refresh times are 64 or 32 ms depending on the DRAM type. The leakage current of the DRAM capacitor is determined by several parameters such as dielectric thickness, barrier height, trap energy level and trap density (see Figure 11).

Electrodes have a major impact on the leakage current since they supply both types of charge carriers: electrons and holes. When the dielectric is

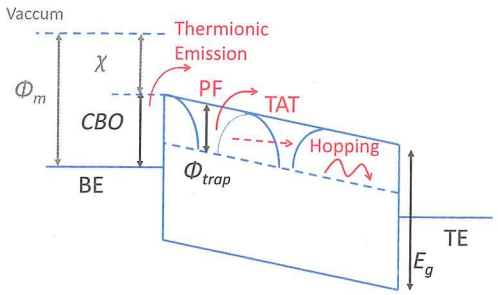

Fig. 11. Schematic overview of different leakage mechanisms for DRAM capacitors.

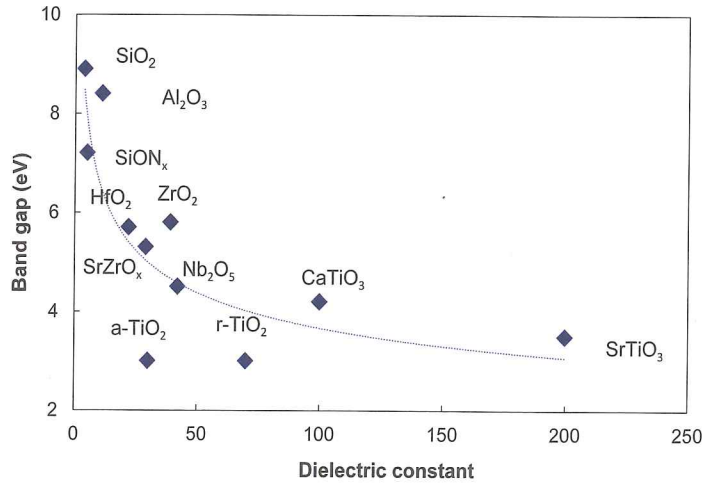

Fig. 12. Empirical trend between the band gap E_g and the dielectric constant ε_r for various dielectrics.[13] The dashed line is a fitting curve.

in contact to the electrodes, a band structure is formed where charged carriers like electrons need to overcome an energy barrier (Schottky barrier or conduction band offset *CBO*). This barrier is a dielectric metal interface material property and dependent to the metal workfunction ϕ and the affinity χ of the dielectric as described in Eq. 2. The band gap E_g was empirically found to show an inversely proportional dependence on the dielectric constant (see Figure 12).[39] Accordingly, materials with high dielectric constant have a low band gap and likely also a lower CBO and need to be deposited with a much higher thickness to compensate for the higher leakage current.

Overall, the leakage current can be divided into three major components: thermionic emission, tunneling, and hopping mechanisms.[40] Thermionic

emission effects could be injection from the Fermi-level of the electrode to the conduction band of the dielectric (Schottky emission: Eq. 6):

$$j = \alpha \cdot T^2 \exp\left(-q\left(\phi_{trap} - \frac{\sqrt{\frac{qF}{\pi\varepsilon}}}{k_B T}\right)\right) \tag{6}$$

(where j is the current density, α is a constant, q is the charge of electron, φ_{trap} is the trap depth without external field, F is the electric field in the dielectric, k_B is the Boltzmann constant, and T is the temperature.

Or by Poole-Frenkel emission of trapped carriers from the trap site to the conduction band (Eq. 7):

$$j = \beta \cdot (qN_{PF}\mu)F \exp\left(\frac{E_A}{T}\right) \text{ with } E_A = -q/k_B \cdot \left(\phi_{trap} - \sqrt{\frac{qF}{\pi\varepsilon_0\varepsilon_\infty}}\right) \tag{7}$$

(where $j, q, \varphi_{\text{trap}}, k_B, T, F$ see above, N_{PF} is the trap density, μ is the electron mobility, ε_0 is the vacuum permittivity, and ε_∞ is the dynamic permittivity) Both effects are field enhanced and increase with temperature.

On the other hand, bulk transport effects need to be discussed: Tunneling can occur from the Fermi-level of the electrode to adjacent trap sites or between different trap locations. This effect follows for a square barrier (Eq. 8):

$$j = \sigma V; \sigma = \frac{q^2\sqrt{2m^* q\phi_e}}{4\pi\hbar^2\omega} \exp\left(-\frac{2\omega}{\hbar}\sqrt{2m^* q \cdot CBO}\right) V \ll CBO \tag{8}$$

or:

$$j = \sigma F^2 \exp\left(-\frac{4\sqrt{2m^*}}{3q\hbar F}(q \cdot CBO)^{\frac{3}{2}}\right) \quad with\ \sigma = \frac{q^3}{16\pi^2\hbar} \cdot q \cdot CBO \tag{9}$$

($j, q, \varphi_{\text{trap}}$, F see above, m^* the effective tunneling mass, ω the relevant width of the barrier, $\hbar$ the Planck constant) for higher applied fields for a triangular shaped barrier according to the Fowler-Nordheim equation (Eq. 9). As a last mechanism, hopping to nearest neighbors is mentioned and further mechanisms are described in literature.[40] Depending on the transport mechanism, different procedures are described to obtain e.g. the trap depth. As one example, the extraction of parameters for Poole-Frenkel emission is described in Fig. 13.[41] Here, the logarithm of the leakage current density versus one over temperature is plotted for a ZAZ capacitor with

TiN electrode. The data should follow a straight line and a trap depth of 0.8–1.4 eV can be calculated.[42]

2.4. *Capacitor band structure*

The knowledge of the DRAM capacitor band diagram can be used to model leakage currents [43] and to further optimize the film stack for future DRAM generations. The band structure has been estimated by several experimental methods. Terraced oxide measurements are performed to determine the work function of an electrode material on a dielectric.[44] A SiO_2 layer is grown on a Si substrate and a stepped structure is formed by wet chemical etching. On this surface, a thin dielectric (eg. ZrO_2) and metal layer pads (e.g. TiN) are deposited. After measurement of the flatband voltage shift for different dielectric thickness, values the work function of the metal can be extracted.[44] In addition, internal photoemission (IPE) spectroscopy enables

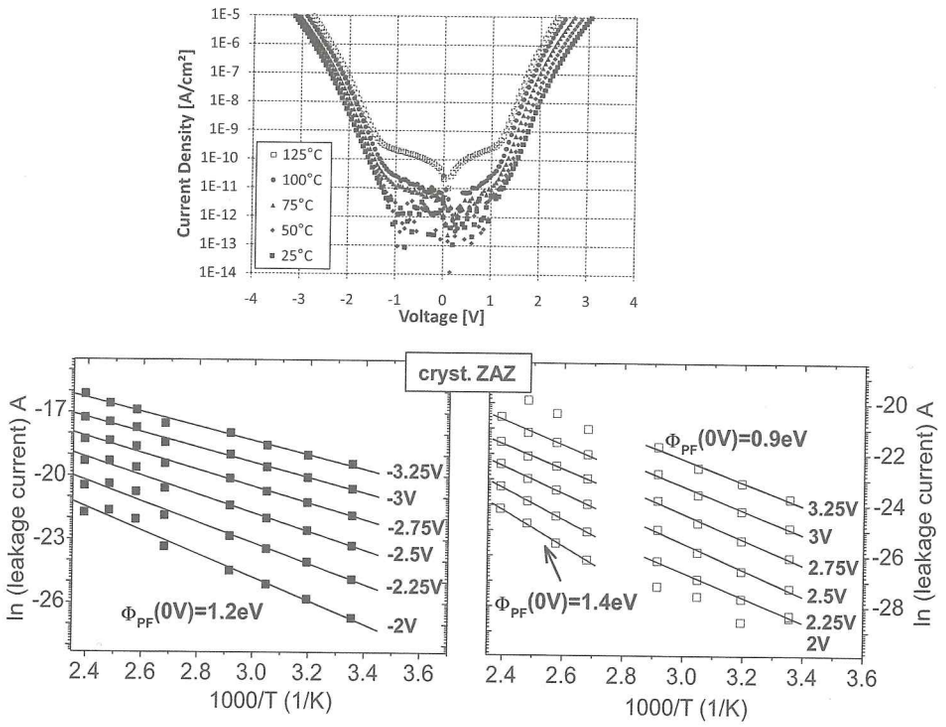

Fig. 13. (Top) Leakage current density of a 10 nm ZAZ capacitor dielectric with TiN top and bottom electrode for different bias voltage and different substrate temperatures (©2014 IEEE. Reprinted, with permission, from Ref. 41). Values for low bias voltages are limited by resolution of measurement setup. (Bottom) Extraction of trap levels assuming a Poole-Frenkel leakage mechanism.[42]

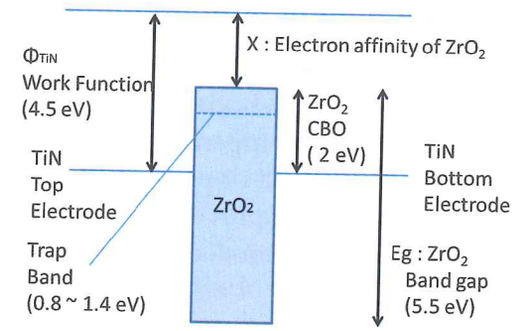

Fig. 14. Band diagram for a MIM capacitor with TiN electrodes and a ZAZ dielectric.[67]

straightforward CBO barrier determination as the minimal energy required to excite an electron from the TiN Fermi-level to the conduction band of the dielectric.[45] Furthermore, the band gap of the dielectric is characterized by photoconductivity (PC) measurements.

The band diagram of a MIM capacitor with a $ZrO_2/SrO/ZrO_2$ very similar to a currently used ZAZ dielectric was summarized as Figure 14[67] The *CBO* between the Fermi-level of the TiN electrode and the conduction band of ZrO_2 is about 2 eV and the band gap of ZrO_2 about 5.5 eV. Both numbers are lower compared to values reported in literature for bulk materials.[42] This can be related to diffusion of electrode atoms into the dielectric, interface oxidation of the electrode material and to effects caused by property changes in thin films. In addition, trap levels at 0.8–1.4 eV below the ZrO_2 conduction band and a TiN work function of ≈4.5 eV were determined.[53]

The band structure of a MIM capacitor with Ru electrode and $SrTiO_3$ dielectric was evaluated by Kaczer *et al.*[46] Again, the IPE method was used to evaluate the conduction band offset and band gap of the dielectric materials. A conduction band offset of ≈1.5 eV and a band gap of 3.2 eV was determined. Considering a *CBO* of ≈ 2 eV for ZAZ based capacitor with TiN electrodes, the *CBO* value for a $Ru/SrTiO_3$ interface needs to be improved to obtain a maximum advantage from their high dielectric constant. Sr rich $SrTiO_3$ was suggested to suppress the leakage current of the $Ru/SrTiO_3$ system.[47]

Moreover, the band structure of Al doped TiO_2 with a RuO_2 electrode was studied. It was suggested that the RuO_2 electrode was inevitable to deposit the rutile high dielectric constant phase of TiO_2. Furthermore, Al doping improved the conduction band offset of the RuO_2/TiO_2 interface,

which reduced the leakage currents effectively.[48] However, due to a low E_g value of TiO_2 (3.1 eV), the conduction band offset of RuO_2/Al doped TiO_2 was estimated as ≈1.5 eV, which is also smaller than the one of a ZAZ capacitor with TiN electrodes. To compensate for these low *CBO* values, IrO_2 electrodes were deposited on Al doped TiO_2. Here, the higher work function values resulted in a *CBO* improvement and a decrease in leakage current for the Al doped TiO_2 capacitor stack.[49]

2.5. *Capacitance equivalent thickness scaling*

As discussed in section 1.3, a CET downscaling of DRAM capacitor can be achieved by two different approaches. On one hand, a decrease of the physical thickness of the current ZrO_2 dielectric is evaluated and on the other hand, new higher- ε_r dielectric materials could be applied to the DRAM capacitor.

Figure 15 shows a plot of the leakage current as a function of the CET value indicating an exponential increase of the leakage current for lower CET values caused by the thickness scaling of the ZrO_2 dielectric. According to the ITRS roadmap[51] a leakage current density of $1 \cdot 10^7$ A/cm^2 is required at a bias voltage of 0.5 V(V_{BLH}). This corresponds to about 1 fA/memory cell for a 3D capacitor when the surface area is not exactly known. At target leakage specification, typical CET values of 0.7 nm are reached for

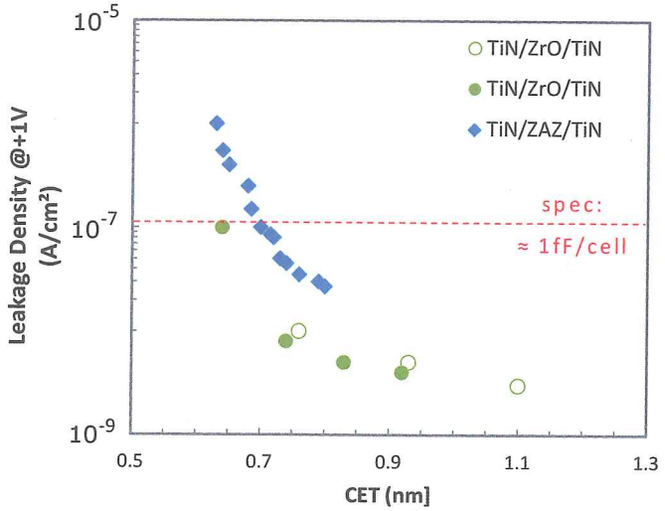

Fig. 15. Leakage current density versus capacitance equivalent thickness for different ZrO_2 based dielectric with TiN electrodes in a MIM capacitor configuration (square dots[23]; open dots;[50] closed dots[18]).

a crystalline pure ZrO_2 dielectric.[50] This material does not meet the 10 year lifetime criteria for DRAM capacitors due to the crystalline structure of the ZrO_2 dielectric. Here, ZrO_2 grains span the whole distance between bottom and top electrode and the leakage current is increased along the grain boundaries.[52] Typically, an amorphous Al_2O_3 interlayer is introduced in the center of the ZrO_2 dielectric to separate the ZrO_2 layer into two crystalline films with smaller grains size and an overall improved leakage and reliability behavior.[15] Due to the lower ε_r- value of the introduced Al_2O_3 the CET value is slightly increased which resulted in a similar CET/leakage performance compared to pure ZrO_2. In the last years the ZAZ process was improved and currently CET values below 0.7 nm at target leakage current can be reached. Furthermore, studies are ongoing to search for an interlayer material with higher dielectric constant than Al_2O_3 and similar electrical properties.[53]

As explained in paragraph 2.3 different leakage mechanisms could be responsible for conduction through the dielectric material. Temperature dependent leakage current measurements could give an indication of the main conduction paths. For the ZAZ capacitor stack a bias dependent leakage current mechanism is reported.[42] Assuming a Poole-Frenkel conduction mechanism, trap levels in the order of 0.8–1.4 eV are extracted between 1.5 to 3 MV/cm and related to oxygen vacancy driven trap sites[54] (see paragraph 1.2). The leakage current at higher field was typically attributed to Fowler-Nordheim tunneling.[56]

More aggressive CET scaling has been achieved by higher-*k* ($\varepsilon_r > 40$) dielectric materials such as Al doped TiO_2 and $SrTiO_3$ with noble metal electrode (see Figure 9). A CET value below 0.5 nm was obtained for Al doped TiO_2 with RuO_2 top and bottom electrode.[54] Even better results were achieved for MIM capacitors with $SrTiO_3$ dielectric and Ru or $SrRuO_3$ electrodes. A CET value below 0.4 nm was successfully shown (see Figure 9) and recent leakage current simulations using conduction band offset and oxide tunneling mass as a key parameter suggested that $SrTiO_3$ might be the only high-*k* dielectric candidate which is able to attain CET values below 0.3 nm.[21]

2.6. *3D capacitor fabrication*

Unlike planar structure MIM capacitor, formation of 3D structure DRAM capacitors requires additional process step and technology.

The integration flow for a DRAM capacitor was kept stable since the 50 nm technology but the aspect ratio of the structure drastically increased.

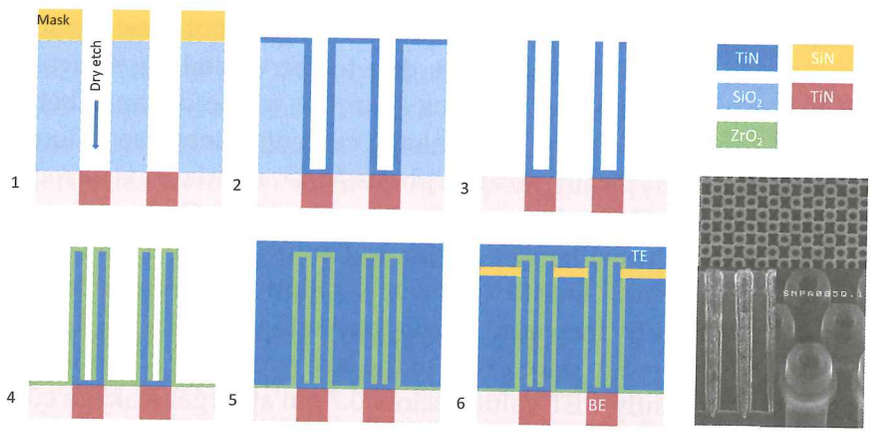

Fig. 16. Integration flow for DRAM stack capacitor fabrication; SEM: (top) top view of capacitor with support structure (bottom left) cross section similar to Figure 16.6 (bottom right) top view of capacitor under certain angle (©2013 IEEE. Part of figure reprinted, with permission, from Ref. 4).

In a first step (Figure 16.1), a mask is deposited on a micrometer thick mold SiO_2 layer before very precise trenches are dry etched into the SiO_2. These trenches need to be placed exactly on top of the contact structures and require an almost 90° taper angle. Both steps are already very challenging for the according process equipment.

After dry etching of trenches a chemical vapor deposition (CVD) of titanium nitride into a trench structure is performed (Figure 16.2). Typically, titanium chloride ($TiCl_4$) and ammonia (NH_3) are used as precursors. The mold oxide material is removed by a wet chemical process (Figure 16.3) followed by the ZrO_2-based dielectric deposition onto the very brittle TiN bottom electrode cup-like structure (Figure 16.4). Due to the layer by layer growth of the ALD processing very conformal films can be deposited in these high aspect ratio structures. For ZAZ film deposition typical precursors are $Zr[N(CH_3)C_2H_5]_4$ or $CpZr[NMe_2]_3$ for Zr, $Al(CH_3)_3$ (TMA) for Al and ozone as the oxygen source at deposition temperatures of about 300°C.[55] Finally, the CVD TiN top electrode is deposited onto the ZrO_2 dielectric (Figure 16.5). After fabrication, each capacitor in the array has a separate bottom contact to the select transistor and a common top electrode. To stabilize the cup shaped bottom electrode and to prevent bending and leaning a supporting SiN-based structure was implemented in the processing sequence starting with 50 nm technology node (Figure 16.6). For future DRAM capacitor structures the cell area is decreasing further and even higher aspect ratio structures are necessary to compensate the area

loss. As shown in Figure 5, the aspect ratio might increase to 100:1. This will drastically enhance the surface area of the capacitor and accordingly, also of a 300 mm wafer and impact process specifications. Since the electrode layer might need to be thinned to relax the scaling requirements for future devices the resistivity within the electrode layer will become increasingly more critical.

As described in literature,[56] during the ZrO_2 ALD deposition process the underlying TiN bottom electrode is slightly oxidized by the usage of the ozone precursor and a TiO_xN_y is formed at the interface. During top electrode deposition only a nitridation of the dielectric is occurring and oxygen is diffusing into the TiN during subsequent anneal processing steps. Hence, the top electrode is less oxidized and a slightly asymmetric capacitor stack is formed. Since the leakage current is partially impacted by the interfaces these structural differences are leading to a non-symmetric leakage current behavior.

The high aspect ratio DRAM capacitor is fabricated on top of the transistor and further back end metal lines are processed on the capacitor. Compatibility to current DRAM integration scheme is essential for the DRAM capacitor. From all possible integration parameters, a conformal physical thickness of dielectric material and electrode are one of the most important process parameters for capacitor integration. The ratio between thinnest and thickest physical thickness in 3D structure is called as step coverage. The step coverage of dielectric material is important for both the cell capacitance and the leakage current. Due to the high aspect ratio of a DRAM capacitor structure, the thickness of the dielectric layer at the top of the structure is thicker than that on the bottom. Precursor and reactant concentration differences between top and bottom during the deposition are considered to be the origin of this difference.[57] The region with the thinnest dielectric — most likely at the bottom of the structure determines the leakage current of the storage capacitor. Hence, a minimum bottom dielectric thickness should be maintained to prevent high leakage currents and early breakdown of the device. On the contrary, a thicker dielectric at the top reduces the overall cell capacitance. Therefore, the target would be to improve the step coverage for best capacitance and leakage current performance. This becomes more and more challenging for smaller capacitor structures with higher aspect ratio. Novel atomic layer deposition processes were successfully developed for Al_2O_3 and ZrO_2 deposition to maintain conformal step coverage down to 18 nm DRAM generations on a complete 300 mm wafer.[58] Physisorption and chemical decomposition

of precursors and incomplete chemisorption or chemical reaction are considered as the main reasons for conformality degradation.[59,60] Further improvements are necessary below the 18 nm node to be able to continue to achieve these step coverage requirements.

A poor conformality of the TiN electrode at the bottom of the structure degrades the mechanical strength. In addition, a reduced thickness of TiN in the top region causes resistance degradation (see section 2.2.2). Again, novel deposition process needs to be developed to guarantee further scaling of the capacitor.

These issues also impact the introduction of possible new dielectric or high work function electrode materials. Although perovskite type high-*k* materials such as $SrTiO_3$ have been successfully applied to bulk capacitors starting in middle of 20th century,[61] they are still not implemented in DRAM capacitor despite of the tremendous development efforts.[73] Poor step coverage of the current ALD processes for $SrTiO_3$ and the Ru electrode are some of the typical issues for device integration.[62]

3. Reliability of the Capacitor

The stored charge on the capacitor electrodes decreases over time due to leakage via the capacitor dielectric and the select transistor structure within the memory cell (see Figure 1). According, the charge needs to be restored in 64 or 32 ms (refresh time depends on the DRAM type). For an accurate sensing of the memory state the sense amplifier requires a maximum charge drop of less than 10% within the refresh time. For this reason, potential detractors will be discussed in the following chapter.

3.1. *Relaxation currents*

Dielectric relaxation is ability of a capacitor to completely discharge to zero. As depicted in Figure 18, the leakage current density in a capacitor is dominated during the initial time period by relaxation currents. For most dielectrics, they follow the empirical Curie-von Schweidler relation with a time dependence of the relaxation current density $j_{relax}(t)$[63] (see Eq. 10):

$$j_{relax}(t) = j_0 \left(\frac{t}{t_0}\right)^{-\alpha} \quad \text{with } 0.5 < \alpha < 1 \tag{10}$$

The time dependence was typically explained by a sequence of "Debye" relaxations ($j_i(t) \propto \exp(-t/\tau_i)$) with very different relaxation times τ_i. Since there is no microscopic physical model, the charge loss is

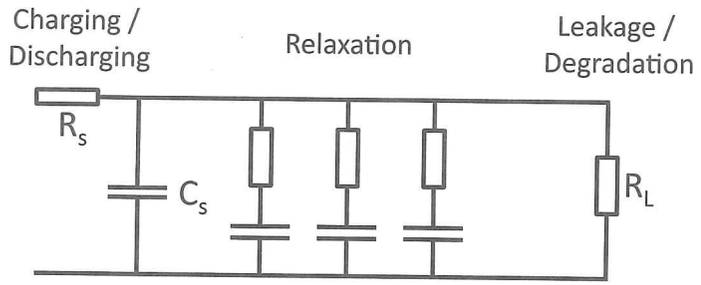

Fig. 17. Schematic diagram of equivalent current for dielectric relaxation.

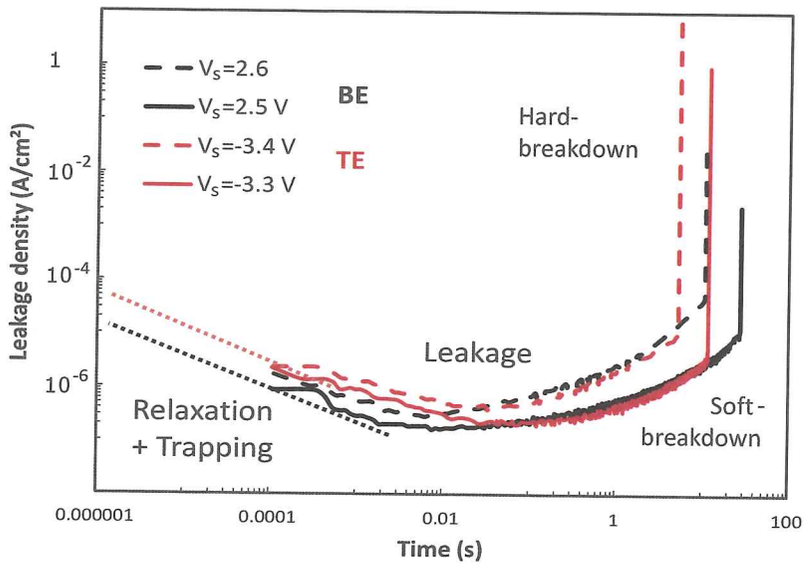

Fig. 18. Time evolution of current response after charging a MIM capacitor with ZAZ dielectric.

described in a model of parallel RC elements with different time constants (see Figure 17).[64]

After this initial relaxation phase (typically above the ms range) a steady state leakage current is visible before resistance degradation of the device (see section 3.2), i.e. the high resistivity of the insulator decreases gradually (soft breakdown) or nearly instantaneously by several orders of magnitude (hard breakdown) (see Figure 18). Both are unacceptable for DRAM operation because of possible lifetime restrictions.

The relaxation current can be determined by charging the capacitor for a defined amount of time, discharging the device for a short time followed by a measurement of the relaxation current. These relaxation currents degrade

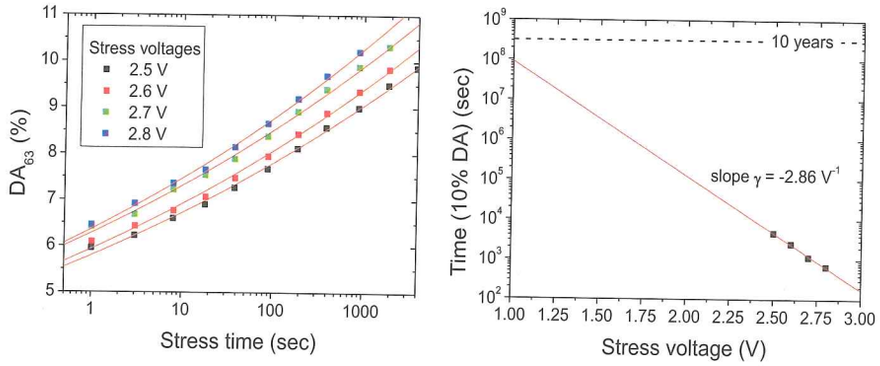

Fig. 19. (Left) Dielectric relaxation for different stress times and stress voltages. (Right) Extrapolation of dielectric relaxation to conditions at which a DRAM capacitor is used.

over time and the behavior was characterized for planar ZAZ capacitors at accelerated stress conditions (see Figure 19). For an extrapolation, the time is plotted when a capacitor showed a loss of 10% due to relaxation at a certain voltage. This time can be extrapolated to 10 years and typical conditions where the capacitor is used ($V_{BLH} \sim 0.5$ V). Hence, relaxation is uncritical for a capacitor when the device is used at room temperature and with charging pulses in the μs range. This phenomenon might become more critical at elevated temperatures or for shorter switching times.

3.2. *Dielectric resistance degradation and breakdown*

The above mentioned constant leakage current regime is followed by an increasing leakage current and subsequently by a slow (soft) or abrupt (hard) breakdown (see Figure 20). A clear distinction of this different breakdown behavior is visible for amorphous versus crystalline ZrO_2 caused by different amounts of defects in the layer.[41] These determine the lifetime and reliability of the capacitor. The lifetime of a single capacitor can be defined as the time for which the leakage current has increased ten times compared to the steady state minimum. Overall, the benchmark for the lifetime of capacitors is typically 10 years at an operation voltage of $\approx$0.5 V ($= V_{BLH}$). Data for the lifetime evaluation has to be collected in accelerated tests for a statistical relevant set of production type stack capacitors. Here, higher stress temperatures and voltages are used to avoid extremely long testing times. A statistical distribution of a larger number of breakdown events is plotted in a Weibull graph (see Figure 21 (left)). The most likely breakdown time is extracted at the time when 63% of the devices failed. This time can be plotted for different stress voltages and extrapolated to

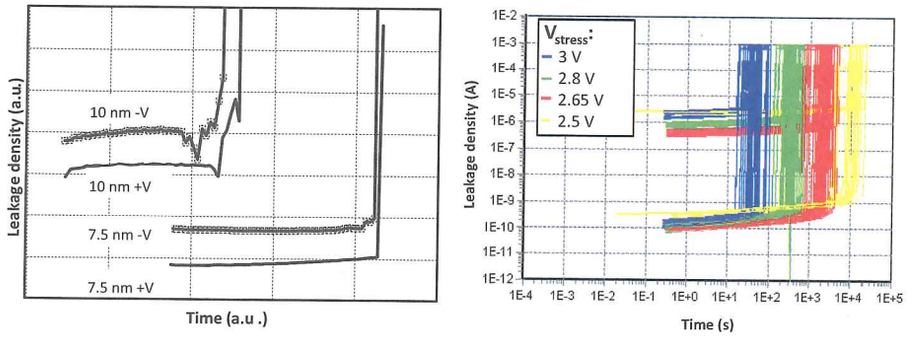

Fig. 20. (Left) Leakage current increase over time caused by dielectric breakdown of a 10 nm thick crystalline ZAZ layer (soft + hard breakdown) compared to a 7.5 nm amorphous layer (only hard breakdown).[19] (Right) breakdown behavior for different bias voltages applied to a production type ZAZ based DRAM capacitor structure.[65]

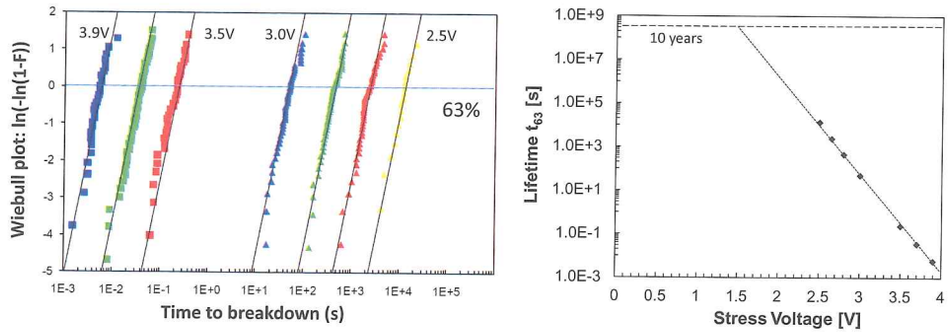

Fig. 21. (Left) Weibull plot of a breakdown lifetime distribution in Figure 20: the failure rate is plotted vs. the lifetime of the device. (Right) The lifetime of a device (from Figure 21 left) that broke down after 63% of similar devices showed a breakdown event (see line) is plotted versus the applied stress voltage. Data points are extrapolated to use voltage of 0.5 V.

operation conditions of $V_{BLH} \approx 0.5$ V (see Figure 21 (right)). Since devices are stressed at elevated temperatures, this should be taken into account for the determination of the overall lifetime. The temperature dependence of the lifetime can be described by Arrhenius behavior, i.e. the underlying mechanism is thermally activated. The extracted thermal activation energies for ZrO_2 thin films vary between 0.7 eV and 1.6 eV.[41] Overall, ZAZ dielectric layers in TiN electrode based capacitor configurations meet the reliability criteria for current DRAM specifications.[41]

AC stress measurements are reported for MIM capacitors with a thin SiO_2 instead of Al_2O_3 interlayer in the middle of the ZrO_2 dielectric.[66] A rectangular 100 Hz signal was applied, varying between the constant

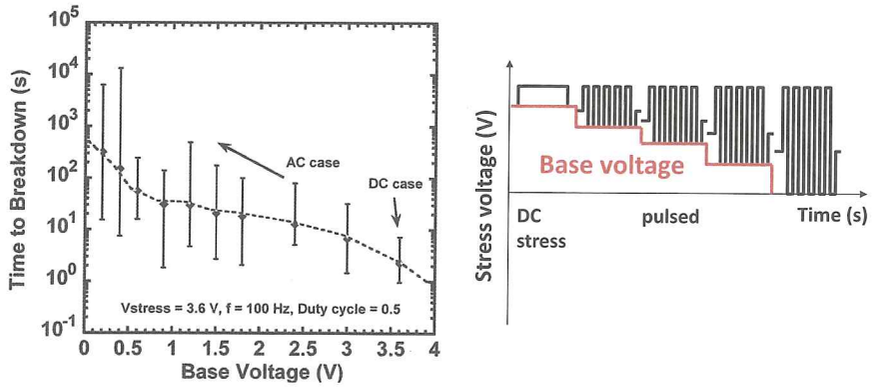

Fig. 22. (Left) Time to breakdown versus base voltage as applied in AC stress condition. The lifetime of the capacitors are improving with lower base voltage. (Right) Schematic overview of pulsing scheme (© 2009 IEEE. Reprinted, with permission, from Ref. 66).

stress voltage of 3.6 V and the base voltage (Figure 22 (right)). The base voltage was lowered in several steps. At each step, a certain number of devices were allowed to breakdown and the average lifetime is extracted (Figure 22 (left)). Overall, for lower base bias conditions an improvement by two to three orders of magnitude in time-to-breakdown is observed. This is very likely due to a reduction of the charge build-up in the dielectric. Furthermore, the frequency dependence of the time-to-breakdown was studied[67] and an improvement for higher test frequencies was found (see Figure 23). The breakdown time increased by two orders of magnitude since charge carriers in the dielectric are more and more unable to follow the higher frequencies and less damage can occur in the dielectric. Since refresh times are in the millisecond range and the clock speed of processors is in the GHz range, a considerable reliability and lifetime margin can be gained under DRAM AC operating bias conditions with this frequency range.

4. Scaling Challenges for DRAM Capacitors

The groundrule for DRAM has been reduced continuously down to 18 nm generations, which resulted in different benefits such as high speed, low power consumption and lower production cost. However, beyond 18 nm generation, there are many technological challenges for further shrinking of the technology. Innovative approaches are necessary to overcome the technological challenges. It is commonly discussed that the scaling limit of DRAM is determined by the capacitor scaling limit.[23] Therefore, the expectation of a scaling limit for the DRAM capacitor implies a scaling limit

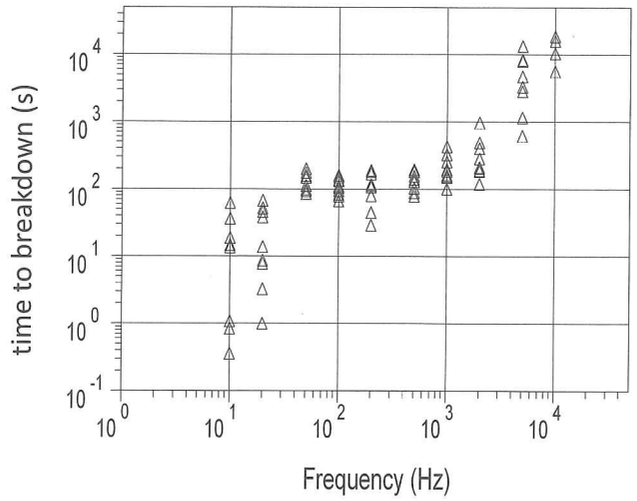

Fig. 23. (Left) Frequency dependence of time-to-breakdown (tbd). The measurements were performed at stress voltage of 3.8 V on ZrO_2 based capacitors.[67]

of future DRAM technologies. A minimum capacitance needs to be obtained to guarantee the functionality of every new DRAM generation. The aspect ratio of the capacitor has been increased and the equivalent oxide thickness has been decreased continuously.

The key question in the discussions on a DRAM capacitor scaling limit is the required minimum cell capacitance to operate DRAM. In fact, the question cannot be answered without discussing the device architecture (e.g. length of the wordlines) and the sensing circuits, which determine the ability to sense the charge of the cell capacitance. Improvements in sensing resulted in a reduction of the required capacitance value from 30 fF/cell in 2000 to 25 fF/cell in 2009 down to 20 fF/cell for the current 18 nm DRAM generations (see Figure 3). Therefore, it is hard to predict the scaling limit of DRAM capacitor without knowledge of the minimum cell capacitance requirement. In the near future, 10 fF/cell might be sufficient to operate DRAM device. If a minimum capacitance value of 10 fF/cell is feasible, further DRAM scaling might be easier. Therefore, a new device architecture or new processes which could improve the capacitor sensing ability can extend the shrinking limits in the roadmap for future DRAM generations.

The second key topic for the DRAM capacitor scaling limit is the maximum cell capacitance that can be manufactured in a future DRAM. The cell capacitance is determined by the CET value and the capacitor area (see chapter 1.3). Up to now, new material and patterning technology made it possible to reduce the CET value and increase the aspect ratio of 3D capacitor

(Figures 4 and 5). Innovative future technologies could reduce the CET value dramatically. For example, it was reported that a $SrTiO_3/Ba_xSr_{1-x}TiO_3$ super lattice can increase the dielectric constant by several orders of magnitude ($\varepsilon_r > 30,000$).[68] Even though the fabrication of a super lattice in a 3D structure is still a technical challenge, perovskite structured $SrRuO_3$ electrodes as a template for super lattice growth of $SrTiO_3/Ba_xSr_{1-x}TiO_3$ could be a possible solution.[69] Considering the worldwide efforts and the high speed of technology evolution, it is also hard to predict the limit of CET scaling and the highest possible aspect ratio of future DRAM structures.

The third and more obvious key question concerning the DRAM capacitor scaling limit is "What is the minimum thickness of DRAM capacitor?" Each 3D cell capacitor in a cup structure is composed of two bottom electrodes, four layers of dielectrics and four layers of top electrodes (10 layers, see Figure 16). The maximum available space for this film stack decreases for smaller groundrule. Each electrode and dielectric layer requires a certain thickness for best performance in the capacitor structure (see Figure 15 for the trend of leakage current density for different dielectric thickness). If the overall thickness requirement for the DRAM capacitor is thicker than the available space determined by the groundrule, the physical thickness would be the limiting factor for future scaling. One possibility to overcome this issue would be the introduction of a pillar capacitor with five layers (one bottom electrode, two dielectric layers, two top electrode layers) instead of a cup structure with ten layers (see Figure 7). This would lead to a drastic increase of the aspect ratio of the capacitor to compensate for the reduced capacitor footprint. But even for the pillar structure a limitation in the available space is critical. The limit will only be shifted to smaller groundrules. Therefore, a thickness scaling of the dielectric layer and of the electrode is the key challenge to overcome DRAM capacitor scaling limit.

In these discussions, only optimal parameters are mentioned so far. In addition, variations in the lithography of the capacitor pattern layout and non-perfect taper angles of the capacitor structure caused during dry etching of the initial trench structure to form the capacitor (see Figure 16) hinder an optimal structure formation. Furthermore, the conformality of the dielectric and the electrode layer is slightly reduced due to the high aspect ratio of the capacitor structure. Hence, the allowed film thickness for each dielectric or electrode layer might be lower than maximum space allowed by the groundrule.

The final key question about the DRAM capacitor scaling limit is "What is the advantage of DRAM capacitor scaling?" It should be noticed that the main purpose of the device scaling is to reduce production cost. Device scaling has increased the number of chips on the same wafer, which has reduced the cost per chip. If the cost of the scaling is higher than the cost reduction, the scaling has no economic advantage anymore. In this case, the driving force for the scaling would diminish. Device capacitor scaling is accompanied by a high aspect ratio etch, a conformal deposition process, thickness scaling, and a new high-*k*/high work function material. All of them increase the production cost of the DRAM.[70] Therefore, new, cost effective technologies are necessary to extend the DRAM capacitor scaling limit. Otherwise, the first scaling limit for the DRAM capacitor will not be a physical limit, but a cost limit.

Acknowledgements

The authors gratefully acknowledge Steve Knebel for fruitful discussions and electrical characterization and Tony Schenk for carefully reviewing the chapter and checking the symbols and formulas.

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