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Data Center Power System Emulation and GaN-Based High-Efficiency Rectifier with Reactive Power Regulation

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I am submitting herewith a dissertation written by Jingjing Sun entitled "Data Center Power System Emulation and GaN-Based High-Efficiency Rectifier with Reactive Power Regulation." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

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Data Center Power System Emulation and GaN-Based High-Efficiency Rectifier with Reactive Power Regulation

A Dissertation Presented for the

Doctor of Philosophy

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To my Mom

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Abstract

Data centers are indispensable for today's computing and networking society, which has a considerable power consumption and significant impact on power system. Meanwhile, the average energy usage efficiency of data centers is still not high, leading to significant power loss and system cost.

In this dissertation, effective methods are proposed to investigate the data center load characteristics, improve data center power usage efficiency, and reduce the system cost.

First, a dynamic power model of a typical data center ac power system is proposed, which is complete and able to predict the data center's dynamic performance. Also, a converter-based data center power emulator serving as an all-in-one load is developed. The power emulator has been verified experimentally in a regional network in the HTB. Dynamic performances during voltage sag events and server load variations are emulated and discussed.

Then, a gallium nitride (GaN) based critical conduction mode (CRM) totem-pole power factor correction (PFC) rectifier is designed as the single-phase front-end rectifier to improve the data center power distribution efficiency. Zero voltage switching (ZVS) modulation with ZVS time margin is developed, and a digital variable ON-time control is employed. A hardware prototype of the PFC rectifier is built and demonstrated with high efficiency. To achieve low input current total harmonic distortion (iTHD), current distortion mechanisms are analyzed, and effective solutions for mitigating current distortion are proposed and validated with experiments.

The idea of providing reactive power compensation with the rack-level GaN-based front-end rectifiers is proposed for data centers to reduce data center's power loss and system cost. Full-range ZVS modulation is extended into non-unity PF condition and a GaN-based T-type totem-pole rectifier with reactive power control is proposed. A hardware prototype of the

proposed rectifier is built and demonstrated experimentally with high power efficiency and flexible reactive power regulation. Experimental emulation of the whole data center system also validates the capability of reactive power compensation by the front-end rectifiers, which can also generate or consume more reactive power to achieve flexible PF regulation and help support the power system.

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Chapter 1

Introduction

1.1 Background of Data Centers

Global internet data tripled between 2015 and 2019, and is expected to double again by 2022 [2, 25]. Most of the data makes use of data centers for generation, processing, storage, transmission, and distribution. As shown in Figure 1.1, the worldwide data center IP traffic is expected to reach 20.6 zettabytes by 2021, and the installed workloads exhibit 2.5-fold growth from 2016 to 2021. The increasing computing and networking data has driven construction of data centers over the past decade, leading to more than $200 billion global cost in 2020 [26].

1.1.1 Load Performance

Rapid expansion results in widespread distribution of data centers. As presented in Figure 1.2, data centers have been established all over the nation in the U.S., consuming 70 billion kilowatt hours (kWh) of energy in 2016 [8]. Also, the global annual electricity demand by data centers has increased to 400 TWh in 2018, accounting for around 2% of the world's energy use [27]. The power consumption of data centers is anticipated to grow continuously with the increase of the internet traffic.

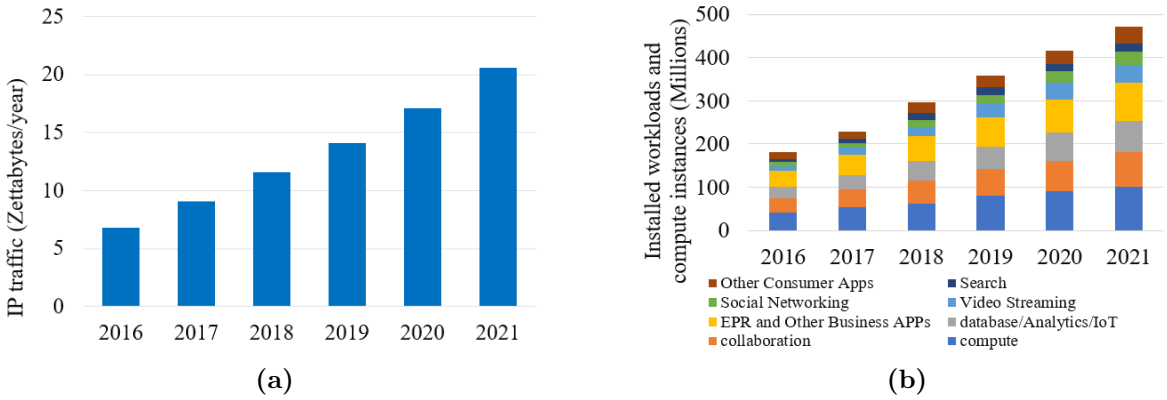


Figure 1.1: (a) Global data center internet protocol (IP) traffic growth; (b) Global data center workloads and compute instances by applications [2].

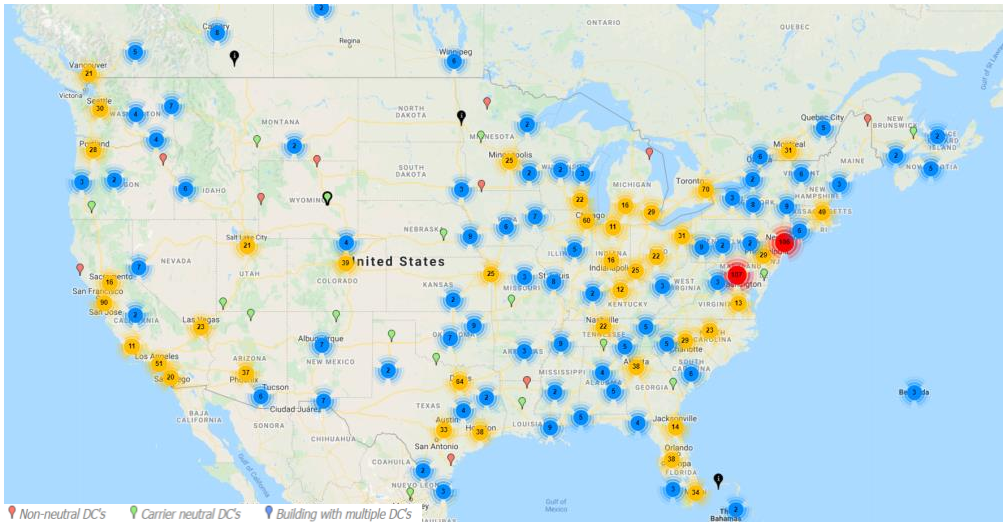


Figure 1.2: Data center colocation in the U.S. [3].

Apart from a large energy consumer, data centers are also complicated systems with a high density of power electronics (PE) and controls [4]. As shown in Figure 1.3, a typical data center is composed of a power supply system, cooling system, backup energy, lighting system, server loads, etc., which contains several PE converters in different stages. Correspondingly, the control strategy is complex in order to enable the cooperation of different power components and ensure normal system operation [28].

Compared with conventional power loads, a data center has distinct characteristics, which significantly influence the power system. On one hand, a data center exhibits a dynamic server load profile. Figure 1.4 shows an example utilization condition of a central processing unit (CPU), which performs as a fast dynamic load with high slew rate. Such dynamic power draw tends to cause apparent power demand fluctuations of the data center in a short time [29]. On the other hand, grid disturbances and contingencies, like a voltage sag event, result in reconfigured structure and operation mode transition within the data center, leading to transient response on the power grid [28].

1.1.2 Energy Efficiency

The large magnitude of energy consumption becomes particularly problematic when considering the end use of the power in data centers. Figure 1.5 presents the traditional ac power distribution system in data centers. Before distributed to the end server loads, the source power is processed by the electrical power supply system, including the centralized uninterrupted power supply (UPS), power distribution unit (PDU), rack-level power supply units (PSUs), and voltage regulation modules (VRMs) in server boards [4]. Particularly, the centralized UPS and the server rack power supplies have lower power efficiency, leading to around $22\% - 27\%$ electrical loss during the stage-by-stage power conversion. Meanwhile, another large segment of the source power is supplied for the cooling system, which also generates power loss [30]. In addition, non-essential loads like lighting also consume some power.

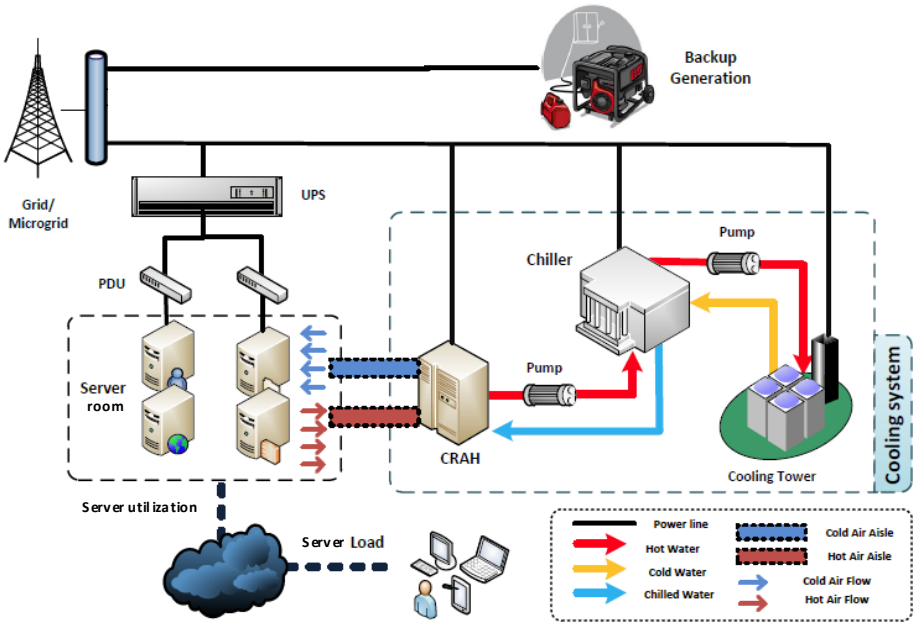


Figure 1.3: Structure of a typical data center system [4].

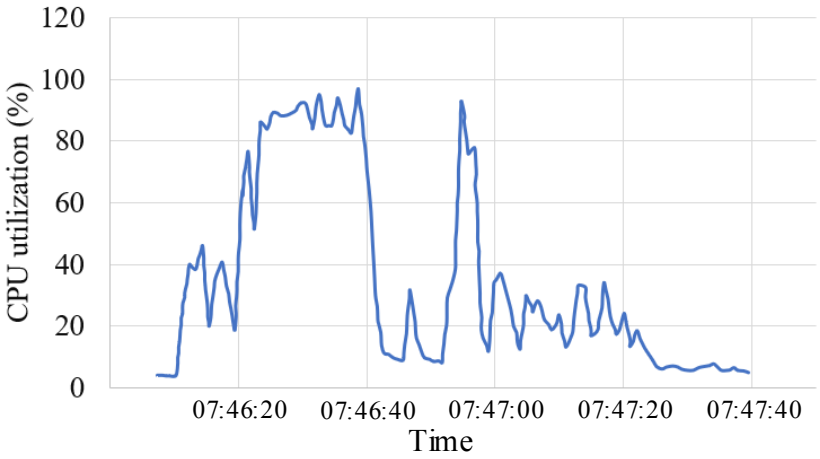


Figure 1.4: CPU utilization within 100 s [5].

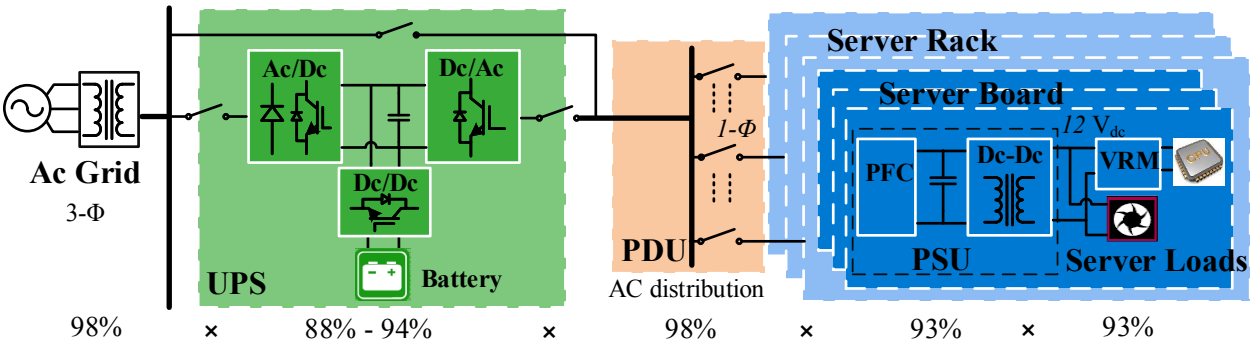


Figure 1.5: Traditional data center ac power distribution system [6, 7].

Two important figure-of-merits (FOMs), known as the power usage effectiveness (PUE) and the server power usage effectiveness (SPUE), are often used to evaluate the energy usage efficiency in data centers [31]. PUE represents the facility efficiency,

$$\text{PUE} = \frac{\text{Total Facility Power}}{\text{Information Technology (IT) Equipment Power}} \tag{1.1}$$

As shown in Figure 1.6, the worldwide data centers' average PUE has kept decreasing over the years and leveled at 1.6 since 2014, while the giant internet company Google's data centers have achieved PUE down to 1.1 [6, 7].

However, PUE cannot truly reflect the server power usage efficiency, as the IT equipment accounts for the overhead of infrastructures at the server level, *i.e.,* PSUs, VRMs, and server cooling fans. Accordingly, SPUE is developed to evaluate the server efficiency.

$$\text{SPUE} = \frac{\text{IT Equipment Power}}{\text{Computation Hardware Power}} \tag{1.2}$$

Currently, worldwide data centers have SPUEs ranging from 1.2 to 1.6 [32]. As illustrated in Figure 1.5, for each 10 W power sent to the IT equipment, only 8.5 W power can be used for the end servers. Efficiency of the server rack power supplies including the front-end PFC rectifier, the dc-dc isolated converter and VRM needs to be improved to achieve a lower SPUE.

Combining PUE and SPUE, the data center energy usage efficiency is estimated as

$$\text{Efficiency} = \frac{1}{\text{PUE}} \times \frac{1}{\text{SPUE}} \tag{1.3}$$

Figure 1.7 illustrates the power breakdown of a typical data center ac power distribution system. On average, only half of the total power is transferred to the end server loads. Approximately 32% of the power is used for the cooling system and 16% of the power is lost as electrical loss during the power distribution.

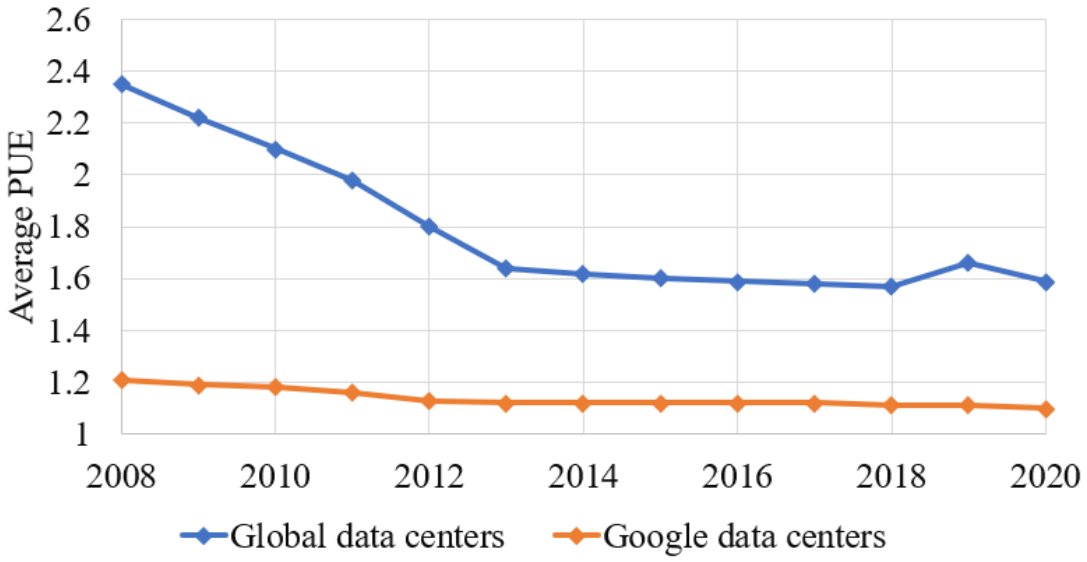


Figure 1.6: Average PUEs of data centers [6, 7].

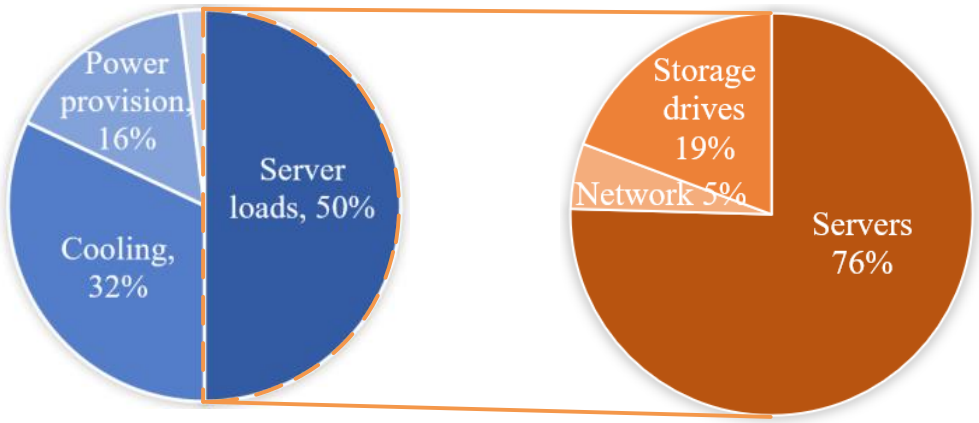


Figure 1.7: Power breakdown of a typical data center [8].

Cooling system and power supply system are two major parts in the data center power distribution system. Various cooling solutions have been developed, among which air cooling is the most conventional and popular approach [33]. As presented in Figure 1.8, a standard configuration of the air cooling system is composed of air-side loop including the computer room air handler (CRAH) and server fans in racks, and water-side loop containing chiller-CRAH water loop and chiller-cooling tower water loop [9]. To improve the energy efficiency, some advanced data centers use the cold water from natural resources to replace the water-side loop, or directly inject the cold air to the server room, *e.g.,* the Google data center in Hamina, Finland uses the ocean water to produce the cold air [34].

1.1.3 Power Distribution Architecture

For the power supply system, there are three different types. The first architecture is the ac power distribution system with a centralized UPS, as shown in Figure 1.5. Traditionally, the system operates in double-conversion mode, where the UPS is always online to condition the input power and send the regulated power to the following power supplies [28]. As aforementioned, such multiple power conversions cause significant power loss. To enhance the power distribution efficiency, an alternative UPS structure, known as eco-mode or line-interactive UPS is developed [35]. The UPS is bypassed in the normal operation to avoid the "double-conversion" power processing loss, but remains active with small power to minimize the response time in the event of a power transient. When input power problems are detected, the UPS switches back to double-conversion mode, and it supports the server loads.

The second structure, made by Google, eliminates the centralized UPS, and adopts low-voltage battery backup on each server board to conduct the distributed UPS functionality [36]. As illustrated in Figure 1.9, this approach avoids the second conversion of the ac power and reduces power distribution loss by 10%. However, the distributed battery and the according implementation result in increased initial investment and implementation complexity, which is prohibitive for smaller companies or data centers.

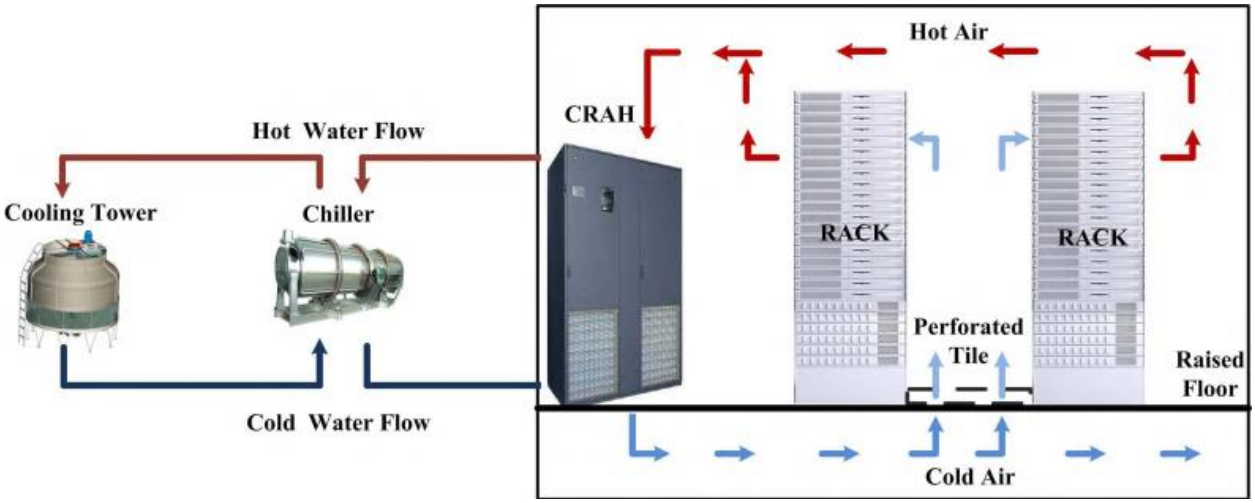


Figure 1.8: Typical air cooling system in data centers [9].

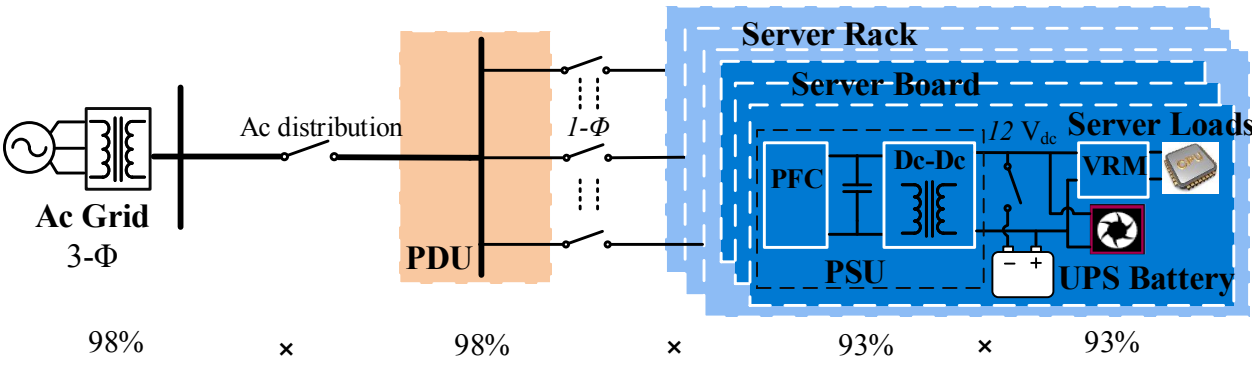


Figure 1.9: Google data center ac power distribution system with distributed UPSs.

The third type is the recently proposed dc power distribution system, as presented in Figure 1.10. The centralized dc-ac stage and the distributed ac-dc stage are eliminated from the system. Instead, the input ac power is rectified into a 350 V − 400 V dc power that is distributed to the server board directly. Because of the simplified structure, the system has the advantages of higher power conversion efficiency, lower wiring conduction loss, and easier connection to renewable energy sources [37]. Reduced capital cost, smaller overall footprint, and increased reliability are also promised [38]. Although dc power distribution data center systems have been demonstrated, there are some obstacles standing in the way of wider adoption of the system [39]. Commercial power supplies, air conditioning units, fire protection equipment, and building controls that run on dc are required. The absence of related standards and lack of operation experience also obstruct the implementation of the dc system.

1.1.4 Reactive Power

Power quality is another important qualification of data centers, especially power factor (PF) and current total harmonic distortion (THD). Generally, for a nonlinear load, the terminal power is composed of the real power P, the displacement reactive power Q, and the distortion reactive power D [40].

$$\begin{cases} P = V_{rms} I_{1,rms} \cos\phi \\ Q = V_{rms} I_{1,rms} \sin\phi \\ D = V_{rms} \sqrt{\sum_{n=2}^{\infty} I_{n,rms}^2} \end{cases} \tag{1.4}$$

where $I_{1,rms}$ is the RMS value of the fundamental current, $I_{n,rms}$ is the RMS value of the n_{th} order harmonic current, and ϕ is the phase shift between the voltage and fundamental current. The final power factor is calculated as

$$\mathrm{PF} = \frac{\cos\phi}{\sqrt{1 + \mathrm{iTHD}^2}} \tag{1.5}$$

where $\mathrm{iTHD} = \sqrt{\sum_{n=2}^{\infty} I_{n,rms}^2} / I_{1,rms}$ is the current THD.

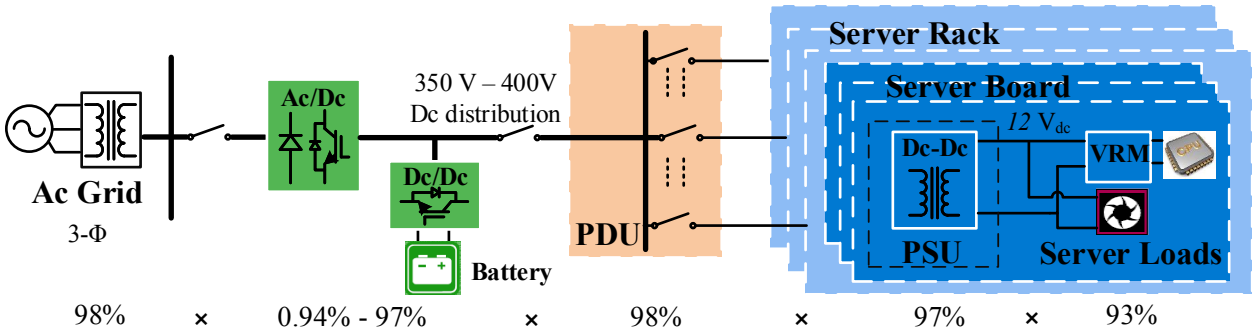


Figure 1.10: Data center dc power distribution system.

As previously discussed, a data center is a complicated system with a high density of power electronics, which has a nonlinear load performance. Figure 1.11 shows the measured terminal voltage and current waveforms of a data center. As can be seen, both displacement and distortion reactive power exist in the data center terminal power, leading to 0.96 power factor, 21% current THD, and 3% voltage THD [10]. For a traditional data center with on-line UPS, the power factor is in the range of 0.9-0.98, and the current THD is around 20% [41]. Voltage distortion may also appear due to the harmonic currents.

There are several factors contributing to the reactive power in data centers. First, inductive loads, such as induction motors in the cooling system, result in lagging current and displacement reactive power. Second, the nonlinear load due to power electronics, *e.g.,* the six-pulse diode rectifier used in the UPS or in the air conditioner's variable frequency drive (VFD), generates harmonic current and reactive power, as illustrated in Figure 1.12. Although rack PSUs contain active power converters, they generate almost no reactive power because of the front-end PFC rectifier. In addition, equipment like light ballasts also generates reactive power [42].

The reactive power increases the total power demand and generates more loss and heat in data centers, accelerating the aging of wiring and electrical equipment. To regulate the power quality, grid standards and penalties are published [43, 44], and data center operators need to compensate the reactive power to meet the constraints. Typically, a power compensator, such as the static VAR compensator (SVC) or static synchronous compensator (STATCOM), is installed in parallel with the data center to correct the terminal power [45]. Though improving the power quality issue, extra power loss and capital investment are caused by the power compensator. It is calculated that, for a 10 MW data center system with PF = 0.97 during the normal operation, a STATCOM with power rating > 2510 kVA is required. The power loss induced by the STATCOM is about 99.5 kW, accounting for almost 1% of the total data center power, and the initial cost of the STATCOM is around $\$210,000$ [46].

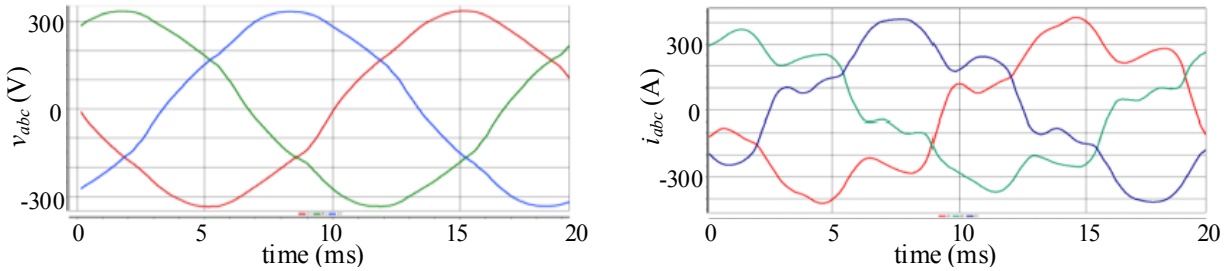


Figure 1.11: Measured data center terminal voltage and current [10]. (a) Terminal voltage waveform; (b) Terminal current waveform.

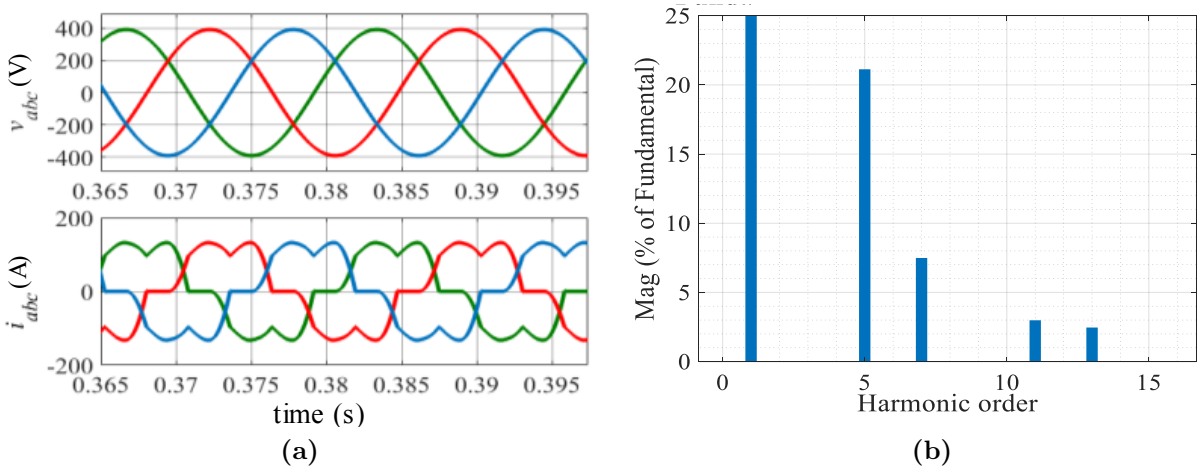


Figure 1.12: (a) Voltage and current waveforms of a six-pulse diode rectifier; (b) Current waveform FFT analysis of a six-pulse diode rectifier.

1.2 Motivation and Strategy

1.2.1 Motivation

Based on the above introduction, several characteristics of current data centers are observed.

(1) Data centers have a considerable power consumption and wide-range distribution, performing as a large electric load in the power grid.

(2) Data centers' complicated systems with a high density of power electronics, resulting in a nonlinear load and significant impact on the power grid.

(3) For average data centers, the energy usage efficiency is low, with only half of the input power used for the end server loads. High-efficiency power supplies are required to improve the data center power usage efficiency.

(4) Although advanced power distribution systems (such as the ac distributed power system and the dc power system) are able to increase efficiency, they are still prohibitive for most data centers due to high capital cost and lack of regulation standards. Currently, the ac power distribution system with line-interactive UPS is popular in the market.

(5) Reactive power compensation is indispensable in data centers, but conventional power compensators lead to high power loss and extra capital investment.

For power system studies, it is important to investigate data center's load characteristics and evaluate the dynamic performance of the power grid. For data centers, advanced high-efficiency server rack power supplies are required to improve the power distribution efficiency. Also, innovative solutions for reactive power compensation need to be investigated to increase the system energy usage efficiency.

With the focus on the data center ac power distribution system, this dissertation aims to study the effective methods to characterize the data center load performance and improve the system energy usage efficiency.

1.2.2 Strategy

1.2.2.1 Dynamic Power Load Model and Simulator/Emulator

Power system modeling is required to evaluate the grid voltage stability and transient stability performance. Especially, the accuracy of the power load model has been emphasized, and efforts have been made to develop effective dynamic load models [47, 48, 49, 50]. Meanwhile, to validate novel power system control or devices, software simulation [11, 51] and hardware emulation [48, 52] are normally performed before the actual test. Therefore, developing the data center dynamic model and the corresponding simulator/emulator to carry out the related grid test is one potential approach to investigate the data center load characteristics and to assess the power grid dynamic performance.

1.2.2.2 Wide Bandgap (WBG) Devices and Soft Switching Techniques

High efficiency and high power density are two factors driving the power supply technology innovation and evolution. Traditional Silicon (Si)-based ac-dc power supplies have been used for many years, with limited performance of up to 95% power efficiency and 50 W/in^3 power density [31]. The appearance of WBG power devices provides new opportunities for advancing the power supply design. Particularly, the emergence of 650 V gallium nitride (GaN) devices, which have lower on-resistance, faster switching speed, higher thermal performance, and no body diode reverse recovery loss, is changing the server power supply design [53, 54]. Meanwhile, soft switching techniques have been developed to reduce the switching loss and improve the switching frequency for higher power density [55]. For the data center power supply, research efforts will be made on utilizing GaN devices and soft switching techniques to achieve higher converter efficiency and power density.

1.2.2.3 Reactive Power Compensation in Server Rack Front-End Rectifiers

A traditional reactive power compensator induces large power loss and increases the data center capital investment. To decrease the data center power loss and system cost, efficient and cost-effective alternatives are desired for reactive power compensation. Distributed on server racks, the front-end rectifiers are able to compensate the data center reactive power as

a replacement of the conventional power compensator. A similar concept has been proposed for electric vehicles (EVs) to achieve vehicle-to-grid (V2G) reactive power operation by using the on-board single-phase bidirectional charger [21, 56]. It is demonstrated the on-board charger is able to provide both reactive power for grid compensation and active power for battery charging/discharging simultaneously with stable dynamic response. For data centers, impacts of using GaN-based front-end rectifiers for reactive power compensation need to be analyzed in terms of the system cost and power loss.

1.3 Dissertation Outline

The outline of this dissertation is as follows:

Chapter 2 presents a literature review of the data center power model and simulator/emulator, single-phase ac-dc rectifier topologies, soft switching techniques, control strategies, and reactive power compensation.

Chapter 3 proposes a complete data center dynamic power model for accurate prediction of the data center load characteristics. Also, a data center power emulator serving as an all-in-one load is developed based on a unique HTB platform to evaluate the power system dynamic performance.

Chapter 4 designs a high-efficiency single-phase GaN-based power factor correction (PFC) rectifier for the data center front-end power supply. An adaptive ZVS modulation with ZVS time margin is proposed, and full-line-cycle ZVS is achieved by employing the digital-based variable on-time control.

Chapter 5 explores the current distortion issues of the GaN-based PFC rectifier. Reasons for the line-cycle current distortion and the ac-line zero-crossing current spike are identified. Effective approaches are proposed to mitigate the current distortion and maintain stable ZVS control in a noise-susceptible environment.

Chapter 6 proposes the idea of using GaN-based front-end rectifiers for reactive power compensation in data centers. Advantages of the idea in terms of data center system cost

and power loss are evaluated, and a GaN-based T-type totem-pole rectifier is proposed. Full-line-cycle ZVS modulation at non-unity PF is proposed and the associated control strategy is developed.

Chapter 7 presents the experimental verification of using GaN-based front-end rectifiers for reactive power compensation in data center system. A prototype of the GaN-based T-type totem-pole rectifier is designed and demonstrated with full-range ZVS operation and flexible reactive power regulation. The data center power emulator is modified and validated experimentally in the HTB with reactive power regulation.

Chapter 8 concludes this work and presents the future work.

Chapter 2

Literature Review

This chapter reviews the state-of-the-art of data center power load models, simulation and emulation tools, circuit topologies of single-phase rectifiers, soft-switching techniques, as well as control strategies, current distortion issues, and reactive power compensation.

2.1 Data Center Power Model and Simulator/Emulator

2.1.1 Data Center Power Model

A power load model is critical for investigating the data center's load characteristics and its impact on the power grid. To ensure accurate modeling results, the power model is required to cover different power components and is capable of predicting dynamic power performance of the data center system. Researchers have developed several data center power models, which can be generally divided into four categories.

The first kind of model focuses on one or two aspects of the data center that is of interest for the research. In [57], a holistic cloud data center energy consumption model for IT loads is proposed including CPU, memory, disk, and network interface card as well as the application characteristics. In [58], a cooling system model is developed to reduce the total data center energy consumption without violating temperature constraints. Works in [59, 60] concentrate more on building the server room model, containing the server power,

room temperature, and airflow demand. However, these models are incomplete in terms of reflecting the overall performance of the data center power distribution system.

The second type of model is based on linear calculation of the whole system [29, 61]. For example, a coherent data center model is proposed in [61] that covers the complete facilities including the surrounding power grid, electrical infrastructure, cooling system, server room, and server loads. A simulation model is established based on linear calculation, which is complete and able to capture the data center static operating states. However, lacking detailed circuit modeling, this model cannot predict dynamic operation performance during transient conditions.

The third group of models is data driven, where pre-recorded data from an existing data center are imported as the input parameter to estimate the data center performance [62, 63, 64]. Such models are highly dependent on the specified data centers, which cannot be flexibly applied for various operation states. Also, the provided data is usually not openly available.

The last category builds circuit models of various power components for dynamic simulation of the data center [65, 66]. In [65], to understand the influence of data center dynamic server load on the regional grid and the impact of grid transient faults on data center performance, a data center power circuit model is built in Matlab Simulink. Though dynamic operation can be simulated, the established model is oversimplified, *i.e.,* using a resistor to represent the server load or RL impedance for cooling load. Also, the PSU converters and closed-loop controls are not modeled, which cannot ensure the accuracy of the simulation results.

2.1.2 Simulation and Emulation Tools for Power System

Simulation and emulation tools are important to validate novel power controls or new devices before actual testing in the power grid. Also, they can be used to evaluate system voltage stability and transient stability. Since a data center is a large dynamic electric load, the corresponding simulator and/or emulator are required to help evaluate the dynamic performance of the power grid.

There are several digital simulation tools targeting different power circuits [11]. Simulation platforms like power system simulation for engineering (PSS/E) and transient security assessment tool (TSAT), are based on second-order integration time step and are suitable for large-scale power systems, where only slow electromechanical behaviors are concerned. The electromagnetic transient program (EMTP) based simulation tools, such as PSCAD, are implemented with millisecond-level integration time step and are often used in detailed model simulation representing nonlinear behaviors. Matlab/Simulink is a generic tool to simulate smaller scale power systems and electronic circuits in different time scales. Simulators like Saber and LTspice, are preferable for detailed simulation of semiconductor devices and high-frequency circuits.

With the appearance of advanced microprocessors, real-time digital simulators, such as RTDS [51] and Opal-RT [67] have been developed, which combine the digital simulation and physical test together to form a hardware-in-the-loop (HIL) emulation [68]. The HIL technique has been widely used in power system study in applications of microgrids, motor drives, wind turbines, etc. With parallel computation architectures using dedicated field-programmable gate arrays (FPGAs) and/or CPUs, large systems can be emulated in real time without the requirement of actual hardware experimental platform [69]. HIL can also be extended to verify an actual power device under test (DUT) by connecting the DUT through a power amplifier and maintaining the rest of the controllers and power components simulated digitally in the software, forming a power HIL (PHIL) test platform [70].

Analog-based system emulation is another area, where down-scaled power system and hardware-based grid testbed are the main approaches to emulate a system or test certain controls or devices. The analog-based emulation tracks back to the 1920s, where a miniature ac grid of down-scaled power components was built by General Electric (GE) [71]. Modern hardware-based emulators like national renewable energy laboratory's (NREL) energy systems integration facility (ESIF) [52] and the consortium for electric reliability technology solutions' (CERTS) microgrid testing platform [72] have been developed to study power system performance.

Compared with analog-based emulators, digital-based simulators/emulators are relatively cheaper, smaller, and easy to be installed or modified. However, digital simulation/emulation

fully depends on numerical computation, thus suffering from numerical instability and convergence issues. Also, digital-based platforms tend to ignore practical conditions such as sensing error, communication time delay, control bandwidth, and cannot reflect some physical nonlinear characteristics like switching noise and electromagnetic field interference (EMI) [73, 74]. Although analog-based emulators are more expensive, heavier, less flexible and accessible, numerical instability or convergence issues are unlikely to occur, and the testing results are more realistic and convincing [75].

To overcome the issues of digital simulators and conventional hardware-based emulators, a unique ultra-wide-area transmission network emulator, also named as hardware testbed (HTB) platform, has been developed in the NSF/DOE Engineering Research Center, CURENT [48, 76, 12]. As shown in Figure 2.1, the HTB is a power electronics based reconfigurable real-time grid emulator, where many down-scaled voltage source inverters (VSIs) are used to model various power components and implement the controls. All VSIs are connected to a common dc bus, and controlled by individual digital signal processors (DSPs) and communication CAN bus. By digitally programming the interconnected VSIs, different grid infrastructures and regional or large-scale power networks can be emulated, including generators, wind farms, battery energy storage systems (BESSs), power loads, etc.

The HTB has real-time measurement, control, and communication systems, as illustrated in Figure 2.2. The hardware converters are connected with the cabinet controllers (CompactRIO) and the central controller (LabVIEW) through the built-in DSPs, communication CAN bus, and ethernet. Depending on the emulated system and control, the cabinet controllers are configured to access certain data, which is collected by the installed sensors, such as potential transformers (PTs), current transformers (CTs), frequency disturbance recorders (FDRs) and phasor measurement units (PMUs). With its reconfigurable structure and fast time response, the HTB works as a versatile platform to perform different real power tests and emulate the power grid with precise transient response and broad time scales ranging from µs to hundreds of s.

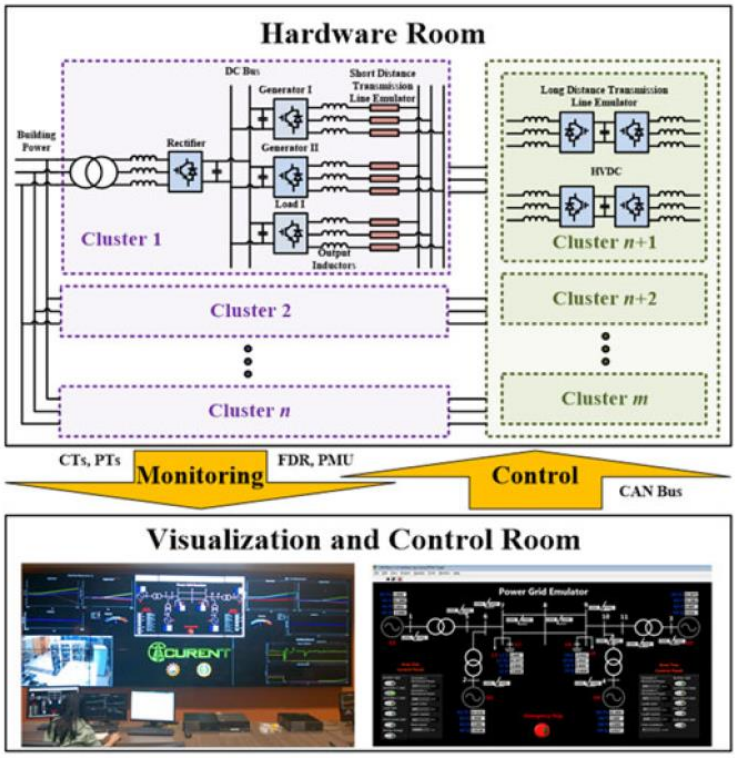


Figure 2.1: Architecture of the CURENT HTB [11].

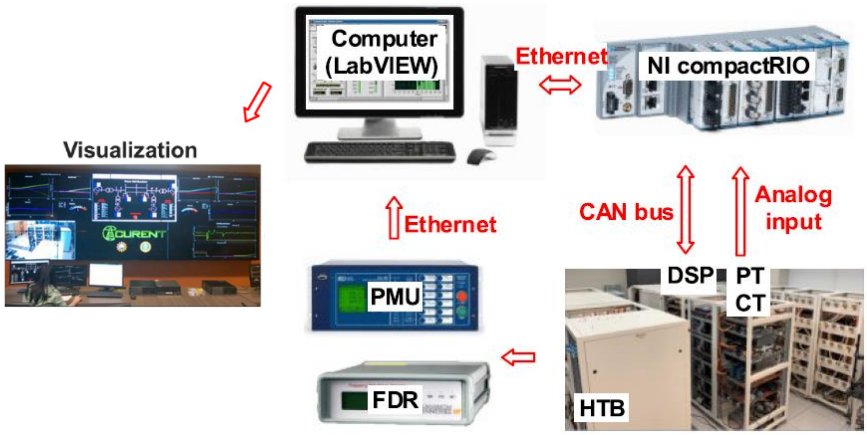


Figure 2.2: measurement, control and communication system in the HTB [12].

In comparison with digital emulators, the HTB requires reduced computational resources and is less likely to have numerical issues. Compared with other down-scaled power systems or hardware-based emulators, the HTB system is more flexible because VSIs can be reprogrammed and reconfigured into various devices and power conditions. Based on the HTB, several power load emulators have been developed, *e.g.,* ZIP load [48], induction motor load [77], variable frequency drive (VFD) based load [78], and battery energy storage system (BESS) load [79].

2.2 Topologies of Single-Phase Front-End Rectifier

Single-phase front-end rectifier is required in the data center power supply to rectify the voltage, correct the PF and improve current THD. This section provides a literature review of the state-of-the-art of the front-end rectifier topologies. Advantages and drawbacks of different topologies in terms of power efficiency, part count, voltage and current stress of the semiconductor devices are discussed.

The simplest rectifier circuit combines a diode full bridge and a dc-dc converter, as illustrated in Figure 2.3(a), where the diode bridge is responsible for rectifying the ac voltage to dc voltage, and the subsequent dc-dc converter is in charge of adjusting the dc voltage. Depending on the application, the dc-dc circuit can be a boost converter [80], buck converter [81], buck-boost converter [82], Cuk converter [83], SEPIC converter [84], flyback converter [85], etc.

In the data center market, the boost PFC converter is widely used in the front-end rectifier, as shown in Figure 2.3(b). Compared to other circuits, the boost PFC has advantages in simple topology, low part count, and continuous input current, which leads to smaller input filter, high PF and low current THD with a simple control method [86]. However, the output dc voltage should be higher than the peak ac voltage, *e.g.,* v_{dc} is greater than 380 V − 400 V in data center applications with $>$ 200 Vac input. Such high voltage stress becomes an obstacle in applications where low-voltage output or low-voltage devices are preferred.

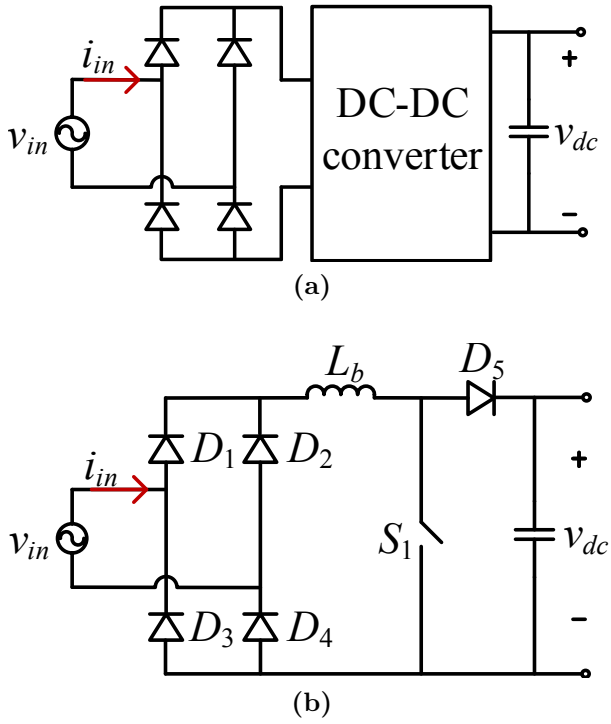


Figure 2.3: (a) Diode bridge based PFC rectifier; (b) Boost PFC rectifier.

Buck, buck-boost, and flyback PFC rectifiers are the other three circuits with simple topology and low part count. Although the buck PFC rectifier has low device voltage stress and high efficiency at low line voltage, it suffers from dead angle where the input current cannot be shaped when $|v_{in}| < v_{dc}$, leading to increased current THD and low PF. Buck-boost PFC rectifier is able to avoid the dead angle, and regulate the voltage up and down. However, it has a relatively low power efficiency due to indirect energy transfer compared with buck or boost PFCs. Flyback PFC rectifier is advantageous in galvanic isolation and has no dead angle. Nevertheless, the flyback PFC incurs high voltage stress in the semiconductor device and circulating energy due to leakage inductance and parasitic capacitance. Also, the input current of buck PFC, buck-boost PFC, and flyback PFC are discontinuous, which requires a larger input filter. Therefore, the diode-bridge buck, buck-boost, and flyback PFC rectifiers are more popular in low-power and low-voltage applications like light-emitting diode (LED) light driver [87] and notebook adapter [88]. Other diode bridge based PFC rectifiers, such as Cuk PFC and SEPIC PFC, perform inferior to the aforementioned topologies, suffering from additional components and higher loss.

No matter in which topology, rectifiers with diode full bridge cause high conduction loss, and are no longer attractive for high-efficiency front-end rectifiers. In order to remove the diode bridge, several bridgeless PFC rectifiers have been developed [89, 90], such as bridgeless buck PFC [91, 92, 93], bridgeless buck-boost PFC [94, 95, 96], bridgeless flyback PFC [97, 98], bridgeless SEPIC PFC [84, 99, 100, 101], bridgeless Cuk PFC [83, 102, 103, 104], and bridgeless boost PFC [80, 105, 106, 107].

Bridgeless buck type PFC rectifiers still exhibit dead angle, which greatly deteriorates the PF and input current THD. To remove the dead angle, the bridgeless buck PFCs proposed in [91] and [93] are integrated with a flyback circuit. Despite the fact that the current THD limit is satisfied, an extra auxiliary circuit is required, and the converter efficiency is below 90%. In [108] and [109], the buck PFC is incorporated with a buck-boost circuit with critical conduction mode (CRM) operation and variable on-time control. Although dead angle is eliminated and the rectifier efficiency is up to 96%, the control implementation is complicated which requires two sets of control circuits for different modes. In [98], a bridgeless flyback PFC rectifier is developed based on the dc-dc flyback circuit by adding an active switch

on the primary side, and a diode plus a winding on the secondary side. However, the flyback PFC still suffers from high voltage stress on the main switch and high switching loss, leading to 89% power efficiency. Bridgeless buck-boost PFC rectifiers proposed in [94] and [95] are composed of two identical buck-boost circuits that operate alternatively in different half line cycles. Although the rectifiers are demonstrated with high power factor and low current THD at output power up to 800 W, they contain 9 power components, and the efficiencies are lower than 94%. Inherently offering voltage buck-boost capability and a continuous input current, various bridgeless SEPIC and CuK PFC rectifiers are also derived [99, 100, 101, 102, 103, 104]. Nevertheless, these rectifier topologies have drawbacks including too many passive components, floating output load terminals, high device current stress, high circulating current, and low efficiency.

Advantageous in its simple circuit, high efficiency, high PF and low current THD, the bridgeless boost type PFC rectifier has been extensively investigated, as shown in Figure 2.4. Figure 2.4(a) is the basic bridgeless boost PFC, where two diodes are eliminated compared to the conventional boost PFC, resulting in reduced conduction loss. Nevertheless, due to the high diode forward current and high output voltage, the diodes have severe reverse-recovery loss. Also, this topology suffers from significant common-mode (CM) noise. During the positive half line cycle, $L_b - D_1 - S_1$ conducts, and the output ground is connected to the ac source through switch S_2; whereas, during the negative half cycle, $L_b - D_2 - S_2$ becomes active, and the output ground is connected with the ac source via S_1 with a high-frequency pulsating voltage. Such pulsating voltage has high magnitude of the output voltage, and charges and discharges the equivalent parasitic capacitance between the ac line ground and the output ground, leading to a considerable CM noise [110, 111].

In order to suppress the CM noise, the basic bridgeless boost PFC is modified by adding two more diodes, as shown in Figure 2.4(b) and Figure 2.4(c). For both topologies, switches S_1 and S_2 operate in the positive half line cycle and negative half line cycle, respectively, D_1 and D_2 are fast-recovery diodes, and D_3 and D_4 are slow-recovery diodes. For the boost PFC with bidirectional switch, the ac source is connected to the output ground through D_4 during the positive half cycle, and during the negative half cycle, the ac source is connected to the output positive terminal through D_3. In the dual boost bridgeless PFC, the ac source

is always connected to the output ground via D_4 in the positive half cycle and D_3 in the negative half cycle. Because of the greatly reduced CM noise, the two bridgeless boost PFC topologies are widely-used in industry. However, drawbacks include the increased conduction loss due to extra diodes, additional gate drive circuit in the PFC with bidirectional switch, and two boost inductors in the dual boost PFC topology.

Totem-pole PFC rectifier is another topology derived from the basic bridgeless boost PFC rectifier by exchanging the location of one diode and one switch, as shown in Figure 2.4(d). The CM noise is reduced significantly because the ac source is tied to the output ground through D_2 in the positive half cycle, and connected to the output positive terminal through D_1 during the negative half cycle. However, with Si MOSFETs, the body diode reverse-recovery loss is significant, leading to low PFC efficiency. Thanks to the emergence of GaN devices, not only the body diode reverse recovery loss is eliminated, but also the device has lower on-resistance, faster switching speed, and higher thermal performance [53, 54, 112]. By replacing Si MOSFETs with GaN devices (Figure 2.5(a)), the efficiency of the totem-pole PFC is increased greatly. Higher efficiency can be achieved by using Si MOSFETs as substitutes for the low-frequency diodes, as presented in Figure 2.5(b). Because of the simple structure, low conduction loss, reduced CM noise, and low part count, the GaN-based totem-pole PFC rectifier has been extensively investigated [55, 113], which is demonstrated with almost 99% peak efficiency at kW power level [107, 114].

Although the hard-switching GaN-based totem-pole rectifier realizes high efficiency, the switching frequency is usually limited below 120 kHz due to high switching loss. Recently, to reduce the switching loss and improve the switching frequency for higher power density, zero-voltage-switching (ZVS) modulations and control strategies with critical conduction mode (CRM) operation have been proposed for GaN-based totem-pole PFC rectifiers [115, 13, 116, 117]. With ZVS control, turn-on switching loss of the GaN devices is eliminated, and the switching frequency is pushed to hundreds of kHz or even MHz. Also, the converter volume and EMI filter size can be significantly reduced.

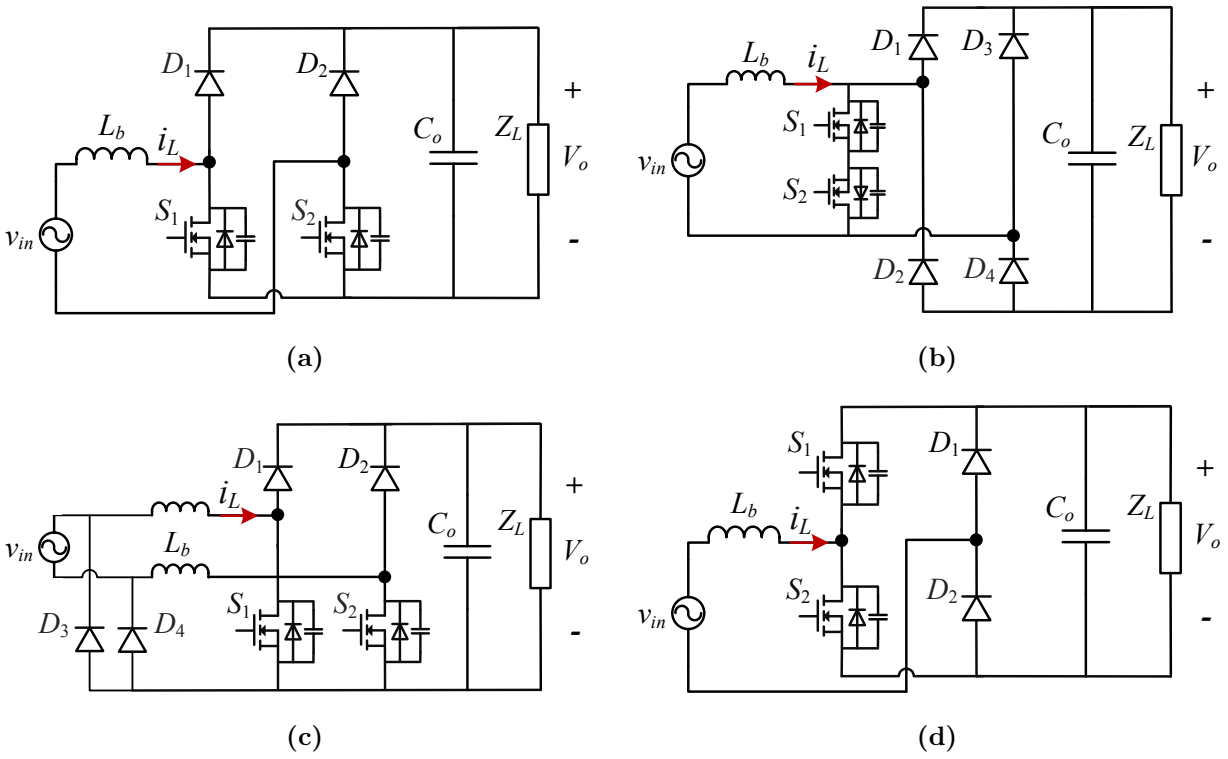


Figure 2.4: Bridgeless boost PFC rectifier topologies. (a) Basic bridgeless boost PFC; (b) Bridgeless boost PFC with bidirectional switch; (c) Dual boost bridegeless PFC; (d) Bridegeless totem-pole PFC.

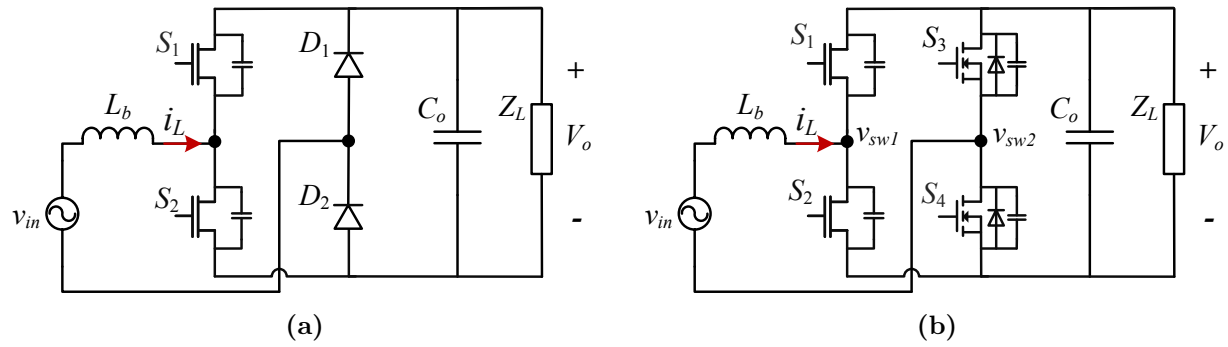
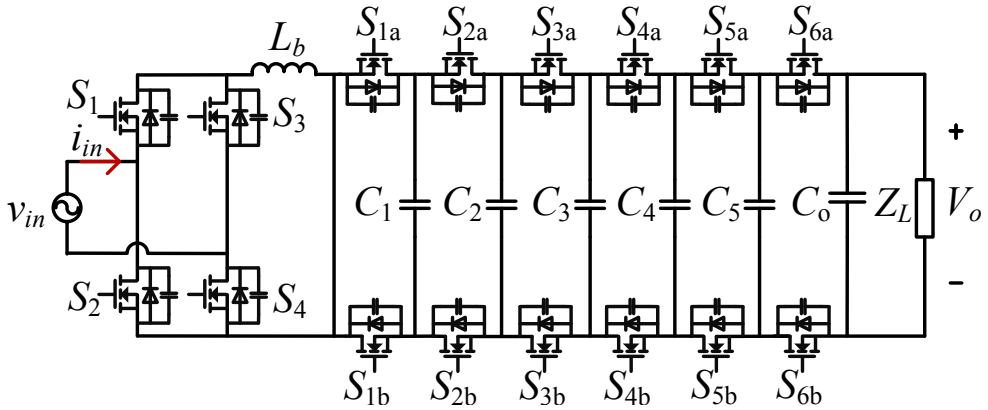


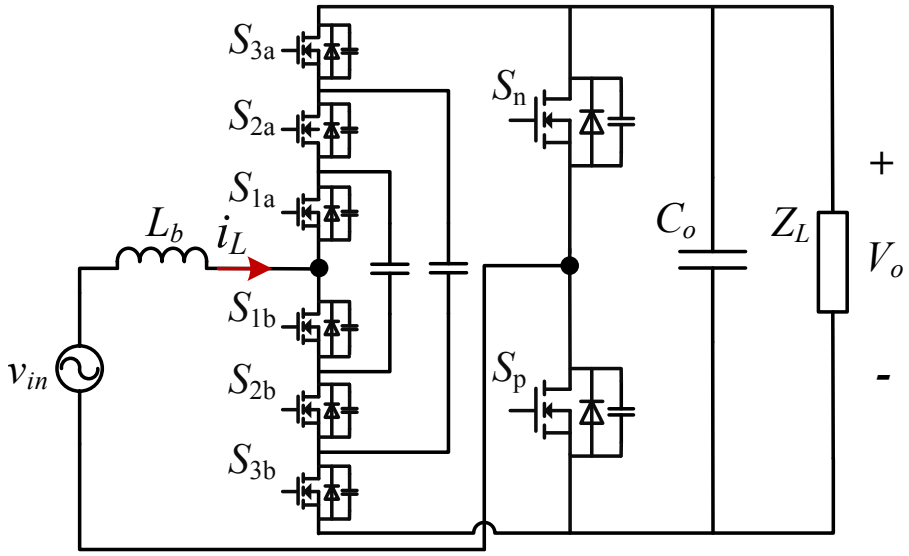
Figure 2.5: GaN-based totem-pole PFC rectifiers.

Multilevel converter provides another choice for the rectifier topology. Compared with the traditional two-level converter, multilevel structure benefits in utilization of low-voltage devices, reduced switching voltage, reduced inductor voltage swing, and increased equivalent ripple frequency. Recently, the flying capacitor multilevel (FCML) PFC rectifiers have been developed for medium and high power applications [118, 119, 120, 121]. In [119], a 1.5 kW seven-level flying capacitor boost PFC rectifier is developed with twelve 100 V GaN devices ($S_5 - S_{16}$), as presented in Figure 2.6(a). Although the peak efficiency reaches almost 99%, four line-frequency Si MOSFETs are used, and the power loss is not evenly distributed between high-side and low-side devices because of the asymmetrical structure. To address the issues in FCML boost PFC rectifier, the FCML totem-pole bridgeless PFC rectifier consisting of the FCML boost circuit and the totem-pole circuit was developed, as shown in Figure 2.6(b). In [120], a 3 kW three-level FCML totem-pole PFC rectifier with 150 V Si MOSFETs was developed and demonstrated with high efficiency. However, the inductor size is quite large with switching frequency at 70 kHz. To improve the power density and maintain high efficiency, a flour-level FCML totem-pole PFC rectifier with 200 V GaN devices was established in [121], where low-profile high-density commercial composite inductors are used. The rectifier prototype is claimed to have a power density at 1380 W/in^3 and 99% peak efficiency. Nevertheless, a major drawback of the multilevel rectifier is the increased number of gate drivers, and complicated design of gate drive circuits. Also, capacitor voltages should be balanced in the FCML multilevel configuration.

In data center rack-level front-end power supply, the typical two-stage rectifier is composed of a PFC converter and an isolated dc-dc converter. In order to improve the power density and efficiency, research efforts are also made on single-stage ac-dc structures. Excluding single-phase rectifiers with front-end diode bridge, bridgeless isolated PFC topologies are developed [122, 123, 124, 125, 126]. A comparison is made based on the state-of-the-art of the two-stage rectifiers and single-stage rectifiers, as displayed in Table 2.1. Most of the single-stage rectifier prototypes at kW level have high output voltage (> 100 V), which are more suitable for electric vehicles (EVs) on-board chargers, not for data center server power supplies. Although the two-stage rectifier requires more devices, it is superior to the single-stage system in terms of efficiency and power density.



(a)



(b)

Figure 2.6: Multilevel flying capacitor PFC topologies. (a) Seven-level flying capacitor PFC topology; (b) Four-level flying capacitor totem-pole PFC topology.

Table 2.1: Comparison of single-phase ac-dc rectifiers.

Ref.	Topologies	Power density	P_o	V_o	η	Part count
[122]	Single-stage, isolated half-bridge	17.3 W/in^3	1.25 kW	125 V	94%	14
[123]	Single-stage, isolated full-bridge	–	3 kW	300 V	94%	14
[124]	Single-stage DAB	40 W/in^3	3.3 kW	280 – 420 V	96.5%	13
[125]	Two-stage, totem-pole PFC+isolated LLC	100 W/in^3	3 kW	54 V	96.6%	9+16
[126]	Two-stage, totem-pole PFC+isolated LLC	66 W/in^3	3.2 kW	48 V	97.4%	9+18

2.3 Soft Switching Techniques

Hard-switched PWM converters suffer from significant switching loss especially in high frequency, which are unlikely to satisfy the increasing requirements of higher efficiency and higher power density [127]. The high switching noise and device voltage/current stresses also make the filter design and circuit protection more difficult. Resonant converters process power in sinusoidal or near sinusoidal waveforms, leading to considerably reduced switching loss. However, the sinusoidal waveforms exhibit higher peak current or voltage, and may also circulate within the circuit, causing in higher conduction loss [128, 129]. Accordingly, soft switching techniques containing zero voltage switching (ZVS) and zero current switching (ZCS) are developed, and power converters have evolved from pure PWM converters and resonant converters to hybrid resonant switch converters, including quasi-resonant converters (QRC) [130, 131, 132], multi-resonant converters (MRC) [133, 134], quasi-square-wave (QSW) resonant converters [135], etc. Soft switching PWM converters are deemed as optimal solutions for further enhancing the system efficiency and power density [136, 137].

2.3.1 Principle of Soft Switching

In general, soft switching operation refers to one or more device ZVS/ZCS switching transitions in a converter. ZVS approach makes the device voltage drop to zero by discharging the parallel capacitance before the turn-ON gate signal is applied, thus the $i - v$ overlap switching loss and the capacitive loss due to energy dissipation are eliminated during the turn-ON process. By paralleling a substantial capacitance across the device, the voltage is held close to zero while the device turns OFF, hence the turn-OFF $i - v$ overlap loss is minimized [136]. ZCS method allows the switch current to reduce to zero before the voltage increases, so that the $i - v$ overlap loss is eradicated. Nevertheless, ZCS is of little help in reducing the capacitive loss during the turn-ON transition.

For the specific device switching loss, diodes mainly suffer from reverse-recovery loss during the turn-OFF process. ZCS turn-OFF by adopting a resonant inductor L_r in series

with the diode limits the current change rate, thus lowering the recovered charge Q_r and loss. However, larger peak inverse voltage is often induced by ringing of L_r and diode junction capacitance C_j, possibly causing diode voltage breakdown or failure. In contrast of ZCS, ZVS turn-OFF with the help of an extra capacitor C_r in parallel with the diode constricts the change slopes of both diode current and voltage, leading to diminished reverse-recovery loss and relatively-low peak diode voltage.

For MOSFETs, the major constituents of switching loss are the loss of energy stored in the output capacitance C_{oss}, and the large $i-v$ overlap loss owing to the diode reverse recovery process if existing in the circuit, which all occur during the MOSFET turn-ON process. Because of the consequential C_{oss}, MOSFET turn-OFF switching loss is relatively small. With the assist of a resonant tank, ZVS turn-ON can be achieved to avoid both the C_{oss} loss and the $i-v$ overlap loss, and turn-OFF switching loss is further minimized by ZVS or ZCS.

Similar to MOSFETs, IGBTs usually exhibit considerable turn-ON switching loss due to $i-v$ overlap loss and diode reverse-recovery mechanism. Additionally, IGBTs encounter large turn-OFF switching loss due to the current tailing phenomenon [127]. Although ZVS can successfully remove the IGBT turn-ON switching loss, it is difficult to eliminate the significant loss resulting from current tailing. Instead, ZCS is more useful in removing the turn-OFF switching loss for IGBT as well as other minority carrier devices [138, 139].

2.3.2 ZVS Realization

2.3.2.1 ZVS with Inherent LC network

For a converter with an inherent inductor connected to the switching node, soft switching can be realized by utilizing the inductor and the device output capacitance as the resonant network. Figure 2.7-Figure 2.8 illustrate the ZVS operation principle of a synchronous dc-dc boost converter, where the low-side device S_2 is the active switch, the high-side device S_1 is the synchronous rectifier, and Z_n represents the characteristic impedance defined as $Z_n^2 = {}^{L_b}/_{(2C_{oss})}$ with $C_{oss1} = C_{oss2} = C_{oss}$. To achieve S_2 ZVS turn-ON, the converter operates

in CRM, where S_1 is turned OFF immediately when i_L drops to zero, and the inductor L_b resonates with device output capacitance.

As shown in Figure 2.8(a), when $V_{in} \leq 0.5V_o$, the drain-to-source voltage $v_{ds,S2}$ is able to resonate to zero, and S_2 can be turned ON in ZVS naturally. However, when $V_{in} > 0.5V_o$, the energy stored in the inductor is not enough to fully discharge the device output capacitance, and $v_{ds,S2}$ cannot decrease to zero, leading to some hard switching loss when S_2 turns ON. To extend the conversion ratio for ZVS achievement, ZVS extension method is adopted when $V_{in} > 0.5V_o$ [140, 141, 142, 13]. As illustrated in Figure 2.8(b), the conduction time of S_1 is purposely prolonged to obtain a lower negative current. As a result, the inductor has sufficient energy to discharge the output capacitance during the resonance, and v_{ds_S2} can decrease to zero, ensuring ZVS turn-ON. Such full-range ZVS operation has been successfully implemented in different converters, regarded as an effective way for soft switching [143, 144].

2.3.2.2 ZVS with Auxiliary Circuit

For those converters without an inductor connected to the switching node, or the load impedance is not designed for soft switching, an auxiliary circuit can be adopted as an alternative. Figure 2.9 elaborates the basic idea of using an auxiliary circuit to achieve ZVS during the $S_1 - S_2$ commutation [145]. Before turning OFF S_1, a redirection current I_r is switched into the switching node. As I_r increases, the current flowing into the device decreases with $I_{s1} = I_r - I_s$. Eventually, I_r grows larger than I_s, and I_{s1} flows inversely, allowing S_1 to be shut OFF at zero voltage. Then, during the dead time, I_{S1} charges C_{oss1} and discharges C_{oss2}, and S_2 can be turned ON with ZVS when v_{sw} drops to zero.

A number of auxiliary circuits have been developed, which can be classified into passive auxiliary circuits [146, 147] and active auxiliary circuits [145, 148, 149]. The passive auxiliary circuit is composed of inductors and capacitors, which has low cost but also suffers from limited control flexibility. The active circuit requires additional active switches to generate the auxiliary current, which is capable of performing accurate soft switching, but increases the circuit and control complexity. Although switching loss is reduced, additional loss is added by the auxiliary circuit. Hence, an auxiliary circuit with smaller loss is desired, and trade-OFF design might be required for the optimal system efficiency.

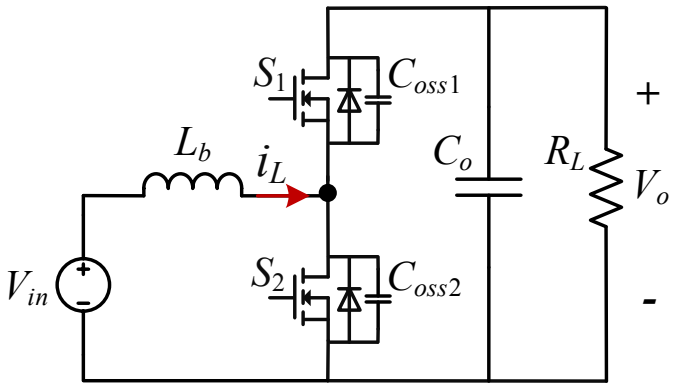


Figure 2.7: Dc-dc synchronous boost converter.

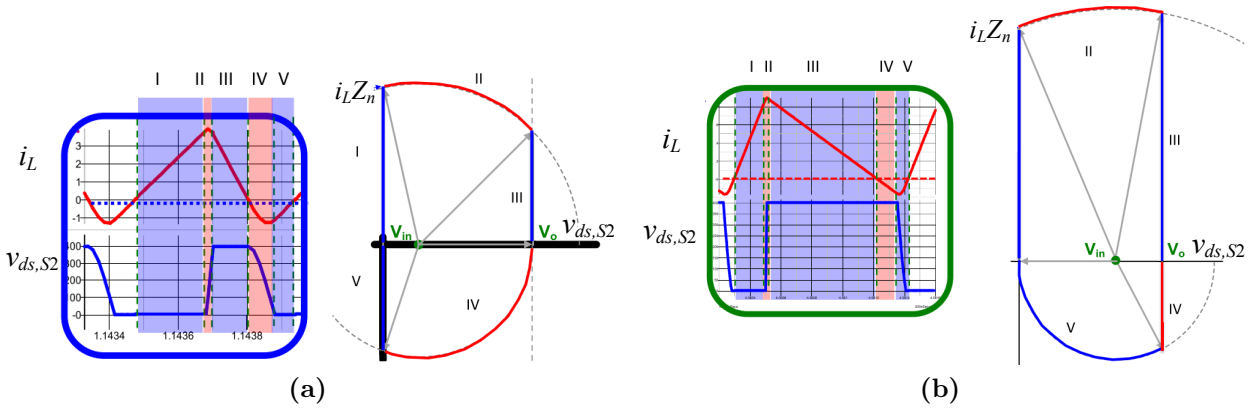


Figure 2.8: ZVS operation and state-plane trajectories of synchronous boost converter [13]. (a) Natural ZVS when $V_{in} \leq 0.5V_o$; (b) Extended ZVS when $V_{in} > 0.5V_o$.

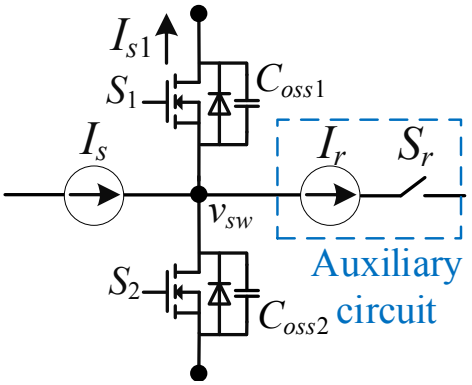


Figure 2.9: The principle of auxiliary circuit for ZVS.

2.4 ZVS Control Strategies of Single-Phase Rectifier

The front-end ac-dc rectifier is necessary for almost all power supplies. Typical control targets of a single-phase front-end rectifier include: (1) regulate input current with near unity power factor and low THD; (2) stabilize the dc output voltage with small ripple; (3) buffering the pulsating energy between the instantaneous input ac power and output dc power, where predominant approaches for energy buffering include dc-link capacitor, LC resonant notch filter [150], and active power filters [151]; (4) achieve specific requirements in different applications, such as hold-up time in telecommunication and data centers [152] or fast dynamic response in consumer electronics wireless power supply [153]. Conventional control methods for ac-dc rectifier include the average current mode control, current programmed control, and hysteresis control, etc [127]. However, these control strategies target traditional Si-based PWM converters with hard switching modulation, and are not applicable for GaN-based rectifier with soft switching and high frequency.

As aforementioned, CRM operation is popular in low or medium power PFC rectifiers (under several kilowatts), advantageous in small inductor size and possibility of achieving soft switching. Different control methods can be used to enable CRM operation. Among these, constant ON-time (COT) control is a simple and popular scheme [14], where the active switch is turned on when the inductor current reaches zero, and turned off after a constant conduction time t_{on}. Figure 2.10 shows a typical implementation of the COT control. The low-bandwidth voltage controller generates the control signal V_c that is almost constant at steady state. A ramp voltage signal V_{ramp} is compared with v_c, and the device is turned off when $V_{ramp} > v_c$. Meanwhile, the inductor current zero-crossing point is detected to generate a zero-current-detection (ZCD) signal which is used to reset V_{ramp} and switch the device on.

With the COT control, the peak inductor current is proportional to the input voltage. If neglecting the deadtime, the peak inductor current is twice the average current, that is $i_{peak} = 2i_{ave}$. Hence, the input current follows the input voltage, and unity power factor is realized. Assuming $v_{ac} = \sqrt{2}V_{rms}\sin\omega t$ and $i_{ac} = \sqrt{2}P/V_{rms}\sin\omega t$, the ON time is

$$t_{on} = \frac{2PL_{boost}}{V_{rms}^2} \tag{2.1}$$

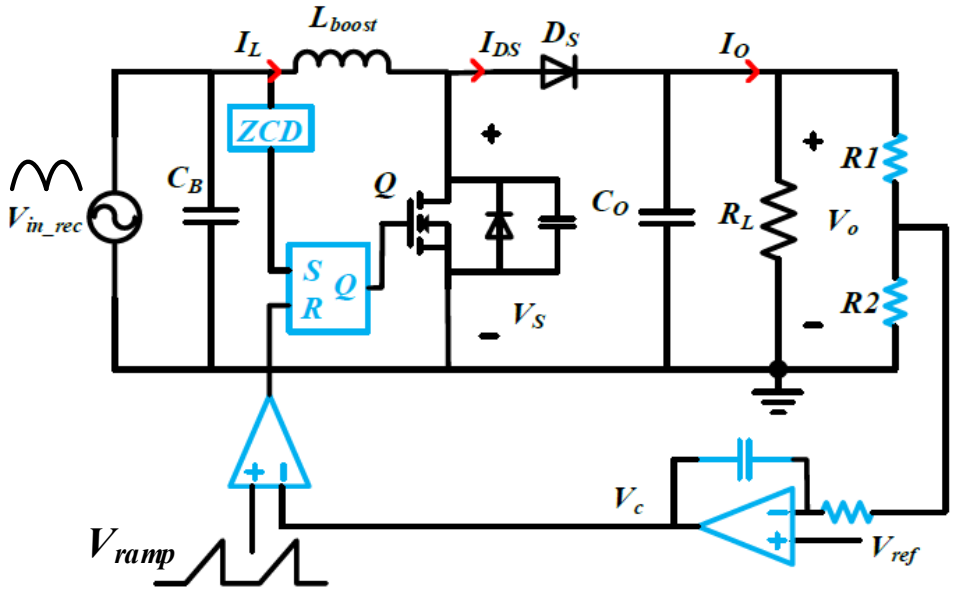


Figure 2.10: A typical implementation of CRM COT control [14].

The OFF-time of the MOSFET is

$$t_{off} = \frac{v_{ac}}{V_o - v_{ac}} t_{on} \tag{2.2}$$

Accordingly, the switching frequency is variable within the line cycle,

$$f_s = (1 - \frac{v_{ac}}{V_o}) \frac{V_{rms}^2}{2PL_{boost}} \tag{2.3}$$

COT control has been widely used for CRM operation, but issues occur when the CRM COT control is applied in high-frequency rectifiers. Take the GaN-based totem-pole PFC rectifier for example. When the converter switching frequency is pushed to MHz, notable current distortion occurs in the ac-line zero-crossing region, as shown in Figure 2.11. This is because the inverse current used for achieving ZVS cannot be neglected with small inductor in the high-frequency operation. In order to overcome the zero-crossing current distortion issue, CRM operation with variable ON-time (VOT) has been is developed [154, 155]. As illustrated in Figure 2.12, by increasing the ON time close to the ac-line zero crossing, the current distortion is compensated, and input current is regulated with good PF.

Compared with the traditional analog-based controller, digital controllers feature more flexibility, easy programmability, and improved integration of power management. Accordingly, digital-based predictive VOT control is developed, which can accurately regulate the input current and achieve ZVS within the whole line cycle [140, 15, 16]. In [15], accurate modeling of the inductor current is developed and switching time intervals are calculated precisely considering non-linear effects. Since the calculation is complicated and time-consuming, the conduction time is calculated offline and loaded into the controller through a look-up table (LUT), as shown in Figure 2.13. Although ZVS is achieved precisely, such control limits the adaptability of the converter in wide input voltage range and varying output loads. To program the conduction time in real time with one microcontroller, a simplified but accurate calculation method is proposed in [16], where the inductor current is approximated as a triangular waveform. As illustrated in Figure 2.14, the variable conduction time is generated based on the real-time calculation and the voltage control loop, which is implemented in one DSP.

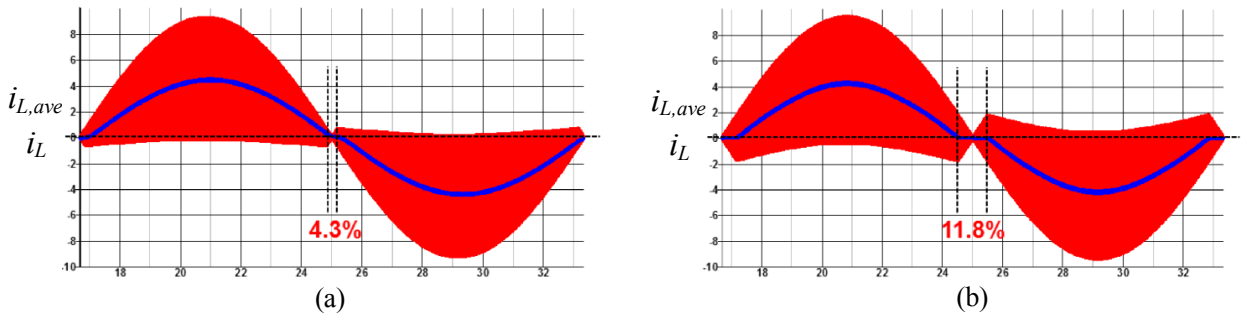


Figure 2.11: Inductor current waveform of constant ON-time CRM PFC [13]. (a) f_s = 100 kHz with higher boost inductance; (b) f_s = 1 MHz with lower boost inductance.

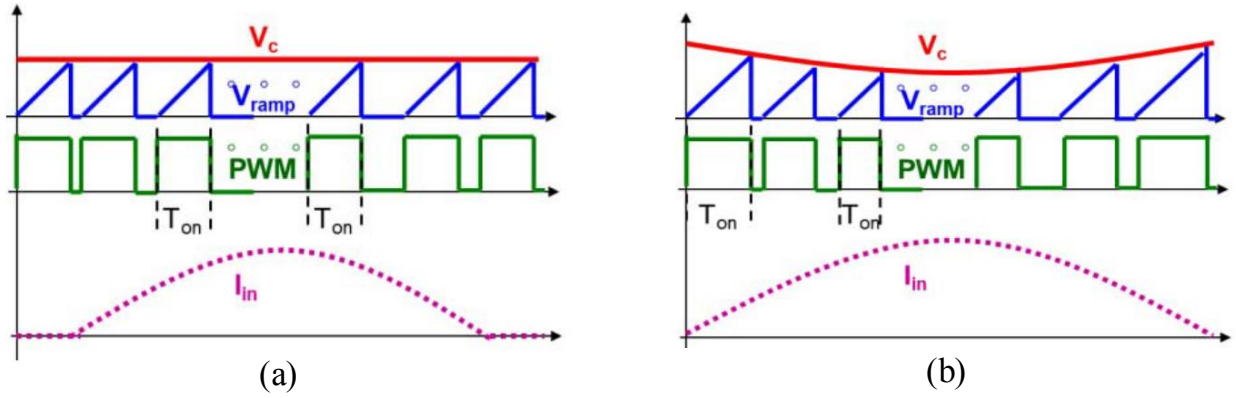


Figure 2.12: Concept illustration of CRM PFC with (a) constant ON-time control; (b) variable ON-time control [13].

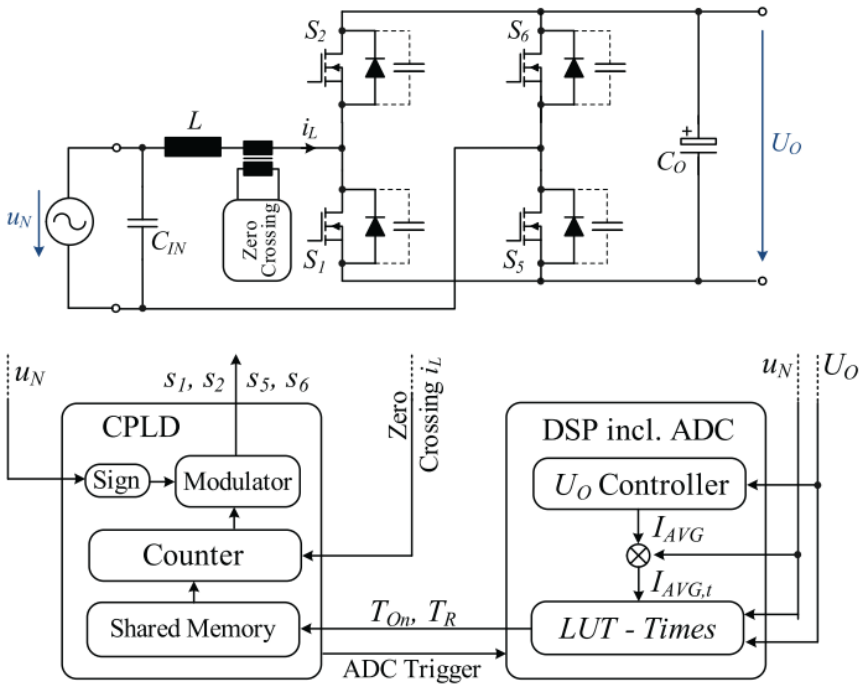


Figure 2.13: Digital-based variable ON-time control with offline calculation [15].

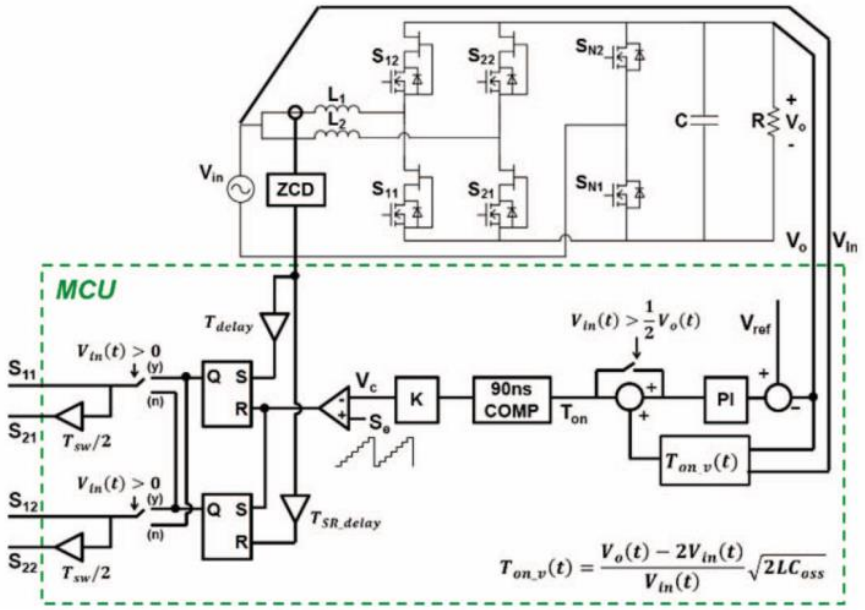


Figure 2.14: MCU-based variable ON-time control with real-time calculation [16].

Dual current programmed mode (DCPM) control, also named as hysteretic current mode control, can also be used to achieve ZVS operation [17, 156]. Instead of adjusting the device conduction time, the controller determines the switching instants by comparing the sensed current signal with two current reference limits, which are pre-defined and loaded into the controller. As illustrated in Figure 2.15, different current limits can be programmed to regulate the required current accurately. However, instantaneous current sensing signal is required and compared with the upper and lower limits, which is easy to be impacted by switching noise.

Another type of control for achieving the ZVS operation is known as variable frequency PWM (VFPWM) control [18, 157, 158]. Rather than adjusting the conduction time or regulating the current ripple, VFPWM control changes the instantaneous switching frequency to realize ZVS. Figure 2.16 presents the control diagram of a VFPWM control proposed in [18]. The converter duty cycle is generated based on the traditional PWM and average current control loop, but the carrier wave's frequency is adjusted instantaneously based on a real-time calculation. In comparison with other ZVS control methods, the VFPWM control eliminates the noise-susceptible high-speed current sensing required in DCPM control and the ZCD circuit demanded in VOT control. However, lacking of real-time synchronization between the inductor current and the switching time intervals, it is difficult to maintain accurate ZVS operation.

2.5 Current Distortion and Mitigation

Maintaining a low-harmonic input current is an important qualification for front-end rectifiers. However, in practical applications, the input current can be distorted because of sensing error, control signal time delay, noise disturbance, etc. Such current distortion is more likely to occur in GaN-based rectifiers with high switching speed, noise susceptible sensing circuit, and high-frequency noise impact. For the GaN-based ZVS bridgeless boost-type PFC rectifier, two distinct distortion mechanisms are found: the low-frequency line-cycle current distortion [159, 19] and the ac line zero-crossing current spike [160, 161].

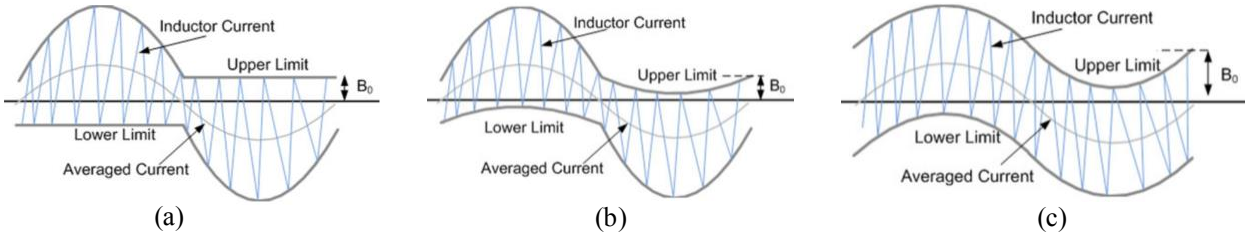


Figure 2.15: Different current profiles for ZVS operation with dual current programmed control [17]. (a) with fixed reverse current; (b) with variable reverse current; (c) with fixed bandwidth.

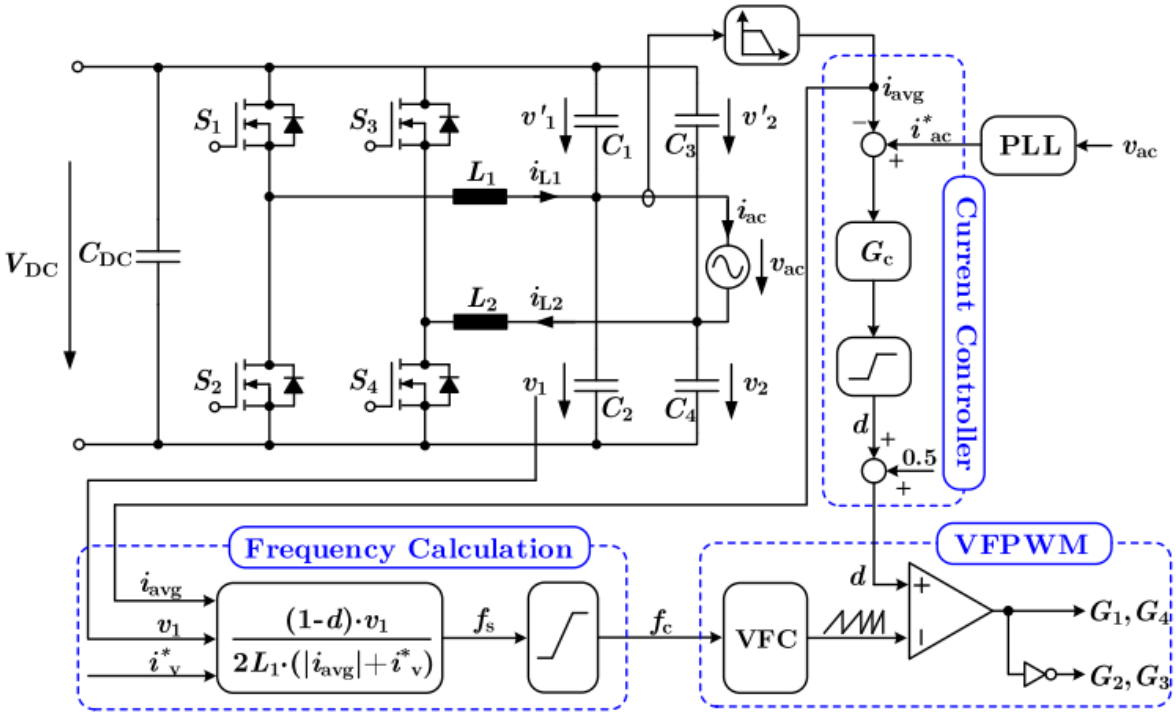
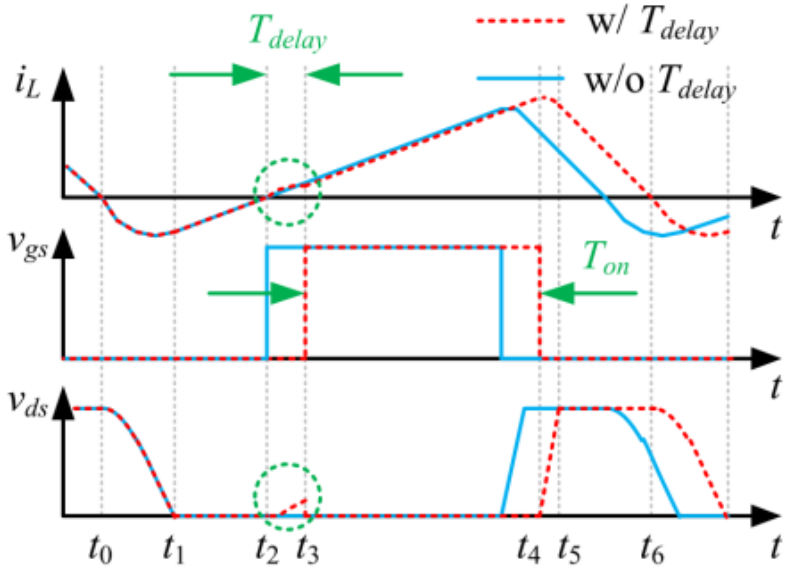


Figure 2.16: Control diagram of the variable frequency average current mode control [18].

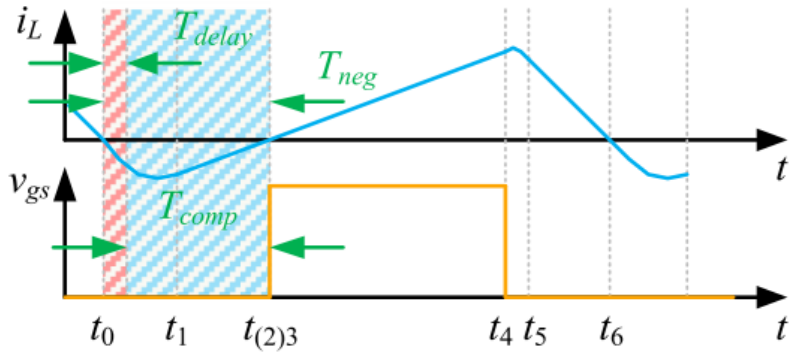
The low-frequency line-cycle current distortion is mainly induced by the propagation time delay of the current sensing signal. To compensate the time delay T_{delay}, [19] proposes a method by subtracting T_{delay} from the time difference T_{neg} between the two inductor current zero-crossing points based on the numerical relationship $T_{delay} < T_{neg}$, as shown in Figure 2.17. However, such method is not applicable for the high-frequency rectifier with much smaller boost inductance where T_{neg} is close or even smaller than T_{delay}. In [156], a simple compensation method is proposed by tuning the propagation delay time and the parasitic inductance $L_{p,R}$ of the current sensing resistor R_{shunt}. Given that the current sensing time error introduced by $L_{p,R}$ is a leading time error, it can be used to cancel out the propagation delay time. Nevertheless, the leading time may not be large enough to fully compensate the time delay, and effort on tuning or purposely enlarging $L_{p,R}$ is required.

The ac-line zero-crossing current spike results from two phenomena. The first is the asynchronization between the line-rectification device switching and the ac voltage zero-crossing caused by the slower commutation of the Si devices and practical implementation issues like inaccurate zero-crossing detection, sensing, and control time delay. The second is the high dv/dt noise induced during the switching transition of the line-rectification devices [160, 162, 163, 161].

In order to avoid the current spike, soft transition approaches are proposed by turning on the GaN devices after each zero-crossing with gradually increased duty cycle or fixed small duty cycle [162, 140, 161]. However, these soft transition methods are either complicated or difficult to control precisely, and cannot be directly applied on the high-frequency PFC rectifiers with ZVS operation. In [164], the current spike is completely suppressed by utilizing the LC resonance in a proposed auxiliary circuit. However, the auxiliary circuit is complicated including two capacitors, one inductor, two MOSFETs, and two diodes, which increases the circuit and control complexity. A hybrid PWM scheme is adopted in [165], where modulation switches from unipolar to bipolar during the region near the zero-crossing to eliminate the current spike. However, bipolar modulation causes larger switching loss with the Si MOSFETs, and GaN devices need to be used for lower switching loss but leads to a higher cost.



(a)



(b)

Figure 2.17: (a) Impact of current sensing time delay [19]; (b) Proposed delay compensation method in [19].

On the other hand, in GaN-based high-frequency power converters, high dv/dt or di/dt noise could induce nonlinear dc bias or low-frequency shift on the voltage or current sensing signals, further impacting the control stability and distorting the current [166]. The high-frequency noise impact has been demonstrated in [166] based on a Vienna-type rectifier plus a dc-dc converter, and corresponding solutions are proposed to mitigate the input current THD. Such high-frequency noise related issues should be analyzed according to the specific application, and effective approaches are required to reduce the noise impact.

2.6 Reactive Power Compensation

The concept of reactive power compensation embraces a diverse field of both customer and system problems, and it can be categorized into two aspects: load compensation and power system support. For electric loads, reactive power compensation is mainly used to correct the power factor and eliminate current harmonic components generated by nonlinear loads. For example, a data center, as a critical load, needs to compensate the reactive power generated from the cooling system, and correct the terminal power factor to meet grid regulations. For the power system, reactive power compensation improves the active power transfer efficiency and reduces voltage fluctuation in a transmission system or distributed power network. Therefore, reactive power compensation is necessary and important for both the power system and loads.

2.6.1 Traditional Techniques of Reactive Power Compensation

The most conventional techniques for reactive power compensation are mechanically switched capacitors or inductors and rotating synchronous condensers [167]. However, they are no longer popular for today's power system. Switched capacitors or inductors have simple structure and easy control, but they are disadvantageous in being unreliable and sluggish. Also, since the capacitor or inductor bank is fixed, they often cause over-compensation or under-compensation, leading to an inaccurate reactive power compensation for fluctuating loads. A synchronous condenser is simply a synchronous machine connected to the power grid, and its field current can be adjusted to absorb or generate reactive power as required.

However, synchronous condensers are rarely used today because of the high capital cost, complicated startup and protection equipment, and slow response to quick load change [168].

Static VAr compensators (SVCs) are another traditional type of reactive power compensator, like thyristor-switched capacitors (TSCs), thyristor controlled reactors (TCRs), thyristor-controlled series static compensators (TCSCs) [169]. By controlling the thyristor gating angle, SVCs provide more accurate reactive power compensation and faster dynamic response (0.5 to 2 line cycles). Also, they are less expensive than synchronous condensers. Nevertheless, SVCs have limited capability of phase balancing, and a large number of passive components are still required, causing high cost and large size.

Self-commutated VAr compensators such as the static synchronous compensators (STATCOMs) and static synchronous series compensators (SSSCs) are more popular in today's market for reactive power compensation [169, 45]. Enabled by power electronic converters like voltage-source converters (VSCs), current-source converters (CSCs), and multilevel converters, self-commutated VAr compensators can achieve flexible reactive power regulation without substantial passive components, thus leading to small size and cost reduction. With high-bandwidth PWM modulation and control, self-commutated VAr compensators result in a low level of current distortion and faster time response than the fundamental line frequency. Apart from those typical self-commutated VAr compensators, active front-end UPS with battery energy storage and solid state transformer have also been proposed for reactive power compensation [170, 66].

2.6.2 Single-Phase Rectifier for Reactive Power Compensation

The previously discussed reactive power compensation schemes are all based on centralized power compensators, which require high initial investment and consume large power loss during the power processing. Also, with an increasing deployment of distributed energy resources (DERs) such as photovoltaic and critical loads like electric vehicles (EVs) or data centers, the grid voltage may fluctuate in a fast pattern that is difficult to be dealt with traditional power compensators [171]. With advanced single-phase inverters and rectifiers, DERs and critical loads can also provide fast and flexible reactive power

compensation [172, 173, 174, 175, 20, 21, 176, 177]. Since a rectifier is the design target in this work, the single-phase rectifier with reactive power regulation will be investigated.

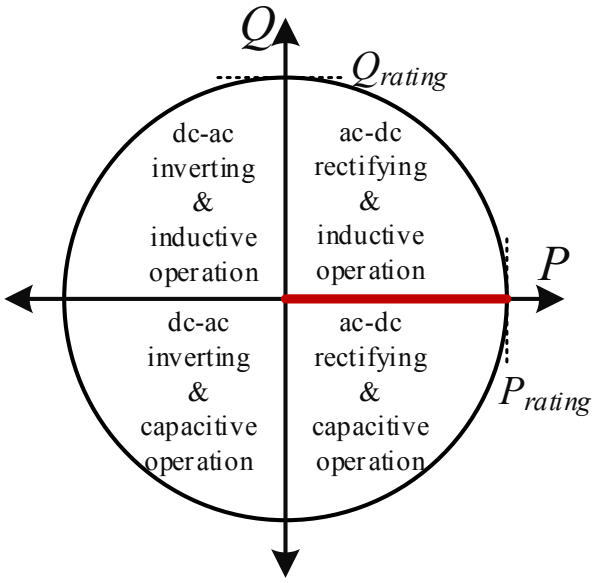
An active ac-dc converter can be configured into four operation zones in terms of the active and reactive power transfer. As illustrated in Figure 2.18(a), traditional PFC rectifiers work in the positive power axis with only active power transferred. When extending the rectifier with reactive power transfer (Figure 2.18(b)), the operation boundary is enlarged into a half circle, that is, the reactive power can be transferred bidirectionally between the source and the converter simultaneously with the active power supplied to the load.

Reactive power regulation can be integrated in single-phase unidirectional rectifiers, such as diode-bridge based rectifiers and bridgeless rectifiers [174, 175]. However, such rectifiers have limited capability of reactive power regulation. Due to the characteristic of diode unidirectional current flow, an uncontrollable region appears whenever the polarities of current and voltage become opposite. Within this region, the input current is uncontrollable, leading to severe input current distortion. Compared with unidirectional rectifiers, active front-end rectifiers, such as totem-pole PFC rectifier and the FCML PFC rectifier, allow bidirectional power flow and are able to achieve reactive power operation with low current distortion. In addition, the full-bridge active ac-dc rectifier with bipolar modulation is also capable of realizing reactive power operation [21, 20].

To achieve reactive power control, the single-phase power is often decoupled through direct-quadrature (dq) rotating frame [178, 179]. First, signals in abc frame are transformed into stationary $\alpha\beta$ frame through Clarke transformation. Second, signals in $\alpha\beta$ frame are transformed into dq rotating frame through Park transformation. In single-phase rectifiers, assuming $X_\alpha = A\cos\omega t$ is the original single-phase signal, its orthogonal signal is $X_\beta = A\sin\omega t$, then the signal in the dq frame is

$$\begin{bmatrix} X_d \\ X_q \end{bmatrix} = T_{\alpha\beta-dq} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} \tag{2.4}$$

In practical implementation, the orthogonal signal generator (OSG) phase locked loop (PLL) can be used to generate X_α, X_β, calculate X_d, X_q for instantaneous power estimation, and detect the grid phase angle [180].



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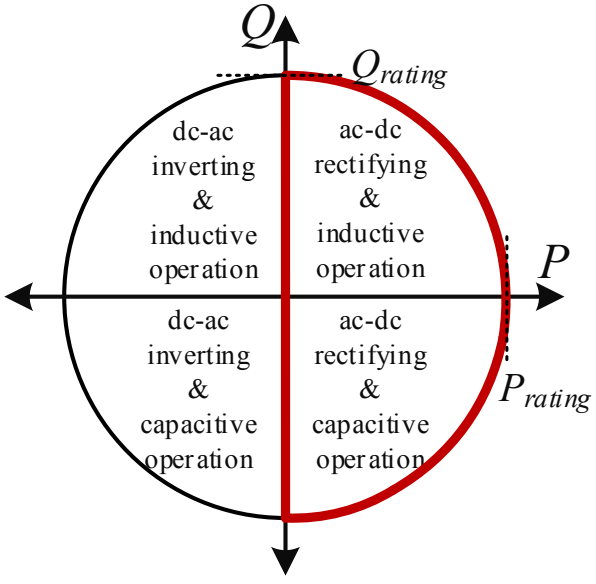


(b)

Figure 2.18: P-Q power plane. (a) Ac-dc rectifier with unity PF; (b) Ac-dc rectifier with non-unity PF.

Research efforts have been made on implementing two-quadrant or four-quadrant power operation in single-phase rectifiers [20, 21, 176, 177]. In [20], a control scheme of regulating the active and reactive power flow is developed in a bidirectional ac-dc converter used for telecom backup systems. As shown in Figure 2.19, full-bridge boost rectifier is employed, and the control strategy is implemented in dq frame by using the all-pass filter and dq rotating transformation. The active power and reactive power are regulated in d and q axis respectively to control the power flow between the grid and the telecom power supply. Also, internal current controllers are adopted in dq frame to generate the duty cycle d_{dq}, which is converted back in the single-phase system to control the rectifier current. In [21], a full-bridge ac-dc boost rectifier is applied in an on-board bidirectional plug-in electric vehicle (PEV) charger that can provide reactive power support to the utility grid in addition to charge the vehicle battery. As illustrated in Figure 2.20, instead of transforming into dq frame, orthogonal signals are generated by a delay block, and the instantaneous active and reactive power are calculated in the $\alpha\beta$ frame. Both active and reactive power are controlled to follow the power demands, and output voltage is regulated by an inner voltage loop. To control the rectifier current, a nonlinear proportional and resonant (PR) controller is adopted.

Existing work concentrates on achieving reactive power operation with hard-switching rectifiers and traditional PWM control. Few studies investigate the reactive power operation in rectifiers with soft-switching control. In [181], non-unity PF operation of a CRM totem-pole inverter with ZVS operation is briefly mentioned. Implementation challenges occur at the ac-line zero-crossing. With reactive power operation, zero-crossing points of the ac current and ac voltage are not at the same time, leading to extreme minimum and maximum switching frequencies. To clamp the peak frequency at the ac current zero-crossing, frequency limitation with DCM operation is adopted. However, the method for the ac voltage zero-crossing issue is not discussed, and no further practical implementation is provided. In addition, the impact of using front-end rectifiers for reactive power regulation on the system loss, cost, and component design is hardly discussed in the existing work. Systematic analysis of a data center's power loss and cost with reactive power compensation on the front-end rectifiers is required.

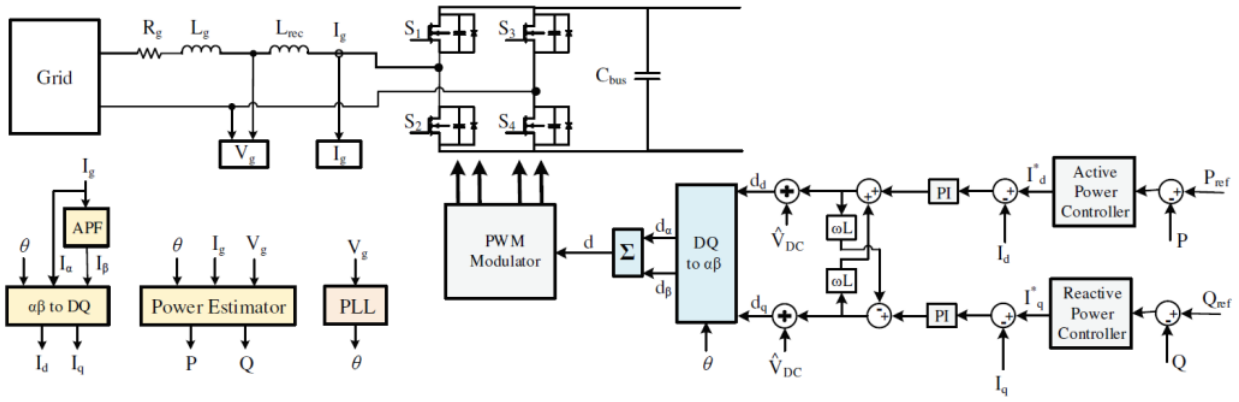


Figure 2.19: Control diagram of a single-phase bidirectional ac-dc converter [20].

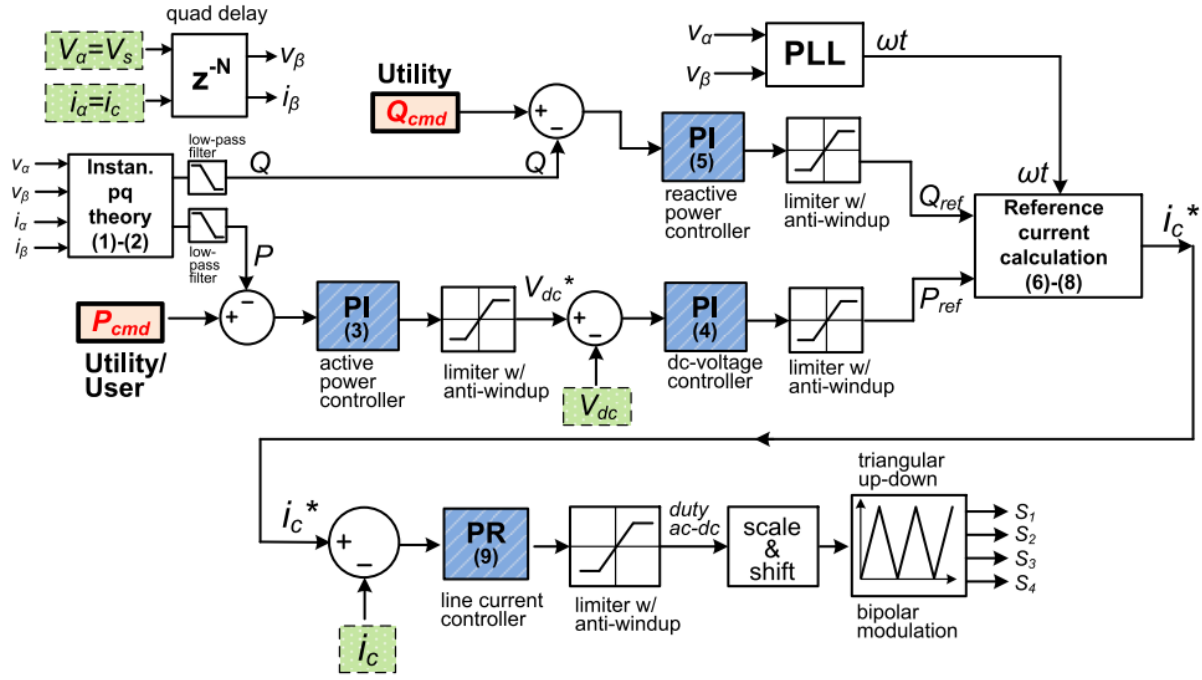


Figure 2.20: Control diagram of a single-phase bidirectional ac-dc converter [21].

2.7 Summary

This section summarizes the literature review in the following aspects:

(1) Existing data center power models have disadvantages of incompleteness, incapability of predicting dynamic performance, limited availability, and imprecision. There is a lack of data center dynamic power load model that is complete and accurate to reflect the dynamic load performance.

(2) The HTB is a versatile platform to perform different real power tests and emulate the power grid with precise transient response. However, none of the developed load emulators can reflect the data center load characteristics. Hence, it is critical to create a data center power load emulator to carry out the related grid experiments for evaluating the grid dynamic performance and transient stability.

(3) Advantageous in simple topology and low power loss, bridgeless PFC topologies are popular and attractive in the power supply ac-dc rectifier. Table 2.2 summarizes the performance of the reviewed bridgeless PFC topologies. Considering the efficiency, PF, current THD, and part count, the bridgeless totem-pole PFC (Figure 2.5) and the four-level flying capacitor totem-pole PFC rectifier (Figure 2.6(b)) are promising candidates for the high-efficiency and high-density rectifier in data center power supply units.

(4) Soft switching can significantly reduce the converter switching loss and improve the efficiency. For boost-type or totem-pole PFC rectifiers, CRM operation combined with extended ZVS method are effective modulation to achieve full-range ZVS with minimal increased conduction loss. However, the existing ZVS extension method does not consider any time margin, where inverse current is only enough to ensure ZVS at one time instant. It is easy to lose ZVS operation in the practical implementation when sensing error or signal propagation time delay exists.

Table 2.2: Comparison of bridgeless PFC converters.

Ref.	Topology	P_o	Peak η	Component count	Merits	Limitations
[98]	Flyback	72 W	89%	12	Isolated	Need snubber Low efficiency High part count
[91]	Buck	100 W	85%	14	Low THD	Low efficiency High part count
[182]	Boost	1.6 kW	96.5%	6	Low part count High efficiency High PF Low THD	High bus voltage
[95]	Buck-boost	780 W	94%	10	High PF Low THD	High part count
[103]	Cuk	150 W	93%	13	Low THD	High part count
[101]	SEPIC	100 W	94%	13	High PF Low THD	High part count
[107]	Totem-pole boost	1 kW	98.6%	6	Low part count High efficiency High PF Low THD	High bus voltage CM noise
[119]	Multilevel	1.5 kW	98.5%	23	High efficiency High PF Low THD	High bus voltage High part count
[121]	Four-level totem-pole	3 kW	estimated 99%	12	High efficiency High PF Low THD	High bus voltage High part count

(5) Popular ZVS control strategies for GaN-based converters include hysteretic current mode control, predictive variable on-time control, and variable frequency PWM control. The predictive variable on-time control is selected as the start point for the rectifier control in the research.

(6) In high-frequency GaN-based rectifiers, the current THD and control stability can be sabotaged by factors like high-frequency current sensing delay, high dv/dt switching noise, and switch timing asynchronization in practical implementations. Effective solutions are required to mitigate the current distortion and improve the stability of the power supply system.

(7) Achieving reactive power operation of the front-end rectifiers provides another approach for reactive power compensation in data centers. Impacts of using the GaN-based rectifiers for data center reactive power compensation need to be analyzed, and rectifier design for achieving both ZVS control and non-unity PF operation is required.

Chapter 3

Modeling and Emulation of Data Center Power Distribution System

This chapter concentrates on modeling and emulation of the data center power distribution system, to investigate data center load characteristics and improve the efficiency of power grid dynamic simulation and evaluation. A complete dynamic data center power model is proposed, and a data center power emulator serving as a all-in-one load is developed based on the HTB platform. The model and emulator are designed to achieve:

(1) Predict the operation performance of the data center power system, including the power factor, power consumption, and transient responses during load variations and grid disturbances.

(2) Demonstrate the data center load characteristics by performing realistic real power test in real-time.

(3) Assess the power grid dynamic performance by emulating power system experiments with data center load.

Research work in this chapter has been published in:

(1) J. Sun, S. Wang, J. Wang, L. M. Tolbert, "Dynamic model and converter-based emulator of a data center power distribution system," *IEEE Transactions on Power Electronics*, early access, Jan. 2022.

(2) J. Sun, S. Wang, L. M. Tolbert, D. Costinett, "Emulation of voltage sag event for a data center power distribution system," in *IEEE Applied Power Electronics Conference (APEC)*, Phoenix, AZ, 2021, pp. 126-133.

3.1 System Circuit and Operation Principle

3.1.1 Circuit Topology and Control

The widely-used ac power distribution system with line-interactive UPS and air cooling is investigated. According to the system specifications like annual downtime, energy backup redundancy, and power scale, data centers are classified into multiple levels ranging from Class F0 to Class F4 [28]. In this design, a Class F1 system is employed, and Figure 3.1 illustrates the typical structure of the power distribution system.

Utility power is first scaled from medium voltage (MV) to low voltage (LV) at 4-wire 60 Hz 480Y/277 V_{ac} [183]. For the power supply system, the three-phase ac power is converted into many single-phase circuits through PDUs. Then, the single-phase ac power is assigned to different server racks and converted into low-voltage dc power via the server rack PSUs to supply the server loads. To prevent grid disturbances and ensure stable power for server loads, a UPS is implemented to condition and compensate the input ac power.

The cooling system is primarily composed of a cooling tower, chiller, water pumps, CRAH, and distributed server fans in rack cabinets. In terms of electrical equipment, grid-connected induction motors can be used to stand for the cooling tower, chiller and water pumps, and the CRAH is represented by a VFD-based motor which is capable of adjusting the motor speed according to the required air flow. Distributed server fans are powered by the dc voltage from PSU, and are considered as part of the electric load in the power supply system.

In order to practically demonstrate the data center system, commonly-used circuit topologies and control strategies of each component are investigated [184, 185, 186, 187, 105, 188, 189, 190]. Figure 3.2 shows the circuit topologies of the UPS, PSU, and CRAH VFD, and Table 3.1 summarizes the adopted circuits and control methods.

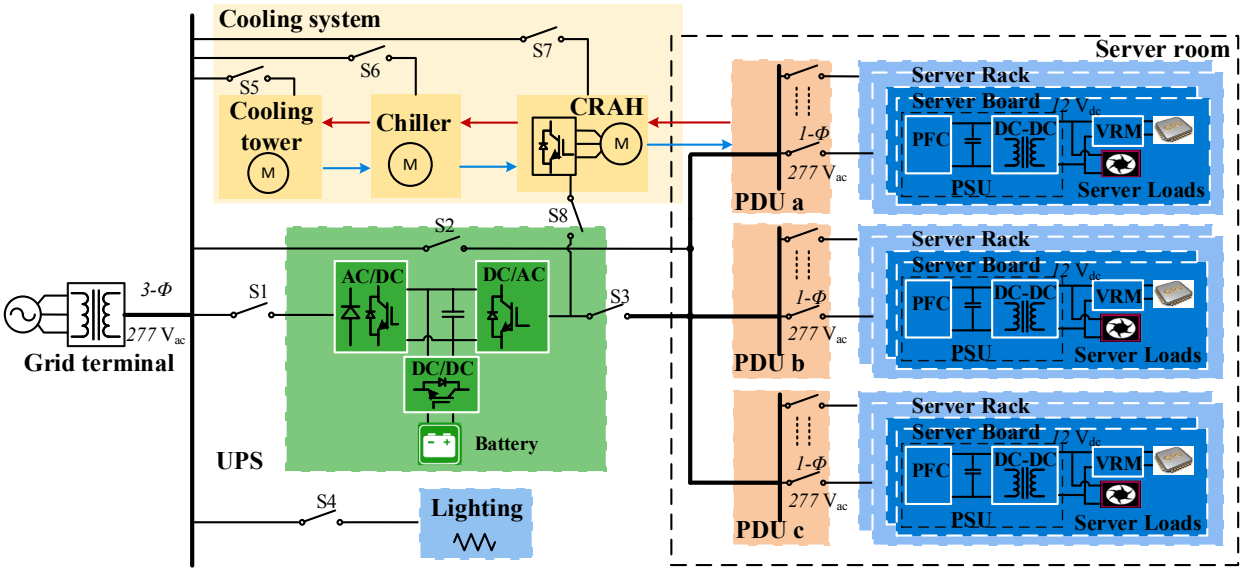
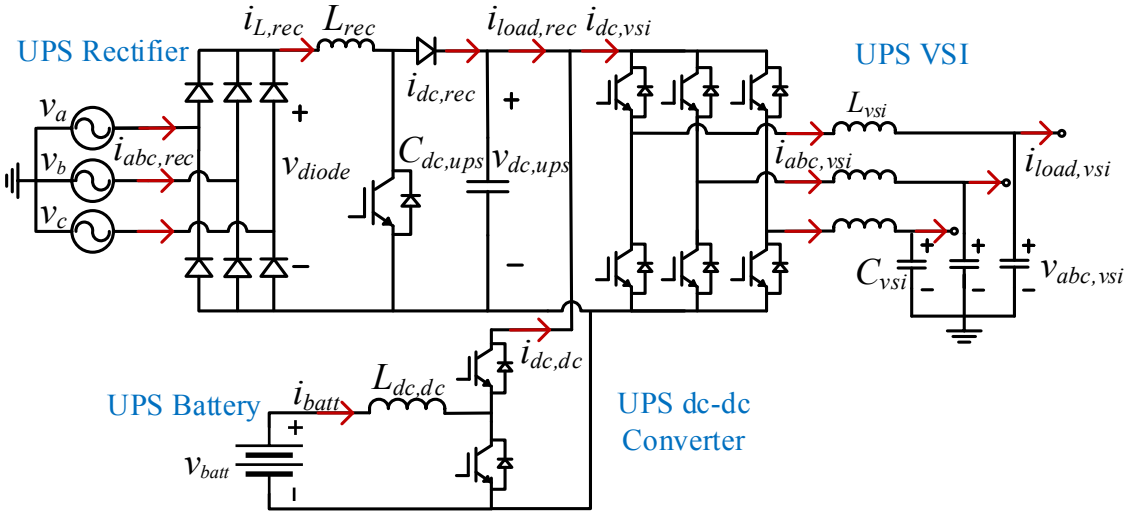
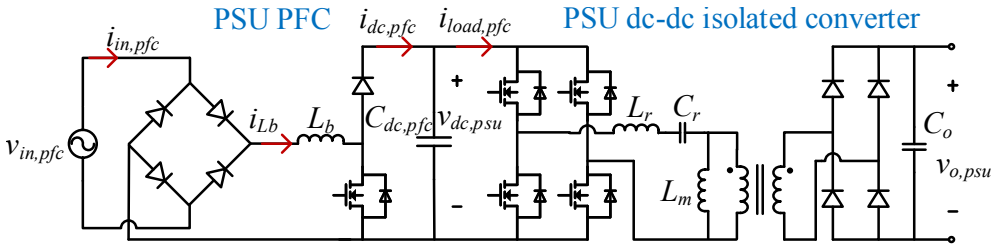


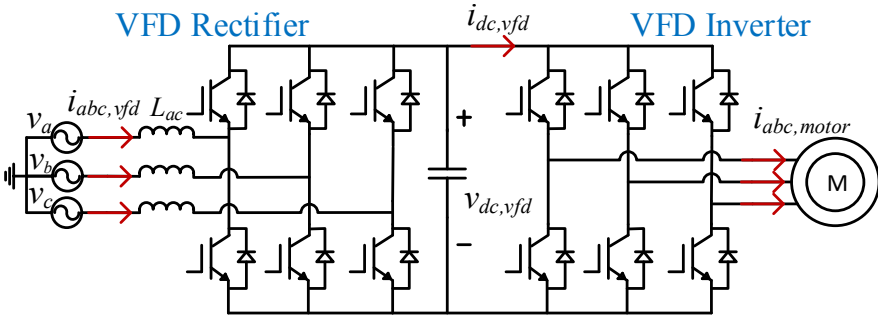
Figure 3.1: Typical structure of a Class F1 data center ac power distribution system.



(a)



(b)



(c)

Figure 3.2: Circuit topologies of the power converters in the data center system. (a) UPS circuit; (b) PSU circuit; (c) VFD-based motor circuit.

Table 3.1: Circuit topology and control methods of power converters in the data center.

UPS front-end rectifier	
Topology	3-phase boost-type PFC rectifier [170]
Nominal voltages	3-phase 480/277 V_{ac}, 60 Hz - 960 V_{dc}
Control method	Peak current control [191]
UPS inverter	
Topology	3-phase voltage source inverter [178]
Nominal voltages	960 V_{dc} - 3-phase 480/277 V_{ac}, 60 Hz
Control method	Dual-loop space vector control [192]
UPS dc-dc stage	
Topology	Half-bridge dc-dc converter
Nominal voltages	600 V_{dc}-960 V_{dc}
Control method	Average current mode control [193]
UPS battery	
Battery type	Lithium-ion battery [184]
Nominal voltage	600 V_{dc} with 2×182 cells
PSU PFC converter	
Topology	1-phase boost PFC converter [186]
Nominal voltages	1-phase 277 V_{ac}, 60 Hz - 480 V_{dc}
Control method	Average current mode control
PSU dc-dc isolated converter	
Topology	Full-bridge LLC converter [188]
Nominal voltages	480 V_{dc} - 48 V_{dc}
Control method	Variable frequency control [194]
CRAH VFD front-end rectifier	
Topology	3-phase active boost rectifier [178]
Nominal voltages	3-phase 480/277 V_{ac}, 60 Hz - 800 V_{dc}
Control method	Dual-loop space vector control
CRAH VFD inverter	
Topology	3-phase voltage source inverter
Control method	Constant V/Hz control [195]

3.1.2 Operation Principle

The principal task of the data center is to maintain reliable server operation regardless of the grid disturbances or power outage. In order to achieve this and improve the system power usage efficiency, data centers are normally implemented with multiple operation modes, which are realized by reconfigurable structures and controls [35, 196]. In this work, three widely-used operation modes are employed.

- *Normal Eco Mode* : When the utility power is within the acceptable limits, the UPS is bypassed, and the server loads are directly supported by the utility power through PDUs. To achieve seamless transition and reduce the start-up delay when power failure occurs, the UPS is turned on and operates at light load (*e.g.,* 1% load).

- *Double Conversion Mode* : When the utility voltage is not within the data center allowed range but still within the UPS input range, the static bypass is disconnected, and the UPS switches into double conversion mode. Server loads are directly fed by the regulated power from the UPS, and are not influenced by grid disturbances.

- *Battery Mode* : When power failure or severe grid interruption occurs, the UPS is disconnected from the grid and switches into battery mode, where the backup battery provides the dc power to the inverter. Server loads are continually supplied by the UPS until utility power is restored or an alternative power source comes online.

During severe power disruption, the cooling system, including the cooling tower, chiller, water pumps, and the CRAH, is disconnected from the grid [197]. To maintain the air circulation and keep the server room temperature within an acceptable range, CRAH is powered by the UPS backup power until the ac source is restored.

On the other hand, input power of the IT equipment should remain in the safe area as stipulated by the information technology industry council (ITIC), which means the operation mode transition time must be less than the allowed power downtime [198]. Considering the ITIC standard and commercial applications, an operation principle in response to different voltage levels is presented in Table 3.2, where S_1-S_8 correspond to switches in Figure 3.1.

Table 3.2: Data center operation modes in different voltage levels Figure 3.1.

Operation	$V_{t,pu}$	$t_{transition}$	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Normal eco mode	0.9 - 1.1	N/A	ON	ON	OFF	ON	ON	ON	ON	OFF
Double conversion mode	0.7 - 0.9	500 ms	ON	OFF	ON	ON	ON	ON	ON	OFF
Battery mode	≤ 0.7	20 ms	OFF	OFF	ON	ON	OFF	OFF	OFF	ON

3.2 Dynamic Data Center Power Model

In this section, a dynamic model of the data center power distribution system illustrated in Figure 3.1 is proposed. The circuit topologies, control methods, and system operation principle identified in Section 3.1 are adopted, and an average model that neglects switching ripple is built. All controller parameters are designed under pu system, so that the system can be scaled flexibly with different power ratings without rebuilding the controllers.

3.2.1 UPS Model

As shown in Figure 3.2(a), the UPS contains a three-phase front-end rectifier, a three-phase VSI, and energy storage system with battery pack and a dc-dc converter. The front-end rectifier conditions the input power and regulates the ac voltage into a dc voltage. The VSI further converts the dc voltage into an uninterrupted ac voltage to power the next stage. The battery, as the backup energy, is connected to the dc bus via a dc-dc converter, which controls the charging and discharging behavior of the battery.

3.2.1.1 UPS Rectifier Model

Advantageous in low cost and simple topology, the three-phase boost-type PFC rectifier is widely-used in UPS systems [170, 191]. The rectifier consists of a diode rectifier and a boost dc-dc converter. Peak current mode control including a current-programmed controller and a conventional voltage controller is adopted. In CCM operation, the average model of the boost converter is

$$\begin{cases} \bar{i}_{dc,rec} = \dfrac{\bar{v}_{diode}\bar{i}_{L,rec}}{\bar{v}_{dc,ups}} \\ \dfrac{d\bar{v}_{dc,ups}}{dt} = \dfrac{\bar{i}_{dc,rec}}{C_{dc,ups}} - \dfrac{\bar{i}_{load,rec}}{C_{dc,ups}} \end{cases} \tag{3.1}$$

Figure 3.3 shows the equivalent average model, where the switching network is represented by a current source and a dependent power sink. Figure 3.4 shows the control diagram of the boost dc-dc converter in pu system.

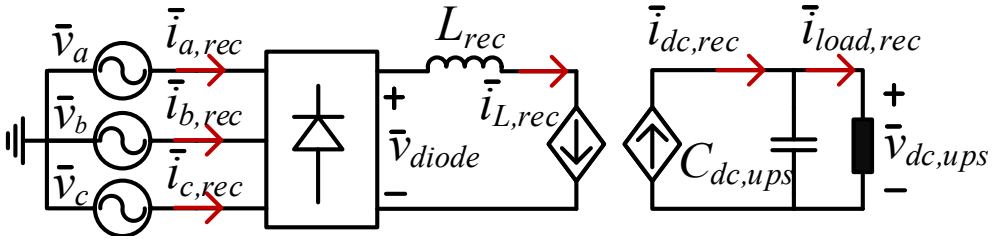


Figure 3.3: Average model of the three-phase boost-type PFC rectifier in UPS.

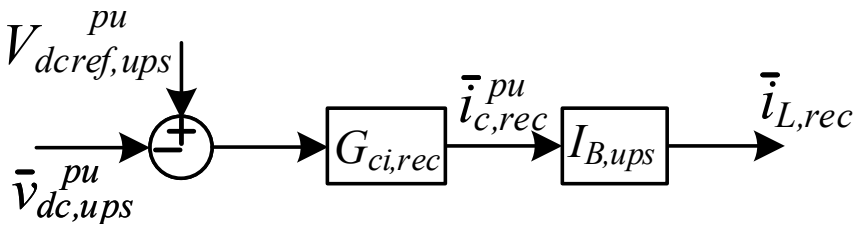


Figure 3.4: Control diagram of the three-phase boost-type PFC rectifier in UPS.

Assuming the input current is well regulated with near unity PF, the diode bridge can be modelled as

$$\begin{bmatrix} \bar{v}_{ab,rec} \\ \bar{v}_{ac,rec} \\ \bar{v}_{bc,rec} \\ \bar{v}_{ba,rec} \\ \bar{v}_{ca,rec} \\ \bar{v}_{cb,rec} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 0 & 1 & -1 \\ -1 & 1 & 0 \\ -1 & 0 & 1 \\ 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} \bar{v}_{a,rec} \\ \bar{v}_{b,rec} \\ \bar{v}_{c,rec} \end{bmatrix} \tag{3.2}$$

$$\bar{v}_{diode} = \max\{\bar{v}_{ab,rec}, \bar{v}_{ac,rec}, \bar{v}_{bc,rec}, \bar{v}_{ba,rec}, \bar{v}_{ca,rec}, \bar{v}_{cb,rec}\} \tag{3.3}$$

$$\begin{cases} \bar{i}_{a,rec} = \bar{i}_{L,rec},\ \bar{i}_{b,rec} = -\bar{i}_{L,rec},\ \bar{i}_{c,rec} = 0 & if\ \ \bar{v}_{diode} = \bar{v}_{ab,rec} \\ \bar{i}_{a,rec} = \bar{i}_{L,rec},\ \bar{i}_{b,rec} = 0,\ \bar{i}_{c,rec} = -\bar{i}_{L,rec} & if\ \ \bar{v}_{diode} = \bar{v}_{ac,rec} \\ \bar{i}_{a,rec} = 0,\ \bar{i}_{b,rec} = \bar{i}_{L,rec},\ \bar{i}_{c,rec} = -\bar{i}_{L,rec} & if\ \ \bar{v}_{diode} = \bar{v}_{bc,rec} \\ \bar{i}_{a,rec} = -\bar{i}_{L,rec},\ \bar{i}_{b,rec} = \bar{i}_{L,rec},\ \bar{i}_{c,rec} = 0 & if\ \ \bar{v}_{diode} = \bar{v}_{ba,rec} \\ \bar{i}_{a,rec} = -\bar{i}_{L,rec},\ \bar{i}_{b,rec} = 0,\ \bar{i}_{c,rec} = \bar{i}_{L,rec} & if\ \ \bar{v}_{diode} = \bar{v}_{ca,rec} \\ \bar{i}_{a,rec} = 0,\ \bar{i}_{b,rec} = -\bar{i}_{L,rec},\ \bar{i}_{c,rec} = \bar{i}_{L,rec} & if\ \ \bar{v}_{diode} = \bar{v}_{cb,rec} \end{cases} \tag{3.4}$$

3.2.1.2 UPS VSI Model

For the VSI, the average model is simplified using the synchronous dq coordinate system. The abc phase voltages and currents are transformed into dq coordinates by Park and Clarke transformations, which together create the following transformation matrix

$$T_{abc-dq0} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos\theta - \frac{2\pi}{3} & \cos\theta + \frac{2\pi}{3} \\ -\sin\theta & -\sin\theta - \frac{2\pi}{3} & -\sin\theta + \frac{2\pi}{3} \\ \sqrt{\frac{1}{2}} & \sqrt{\frac{1}{2}} & \sqrt{\frac{1}{2}} \end{bmatrix} \tag{3.5}$$

The average model of the VSI in dq axis is shown in Figure 3.5, and expressed as

$$\begin{cases} \frac{d\overrightarrow{\bar{i}_{dq,vsi}}}{dt} = \frac{\bar{v}_{dc,ups}}{L_{vsi}}\overrightarrow{\bar{d}_{dq,vsi}} - \frac{\overrightarrow{\bar{v}_{dq,vsi}}}{L_{vsi}} - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \overrightarrow{\bar{i}_{dq,vsi}} \\ \frac{d\overrightarrow{\bar{v}_{dq,vsi}}}{dt} = \frac{\overrightarrow{\bar{i}_{dq,vsi}}}{C_{vsi}} - \frac{\overrightarrow{\bar{i}_{load\_dq,vsi}}}{C_{vsi}} - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \overrightarrow{\bar{v}_{dq,vsi}} \\ \bar{i}_{dc,vsi} = \overrightarrow{\bar{d}_{dq,vsi}}^T \overrightarrow{\bar{i}_{dq,vsi}} \end{cases} \tag{3.6}$$

Traditional dual-loop space vector control is used to control the VSI voltage and power [192], as presented in Figure 3.6. The sensed three-phase voltages and currents are converted into dq coordinate and used as feedback signals for the outer voltage loop and inner current loop. With the dual-loop control, the converter real power and reactive power are regulated in the d-axis and q-axis respectively.

3.2.1.3 Half-Bridge dc-dc Converter Model

The bidirectional half-bridge dc-dc converter is used to control the active power by charging and discharging the battery, and regulate the dc link voltage during the battery mode when UPS rectifier is off. When the battery is charged, it serves as a buck converter stepping down the dc bus voltage $v_{dc,ups}$ to the battery terminal voltage v_{batt}. When the power flow reverses for battery discharging, it behaves like a boost converter amplifying v_{batt} to $v_{dc,ups}$. With the average current mode control, the converter average model is presented in Figure 3.7 and (3.7).

$$\begin{cases} \frac{d\bar{i}_{batt}}{dt} = \frac{\bar{v}_{batt}}{L_{dcdc}} - (1 - \bar{d}_{dcdc})\frac{\bar{v}_{dc,ups}}{L_{dcdc}} \\ \bar{i}_{dcdc} = (1 - \bar{d}_{dcdc})\bar{i}_{batt} \end{cases} \tag{3.7}$$

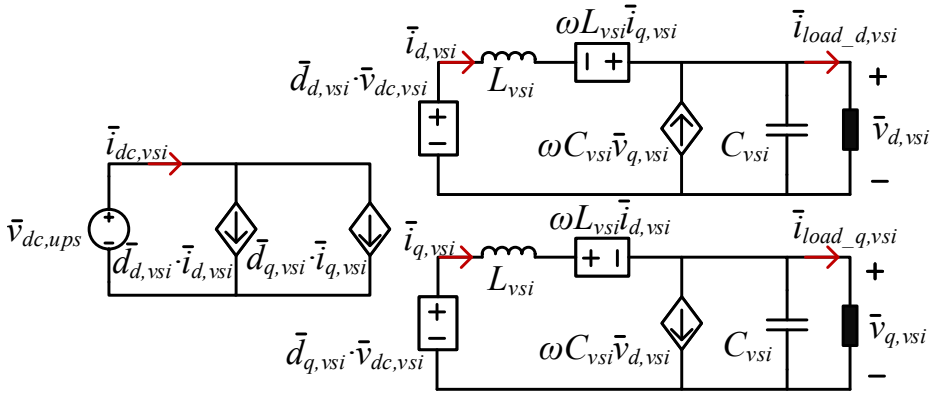


Figure 3.5: Average model of the three-phase VSI in UPS.

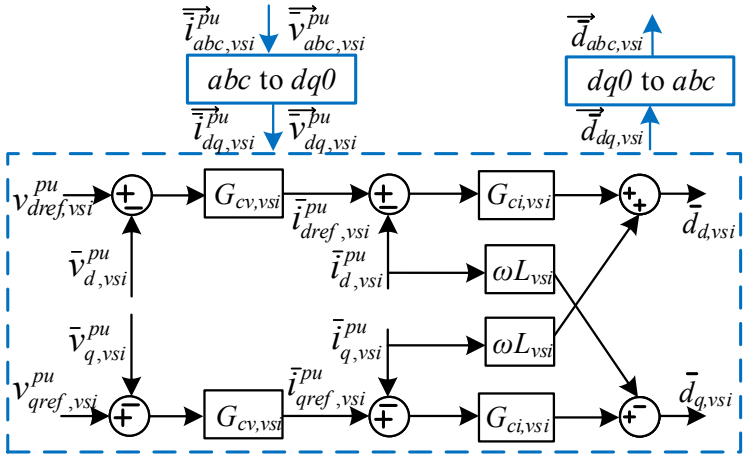


Figure 3.6: Control diagram of the three-phase VSI in UPS.

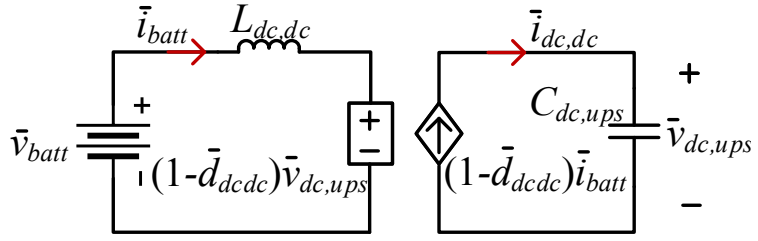


Figure 3.7: Average model of the dc-dc converter in UPS.

Control of the dc-dc converter depends on the system operation mode. During the normal eco mode and double conversion mode, the UPS dc link voltage is regulated by the rectifier, and the dc-dc converter is responsible for charging or discharging the battery. As elaborated in Figure 3.8, the inductor average current is controlled by a proportional integrator (PI) controller, and the current reference is determined by a charging/discharging algorithm. As shown in Algorithm 1, the battery is charged when active power command $P^{pu}_{ref,batt}$ is negative and state-of-charge (SOC) is lower than the maximum value SOC_{max} at 98%, and discharged when $P^{pu}_{ref,batt}$ is positive and SOC is higher than the minimum value SOC_{min} at 20%.

Algorithm 1: Current reference for battery charging and discharging

Input:
$P^{pu}_{ref,batt}$: battery active power reference in pu;
$\bar{v}^{pu}_{batt}$: battery pack terminal voltage in pu;
SOC : battery SOC;
Output:
$\bar{i}^{pu}_{batt\_ref}$: current reference for dc-dc converter in pu;
Procedure:

```
if P^pu_ref,batt > 0 then
    if SOC > SOC_min then
        ī^pu_batt_ref = P^pu_ref,batt ÷ v^pu_batt;        // battery is discharged
    else
        ī^pu_batt_ref = 0;
else if P_ref,batt < 0 then
    if SOC < SOC_max then
        ī^pu_batt_ref = P^pu_ref,batt ÷ v̄^pu_batt;        // battery is charged
    else
        ī^pu_batt_ref = 0;
else
    ī^pu_batt_ref = 0;                                    // battery stands by
```

When the system operates in battery mode, the UPS rectifier is turned off, and server loads are supplied by the battery energy via the VSI. Hence, the dc-dc converter needs to regulate $v_{dc,ups}$ and control the battery discharging, where an outer voltage loop is added, as shown in Figure 3.9.

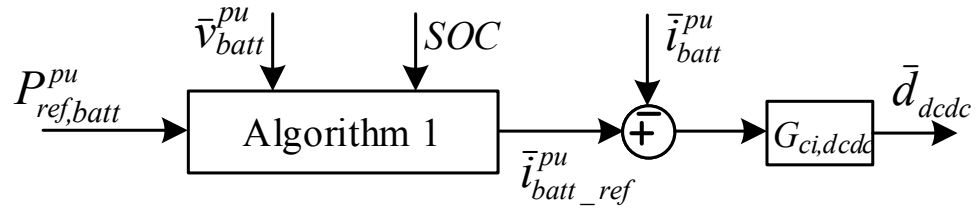


Figure 3.8: Average current mode control of the dc-dc converter in UPS.

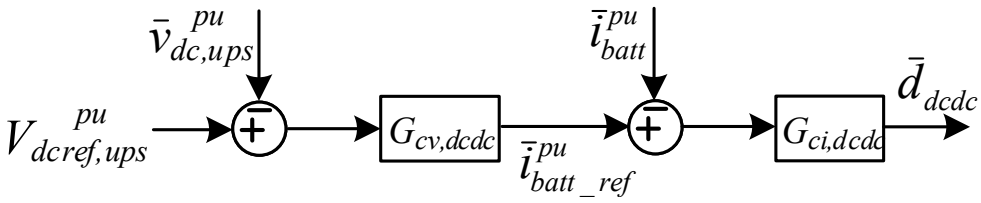


Figure 3.9: Dual-loop control of the dc-dc converter during the battery mode.

3.2.1.4 Li-ion Battery Pack Model

The UPS battery pack is composed of 2-paralleled battery strings of 182 Li-ion battery cells. Assuming all battery cells have the same internal characteristics and the battery current/voltage are evenly distributed, modeling the battery pack is equivalent to model the battery cell.

As shown in Figure 3.10, the equivalent circuit proposed in [1] is used to model the battery's charging and discharging performance. With the current controlled by the dc-dc converter, the battery's SOC is calculated based on the coulomb counting (CC) method [199], as expressed in (3.8). The battery's terminal voltage v_{cell} is represented as the function of the battery current i_{cell}, nominal open-circuit voltage E_{ocv}, series resistance R_o, a polarization constant K, an exponential zone amplitude A, and an inverse exponential zone time constant B. Mathematical calculations of v_{cell} in discharging and charging modes are shown in (3.9) and (3.10). The Li-ion battery demonstrates similar terminal voltage performance except for a small change due to the polarization between discharging and charging process [1]. In both modes, identical battery cell parameters are used as listed in Table 3.3.

$$SOC_{cell} = SOC_0 - \frac{\int_0^t \bar{i}_{cell} dt}{Q_{cell}} \tag{3.8}$$

In discharging mode,

$$\bar{v}_{cell} = E_{ocv} - R_o \bar{i}_{cell} - \frac{KQ_{cell} \int_0^t \bar{i}_{cell} dt}{Q_{cell} - \int_0^t \bar{i}_{cell} dt} - \frac{KQ_{cell} \bar{i}_{cell}}{Q_{cell} - \int_0^t \bar{i}_{cell} dt} + Ae^{-B \int_0^t \bar{i}_{cell} dt} \tag{3.9}$$

In charging mode,

$$\bar{v}_{cell} = E_{ocv} - R_o \bar{i}_{cell} - \frac{KQ_{cell} \int_0^t \bar{i}_{cell} dt}{Q_{cell} - \int_0^t \bar{i}_{cell} dt} - \frac{KQ_{cell} \bar{i}_{cell}}{\int_0^t \bar{i}_{cell} dt - Q_{cell}} + Ae^{-B \int_0^t \bar{i}_{cell} dt} \tag{3.10}$$

Then, the battery pack terminal voltage v_{batt}, current i_{batt}, and SOC are calculated by scaling the cell-level behaviors, as

$$\bar{v}_{batt} = N_{series} \bar{v}_{cell}, \quad \bar{i}_{batt} = N_{parallel} \bar{i}_{cell}, \quad SOC = SOC_{cell} \tag{3.11}$$

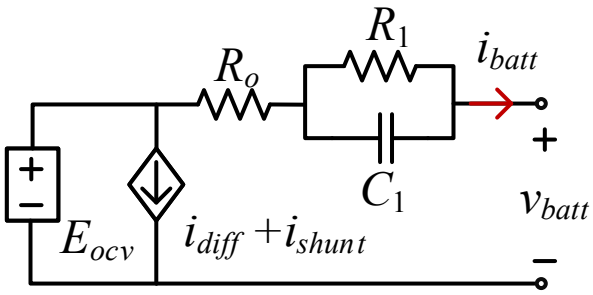


Figure 3.10: Thevenin electrical model of Li-ion battery cell [1].

Table 3.3: Lithium-ion battery dynamic model parameters [1].

Q_{cell}(Ah)	E_{ocv}(V)	$R_o(\Omega)$	$K(\Omega)$	A(V)	B(Ah^{-1})
2.3	3.366	0.01	0.0076	0.26422	26.5487

3.2.1.5 Combined UPS Average Model

Figure 3.12 shows the combined UPS average model. It should be noted that the UPS dc bus voltage and current are modeled differently in various operation modes.

- In normal eco mode and double conversion mode, $v_{dc,ups}$ is regulated by the rectifier.

$$C_{dc,ups}\frac{d\bar{v}_{dc,ups}}{dt} = \bar{i}_{dc,rec} + \bar{i}_{dc,dc} - \bar{i}_{dc,vsi} \tag{3.12}$$

- In battery mode, $v_{dc,ups}$ is controlled by the battery dc-dc converter.

$$C_{dc,ups}\frac{d\bar{v}_{dc,ups}}{dt} = \bar{i}_{dc,dc} - \bar{i}_{dc,vsi} \tag{3.13}$$

3.2.2 PSU Model

3.2.2.1 Single-Phase PFC Model

Advantageous in small current ripple, low cost, and natural filtering effect, single-phase boost PFC with CCM operation is extensively used in data center applications, and average current mode control is predominately adopted [105]. Assuming $i_{in,pfc}$ is regulated in phase with $v_{in,pfc}$ and the diode forward voltage drop is neglected, the average model of the PFC converter is presented in (3.14) and Figure 3.11.

$$\begin{cases} \bar{v}_{diode,pfc} = |\bar{v}_{in,pfc}| \\ \frac{d\bar{i}_{Lb}}{dt} = \frac{\bar{v}_{in,pfc}}{L_b} - (1-d_{pfc})\frac{\bar{v}_{dc,psu}}{L_b} \\ \frac{d\bar{v}_{dc,psu}}{dt} = (1-d_{pfc})\frac{\bar{i}_{Lb}}{C_{dc,psu}} - \frac{\bar{i}_{load,pfc}}{C_{dc,psu}} \end{cases} \tag{3.14}$$

Conventional dual-loop control is employed, as illustrated in Figure 3.13. The outer voltage loop regulates the dc link voltage and generates the average current reference. To avoid the influence of the double-line frequency ripple, voltage control bandwidth is usually designed well below the line frequency (typically < 20 Hz). The inner current loop compensates the average inductor current to achieve unity PF, and the control bandwidth is much faster.

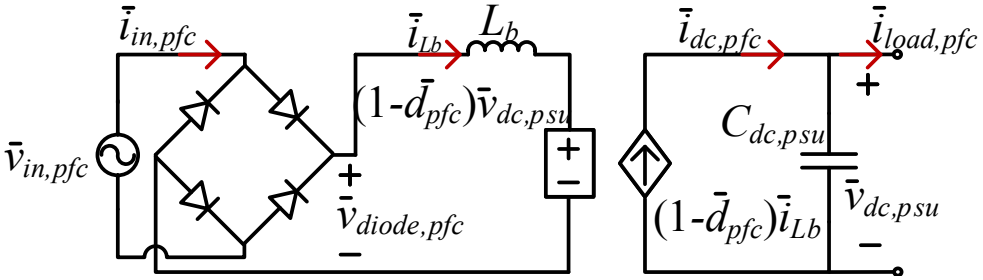


Figure 3.11: Average model of the boost PFC rectifier.

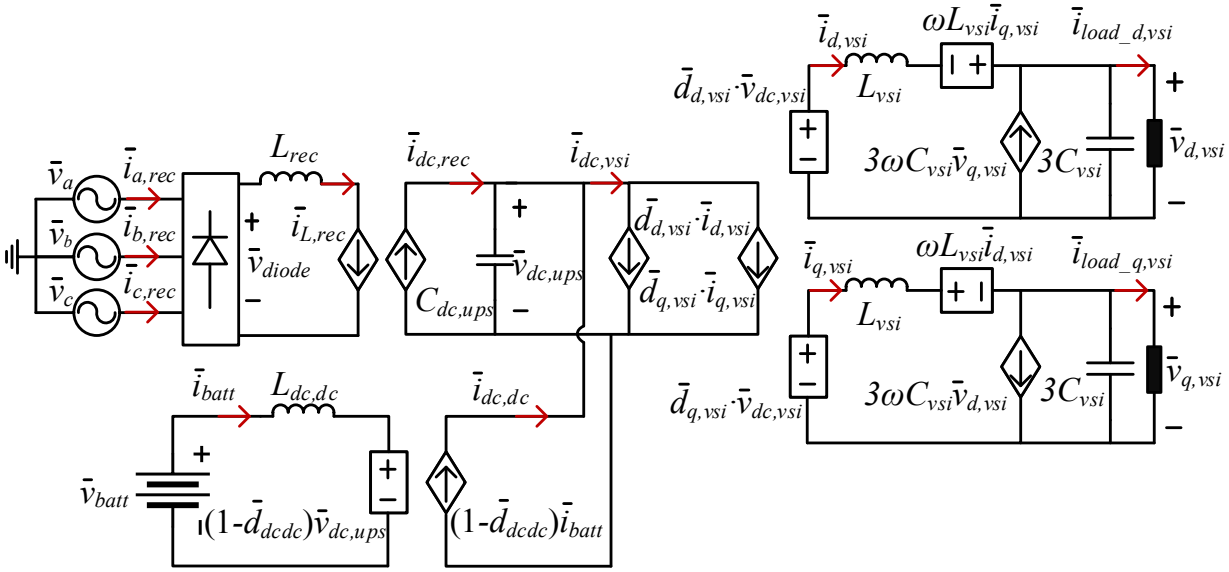


Figure 3.12: UPS average model.

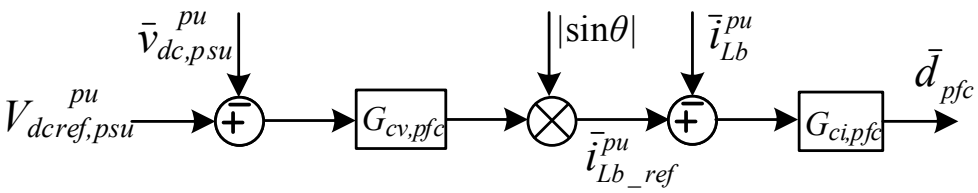


Figure 3.13: Control diagram of the boost PFC converter.

3.2.2.2 Dc-dc Isolated Converter Model

Dc-dc isolated converter is required to step down the voltage for the server board, and isolate the high voltage and low voltage to ensure safety. Conventional resonant phase-shift PWM converters are limited by the low efficiency at light load and wide input voltage range. Nowadays, LLC resonant converter is popular in the isolated dc-dc stage, which has benefits in full-load range zero voltage switching (ZVS) capability and high-efficiency operation with wide input variation [152]. To regulate the output voltage within the acceptable range, variable frequency control is normally used in the LLC converter [194].

Modeling of the LLC converter is nontrivial, since the traditional average model is not adaptable for such high-frequency resonant circuit. Nevertheless, it is not necessary to have the detailed LLC model in the data center emulator. For present LLC converters operating at 50 kHz – 200 kHz, the control bandwidth is usually designed at 1 kHz – 5 kHz. Compared with the PFC slow voltage loop, the dc-dc converter is fully decoupled from the PFC converter in the control perspective, and has little effect on the ac input terminal. In addition, it is verified that, in the low-frequency range within the control loop bandwidth, the LLC converter has a negative input impedance and behaves like a constant power load [200]. Therefore, in the emulator, the isolated LLC dc-dc converter is simplified as a controlled power load depending on the server load.

3.2.3 Cooling System Model

Motors are the predominant electrical components in the cooling system. In the model, an aggregated grid-connected induction motor is used to represent the cooling tower, chiller, and water pumps. CRAH is modeled by an induction motor with variable frequency drive for speed regulation.

3.2.3.1 Induction Motor Model

The dynamic induction motor model illustrated in [201] is used to obtain the transient behaviors, as shown in Figure 3.14 and (3.15)-(3.18).

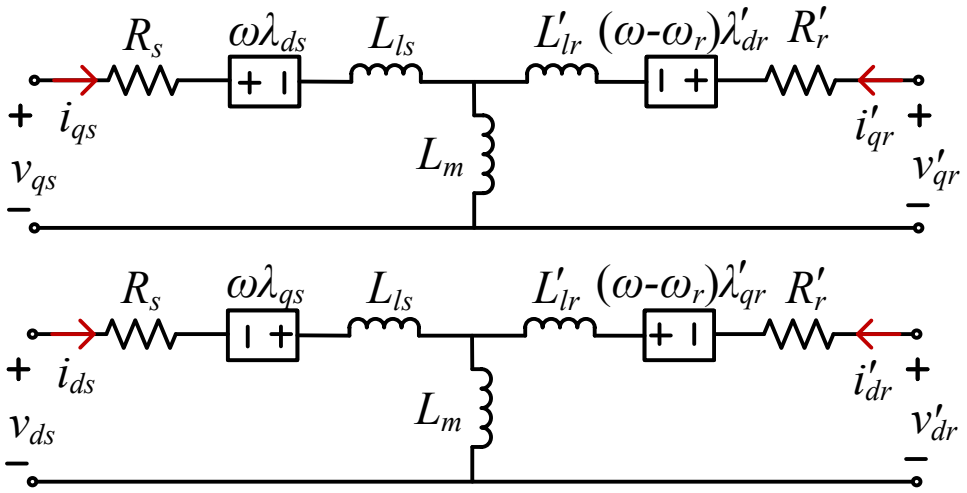


Figure 3.14: Equivalent circuit of the induction motor in dq axis.

$$\begin{cases} v_{qs} = R_s i_{qs} + \omega\lambda_{ds} + \frac{d\lambda_{qs}}{dt} \\ v_{ds} = R_s i_{ds} - \omega\lambda_{qs} + \frac{d\lambda_{ds}}{dt} \end{cases} \tag{3.15}$$

$$\begin{cases} v_{qr}^{'} = R_r^{'} i_{qr}^{'} + (\omega - \omega_r)\lambda_{dr}^{'} + \frac{d\lambda_{qr}^{'}}{dt} \\ v_{dr}^{'} = R_r^{'} i_{dr}^{'} - (\omega - \omega_r)\lambda_{qr}^{'} + \frac{d\lambda_{dr}^{'}}{dt} \end{cases} \tag{3.16}$$

$$\begin{cases} \lambda_{qs} = L_{ls} i_{qs} + L_m(i_{qs} + i_{qr}^{'}) \\ \lambda_{ds} = L_{ls} i_{ds} + L_m(i_{ds} + i_{dr}^{'}) \end{cases} \tag{3.17}$$

$$\begin{cases} \lambda_{qr}^{'} = L_{lr}^{'} i_{qr}^{'} + L_m(i_{qs} + i_{qr}^{'}) \\ \lambda_{dr}^{'} = L_{lr}^{'} i_{dr}^{'} + L_m(i_{ds} + i_{dr}^{'}) \end{cases} \tag{3.18}$$

$$T_e = (\frac{3}{2})(\frac{P}{2})L_m(i_{qs} i_{dr}^{'} - i_{ds} i_{qr}^{'}) \tag{3.19}$$

$$\frac{d\omega_r}{dt} = \frac{P}{2J}(T_e - T_L) \tag{3.20}$$

In the equations, v_{ds} and v_{qs} are variables for stator terminal voltage in d axis and q axis; i_{ds} and i_{qs} are variables for stator current in d axis and q axis; λ_{ds} and λ_{qs} are variables for stator flux linkage in d axis and q axis; R_s is the stator resistance; L_{ls} is the stator leakage inductance. Correspondingly, $v_{dr}^{'}$ and $v_{qr}^{'}$, $i_{dr}^{'}$ and $i_{qr}^{'}$, $\lambda_{dr}^{'}$ and $\lambda_{qr}^{'}$, $R_r^{'}$, and $L_{lr}^{'}$ are variables for rotor voltage, current, flux linkage, resistance, and leakage inductance which are already converted to the stator side with

$$\begin{cases} v_{dr}^{'} = \frac{N_s}{N_r} v_{dr}, v_{qr}^{'} = \frac{N_s}{N_r} v_{qr} \\ i_{dr}^{'} = \frac{N_r}{N_s} i_{dr}, i_{qr}^{'} = \frac{N_r}{N_s} i_{qr} \\ \lambda_{dr}^{'} = \frac{N_s}{N_r}\lambda_{dr}, \lambda_{qr}^{'} = \frac{N_s}{N_r}\lambda_{qr} \\ R_r^{'} = (\frac{N_s}{N_r})^2 R_r \\ L_{lr}^{'} = (\frac{N_s}{N_r})^2 L_{lr} \end{cases} \tag{3.21}$$

Also, N_s, N_r denote the numbers of winding turns in the stator and rotor,L_m is the mutual inductance; ω is the stator electrical angular frequency; ω_r is the rotor rotation angular frequency; P is the number of poles; J is the moment of inertia of the rotor; T_e is the electric torque generated from the motor; T_L is the load torque.

3.2.3.2 VFD Model

As shown in Figure 3.2(c), the VFD contains an active front-end boost rectifier and a VSI. Based on the traditional modeling method [178], the average model of the three-phase rectifier can be transformed into dq coordinates by Park and Clarke transformations, as expressed in (3.22) and Figure 3.15.

$$\begin{cases} \frac{d\overrightarrow{\bar{i}_{dq,vfd}}}{dt} = \frac{\overrightarrow{\bar{v}_{dq,vfd}}}{L_{vfd}} - \frac{\bar{v}_{dc,vfd}}{L_{vfd}}\overrightarrow{\bar{d}_{dq,vfd}} - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \overrightarrow{\bar{i}_{dq,vfd}} \\ \frac{d\bar{v}_{dc,vfd}}{dt} = \frac{1}{C_{dc,vfd}}\overrightarrow{\bar{d}_{dq,vfd}}^T\overrightarrow{\bar{i}_{dq,vfd}} - \frac{1}{C_{dc,vfd}}\bar{i}_{load,vfd} \end{cases} \tag{3.22}$$

Figure 3.16 shows the rectifier control. The dc bus voltage V_{dc} is regulated through the outer loop in the d-axis, and the current reference i_{dq} is generated to control the real power in the inner current loop. Reactive power is controlled in the q-axis inner current loop, where the current reference is predicted based on the required reactive power.

The VSI is used to generate flexible ac power and control the induction motor speed. Among all the induction motor drive strategies, open-loop volt-per-hertz (V/Hz) control is the simplest and least expensive one, which is employed in the model [201]. Such a speed control strategy is based on two observations. The first one is that the torque speed characteristic of an induction machine is normally quite steep in the neighborhood of the synchronous speed. Thus, the electrical rotor speed is near to the electrical frequency, and the motor speed can be controlled by controlling the frequency. The second one is that, at steady state, the flux leakage term dominates the resistive term in the voltage equation. In order to maintain constant flux leakage, the stator voltage magnitude should be proportional to the frequency. Therefore, the motor speed can be regulated by the stator voltage through a constant V/Hz ratio.

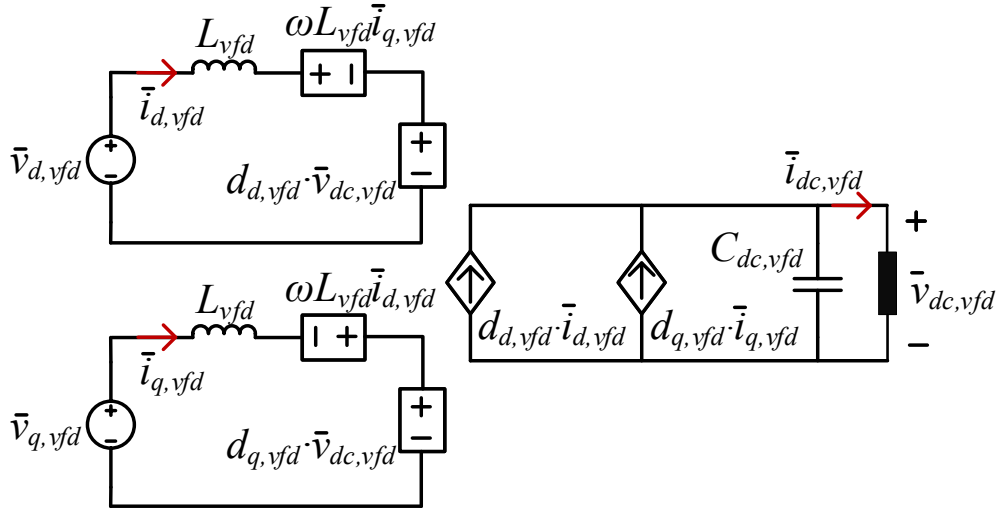


Figure 3.15: Average model of the three-phase boost rectifier in dq axis.

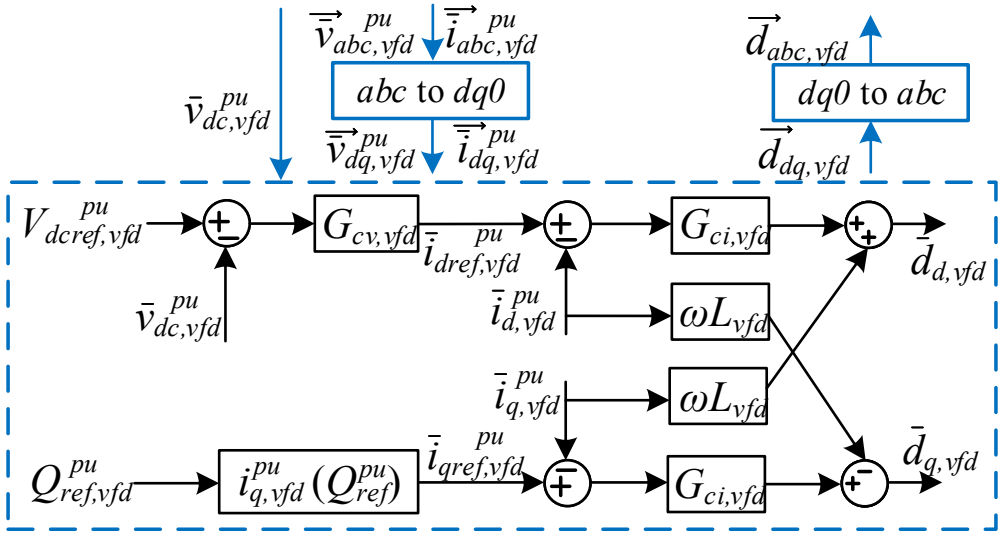


Figure 3.16: Control diagram of the three-phase boost rectifier in dq axis.

Implementation of the V/Hz control is shown in Figure 3.17. The mechanical speed command ω_m is first constrained by a slew rate limiter (SRL), and multiplied by the pole pair number $^P/_2$ to obtain the electrical frequency ω_r. Then ω_r is multiplied by V/Hz ratio V_b/ω_b, where V_b is the rated voltage, and ω_b is the rated radian frequency in order to form an rms voltage command V_s. V_s is then multiplied by $\sqrt{2}$ in order to obtain a q-axis voltage command v_{qs}. The d-axis voltage command is set to zero. In a parallel path, ω_r is integrated to determine the position of a synchronous reference frame θ_r. Together, v_{qs} and v_{ds} can then be passed to one of the modulation strategies to achieve the commanded voltage.

3.2.4 Server and Cooling Load Model

3.2.4.1 Server Load Model

Modeling the power consumption of server loads is challenging, because there are multiple categories and the power consumption is relative to different factors like the core voltage, switching frequency, load capacitance, etc. Various linear and nonlinear power models have been studied to estimate the server load power consumption [202], among which the server utilization based linear power models are extensively used [203, 204, 4]. In this work, the server power consumption is modeled with a linear model, which has an approximately linear increase with the server utilization rate [205, 206], as shown in (3.23).

$$P_{server} = P_{idle} + (P_{rated} - P_{idle})u \tag{3.23}$$

where P_{server} represents the power consumption of a server, P_{idle} is the power consumed in idle mode, P_{rated} is the server power rating, and u stands for the server utilization rate which varies from 0% to 100%. Assuming load balancing is realized, the total server load is

$$P_{tot,server} = N_{rack} N_{server} P_{server} \tag{3.24}$$

where N_{rack} and N_{server} represent the number of racks and the number of servers per rack.

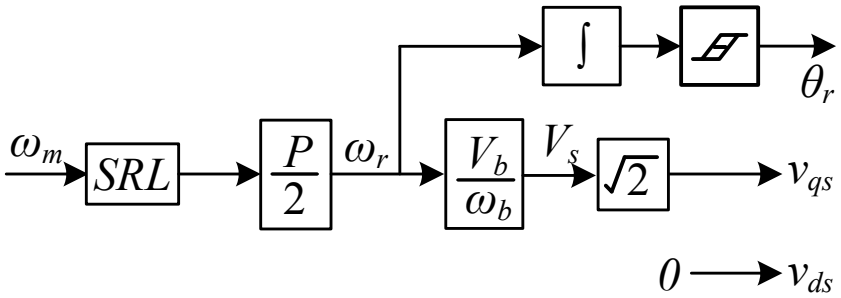


Figure 3.17: Volt-per-hertz (V/Hz) control of the VFD VSI.

3.2.4.2 Cooling Load Model

Cooling system modeling is also an active research area, where different models are developed to estimate the thermal load and improve the thermal management by optimizing the room temperature and air flow cycle and etc. [9]. In this work, a coherent cooling power load model is built based on approaches used in [61, 58]. The cooling load model is divided into five modules: server fans, CRAH, chiller, cooling tower, and water pumps.

Server fan power consumption is assessed with the required air flow rate which is determined by the server power. Assuming N_{fan} fans are used for one server, the required air flow per server is calculated as

$$f_{air,server} = \frac{P_{server}}{\eta_{server} \triangle T_{sir,server} \rho_{air} c_{air}} \quad (\mathrm{m}^3/\mathrm{s}) \tag{3.25}$$

where η_{server} represents the efficiency of the power supply for supplying the server load, $\rho_{air} = 1.18$ kg/m^3 is the air density, $c_{air} = 1010$ J/(kg°C) is the air heat capacity, and $\triangle T_{air,server} = 13.5$ °C is the allowable temperature range. Based on guidance from American Society of Heating, Refrigerating and Air-Conditioning Engineers (ASHRAE), the recommended server room temperature is $18 - 27$ °C, and the allowed temperature range is 5 °C to 45 °C [207]. Then the fan power consumption for each server is estimated based on the third fan law as

$$P_{fan,server} = P_{rated,fan} \frac{f^3_{air,server}}{f^3_{0fan,server}} \quad (\mathrm{W}) \tag{3.26}$$

where $P_{rated,fan}$ is the fan power rating, $f_{0,fan}$ is the nominal air flow rate. Multiplied by the number of servers, the total air flow rate and the fans' power consumption in the server room are

$$f_{air,room} = (1-k) N_{rack} N_{server} f_{air,server} \quad (\mathrm{m}^3/\mathrm{s}) \tag{3.27}$$

$$P_{fan,room} = N_{rack} N_{server} P_{fan,server} \quad (\mathrm{W}) \tag{3.28}$$

where k serves as the re-circulation index, denoting the ratio of the exhausting air that re-circulates with the cool air from the CRAH. $k = 0$ means there is no re-circulated air and $k = 0.3$ shows 30% of the air is re-circulated.

The CRAH is used to remove the hot air from the server room, and inject cold air into the server room, and the power load depends on the air flow rate $f_{air,room}$ in the room outlet and inlet. Usually, there are two fans as the CRAH load, of which one is for pulling hot air in the room outlet, and the other one is for pushing cold air in the room inlet. Assuming the two fans have the same air flow rates and are driven by one motor, the CRAH power load is calculated in (3.29), and the required mechanical rotation speed and load torque of the CRAH motor are expressed in (3.30) and (3.31)

$$P_{load,CRAH} = P_{rated,CRAH} \frac{f_{air,room}^3}{f_{0fan,CRAH}^3} \quad \text{(W)} \tag{3.29}$$

$$\omega_{rm,CRAH} = \omega_{0rm,CRAH} \frac{f_{air,room}}{f_{0fan,CRAH}} \quad \text{(rad/s)} \tag{3.30}$$

$$T_{load,CRAH} = \frac{P_{load,CRAH}}{\omega_{rm,CRAH}} \quad \text{(N/s)} \tag{3.31}$$

where $P_{rated,CRAH}$ is the CRAH rated output power, $f_{0fan,CRAH}$ and $\omega_{0rm,CRAH}$ are the nominal fan speeds.

The hot air from the CRAH is transmitted to the chiller to be cooled down. The chiller power load can be predicted based on the thermal load and the coefficient of performance (COP). The chiller thermal load is actually the heat transferred from CRAH, which is estimated as

$$Q_{chiller} = (1-k)Q_{CRAH} = 1158.2 f_{air,room} \triangle T_{air,CRAH} \quad \text{(W)} \tag{3.32}$$

where $\triangle T_{air,CRAH}$ is the temperature difference between the hot air into the CRAH and the cold air out of the CRAH, and is calculated as

$$\triangle T_{air,CRAH} = \frac{P_{fan,room} + P_{loss,PSU}}{f_{air,room} \rho_{air} c_{air}} \quad (^\circ\text{C}) \tag{3.33}$$

Chiller COP can be estimated based on the water temperature flowing through the chiller.

$$\triangle T_{w,chiller} = \frac{Q_{chiller}}{f_{w,chiller} \rho_w c_w} \quad (^\circ\text{C}) \tag{3.34}$$

$$COP_{chiller} = \frac{T_{wcold,chiller}}{\triangle T_{w,chiller}} \tag{3.35}$$

where $T_{wcold,chiller}$ is the cold water temperature in the chiller, $f_{w,chiller}$ is the chiller water flow rate, $\rho_w = 998.68$ kg/m^3 is the water density, and $c_w = 4187$ J/(kg°C) is the water heat capacity. Therefore, the chiller power load is estimated as

$$P_{load,chiller} = \frac{Q_{chiller}}{COP_{chiller}} \quad \text{(W)} \tag{3.36}$$

Cooling tower is responsible for cooling down the hot water from the chiller, and taking away the heat from the UPS, chiller, CRAH, and other power components. In the model, the cooling tower thermal load is estimated as

$$Q_{CT} = Q_{chiller} + P_{loss,UPS} + P_{loss,CRAH} + P_{loss,chiller} \quad \text{(W)} \tag{3.37}$$

And the COP of cooling tower is determined with

$$\triangle T_{w,CT} = \frac{Q_{CT}}{f_{w,CT}\rho_w c_w} \quad (^\circ\text{C}) \tag{3.38}$$

$$COP_{CT} = \frac{T_{wcold,CT}}{\triangle T_{w,CT}} \tag{3.39}$$

where $T_{wcold,CT}$ is the cold water temperature in the cooling tower, $f_{w,CT}$ is the cooling tower water flow rate. Hence, the power load of the cooling tower is

$$P_{load,CT} = \frac{Q_{CT}}{COP_{CT}} \quad \text{(W)} \tag{3.40}$$

Typically, two water pumps are required; one to push the water flow on the chiller side and one to push the water flow on the cooling tower side. With the water flow rates $f_{w,chiller}$, $f_{w,CT}$ and water temperature differences $\triangle T_{w,chiller}$, $\triangle T_{w,CT}$ in the chiller and cooling tower, power loads of the two water pumps are calculated as

$$P_{load,pump1} = 2.79 \times 10^5 f_{w,chiller} \triangle T_{w,chiller} \quad \text{(W)} \tag{3.41}$$

$$P_{load,pump2} = 2.79 \times 10^5 f_{w,CT} \triangle T_{w,CT} \quad \text{(W)} \tag{3.42}$$

Based on the above load models, the total power load of the data center at normal steady state is calculated as

$$P_{load} = \frac{P_{tot,server+P_{fan,room}}}{\eta_{PSU}} + \frac{P_{load,CRAH}}{\eta_{CRAH}} + \frac{P_{load,chiller}}{\eta_{chiller}} + \frac{P_{load,CT}}{\eta_{CT}} + \frac{P_{load,pump}}{\eta_{pump}} \tag{3.43}$$

where η_{PSU}, η_{CRAH}, $\eta_{chiller}$, η_{CT}, η_{pump} are efficiencies of the power processing components. The coherent power load model is illustrated in Figure 3.18.

3.2.5 Simulation

3.2.5.1 Scaled Data Center System

A scaled data center ac power distribution system is defined according to the circuits, controls, and operation principle identified in Section 3.1. Table 3.4 presents the data center system configuration, and Table 3.5 shows the detailed design of each power component. Figure 3.19 presents the data center active power consumption at various server utilization rates. When $u = 100\%$, the total active power consumption is 12.78 kW, where the server load and the cooling load account for 61% and 32.5%, respectively, of the total.

Simulation of the proposed data center model is built in Matlab Simulink. Figure 3.20 displays the simulated terminal voltage $v_{abc,pu}$, current $i_{abc,pu}$, and power of the data center at steady state with 100% server utilization. In Figure 3.20(a), the data center operates in normal eco mode, and $i_{abc,pu}$ is sinusoidal. When $v_{abc,pu}$ is lower than the acceptable limit (Figure 3.20(b)), the data center works in double conversion mode, and the UPS regulates the ac power for server loads. Since a six-pulse diode rectifier is used in the UPS, $i_{abc,pu}$ is severely distorted, and $P_{t,pu}$, $Q_{t,pu}$ have significant ripples. Although both cases achieve displacement PF at around 0.99, the current THD is 20.25% in double conversion mode, leading to 0.97 PF.

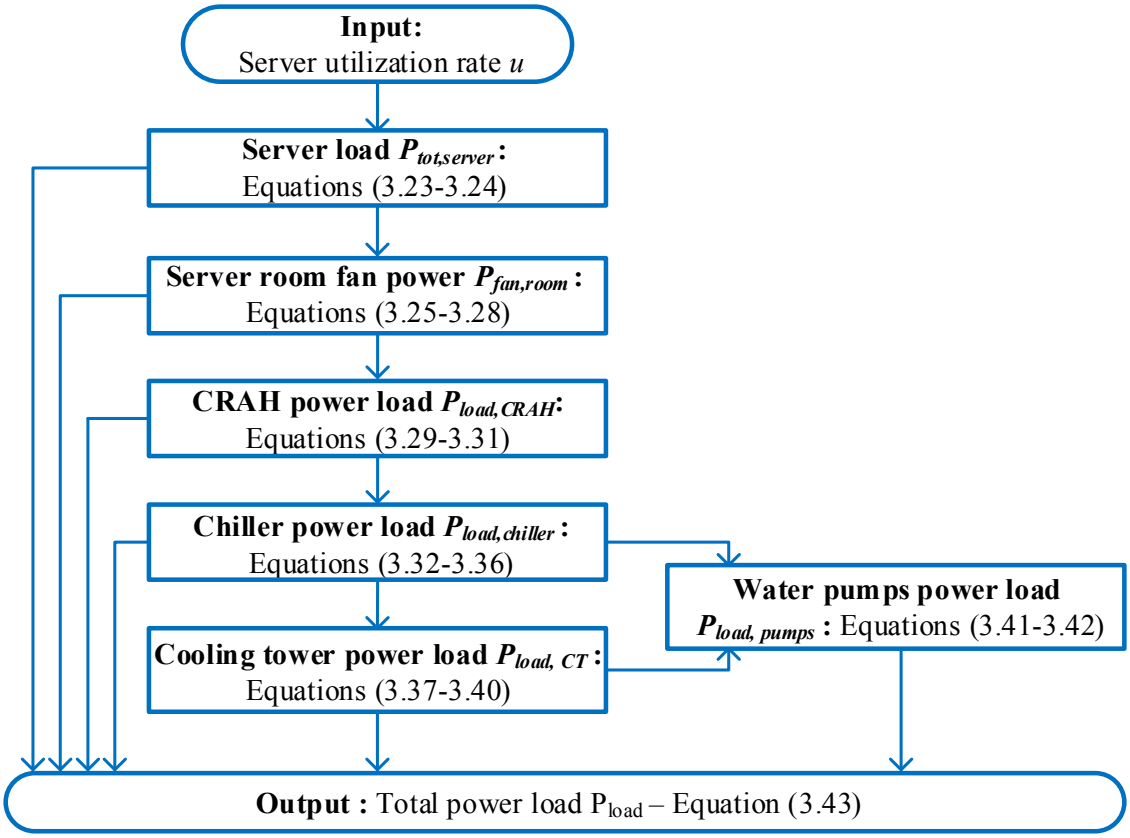


Figure 3.18: Flow chart of the data center server and cooling load model.

Table 3.4: Defined data center configuration.

Parameters	Values
Intel Xeon 5500 processor [208]	$P_{idle} = 10$ W
	$P_{rated,server} = 130$ W
Number of servers per rack, N_{server}	20
Number of racks, N_{rack}	3
Server room $\triangle T_{air,server}$	13.5 °C
Server fan E97379-001 [209]	$P_{rated,fan} = 13.8$ W
Server fan nominal air flow rate	$f_{0fan,server} = 0.0304$ m^3/s
CRAH rated power	$P_{rated,CRAH} = 2$ hp
CRAH fan nominal speed	$\omega_{0rm,CRAH} = 188.5$ rad/s
Chiller rated power	$P_{rated,chiller} = 2$ hp
Pump rated power	$P_{rated,pump} = 2$ hp
Cooling tower rated power	$P_{rated,CRAH} = 2$ hp
$T_{wcold,chiller}$	16 °C
$T_{wcold,CT}$	29.44 °C
Water flow rate	$f_w = 8.2 \times 10^{-4}$ m^3/s
System power rating	$P_{rated} = 15.068$ kW

Table 3.5: Design parameters of power components.

UPS	
Power rating	10 kW
Dc-link capacitor	$C_{dc,ups} = 1$ mF
Rectifier boost inductor	$L_{rec} = 10$ mH
VSI inductor	$L_{vsi} = 2.3$ mH
VSI output capacitor	$C_{vsi} = 1$ nF
Battery dc-dc converter inductor	$L_{dc,dc} = 300$ μH
Rectifier boost dc-dc converter PI controller	$k_{p\_v,rec} = 4.07, k_{i\_v,rec} = 84.9$
VSI voltage loop PI controller	$k_{p\_v,vsi} = 1.16, k_{i\_v,vsi} = 219.9$
VSI current loop PI controller	$k_{p\_i,vsi} = 0.217, k_{i\_i,vsi} = 21.73$
Battery dc-dc voltage loop PI controller	$k_{p\_v,dcdc} = 114, k_{i\_v,dcdc} = 9499.6$
Battery dc-dc current loop PI controller	$k_{p\_i,dcdc} = 0.01, k_{i\_i,dcdc} = 5.06$
PFC	
Power rating	1.5 kW
Boost inductor	$L_b = 476$ μH
Dc output capacitor	$C_{dc,psu} = 1100$ μF
Voltage loop PI controller	$k_{p\_v,pfc} = 2.44, k_{i\_v,dcdc} = 33$
Current loop PI controller	$k_{p\_i,pfc} = 0.5, k_{i\_i,dcdc} = 13222$
CRAH VFD	
Power rating	1.5 kW
Dc-link capacitor	$C_{dc,vfd} = 837$ μF
Ac-side inductor	$L_{vfd} = 7.4$ mH
Voltage loop PI controller	$k_{p\_v,vfd} = 210.76, k_{i\_v,vfd} = 27021$
Current loop PI controller	$k_{p\_i,vfd} = 0.12, k_{i\_i,vfd} = 44.78$
Induction motor	
Power rating	2 hp
Mutual inductance	$L_m = 0.9446$ H
Leakage inductance	$L_{ls} = L_{lr} = 21.77$ mH
Stator resistance	$R_s = 2.368$ Ω
Rotor resistance	$R_r^{'} = 6.21$ Ω
Inertia	1 s

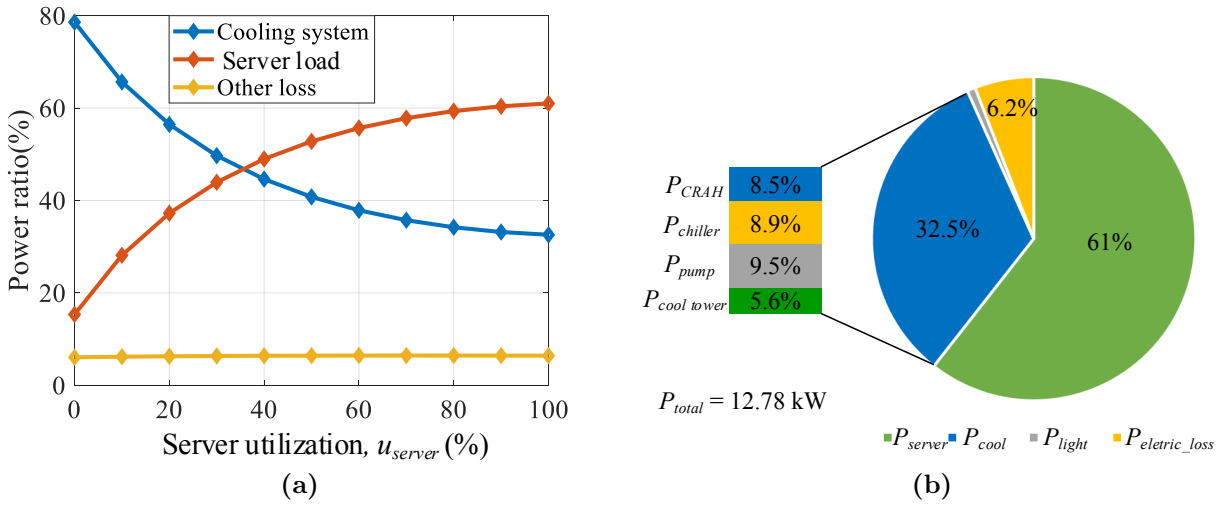


Figure 3.19: Data canter power consumption. (a) Power breakdown at various utilization rates; (b) Power breakdown at 100% utilization rate.

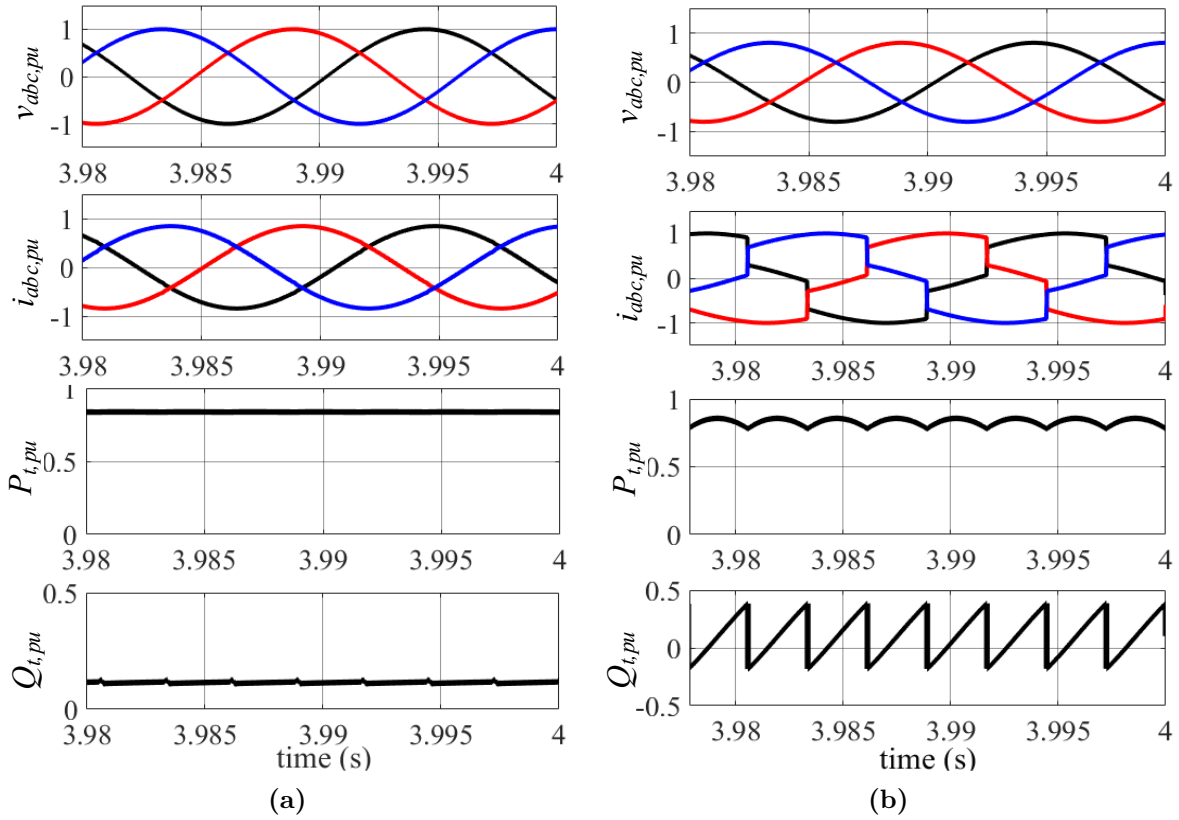
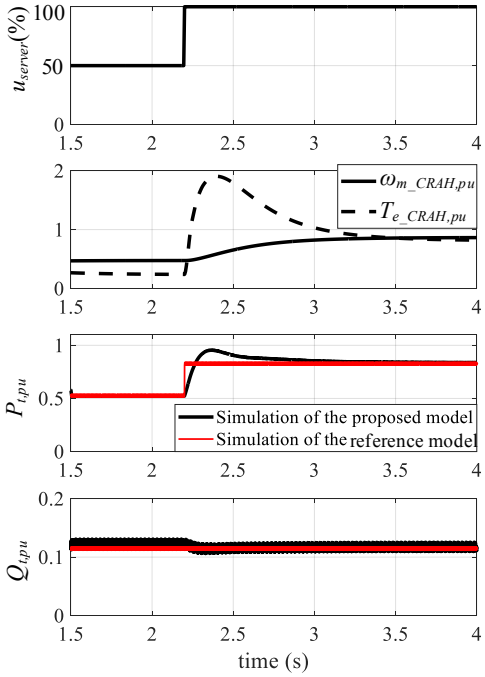


Figure 3.20: Simulation waveforms of the data center power system at steady state with 100% server utilization. (a) During normal eco mode; (b) During double conversion mode.

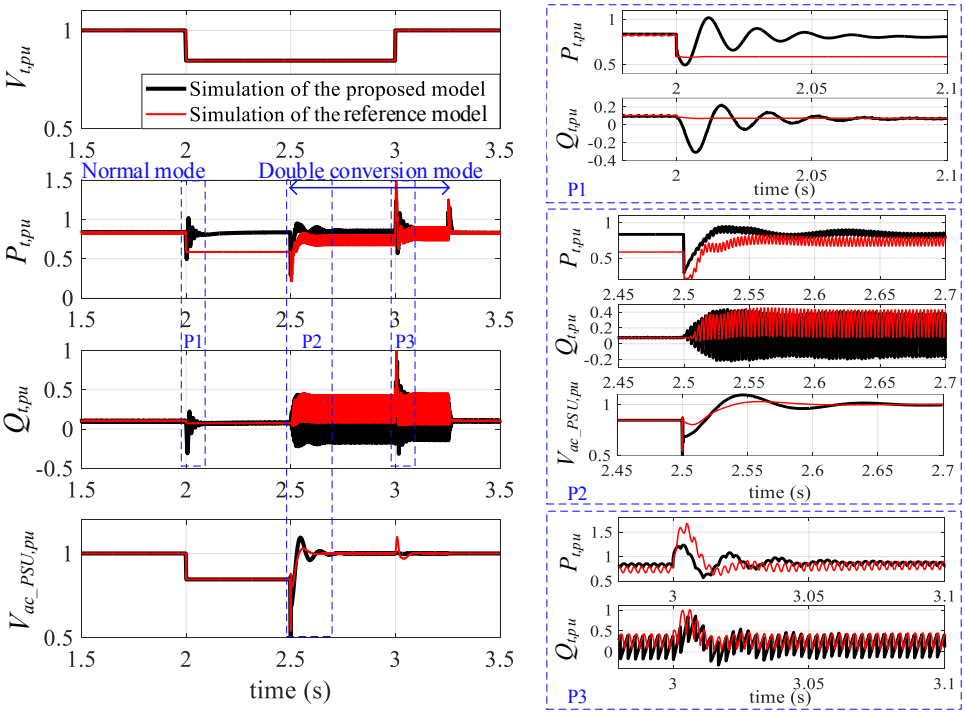
In comparison to the existing work, the data center power model developed in [22] is referred to as the reference model, where the rack-level power supply and server load are represented by a resistive load, and the cooling system is represented by a RL load. Figure 3.21 shows the simulation results during server load change and voltage sag event under the assumption that server tasks are evenly distributed. The simulation waveforms are all normalized into pu values, including the server utilization u_{server}, the CRAH VFD-based motor rotation speed $\omega_{m\_CRAH,pu}$ and mechanical torque $T_{e\_CRAH,pu}$, the terminal voltage magnitude $V_{t,pu}$, the terminal active power and reactive power $P_{t,pu}, Q_{t,pu}$, and the single-phase ac voltage of the rack-level power supply $V_{ac\_PSU,pu}$.

During the load change from 50% utilization to 100% utilization (Figure 3.21(a)), $V_{t,pu}$ is stable and the data center operates in normal eco mode. The proposed model exhibits obvious dynamic response in $P_{t,pu}$ mainly because of the low-bandwidth voltage control in the PSUs. In order to improve the cooling system efficiency, the CRAH VFD motor adjusts its rotation speed in accordance with the server load, leading to variations in $T_{e\_CRAH,pu}$ and $Q_{t,pu}$. However, lacking the detailed modeling of power electronics and control loops, the reference model is incapable of reflecting these dynamic performance as shown in Figure 3.21(a).

At the instant of 16% voltage drop disturbance (Figure 3.21(b)), the data center transits between normal mode and double conversion mode. The proposed model performs more accurate dynamic response. When the sag occurs at $t = 2$ s, the cooling motor and power supply converters respond accordingly to maintain the same output power. After 500 ms, the UPS switches in to carry the server loads, and a distinct response is captured in $P_{t,pu}$ and $Q_{t,pu}$ at 2.5 s in Figure 3.21(b). When the sag ends, server loads are still supported by UPS regulated power until after 0.25 s margin time, and the UPS drops out at $t = 3.25$ s. Because the server power supply and cooling load are simplified as constant RL load, the reference model presents decreased power during $2-2.5$ s, and the dynamic response deviates from the proposed model. Therefore, the proposed data center model is more complete and accurate, which can better identify the data center load characteristics.



(a)



(b)

Figure 3.21: Simulation waveforms of the proposed data center model and the reference model used in [22] under (a) Server load change from 50% utilization to 100% utilization; (b) 16% terminal voltage sag for 1 s.

3.3 Data Center Power Emulator

The data center power emulator is developed based on the proposed model and the HTB grid emulation platform invented in [48, 76]. To be compatible with the HTB grid emulation platform, the data center emulator is achieved by local VSIs, and all data center model and control functions are implemented in the VSI DSP. Therefore, the nonlinear average model derived in Section 3.2 should be transformed into discrete-time version by digitization, and a generalized model with explicit input variables and output variables is required to coordinate all power stages under different operation cases.

3.3.1 Model Digitization and Simplification

The data center nonlinear average model is digitized with sampling frequency at $T_s = 0.2$ ms, which is consistent with the DSP sampling period.

3.3.1.1 Digitized UPS Model

- Digitized UPS Rectifier Model

  Dc voltage loop with PI controller in discrete-time equation:

$$\begin{cases} e_{v,rec}[x] = V^{pu}_{dcref,ups}[x] - \bar{v}^{pu}_{dc,ups}[x-1] \\ \bar{i}^{pu}_{c,rec}[x] = k_{p\_v,rec} e_{v,rec}[x] + \sum_{0}^{x} k_{i\_v,rec} e_{v,rec}[x] T_s \end{cases} \tag{3.44}$$

  Rectifier average model in discrete-time equation:

$$\begin{cases} \bar{i}_{L,rec}[x] = \bar{i}^{pu}_{c,rec}[x] I_{B,ups} \\ \bar{v}_{diode}[x] = \max\{\bar{v}_{ab,rec}[x], \bar{v}_{ac,rec}[x], \bar{v}_{bc,rec}[x], \bar{v}_{ba,rec}[x], \bar{v}_{ca,rec}[x], \bar{v}_{cb,rec}[x]\} \\ \bar{v}_{dc,ups}[x] = \frac{T_s}{C_{dc,ups}} \left(\frac{\bar{v}_{diode}[x] \bar{i}_{L,rec}[x]}{\bar{v}_{dc,ups}[x-1]} - \bar{i}_{load,rec}[x-1] \right) + \bar{v}_{dc,ups}[x-1] \end{cases} \tag{3.45}$$

$$\begin{cases} \bar{i}_{a,rec}[x] = \bar{i}_{L,rec}[x],\ \bar{i}_{b,rec}[x] = -\bar{i}_{L,rec}[x],\ \bar{i}_{c,rec}[x] = 0 & if\ \ \bar{v}_{diode}[x] = \bar{v}_{ab,rec}[x] \\ \bar{i}_{a,rec}[x] = \bar{i}_{L,rec}[x],\ \bar{i}_{b,rec}[x] = 0,\ \bar{i}_{c,rec}[x] = -\bar{i}_{L,rec}[x] & if\ \ \bar{v}_{diode}[x] = \bar{v}_{ac,rec}[x] \\ \bar{i}_{a,rec}[x] = 0,\ \bar{i}_{b,rec}[x] = \bar{i}_{L,rec}[x],\ \bar{i}_{c,rec}[x] = -\bar{i}_{L,rec}[x] & if\ \ \bar{v}_{diode}[x] = \bar{v}_{bc,rec}[x] \\ \bar{i}_{a,rec}[x] = -\bar{i}_{L,rec}[x],\ \bar{i}_{b,rec}[x] = \bar{i}_{L,rec}[x],\ \bar{i}_{c,rec}[x] = 0 & if\ \ \bar{v}_{diode}[x] = \bar{v}_{ba,rec}[x] \\ \bar{i}_{a,rec}[x] = -\bar{i}_{L,rec}[x],\ \bar{i}_{b,rec}[x] = 0,\ \bar{i}_{c,rec}[x] = \bar{i}_{L,rec}[x] & if\ \ \bar{v}_{diode}[x] = \bar{v}_{ca,rec}[x] \\ \bar{i}_{a,rec}[x] = 0,\ \bar{i}_{b,rec}[x] = -\bar{i}_{L,rec}[x],\ \bar{i}_{c,rec}[x] = \bar{i}_{L,rec}[x] & if\ \ \bar{v}_{diode}[x] = \bar{v}_{cb,rec}[x] \end{cases} \tag{3.46}$$

- Digitized UPS VSI Model

  Outer voltage control loop in discrete-time equation:

$$\begin{cases} \overrightarrow{e_{v\_dq,vsi}}[x] = \overrightarrow{V^{pu}_{dqref,vsi}}[x] - \overrightarrow{\bar{v}^{pu}_{dq,vsi}}[x-1] \\ \overrightarrow{\bar{i}^{pu}_{dqref,vsi}}[x] = k_{p\_v,vsi}\overrightarrow{e_{v\_dq,vsi}}[x] + \sum_{0}^{x} k_{i\_v,vsi}\overrightarrow{e_{v\_dq,vsi}}[x]T_s \end{cases} \tag{3.47}$$

  Inner current control loop in discrete-time equation:

$$\begin{cases} \overrightarrow{e_{i\_dq,vsi}}[x] = \overrightarrow{\bar{i}^{pu}_{dqref,vsi}}[x] - \overrightarrow{\bar{i}^{pu}_{dq,vsi}}[x-1] \\ \overrightarrow{\bar{d}_{dq,vsi}}[x] = k_{p\_i,vsi}\overrightarrow{e_{i\_dq,vsi}}[x] + \sum_{0}^{x} k_{i\_i,vsi}\overrightarrow{e_{i\_dq,vsi}}[x]T_s \end{cases} \tag{3.48}$$

  VSI average model in discrete-time equation:

$$\begin{cases} \overrightarrow{\bar{i}_{dq,vsi}}[x] = \frac{T_s}{L_{vsi}}\bar{v}_{dc,vsi}[x-1]\overrightarrow{\bar{d}_{dq,vsi}}[x] - \frac{T_s}{L_{vsi}}\overrightarrow{\bar{v}_{dq,vsi}}[x-1] + \begin{bmatrix} 1 & \omega T_s \\ -\omega T_s & 1 \end{bmatrix}\overrightarrow{\bar{i}_{dq,vsi}}[x-1] \\ \overrightarrow{\bar{v}_{dq,vsi}}[x] = \frac{T_s}{C_{vsi}}\overrightarrow{\bar{i}_{dq,vsi}}[x-1] - \frac{T_s}{C_{vsi}}\overrightarrow{\bar{i}_{load\_dq,vsi}}[x-1] + \begin{bmatrix} 1 & \omega T_s \\ -\omega T_s & 1 \end{bmatrix}\overrightarrow{\bar{v}_{dq,vsi}}[x-1] \\ \bar{i}_{dc,vsi}[x] = \overrightarrow{\bar{d}_{dq,vsi}}^{T}[x]\overrightarrow{\bar{i}_{dq,vsi}}[x-1] \end{cases} \tag{3.49}$$

- Digitized UPS Dc-Dc Converter Model

  Voltage control loop in battery mode in discrete-time equation:

$$\begin{cases} e_{v,dcdc}[x] = V^{pu}_{dcref,ups}[x] - \bar{v}^{pu}_{dc,ups}[x-1] \\ \bar{i}^{pu}_{batt\_ref}[x] = k_{p\_v,dcdc} e_{v,dcdc}[x] + \sum_{0}^{x} k_{i\_v,dcdc} e_{v,dcdc}[x] T_s \end{cases} \tag{3.50}$$

In normal eco mode and double conversion mode, $\bar{i}^{pu}_{batt\_ref}[x]$ is generated based on the demanded active power.

Current control loop in discrete-time equation:

$$\begin{cases} e_{i,dcdc}[x] = \bar{i}^{pu}_{batt\_ref}[x] - \bar{i}^{pu}_{batt}[x-1] \\ d_{dcdc}[x] = k_{p\_i,dcdc} e_{i,dcdc}[x] + \sum_{0}^{x} k_{i\_i,dcdc} e_{i,dcdc}[x] T_s \end{cases} \tag{3.51}$$

Dc-dc converter average model in discrete-time equation:

$$\begin{cases} \bar{i}_{batt}[x] = -\frac{T_s}{L_{dc,dc}}(1 - d_{dcdc}[x])\bar{v}_{dc}[x-1] + \frac{T_s}{L_{dc,dc}}\bar{v}_{batt}[x-1] + \bar{i}_{batt}[x-1] \\ \bar{i}_{dc,dc}[x] = (1 - d_{dcdc}[x])\bar{i}_{batt}[x] \end{cases} \tag{3.52}$$

- Digitized UPS Li-Ion Battery Model

$$SOC[x] = SOC_{cell}[x] = SOC[0] - \frac{\sum_{0}^{x} \bar{i}_{cell}[x] T_s}{Q_{cell}} \tag{3.53}$$

$$\bar{i}_{batt}[x] = N_{parallel} \bar{i}_{cell}[x] \tag{3.54}$$

In discharging mode,

$$\bar{v}_{batt}[x] = N_{series}\left(E_{ocv} - R_o \bar{i}_{cell}[x] - \frac{KQ_{cell}\sum_{0}^{x} \bar{i}_{cell}[x] T_s}{Q_{cell} - \sum_{0}^{x} \bar{i}_{cell}[x] T_s} - \frac{KQ_{cell}\bar{i}_{cell}[x]}{Q_{cell} - \sum_{0}^{x} \bar{i}_{cell}[x] T_s} + Ae^{-B\sum_{0}^{x} \bar{i}_{cell}[x] T_s}\right) \tag{3.55}$$

In charging mode,

$$\bar{v}_{batt}[x] = N_{series}\left(E_{ocv} - R_o \bar{i}_{cell}[x] - \frac{KQ_{cell}\sum_{0}^{x} \bar{i}_{cell}[x] T_s}{Q_{cell} - \sum_{0}^{x} \bar{i}_{cell}[x] T_s} - \frac{KQ_{cell}\bar{i}_{cell}[x]}{\sum_{0}^{x} \bar{i}_{cell}[x] T_s - Q_{cell}} + Ae^{-B\sum_{0}^{x} \bar{i}_{cell}[x] T_s}\right) \tag{3.56}$$

- Digitized Combined UPS Model

In eco normal mode,

$$\begin{cases} \bar{v}_{dc,ups}[x] = \frac{T_s}{C_{dc,ups}}(\bar{i}_{dc,rec}[x] + \bar{i}_{dc,dc}[x] - \bar{i}_{dc,vsi}[x]) + \bar{v}_{dc,ups}[x-1] \\ \bar{i}_{load,rec}[x] = \bar{i}_{dc,vsi}[x] - \bar{i}_{dc,dc}[x] \\ \overrightarrow{\bar{i}_{load\_dq,vsi}}[x] = \frac{\overrightarrow{\bar{v}_{dq,vsi}}[x]}{R_{load,eco}} \end{cases} \tag{3.57}$$

In double conversion mode,

$$\begin{cases} \bar{v}_{dc,ups}[x] = \frac{T_s}{C_{dc,ups}}(\bar{i}_{dc,rec}[x] + \bar{i}_{dc,dc}[x] - \bar{i}_{dc,vsi}[x]) + \bar{v}_{dc,ups}[x-1] \\ \bar{i}_{load,rec}[x] = \bar{i}_{dc,vsi}[x] - \bar{i}_{dc,dc}[x] \\ \overrightarrow{\bar{i}_{load\_dq,vsi}}[x] = \frac{N_{psu}}{3}\overrightarrow{\bar{i}_{in\_dq,pfc}}[x] \end{cases} \tag{3.58}$$

In battery mode,

$$\begin{cases} \bar{v}_{dc,ups}[x] = \frac{T_s}{C_{dc,ups}}(\bar{i}_{dc,dc}[x] - \bar{i}_{dc,vsi}[x]) + \bar{v}_{dc,ups}[x-1] \\ \bar{i}_{load,rec}[x] = 0 \\ \overrightarrow{\bar{i}_{load\_dq,vsi}}[x] = \frac{N_{psu}}{3}\overrightarrow{\bar{i}_{in\_dq,pfc}}[x] + \overrightarrow{\bar{i}_{dq,vfd}}[x] \end{cases} \tag{3.59}$$

N_{psu} is the total number of PSUs.

3.3.1.2 Digitized PFC Model

PFC outer voltage loop in discrete-time equation:

$$\begin{cases} e_{v,pfc}[x] = \bar{v}^{pu}_{dcref,psu}[x] - \bar{v}^{pu}_{dc,psu}[x-1] \\ \bar{i}^{pu}_{Lb\_ref}[x] = \sin\theta[x]\big(k_{p\_v,pfc}e_{v,pfc}[x] + \sum_{0}^{x} k_{i\_v,pfc}e_{v,pfc}[x]T_s\big) \end{cases} \tag{3.60}$$

PFC inner current loop in discrete-time equation:

$$\begin{cases} e_{i,pfc}[x] = \bar{i}^{pu}_{Lb\_ref}[x] - \bar{i}^{pu}_{Lb}[x-1] \\ d_{pfc}[x] = k_{p\_i,pfc}e_{i,pfc}[x] + \sum_{0}^{x} k_{i\_i,pfc}e_{i,pfc}[x]T_s \end{cases} \tag{3.61}$$

PFC average model in discrete-time equation:

$$\begin{cases} \bar{v}_{diode,pfc}[x] = |\bar{v}_{in,pfc}[x]| \\ \bar{i}_{Lb}[x] = -\frac{T_s}{L_b}(1 - d_{pfc}[x])\bar{v}_{dc,psu}[x-1] + \frac{T_s}{L_b}\bar{v}_{diode,pfc}[x] + \bar{i}_{Lb}[x-1] \\ \bar{v}_{dc,psu}[x] = \frac{T_s}{C_{dc,psu}}(1 - d_{pfc}[x])\bar{i}_{Lb}[x] - \frac{T_s}{C_{dc,psu}}\bar{i}_{load,pfc}[x-1] + \bar{v}_{dc,psu}[x-1] \\ \bar{i}_{load,pfc} = \frac{N_{s,psu}P_{server}[x]}{\bar{v}_{dc,psu}[x]} \end{cases} \tag{3.62}$$

where $N_{s,psu}$ is the number of servers supplied by one PSU.

3.3.1.3 Digitized Three-Phase Induction Motor Model

The generated electric torque in discrete-time equation:

$$T_e^{pu}[x] = X_m(i_{qs}^{pu}[x]i_{dr}^{'pu}[x] - i_{ds}^{pu}[x]i_{qr}^{'pu}[x]) \tag{3.63}$$

Rotation angular frequency in discrete-time equation:

$$\omega_r^{pu}[x] = (T_e^{pu}[x] - T_L^{pu}[x])\frac{T_s}{2H} + \omega_r^{pu}[x-1] \tag{3.64}$$

where $H = {}^{J\omega_B^{pu}}/_{(2P_{B,motor}P^2)}$.

Based on (3.15)-(3.18), the normalized motor currents in discrete-time equations are

$$\begin{bmatrix} i_{ds}^{pu}[x] \\ i_{qs}^{pu}[x] \\ i_{dr}^{pu}[x] \\ i_{qr}^{pu}[x] \end{bmatrix} = T_s \begin{bmatrix} XX_{rr} & 0 & -XX_m & 0 \\ 0 & XX_{rr} & 0 & -XX_m \\ -XX_m & 0 & XX_{ss} & 0 \\ 0 & -XX_m & 0 & XX_{ss} \end{bmatrix} \begin{bmatrix} v_{ds}^{pu}[x] \\ v_{qs}^{pu}[x] \\ v_{dr}^{pu}[x] \\ v_{qr}^{pu}[x] \end{bmatrix} +$$

$$T_s \begin{bmatrix} -XX_{rr}R_s^{'pu} & XX_{rr}X_{ss}\omega^{pu} - XX_m^2(\omega^{pu} - \omega_r^{pu}) & XX_mR_r^{'pu} & XX_mX_{rr}\omega_r^{pu} \\ -XX_{rr}X_{ss}\omega^{pu} + XX_m^2(\omega^{pu} - \omega_r^{pu}) & -XX_{rr}R_s^{'pu} & -XX_mX_{rr}\omega_r^{pu} & XX_mR_r^{'pu} \\ XX_mR_s^{'pu} & -XX_{ss}X_m\omega_r^{pu} & -XX_{ss}R_r^{'pu} & XX_{ss}X_{rr}(\omega^{pu} - \omega_r^{pu}) - XX_m^2\omega^{pu} \\ XX_{ss}X_m\omega_r^{pu} & XX_mR_s^{'pu} & -XX_{ss}X_{rr}(\omega^{pu} - \omega_r^{pu}) + XX_m^2\omega^{pu} & -XX_{ss}R_r^{'pu} \end{bmatrix}$$

$$\times \begin{bmatrix} i_{ds}^{pu}[x-1] \\ i_{qs}^{pu}[x-1] \\ i_{dr}^{pu}[x-1] \\ i_{qr}^{pu}[x-1] \end{bmatrix} + \begin{bmatrix} i_{ds}^{pu}[x-1] \\ i_{qs}^{pu}[x-1] \\ i_{dr}^{pu}[x-1] \\ i_{qr}^{pu}[x-1] \end{bmatrix} \tag{3.65}$$

where $\omega^{pu} = \omega^{pu}[x]$, $\omega_r^{pu} = \omega_r^{pu}[x-1]$, $X_m = L_m^{pu}$, $X_{ss} = L_{ls}^{up} + L_m^{pu}$, $X_{rr} = L_{lr}^{'pu} + L_m^{pu}$, $X = {}^{w_b}/_{(X_{rr}X_{ss} - X_m)}$.

3.3.1.4 Digitized VFD Model

Rectifier outer voltage loop in discrete-time equations:

$$\begin{cases} e_{v,vfd}[x] = V_{dcref,vfd}^{pu}[x] - \bar{v}_{dc,vfd}^{pu}[x-1] \\ \bar{i}_{dref,vfd}^{pu}[x] = k_{p\_v,vfd}e_{v,vfd}[x] + \sum_0^x k_{i\_v,vfd}e_{v,vfd}[x]T_s \\ \bar{i}_{qref,vfd}^{pu}[x] = \frac{1}{\bar{v}_{d,vfd}^{pu}[x-1]}\left(Q_{ref,vfd}^{pu}[x] + \bar{v}_{q,vfd}^{pu}[x-1]\bar{i}_{d,vfd}^{pu}[x-1]\right) \end{cases} \tag{3.66}$$

Rectifier inner current loop in discrete-time equations:

$$\begin{cases} \overrightarrow{e_{i\_dq,vfd}}[x] = \overrightarrow{\bar{i}_{dqref,vfd}^{pu}}[x] - \overrightarrow{\bar{i}_{dq,vfd}^{pu}}[x-1] \\ \overrightarrow{\bar{d}_{dq,vfd}}[x] = k_{p\_i,vfd}\overrightarrow{e_{i\_dq,vfd}}[x] + \sum_0^x k_{i\_i,vfd}\overrightarrow{e_{i\_dq,vfd}}[x]T_s \end{cases} \tag{3.67}$$

Rectifier average model in discrete-time equations:

$$\begin{cases} \overrightarrow{\bar{i}_{dq,vfd}}[x] = \frac{T_s}{L_{vfd}}\overrightarrow{\bar{v}_{dq,vfd}}[x-1] - \frac{T_s}{L_{vfd}}\bar{v}_{dc,vfd}[x-1]\overrightarrow{\bar{d}_{dq,vfd}}[x] + \begin{bmatrix} 1 & \omega T_s \\ -\omega T_s & 1 \end{bmatrix}\overrightarrow{\bar{i}_{dq,vfd}}[x-1] \\ \bar{v}_{dc,vfd}[x] = \frac{T_s}{C_{dc,vfd}}\overrightarrow{\bar{d}_{dq,vfd}}^T[x]\overrightarrow{\bar{i}_{dq,vfd}}[x-1] - \frac{T_s}{C_{dc,vfd}}\bar{i}_{dc,vfd}[x-1] + \bar{v}_{dc,vfd}[x-1] \end{cases} \tag{3.68}$$

Based on the constant V/Hz control, the VSI output voltage $v_{dq\_vsi,vfd}$ is proportional to the reference rotation angular frequency $\omega_{r\_ref,vfd}$ that is determined by the required air flow rate.

$$\begin{cases} v_{d\_vsi,vfd}[x] = 0 \\ v_{q\_vsi,vfd}[x] = \omega_{m\_ref}[x]\frac{PV_b}{2\omega_b} \end{cases} \tag{3.69}$$

3.3.1.5 Model Simplification

Recalling the control methods used in the data center, dual-loop control consisting of an outer voltage loop and an inner current loop is embedded in the UPS VSI, UPS dc-dc

converter during the battery mode, the PSU PFC converter, and the CRAH VFD front-end rectifier. Compared with the grid line frequency, the inner current loops have much higher bandwidth, and can be viewed as ideal controls. Therefore, the average model is simplified by neglecting the fast current loop and replacing the current with the current reference generated from the voltage loop.

- The UPS VSI model shown in (3.48) and (3.49) is simplified as

$$\begin{cases} \overrightarrow{\bar{i}_{dq,vsi}} = \overrightarrow{\bar{i}^{pu}_{dqref,vsi}} I_{B,ups} \\ \overrightarrow{\bar{d}_{dq,vsi}}[x] = \frac{\overrightarrow{\bar{v}_{dq,vsi}}[x-1]}{\bar{v}_{dc,vsi}[x-1]} - \\ \frac{L_{vsi}}{T_s \bar{v}_{dc,vsi}[x-1]} \Big(\begin{bmatrix} 1 & \omega T_s \\ -\omega T_s & 1 \end{bmatrix} \overrightarrow{\bar{i}_{dq,vsi}}[x-1] - \overrightarrow{\bar{i}_{dq,vsi}}[x] \Big) \end{cases} \tag{3.70}$$

- The UPS dc-dc converter model shown in (3.51)and (3.52) is simplified as

$$\begin{cases} \bar{i}_{batt}[x] = \bar{i}^{pu}_{batt\_ref}[x] \\ d_{dcdc}[x] = 1 - \frac{\bar{v}_{batt}[x-1]}{\bar{v}_{dc}[x-1]} \end{cases} \tag{3.71}$$

- The PSU PFC converter model shown in (3.61) and (3.62) is simplified as

$$\begin{cases} \bar{i}_{Lb}[x] = \bar{i}^{pu}_{Lb\_ref}[x] \\ d_{pfc}[x] = 1 - \frac{\bar{v}_{diode,pfc}[x]}{\bar{v}_{dc,psu}[x-1]} \end{cases} \tag{3.72}$$

- The VFD rectifier model shown in (3.67) and (3.68) is simplified as

$$\begin{cases} \overrightarrow{\bar{i}_{dq,vfd}}[x] = \bar{i}^{pu}_{qref,vfd}[x] \\ \overrightarrow{\bar{d}_{dq,vfd}}[x] = \frac{\overrightarrow{\bar{v}_{dq,vfd}}[x-1]}{\bar{v}_{dc,vfd}[x-1]} + \\ \frac{L_{vfd}}{T_s \bar{v}_{dc,vfd}[x-1]} \Big(\begin{bmatrix} 1 & \omega T_s \\ -\omega T_s & 1 \end{bmatrix} \overrightarrow{\bar{i}_{dq,vfd}}[x-1] - \overrightarrow{\bar{i}_{dq,vfd}}[x] \Big) \end{cases} \tag{3.73}$$

3.3.2 Generalized System Model

One challenge of the data center emulator is to coordinate all power stages and predict the dynamic performance in various operation modes. To achieve this, a generalized model with a top-level control is proposed for the data center power emulator, as illustrated in Figure 3.22 and Algorithm 2. The model starts with terminal voltage v_t and grid frequency f, and the top-level control determines the operation mode. Multiple power stages are modeled simultaneously. For each stage's model, the input-port voltage is the output voltage of the previous stage, and the input-port current and output-port voltage are calculated based on the model. The output-port voltage is then sent to the next stage as the input voltage, and the input-port current is sent to the previous stage as the output load current. In different operation modes, voltages and currents are calculated following the specific paths which are distinguished in different colors in Figure 3.22. Finally, the top-level control updates the grid terminal current i_t based on the operation mode and starts the next cycle of calculation.

3.3.3 Hardware Implementation

The emulator is implemented on the CURENT HTB, which is a multi-converter based real-time real-power testing platform and can be flexibly emulated by programming the interconnected three-phase VSIs [48]. A local network consisting of three VSIs in one cabinet is used for the data center emulator verification, as illustrated in Figure 3.23. VSI-1 is implemented as a generator emulator to represent the grid power source that is connected to the emulator through a line impedance. The data center is emulated by two VSIs, where VSI-2 is embedded with models of UPS, PDUs, PSUs, and CRAH; and VSI-3 is installed with the aggregated induction motor model for cooling tower, chiller, and water pumps. In each of the load VSIs, the conditioning function, the data center model, and the VSI inner current loop are embedded in one DSP. The conditioned terminal voltage $v_{t,dq}$ and frequency is sent to the load model to generate the reference current i_{t,dq_ref}, which is sent to the inner current loop to control the VSI and generate the required terminal current. In this way, the VSIs are configured to emulate the data center load characteristics. Table 3.6 shows the specifications of the VSIs under test.

Algorithm 2: Top-Level Control

Input:

$v_t[x]$: grid terminal voltage;

$i_{UPS}[x], i_{PDU}$[x],$i_{cool}[x]$, etc. : currents of different power stages;

Output:

$mode[x]$: system operation mode;

$i_t[x]$: grid terminal current;

Procedure:

if $v_t[x] > 0.9V_{nom}$ **then**
    $t_{sag}[x] = 0$; $t_{nom}[x] = t_{nom}[x-1] + T_s$;
    if $t_{nom}[x] > 0.25$ s **then**
        $mode[x] = 0$;
    else
        $mode[x] = mode[x-1]$;
else if $0.7V_{nom} < v_t \leq 0.9V_{nom}$ **then**
    $t_{nom}[x] = 0$; $t_{sag}[x] = t_{sag}[x-1] + T_s$;
    if $t_{sag}[x] > 0.5$ s **then**
        $mode[x] = 1$;
    else
        $mode[x] = mode[x-1]$;
else
    $t_{nom}[x] = 0$; $t_{sag}[x] = t_{sag}[x-1] + T_s$;
    if $t_{sag}[x] > 20$ ms **then**
        $mode[x] = 2$;
    else
        $mode[x] = mode[x-1]$;

if $mode = 0$; `// normal eco mode` **then**
    $i_t = i_{UPS} + i_{PDU} + i_{cool} + i_{CRAH} + i_{light}$;
if $mode = 1$; `// double conversion mode` **then**
    $i_t = i_{UPS} + i_{cool} + i_{CRAH} + i_{light}$;
if $mode = 2$; `// battery mode` **then**
    $i_t = i_{light}$;

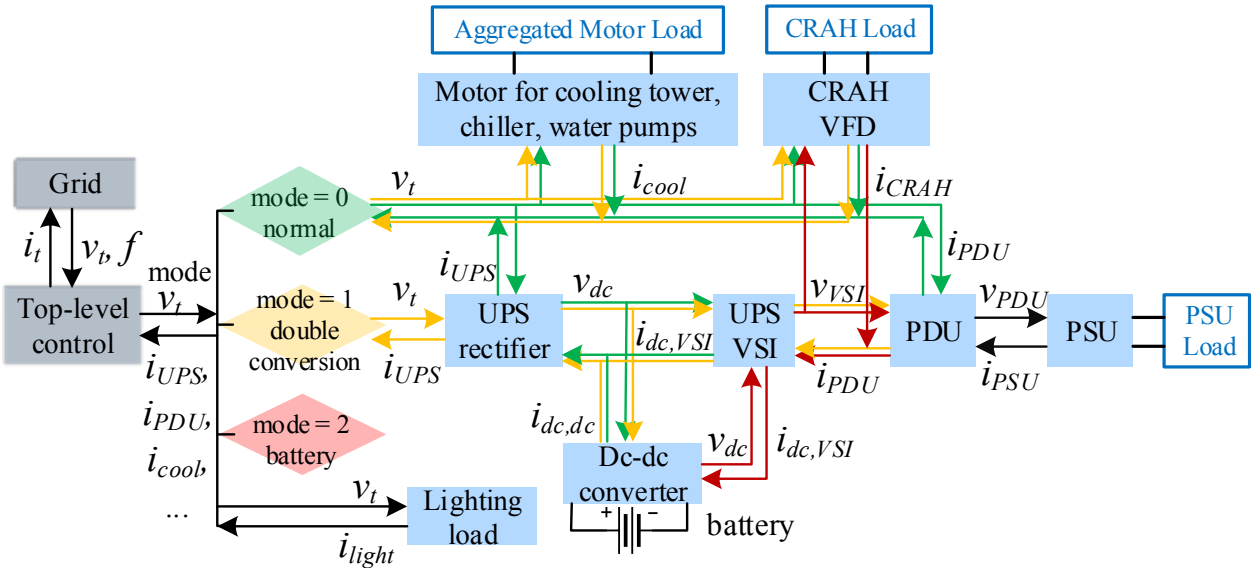


Figure 3.22: Adaptive model with top-level control.

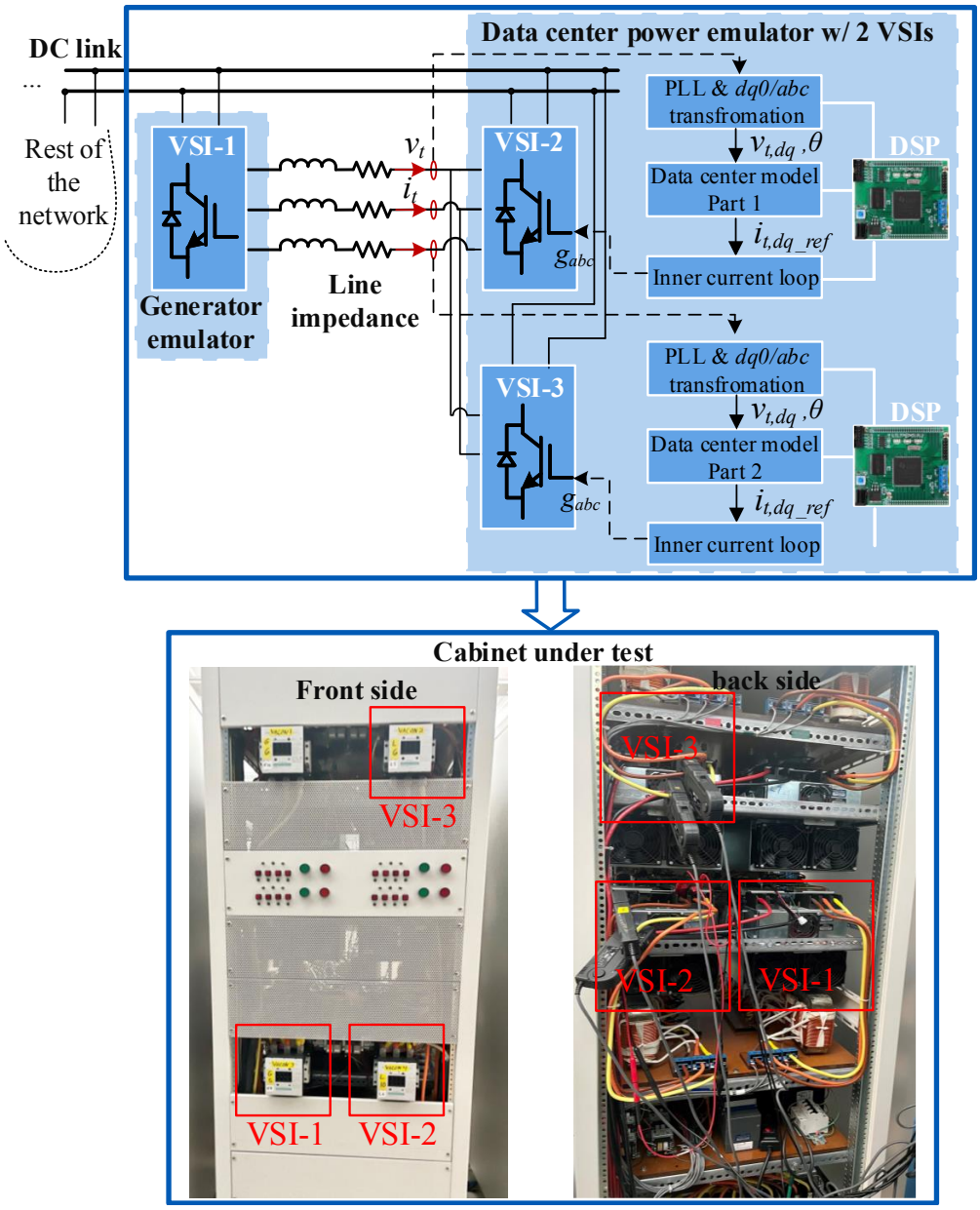


Figure 3.23: Experimental setup for the data center emulator verification.

Table 3.6: Specifications of the VSIs under test.

Parameters	Values
Dc link voltage	200 V
Switching frequency	10 kHz
Power rating	2 kW
Line impedance	1.8 mH
Base power under test	500 W

3.4 Experimental Verification

The data center power emulator is first validated at steady state with normal input voltage. Figure 3.24 shows the tested waveforms, including the three-phase line-to-line voltages v_{line}, three-phase currents i_{abc}, normalized terminal voltage magnitude $V_{t,pu}$, normalized currents in dq axis $I_{dq\_ph,pu}$, and normalized active and reactive power $P_{t,pu}, Q_{t,pu}$. At full load with 100% server utilization, the tested $P_{t,pu} = 0.837, Q_{t,pu} = 0.11$, and $PF = 0.99$, which match well with the simulated results.

3.4.1 Experimental Emulation of Voltage Sag Events

Voltage sag is one of the most common grid disturbances, which are demonstrated to emulate the dynamic response of the data center load. Figure 3.25 shows the experimental results during two voltage sag events. As shown in Figure 3.25(a), when a 16% voltage sag occurs, the data center changes operation from normal eco mode to double conversion mode after 500 ms at $t = 2.5$ s. At the same time, the UPS switches from a very light load to carry the heavy server loads, leading to a transient response with an abrupt power variation and slight $V_{t,pu}$ fluctuation. At both the beginning and end of the voltage sag, the data center performs transient power change due to the sudden voltage variation.

Figure 3.25(b) shows a more severe voltage sag with voltage drop $> 30\%$. To protect PSUs and maintain normal server operation, data center load is disconnected from the grid 20 ms after the sag occurs, and the UPS battery switches in to support the load. Consequently, $P_{t,pu}$ and $Q_{t,pu}$ drop to zero after the data center power system is disconnected from the grid during the battery mode. With the line impedance (1.8 mH) used in the experimental setup, V_t oscillates some after the transition to battery mode and increases slightly from its low point immediately. In both power interruptions, the PSU dc voltage is held at a high level to maintain the normal operation of server loads.

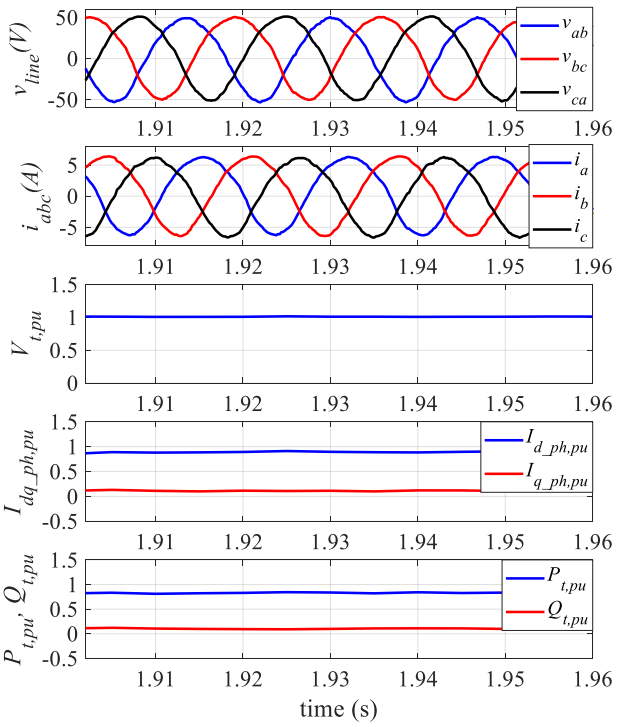
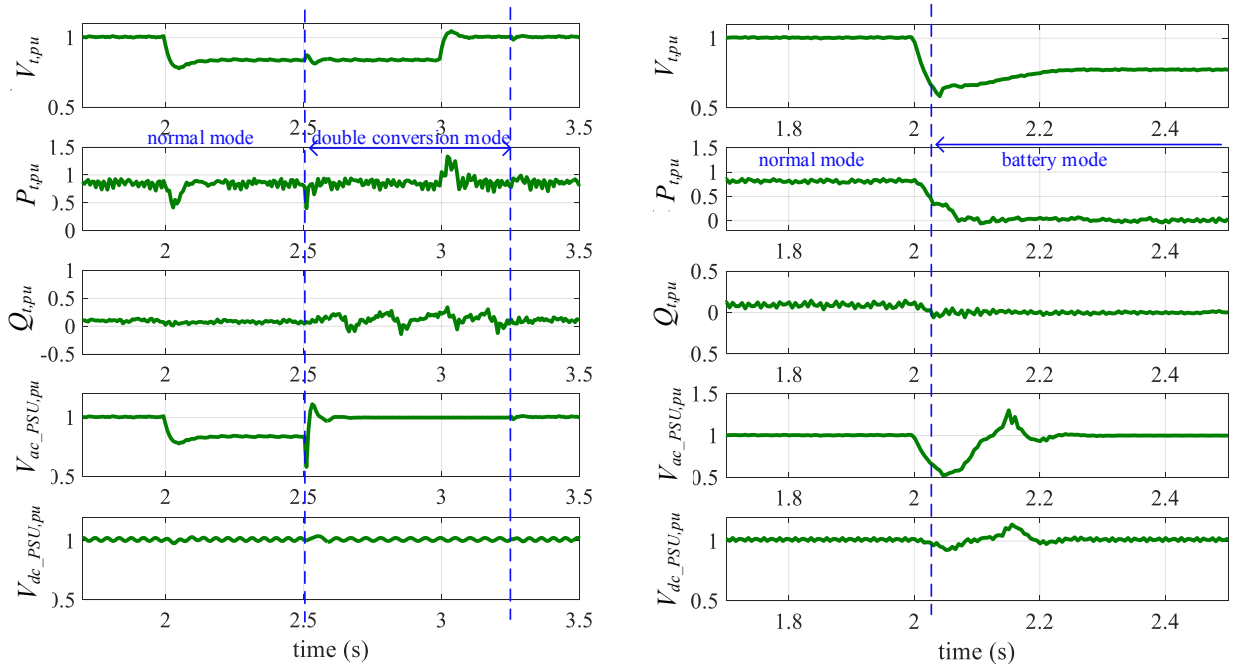


Figure 3.24: Experimental waveforms at steady state with 100% server utilization.



(a) Mode transition between normal eco mode and double conversion mode with 16% terminal voltage sag for 1 s.

(b) Mode transition between normal eco mode and battery mode with > 30% terminal voltage sag.

Figure 3.25: Experimental emulation and simulation results of the data center power system during voltage sag events.

3.4.2 Experimental Emulation of Server Load Variations

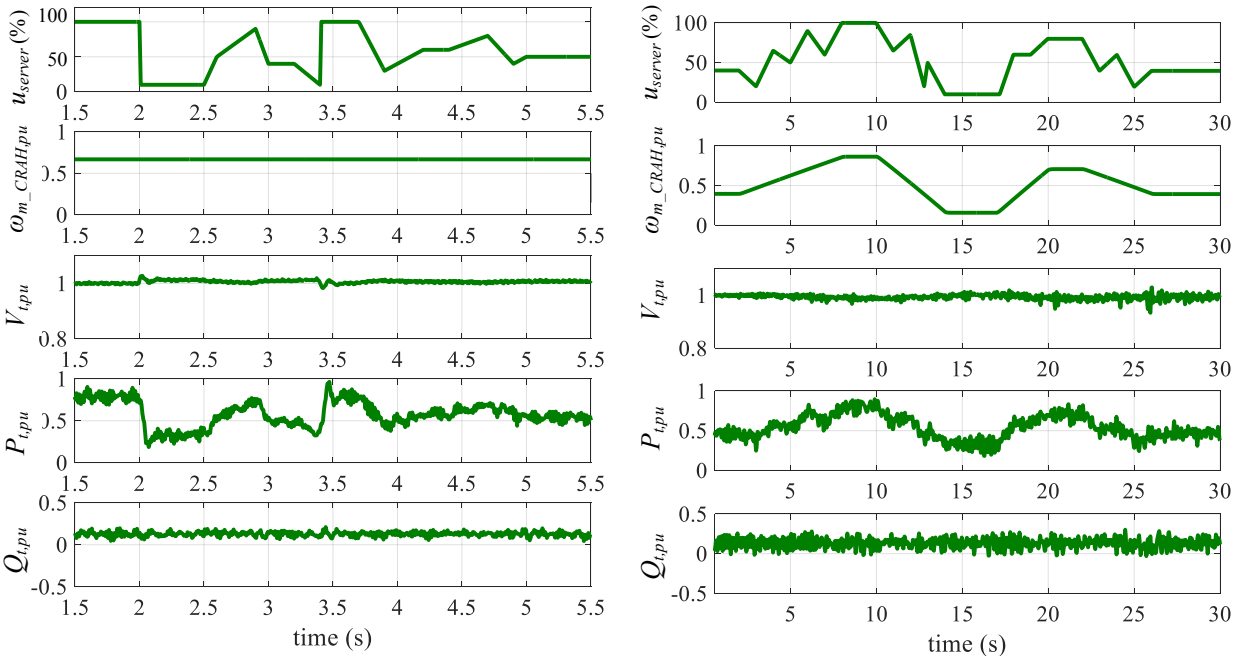
Transient response at grid terminal during the server load variations are investigated. Two load profiles are performed in the emulator under the assumption that server tasks are evenly distributed. In case 1, the server load behaves with extreme variations in a short time (*i.e.,* 3 s), and the server room air flow does not change accordingly due to the slower thermal dynamics. In case 2, the server load changes in a longer time (*i.e.,* 30 s), and CRAH motor adjust rotation speed accordingly to meet the server room air flow demand.

Figure 3.26 presents the experimental results during server load variations. In both cases, the data center power consumption generally follows the server loading, but performs significant variations ranging from 0.18 pu to 0.96 pu in case 1 and 0.25 pu to 0.91 pu in case 2. Such power dynamic response is more obvious at the period with higher u_{server} change rate, and results in terminal voltage fluctuations of the regional grid. The experimental emulation presents practical phenomenon like high-frequency ripple and mutual effect in the local grid, *i.e.,* grid disturbances effect data center load operation, and the data center load variations also cause grid voltage fluctuations.

3.5 Summary

To investigate data centers' load characteristic and help evaluate the grid dynamic performance, a dynamic power model is proposed for data center ac power distribution system, and the corresponding data center power load emulator based on the HTB is developed.

The data center model is complete, containing the power supply system, cooling system, detailed server load and cooling load. Compared with the conventional model, the proposed model has detailed modeling of power converters and control dynamics. Coherent server load and cooling load ensure realistic load model of the data center. Also, the proposed generalized model allows the prediction of data center dynamic power performance in different operation modes. Therefore, the proposed data center dynamic power model leads to a more realistic and accurate prediction of data center load characteristics.



(a) Case 1: Operation waveforms under load variation for 3 s.

(b) Case 2: Operation waveforms under load variation for 30 s.

Figure 3.26: Experimental emulation and simulation results of the data center power system during load variations.

The developed data center power emulator has been verified experimentally in a regional power network in the HTB, and transient characteristics during voltage sag events and server load variations are demonstrated. With model digitization and simplification, the emulator serves as an all-in-one load in the CURENT HTB, and it can be flexibly installed in different bus terminals to perform various local or large-scale power system experiments. Compared with existing emulators, the proposed data center power emulator is capable of assessing dynamic power performance during different transient cases such as voltage sag, server load variation, reactive power support, voltage regulation support, etc. Therefore, the data center emulator provides an effective and easy-to-use alternative to physical data center prototype for power system study.

The data center dynamic model and emulator can also be used to study data center internal operations, such as investigating the UPS battery SOC limit for safe power transition and the power supply peak current for protection. Because all control parameters are designed in pu system, the data center power model and emulator can be easily aggregated to systems with different power ratings without redesigning the controller. Also, the proposed methodology for data center system modeling and emulation can be extended to other architectures, such as data center dc power distribution system.

Chapter 4

GaN-Based Bridgeless PFC Design

Chapter 3 has investigated the data center power performance by building the system dynamic power model and emulator. As can be seen, during the normal operation, the server rack front-end rectifiers are directly connected to the grid terminal, which have significant impact on the system power factor, current THD, and energy efficiency. Hence, a high-efficiency PFC rectifier with high PF and low current THD is desired for the data center power supply system. In this chapter, a GaN-based PFC rectifier is designed for the data center power supply to achieve:

(1) High power efficiency.

(2) High PF and low input current THD.

Research work in this chapter has been published in:

(1) J. Sun, X. Huang, N. Strain, D. Costinett, L. M. Tolbert, "Inductor design and ZVS control for a GaN-based high efficiency CRM totem-pole PFC converter," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, 2019, pp. 727-733.

4.1 Topology Selection

Based on the discussion in Chapter 2, the bridgeless totem-pole PFC (Figure 2.5) and the four-level flying capacitor totem-pole PFC (Figure 2.6(b)) are selected as the candidates

for the PFC rectifier in data center power supply unit. To fairly compare the two PFC topologies, voltage and power ratings of the single-phase PFC are specified at $v_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}, $P_o = 1.5$ kW, and GaN devices are used for the fast-switching switches, *i.e.*, S_1, S_2 for the totem-pole PFC, and $S_{1a} - S_{3a}, S_{1b} - S_{3b}$ for the four-level flying capacitor PFC. Since the dc-link capacitance is determined by the requirements of energy buffering and hold-up time, the dc capacitor designs are the same in the two PFC topologies. Also, switches in the second phase leg operate in line cycle, and the same Si MOSFETs are adopted.

4.1.1 Bridgeless Totem-Pole PFC Design

Operation of the totem-pole PFC has been reviewed in Section 2.2; this section addresses the converter design and performance evaluation. CRM operation is implemented to achieve ZVS [16], and Table 4.1 shows the design specifications. A simulation model with the variable on-time control is built in Matlab simulink to validate the PFC functions, as presented in Figure 4.1. Figure 4.2 shows the simulation waveforms at full load of the totem-pole PFC converter. It can be seen that the output voltage is well regulated at 480 V, and ZVS is achieved with CRM operation.

4.1.2 Bridgeless Four-level Flying Capacitor Totem-Pole PFC

For the four-level flying capacitor totem-pole PFC (Figure 2.6(b)), there are six devices $S_{1a} - S_{3a}, S_{1b} - S_{3b}$ operating at fast frequency and two Si devices S_n, S_p working at line frequency. L_b is the input boost inductor, and C_1, C_2 are the flying capacitors, of which the nominal voltage are

$$V_{c1} = \frac{V_o}{3}, V_{c2} = \frac{2V_o}{3} \tag{4.1}$$

Because of the voltage difference between the adjacent capacitors, the voltage stress of the GaN device is reduced by a factor of three compared to that of the traditional two-level converter. Hence, lower-voltage GaN devices can be used to reduce the cost. Also, the inductor voltage swing is decreased to a third of the value in the two-level converter, and the equivalent current ripple frequency is three times of the switching frequency, resulting in significantly reduced inductor and filter capacitor if the current ripple is the same.

Table 4.1: Design specifications of the totem-pole PFC.

Parameter	Value
V_{in}	277 V_{ac}, 60 Hz
V_o	480 V_{dc}
P_o	1.5 kW
S_1, S_2	GaN systems, GS66508T, 650 V
L_b	26.67 µH, powder core Mix-2-T157
f_{sw}	137 kHz – 400 kHz
Gate drive	Dual-loop isolated gate driver, Silicon Labs SI8273AB-IS1-2
	LDOs, Rohm BD60GC0MEFJ×2
	Isolated power supply, Murata NXE2S1212MC-R7

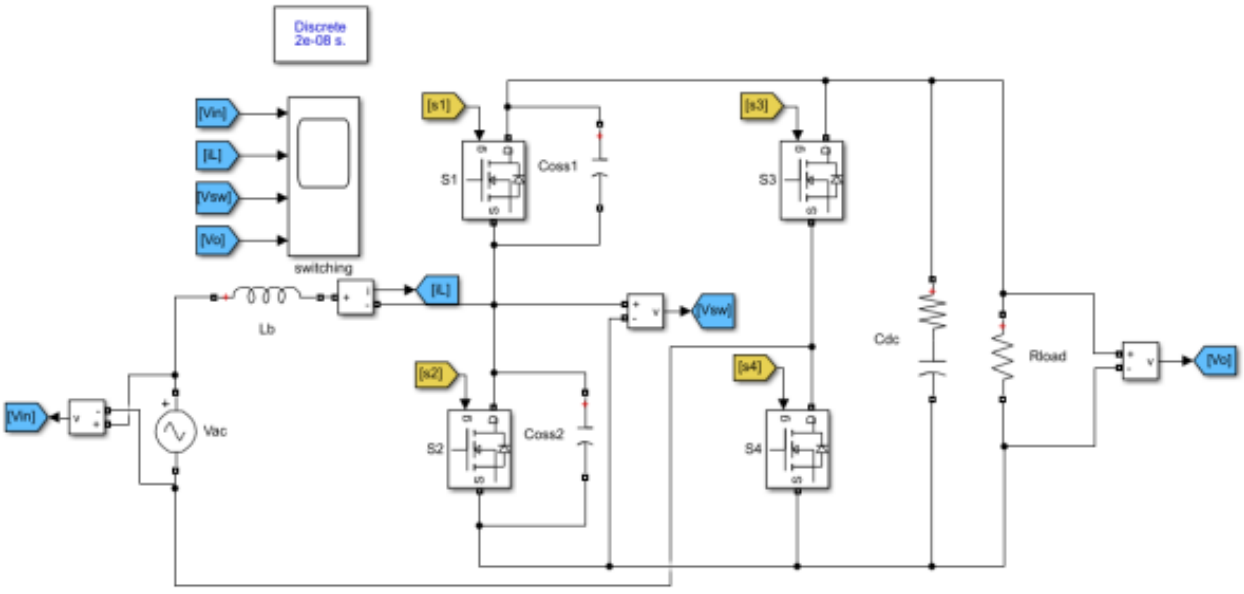
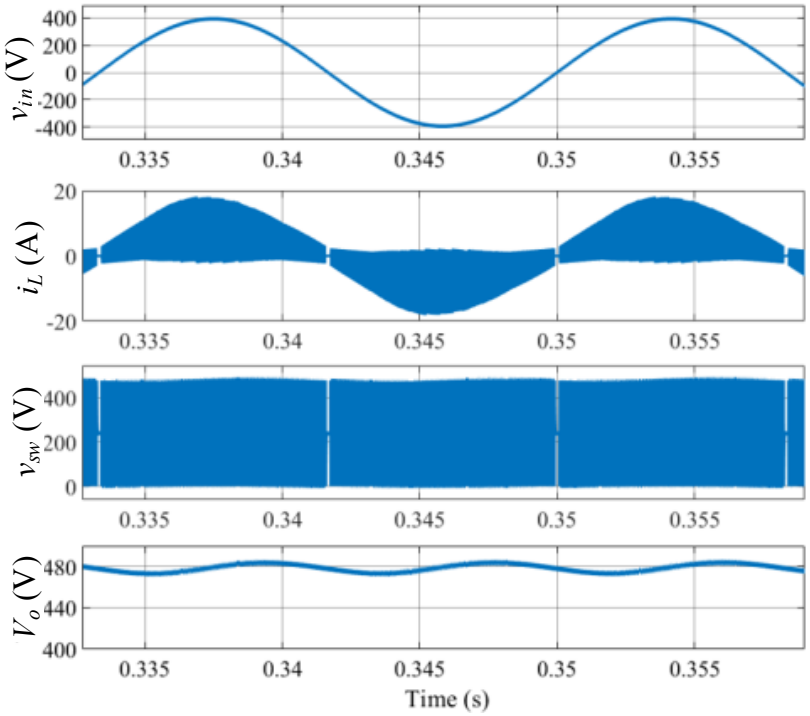


Figure 4.1: Matlab simulation of the CRM totem-pole PFC.



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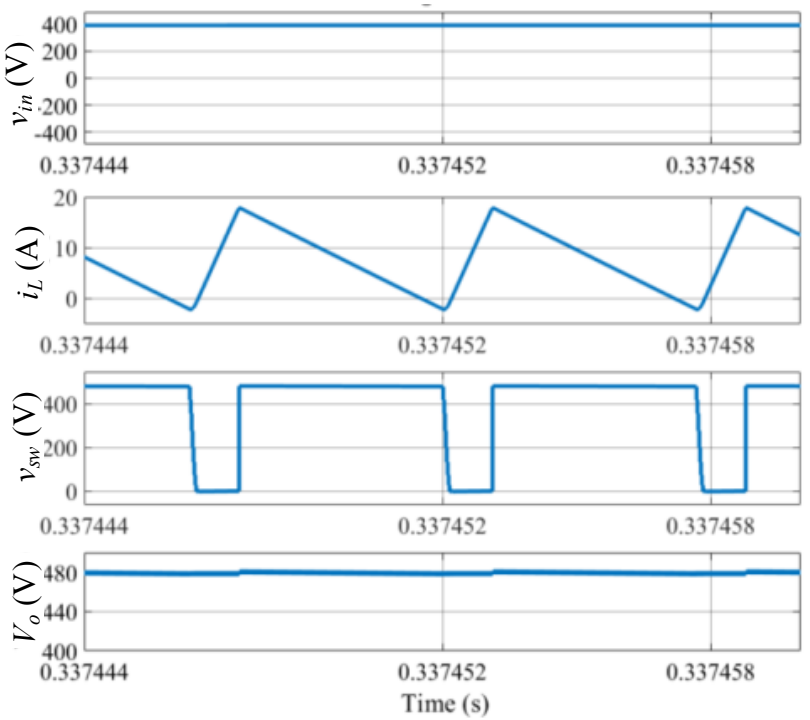


(b)

Figure 4.2: Simulation waveforms of the CRM totem-pole PFC converter with $v_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}, $P_o = 1.5$ kW. (a) Line-cycle waveforms; (b) Switching wavefroms at peak input voltage.

With the phase-shift PWM (PSPWM), gate signals of $S_{1a} - S_{3a}$ are shifted by 120° consecutively, and $S_{1b} - S_{3b}$ use the complementary gate signals of $S_{1a} - S_{3a}$. For the flying capacitor PFC at steady state, the duty cycle of $S_{1a} - S_{3a}$ is shown in (4.2).

$$d = \begin{cases} \frac{v_{in}}{V_o}, & v_{in} \geq 0 \\ 1 + \frac{v_{in}}{V_o}, & v_{in} < 0 \end{cases} \tag{4.2}$$

Table 4.2 shows the design specifications of the four-level flying capacitor totem-pole PFC rectifier. Because of the reduced device voltage stress, 200 V GaN devices are used with lower cost and on resistance. 100 kHz switching frequency is selected so that the equivalent inductor current ripple frequency is 300 kHz, which is similar with the average switching frequency of the two-level CRM totem-pole PFC. The same inductor design as the two-level totem-pole PFC is adopted. Due to the multi-level operation, cascaded bootstrap scheme is employed to achieve a compact gate drive circuit design [119]. Hence, six isolated gate drivers with the associated low-dropout regulators (LDOs) and bootstrap diodes are needed.

To validate the function, a simulation model of the four-level flying capacitor totem-pole PFC is built in Matlab Simulink, as presented in Figure 4.3, and the control strategy developed in [121] is used in the simulation. Figure 4.4 displays the operation waveforms, where v_{sw} represents the voltage across the two switching nodes of the two phase legs. Multi-level operation is achieved, and the output voltage is regulated at 480 V. Also, the inductor current is well-controlled with less than 5 A current ripple and 300 kHz equivalent ripple frequency.

4.1.3 Performance Evaluation and Comparison

To compare the two PFC topologies, converter loss at full load is assessed, including the GaN device conduction loss and switching loss, inductor core loss and winding loss, and the power loss dissipated on the gate drive circuits. Also, cost of the GaN devices, inductors, flying capacitors, and the gate drive circuits are evaluated.

Table 4.2: Design specifications of the four-level flying capacitor PFC.

Parameter	Value
V_{in}	277 V_{ac}, 60 Hz
V_o	480 V_{dc}
P_o	1.5 kW
$S_{1a} - S_{3a}, S_{1b} - S_{3b}$	EPC2215, 200 V
L_b	26.67 µH, powder core Mix-2-T157
C_1, C_2	10 µF, TDK C5750X6S2W225K250KA ×5, 450 V, 2.2 µF
f_{sw}	100 kHz
Cascaded bootstrap gate drive	Isolated gate drivers, Silicon Labs SI8271GB-IS×6 LDOs, Rohm BD60GC0MEFJ-ME2×6 Bootstrap diodes, Vishay VS-2EFH02HM3/I×5

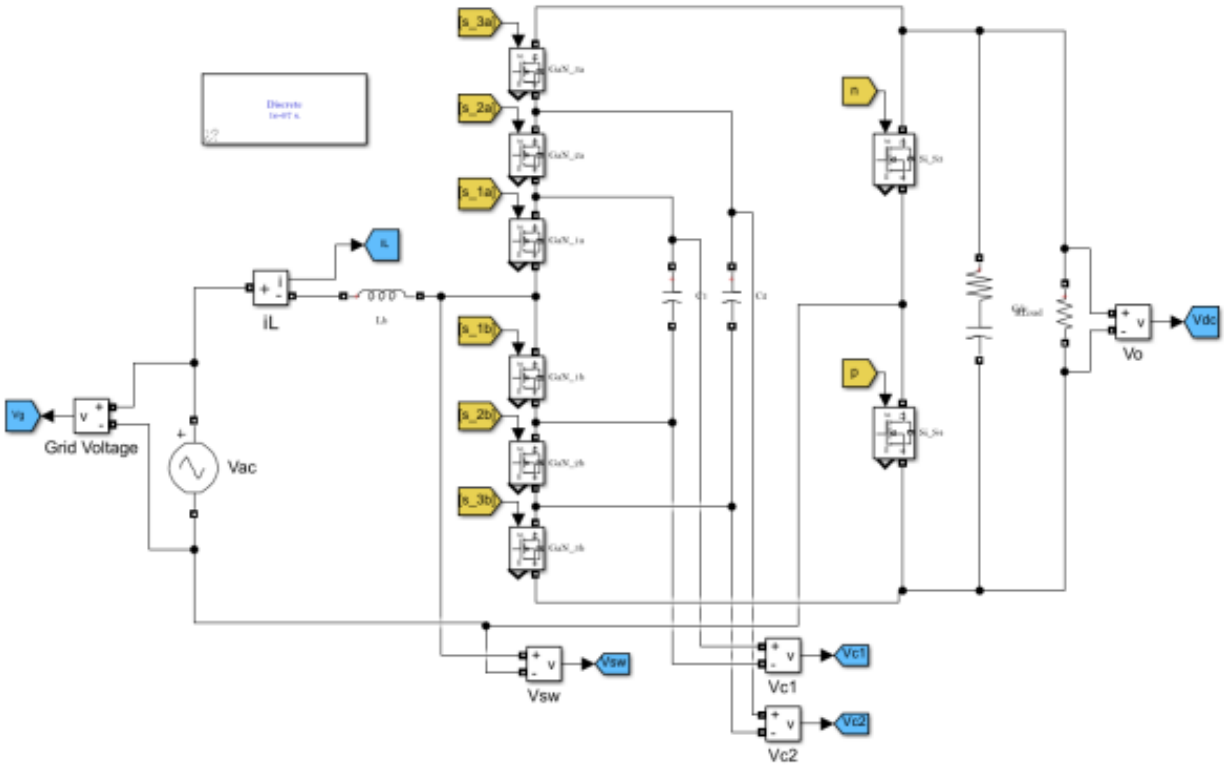
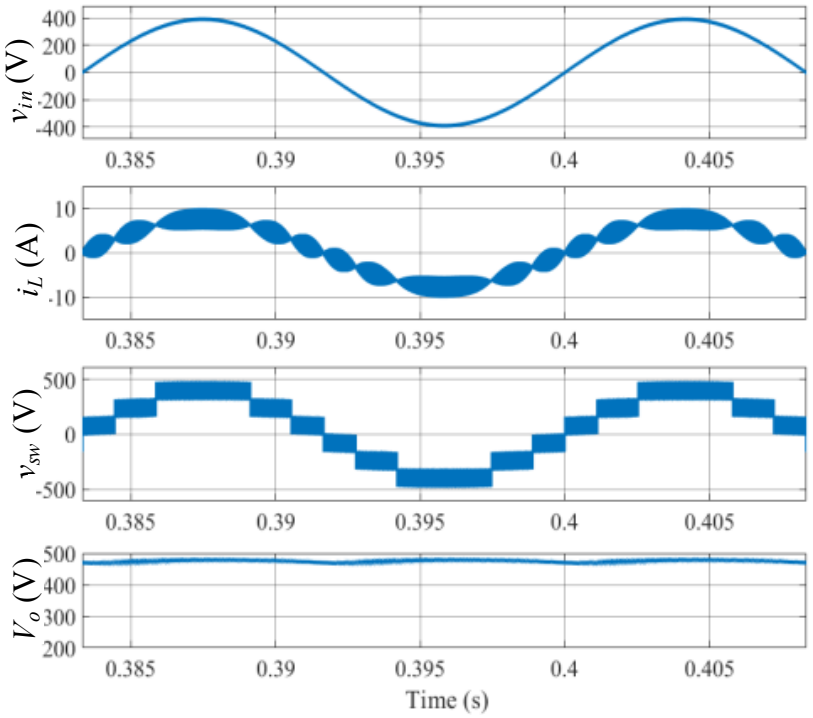


Figure 4.3: Matlab simulation of the four-level flying capacitor PFC.



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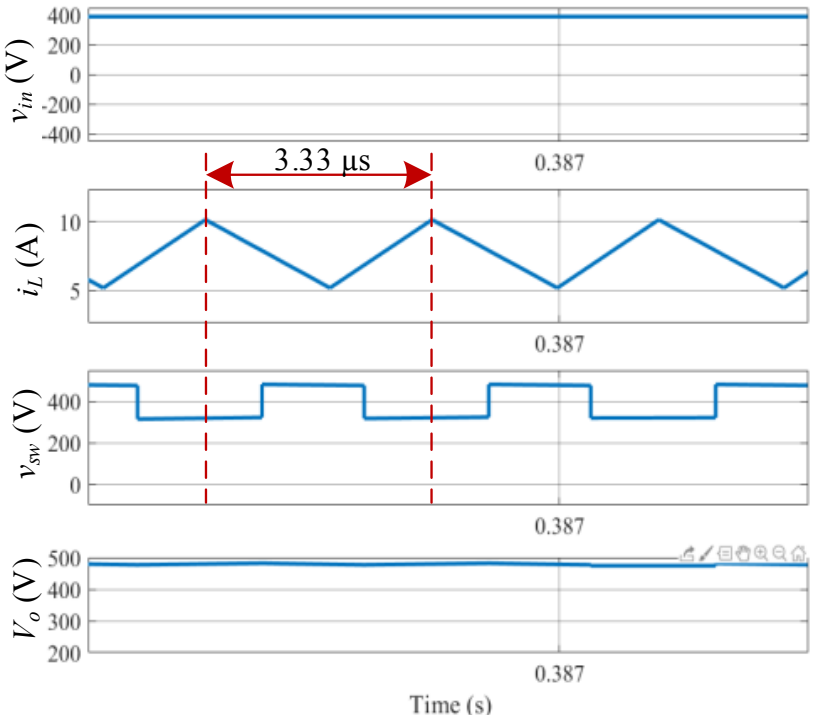


(b)

Figure 4.4: Simulation waveforms of the four-level flying capacitor totem-pole PFC converter with v_{in} = 277 V_{ac}, V_o = 480 V_{dc}, P_o = 1.5 kW. (a) Line-cycle waveforms; (b) Switching wavefroms at peak input voltage.

As displayed in Table 4.3, both the loss and the cost of the four-level flying capacitor PFC converter are higher than that of the CRM totem-pole PFC converter. Although the low-voltage GaN devices are cheaper than 650 V GaN devices, the increased expense on flying capacitors and gate drive components makes the total cost of the four-level PFC much higher than the two-level PFC.

In terms of the converter loss, significant switching loss is induced with hard switching operation of the four-level flying capacitor PFC, while CCM operation with lower inductor current ripple and RMS current leads to reduced inductor loss and device conduction loss. Soft switching is also executable for the multi-level converters to help reduce the switching loss. Nevertheless, switching states with the capability of ZVS transition needs to be identified, and nonlinear device C_{oss} at different voltage levels should be modeled [210, 211]. The increased complexity in ZVS modulation and control implementation makes it less worthwhile to achieve soft switching in the four-level flying capacitor PFC rectifier compared with the two-level totem-pole PFC.

According to the above comparison, the CRM totem-pole PFC converter is selected for the data center power supply due to the following reasons.

- Simple topology with low part count.
- Low conduction loss with 650 V GaN devices and Si MOSFETs.
- Capable of achieving ZVS operation, leading to significantly reduced switching loss and high efficiency. Hence, switching frequency can be pushed to hundreds of kHz or even MHz, resulting in high power density.

Table 4.3: Performance comparison of the two PFC topologies.

CRM Totem-pole PFC		
Component	Loss	Cost
GaN device	2.74 W	24.9 $
Inductor	5.15 W	2 $
Gate drive circuit	0.88 W	7.3 $
Total	8.34 W	34.2 $
Four-level flying capacitor PFC		
Component	Loss	Cost
GaN devices	9.42 W	22.68 $
Inductor	1.51 W	2 $
Flying capacitors	ignored	14.9 $
Gate drive circuit	1.95 W	15.2 $
Total	12.88 W	54.78 $

4.2 GaN-Based Totem-Pole PFC Rectifier with Full-Range ZVS Modulation

4.2.1 Operation Principle

Figure 4.5 shows the topology of the GaN-based totem-pole PFC rectifier, where switches S_1 and S_2 are GaN transistors operating at high frequency, and S_3 and S_4 are Si MOSFETs working at ac line frequency. During the positive half line cycle, S_4 is always ON, S_3 is always OFF, S_2 is the active switch (AS), and S_1 is the synchronous switch (SS). During the negative half-line cycle, S_3 is always ON, S_4 is always OFF, S_1 is the active switch, and S_2 is the synchronous switch. To minimize the switching loss, the PFC converter operates in CRM, where ZVS switching or valley switching are achieved with the resonance between the boost inductor and the device junction capacitors.

The operation principle of the CRM totem-pole PFC is illustrated with the theoretical operation waveforms shown in Figure 4.6 and the state-plane trajectories shown in Figure 4.7. Discussion here is based on the operation within the positive half line cycle, with the assumption that V_{in} is nearly-constant in one switching cycle. For the state-plane trajectories, the characteristic impedance Z_n is defined as $Z_n^2 = {}^{L_b}/_{(2C_{oss})}$, where C_{oss} is the equivalent drain-to-source capacitance of S_1 and S_2, assuming $C_{oss,S1} = C_{oss,S2} = C_{oss}$. The resonance angular frequency ω_r is designated as $w_r^2 = {}^{1}/_{(2C_{oss}L_b)}$.

Interval I - $T_{on,AS}$: during this time interval, AS S_2 is turned ON, and the boost inductor is charged by V_{in}. $V_{ds\_S2} = 0, V_{ds\_S1} = V_o$, and the inductor current i_L keeps increasing until S_2 is turned OFF.

Interval II - T_{r1}: in the deadtime, both S_1 and S_2 are OFF, and resonance happens between the boost inductor and device junction capacitors. $C_{oss,S1}$ is discharged and $C_{oss,S2}$ is charged. Consequently, $V_{ds,S2}$ increases from zero to V_o, $V_{ds,S1}$ decreases from V_o to zero, and i_L resonates through the peak value, $i_{L,pk}$.

Interval III - $T_{on,SS}$: because of the resonance, SS S_1 is always turned ON with ZVS. During the conduction time, the inductor is discharged by $(V_{in} - V_o)$, $V_{ds\_S2} = V_o, V_{ds\_S1} = 0$. S_1 is turned OFF when i_L declines to zero.

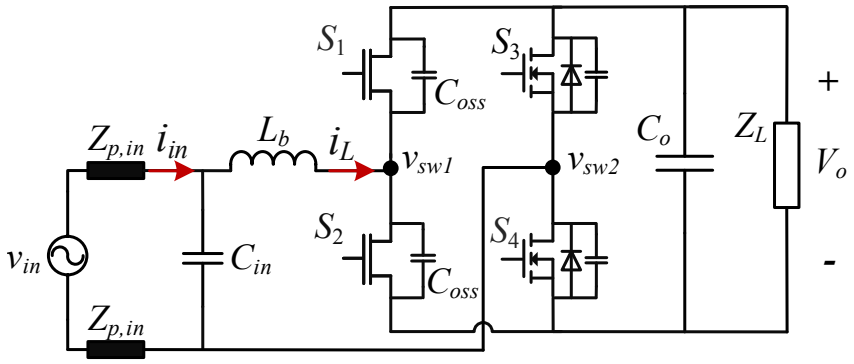
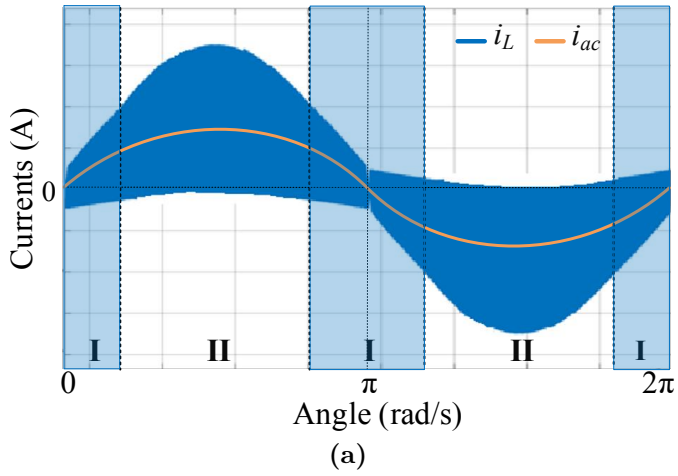


Figure 4.5: GaN-based totem-pole PFC converter.



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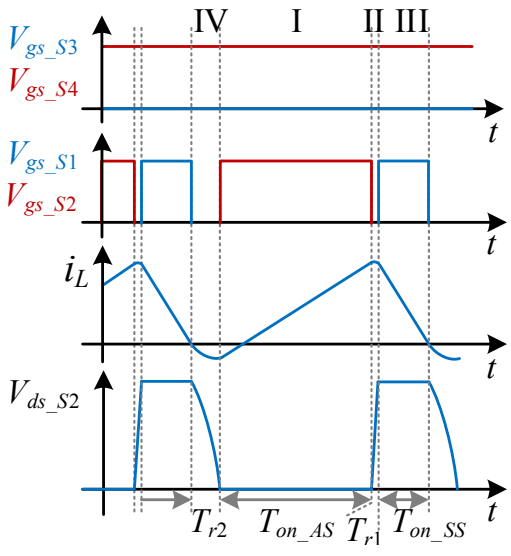

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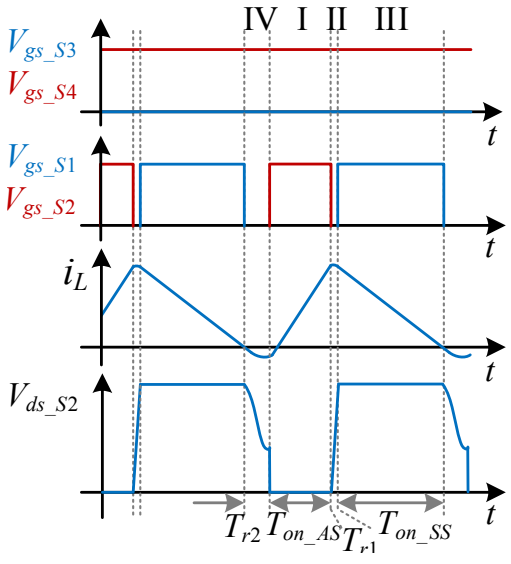
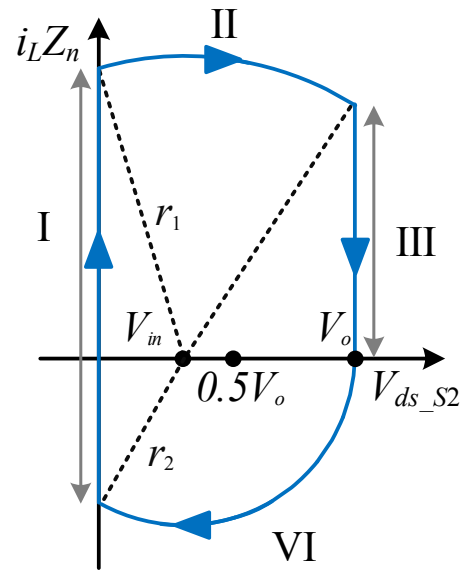


(c)

Figure 4.6: Operation waveforms of the CRM totem-pole PFC converter. (a) Current waveforms in one line cycle; (b) Switching waveforms in natural ZVS region I with $V_{in} \leq 0.5V_o$; (c) Switching waveforms in non ZVS region II with $V_{in} > 0.5V_o$.



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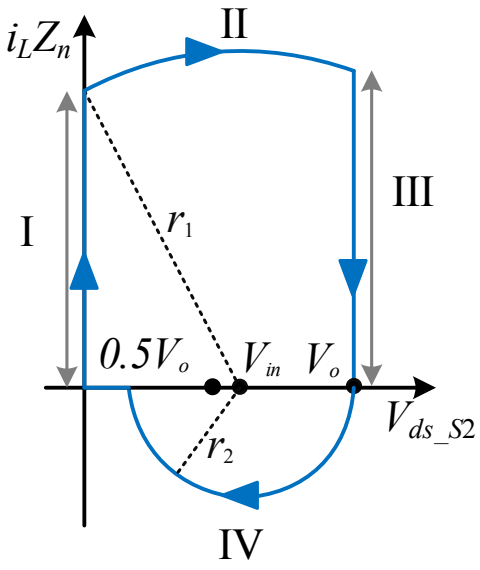


(b)

Figure 4.7: State plane trajectories in the positive half line cycle during (a) ZVS region I with $V_{in} \leq 0.5V_o$; (b) non ZVS region II with $V_{in} > 0.5V_o$.

Interval IV - T_{r2}: During the second deadtime, resonance happens again between the boost inductor and device junction capacitors. In region I where $V_{in} \leq 0.5V_o$, the energy stored in the inductor is sufficient to charge $C_{oss,S1}$ and discharge $C_{oss,S2}$. Hence, V_{ds_S2} is able to decrease to zero, and S_2 can be turned on in ZVS in the following switching cycle. However, in region II where $V_{in} > 0.5V_o$, V_{ds_S2} can only resonate to a valley point which is equal to $(2V_{in} - V_o)$, so partial C_{oss} loss occurs at the following turn-on instant.

Assuming $v_{in} = \sqrt{2}V_{in,rms}\sin\omega t$, the non-ZVS turn-on loss at each switching cycle is

$$P_{coss}(v_{in}, t) = \begin{cases} 0, & V_{in} \leq 0.5V_o \\ \frac{1}{2}C_{oss}(2\sqrt{2}V_{in,rms}\sin\omega t - V_o)^2 \times f(v_{in}, t), & V_{in} > 0.5V_o \end{cases} \tag{4.3}$$

Figure 4.8 shows the C_{oss} related loss at different switching frequencies in the positive half-line cycle. It is clear that the non-ZVS loss increases with the switching frequency.

In order to address the hard switching issue, ZVS extension method is developed in [140, 115, 13]. As elaborated in the green line in Figure 4.9, instead of turning off SS right after i_L reaches zero, SS is kept ON until a negative current is obtained so that there is enough energy to help realize ZVS turn-on of AS. To ensure V_{ds_S2} resonates to zero before turning on AS, the required extended conduction time is

$$T_{ex\_SS} = \frac{\sqrt{(2V_{in} - V_o)V_o}}{(V_o - V_{in})w_r} \tag{4.4}$$

Although the ZVS condition without margin is the ideal condition with no extra circulating current, it does not provide any time margin for the ZVS, and ZVS is only realized in one instant. In the control implementation, it is difficult to guarantee ZVS in each switching period, and even a slightly early turn-on moment would lead to switching loss and decrease the efficiency.

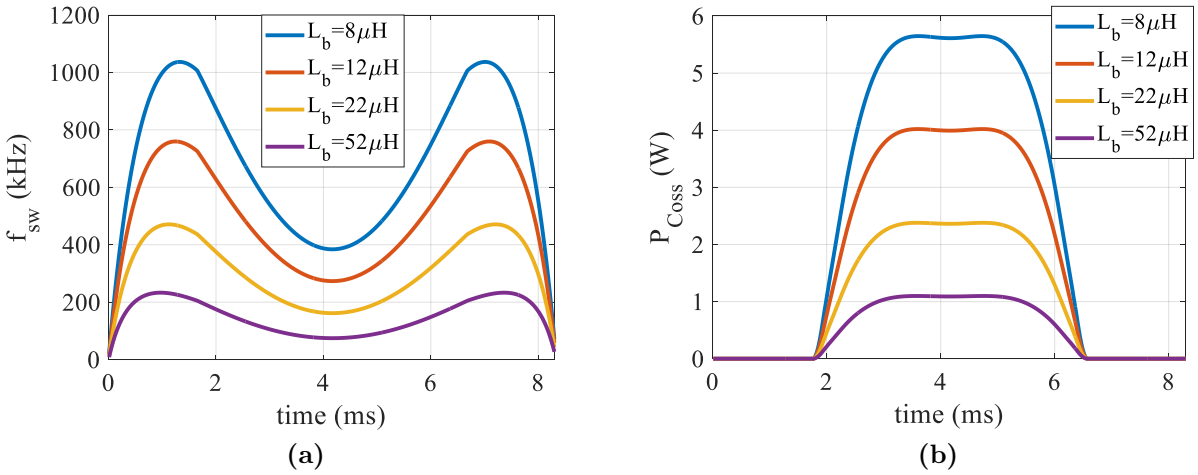


Figure 4.8: Calculated non-ZVS loss with different boost inductances in the positive half-line cycle. (a) Switching frequencies; (b) C_{oss} related loss.

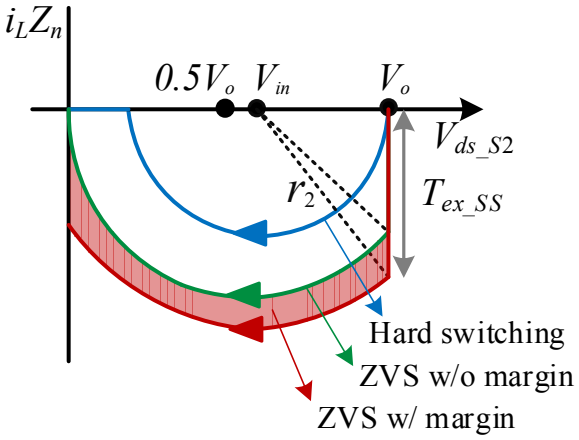


Figure 4.9: Trajectories of resonance for different ZVS conditions.

In this work, a ZVS extension method with a small ZVS margin is proposed. Based on the resonance trajectory, ZVS operation is achieved as long as r_2 is larger than V_{in}. Hence, the resonant radius r_2 is limited as $r_2 = k_0 V_{in}$, where k_0 is the margin coefficient that is slightly larger than 1. The value of k_0 cannot be too large, because large ZVS margin means more negative inductor current, hence larger RMS current and conduction loss. To generally represent the ZVS operation in the whole line cycle, the ZVS constraint parameter k is proposed and defined as

$$k = \frac{r_2}{V_{in}} = \begin{cases} \frac{V_o - V_{in}}{V_{in}}, & V_{in} \le V_{bound} \\ k_0, & V_{in} > V_{bound} \end{cases} \tag{4.5}$$

Because of the ZVS margin, the boundary input voltage V_{bound} between natural ZVS region and non-natural ZVS region is no longer $0.5V_o$, instead, $V_{bound} = {V_o}/{(k_0 + 1)}$. And the adaptive extended conduction time is

$$T_{ex\_SS} = \frac{\sqrt{(k^2 - 1)V_{in}^2 - V_o^2 + 2V_o V_{in}}}{w_r(V_o - V_{in})} \tag{4.6}$$

When $V_{in} \le V_{bound}$, $T_{ex\_SS} = 0$; when $V_{in} > V_{bound}$, $T_{ex\_SS} > 0$. Figure 4.10 shows the switching waveforms of the CRM totem-pole PFC with full-line-cycle ZVS in the positive half line cycle. T_{zvs} is the small time margin for ZVS achievement. Turning on the AS at any time during T_{ZVS} would lead to ZVS.

4.2.2 Adaptive Analytical Converter Model

Converter operation should be modeled analytically for use in the power stage design and control implementation. To program the conduction time in real time with one microcontroller, a simplified but accurate calculation method is proposed in [16], where the inductor current is approximated as a triangular waveform. Hence, based on the simplified calculation, an adaptive analytical model corresponding to the margin ZVS modulation of the CRM totem-pole PFC converter is developed.

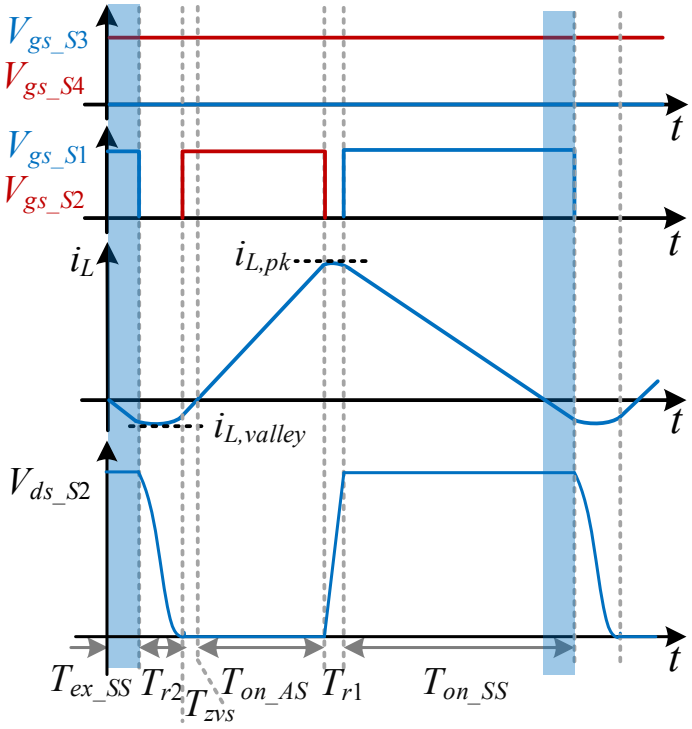


Figure 4.10: Switching waveforms of the CRM totem-pole PFC with full-line-cycle ZVS modulation in the positive half line cycle.

Assuming the input ac voltage is $v_{in} = \sqrt{2}V_{in,rms}\sin\omega t$, the input current is $i_{in} = \sqrt{2}P_o/\eta V_{in,rms}\sin\omega t$ where P_o is the converter output power, η is the converter efficiency, and ω is the input line frequency. Since the resonant intervals are very short, the inductor current can be approximated as a triangular waveform with

$$i_{L,pk} = \frac{V_{in}}{L_b}T_{on\_AS} \tag{4.7}$$

$$i_{L,valley} = -\frac{kV_{in}}{Z_n} \tag{4.8}$$

$$i_{L,ave} = \frac{1}{2}(i_{L,pk} + i_{L,valley}) \tag{4.9}$$

Based on the above equations, the conduction time of AS is given by letting $i_{in} = i_{L,ave}$.

$$T_{on\_AS} = \frac{2P_oL_b}{\eta V_{in,rms}^2} + \frac{k}{w_r} \tag{4.10}$$

where $T_{on\_c} = {}^{2P_oL_b}/\left(\eta V_{in,rms}^2\right)$ is constant at a steady-state operation, and $T_{on\_v} = {}^{k}/_{w_r}$ varies simultaneously with the the input voltage. The conduction time of SS is calculated based on the inductor volt-second balance.

$$T_{on\_SS} = \frac{V_{in}}{V_o - V_{in}}T_{on\_AS} + T_{ex\_SS} \tag{4.11}$$

Also, according to the state-plane trajectory, the resonant time intervals T_{r1}, T_{r2}, and the ZVS margin period T_{zvs} are

$$T_{r1} = \frac{1}{w_r}\left(\pi - \cos^{-1}\left(\frac{1}{\sqrt{1+\left(\frac{Z_nT_{on\_AS}}{L_b}\right)^2}}\right) - \cos^{-1}\left(\frac{V_o - V_{in}}{V_{in}\sqrt{1+\left(\frac{Z_nT_{on\_AS}}{L_b}\right)^2}}\right)\right) \tag{4.12}$$

$$T_{r2} = \frac{1}{w_r}\left(\pi - \cos^{-1}\left(\frac{V_o - V_{in}}{kV_{in}}\right) - \cos^{-1}\left(\frac{1}{k}\right)\right) \tag{4.13}$$

$$T_{zvs} = \frac{\sqrt{(k^2-1)}}{w_r} \tag{4.14}$$

Based on the model, the PFC operation waveforms are predicted, as shown in Figure 4.11.

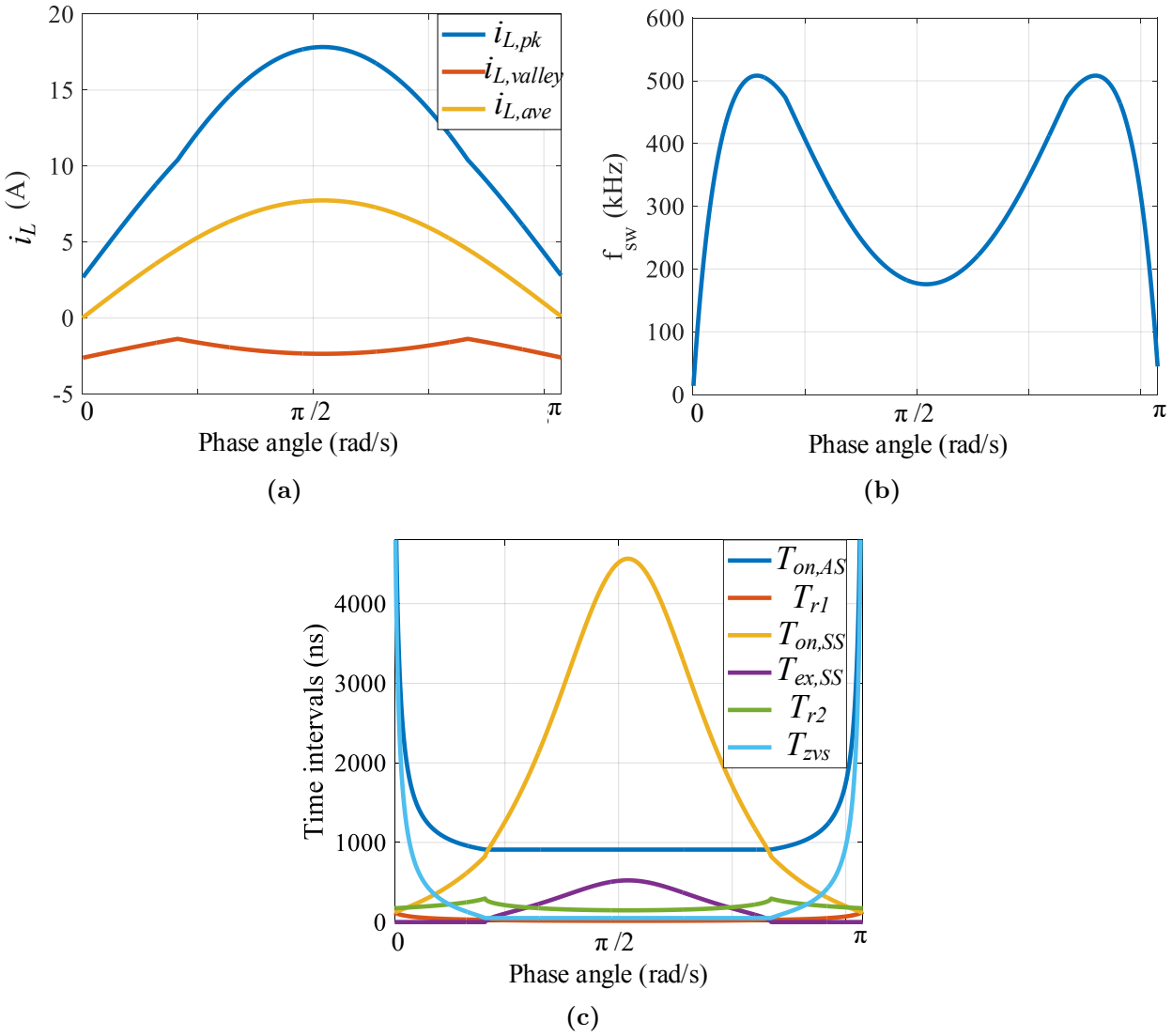


Figure 4.11: Predicted waveforms of a CRM totem-pole PFC within the positive half line cycle with $P_o = 1.5$ kW, $V_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}, $k_0 = 1.1$, $T_{zvs,min} = 50$ ns. (a) Inductor currents; (b) PFC switching frequency; (c) Switching time intervals.

4.3 Component Selection

This section details the component selection of a CRM totem-pole PFC rectifier with $P_o = 1.5$ kW, $V_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}.

4.3.1 Device Selection

Based on the PFC specifications, high-voltage devices with sufficient current rating should be selected. Since GaN devices operate in high frequency with ZVS turn-on, the soft switching figure of merit (FOM) discussed in [212] is adopted to evaluate the performance of the existing high-voltage GaN devices. The value of on resistance R_{on} is used to assess the conduction loss, where lower R_{on} is preferred. For the switching loss, although the output charge Q_{oss} is recovered in ZVS operation, it has a direct influence on the circulating energy required for ZVS achievement. For the sake of improving the power transfer efficiency, lower Q_{oss} is desired for reduced ZVS current and transition time, which leads to lower RMS current and longer power delivery time in high-frequency soft-switching converters. Hence, the FOM for comparing various GaN devices is defined as

$$FOM = \frac{1}{R_{on} Q_{oss}} \tag{4.15}$$

In this work, six GaN devices with voltage rating above 600 V and current rating above 20 A are considered. Figure 4.12 shows the C_{oss} versus device drain-to-source voltage V_{DS}. Based on the C_{oss} curves, the equivalent charge capacitance $C_{eq,Q}$ at $V_{DS} = 480$ V are calculated, thus Q_{oss} is predicted. Table 4.4 presents the cost, $C_{eq,Q}$, Q_{oss}, R_{on}, and FOM of the six GaN devices. As can be seen, GS66508T and PGA26E07BA have competitive FOM with relatively low R_{on} and Q_{oss}. Nevertheless, the price of PGA26E07BA is much higher than that of GS66508T. Given the converter cost, GS66508T is selected for the PFC converter.

For the Si device, the one with low R_{on} is preferred because the switching loss is negligible at low line frequency. In this work, 650 V Si MOSFETs IPW65R019C7 from Infineon are used with $R_{on} = 20$ mΩ.

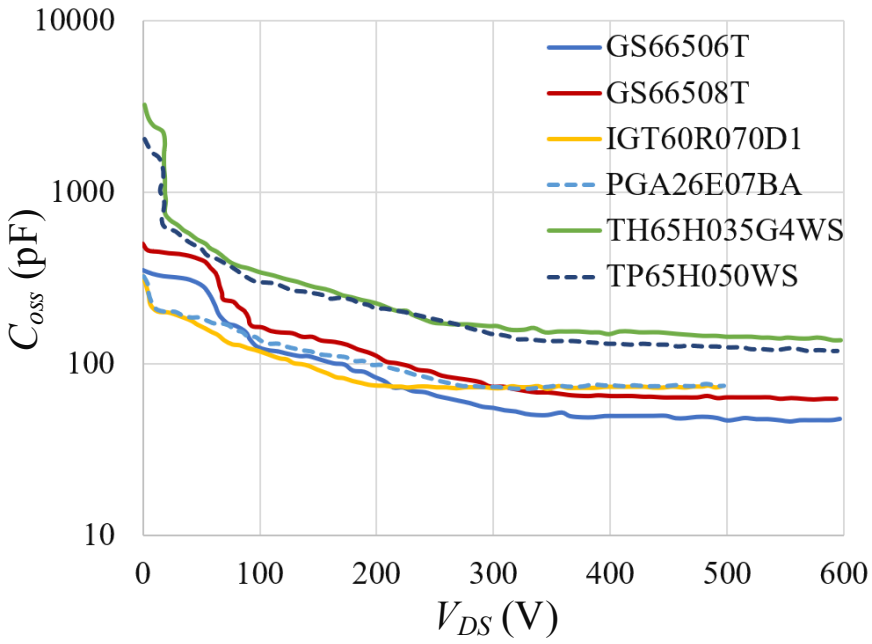


Figure 4.12: C_{oss} curves vs. V_{DS}.

Table 4.4: 600 V GaN device comparison.

Device Part No.	Manufacturer	$C_{eq,Q}$ (pF)	Q_{oss} (nC)	R_{on} (Ω)	FOM ($1/\Omega nC$)	Price ($)
GS66506T	GaN systems	104.5	50.2	0.067	0.298	12.15
GS66508T	GaN systems	124.8	59.9	0.05	0.334	14.42
IGT60R070D1	Infineon	94.1	45.2	0.07	0.316	14.81
PGA26E07BA	Panasonic	105.6	50.7	0.056	0.352	31.5
TP65H035G4WS	Transphorm	304.4	146	0.035	0.196	12.2
TP65H050WS	Transphorm	275.2	132	0.05	0.151	11.8

4.3.2 Dc-Link Capacitor Selection

For the PFC rectifier in data centers, the dc-link capacitance is determined based on the requirements of the output voltage ripple and the hold-up time [152]. First, for the single-phase rectifier, large double-line frequency ripple exists on the output due to the ac-dc power unbalance [151]. So the dc capacitance should be adequate to buffer the ripple energy and maintain the ripple magnitude within the limit. Assume the steady-state output voltage has maximum value at $V_{o,max}$ and minimum value at $V_{o,min}$, the ripple energy needs to be buffered is

$$E_{ripple} = \frac{P_o}{2\pi f_{line}} \leq \frac{1}{2} C_o (V_{o,max}^2 - V_{o,min}^2) \tag{4.16}$$

Thus, the required capacitance for voltage ripple limitation is

$$C_o \geq \frac{P_o}{\pi f_{line}(V_{o,max}^2 - V_{o,min}^2)} \approx \frac{P_o}{\pi f_{line} 2 V_o \triangle V_o} \tag{4.17}$$

For the PFC rectifier with $P_o = 1.5$ kW, $V_o = 480$ V, $\triangle V_o = 10$ V, the dc capacitance should be higher than 829 µF.

On the other hand, in the event of input power failure, the dc capacitance should have sufficient energy to provide the load power for at least one line cycle (16.6 ms), that is the hold-up time for server power supplies. The required capacitance for hold-up time is

$$C_o \geq \frac{2 P_o t_{hold}}{V_o^2 - V_{o,low}^2} \tag{4.18}$$

where $V_{o,low}$ is the lowest dc voltage for the dc-dc stage, which is selected as 408 V here. Hence, the minimum capacitance for hold-up time requirement is 779 µF. Given the two prerequisites, the dc capacitance should be larger than 829 µF, and 6 paralleled 600 V, 180 µF electrolytic capacitors are selected as the dc-link capacitors.

4.3.3 Boost Inductor Design

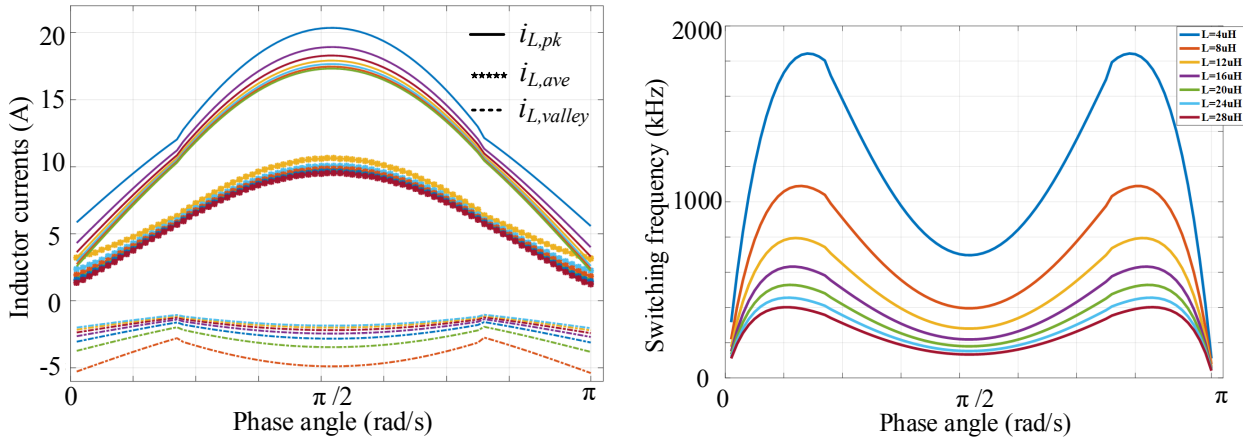
Based on the analytical converter model, the input variables include the input voltage V_{in}, output voltage V_o, output power P_o, boost inductance L_b, and GaN device output capacitance

C_{oss}. Hence, for a given device implementation, where voltages and power level are known, L_b directly determines the switching frequency range and the current waveforms. Figure 4.13 shows the current waveform and switching frequency at various boost inductances. Lower boost inductance results in higher switching frequency and larger current ripple, further impacting the converter loss.

The inductor loss and size are highly dependent on the physical design. Typically, gapped ferrite core is used for the boost inductor due to its lower core loss. However, the ac winding loss in gapped ferrite core can be very high due to the large magnetic field and fringing flux around the air gap. Although the toroidal powder core has larger core loss, the ac winding loss is relatively smaller because most of the winding region is exposed to the free space [213]. As shown in Figure 4.14(a), for the gapped ferrite core, fringing flux near the gap causes larger eddy current related loss. Figure 4.14(b) presents the measured efficiency of the dc-dc converter with boost inductors by a 3F36 ferrite EE core and Mix2 powder toroidal core. Converter with powder toroidal core has higher efficiency than that with ferrite EE core. Hence, in this design, Mix 2 toroidal powder cores from Micrometals are selected. To further decrease the winding loss, litz wire 350/42 is used.

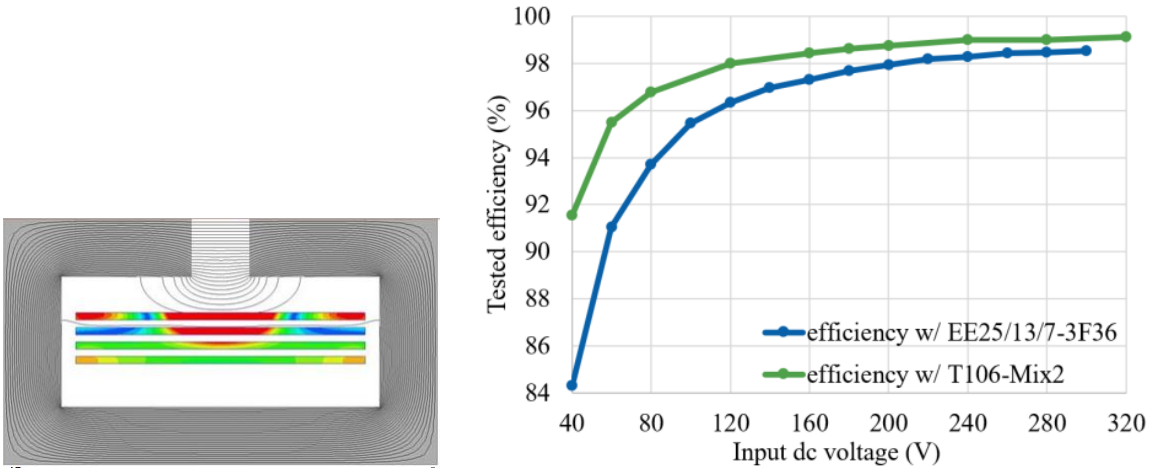
The basic principle is to select the inductor design which leads to lower converter loss and smaller core volume. Different boost inductances from 4 µH to 28 µH are considered. At each inductance, an inductor is designed with toroidal powder cores at different sizes ($T30 - T157$). Based on the loss model shown in Appendix A.1, converter loss including the inductor loss, the device loss, and the capacitor loss is predicted. Generalized Steinmetz equation (GSE) is used to calculate the core loss [214], and squared-field-derivative (SFD) method is adopted to estimate the winding loss [215].

Figure 4.15 shows the estimated converter loss and selected core volume at different boost inductances. As can be seen, the power loss decreases with increased boost inductance, leveling out around 15 W at full load and 7 W at half load when the inductance is larger than 20 µH. The required core volume increases with increased inductance. During the inductance range from 16 µH to 20 µH, core T106 is the one with smaller volume. Hence, the inductor is implemented with a T106 Mix 2, wound with 37 turns to achieve 20 µH, as shown in Figure 4.16.



(a) **(b)**

Figure 4.13: CRM totem-pole PFC performance at different boost inductances when $P_o = 1.5$ kW, $V_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}, $k_0 = 1.1$, $T_{zvs,min} = 50$ ns. (a) Inductor currents at various L_b; (b) PFC switching frequency at various L_b.



(a) **(b)**

Figure 4.14: (a) Fringing flux of gapped ferrite core; (b) Efficiency comparison of the converter in dc-dc operation with different boost inductors at 20 µH.

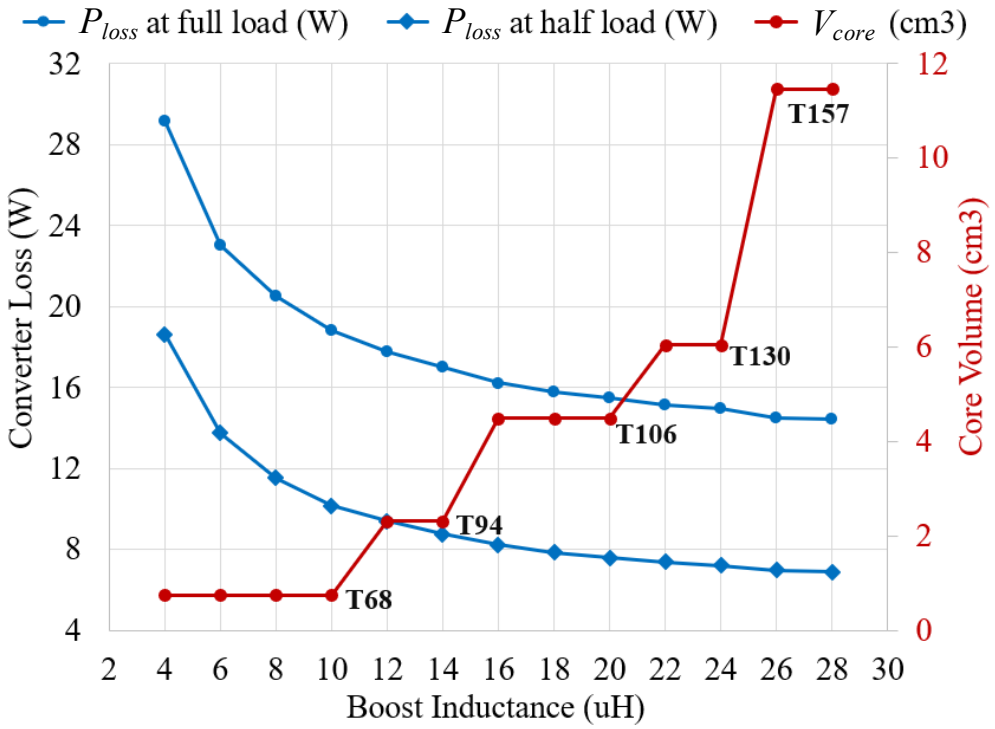


Figure 4.15: Predicted converter loss and core volume of the CRM totem-pole PFC versus various boost inductances when $V_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}, $k_0 = 1.1$.

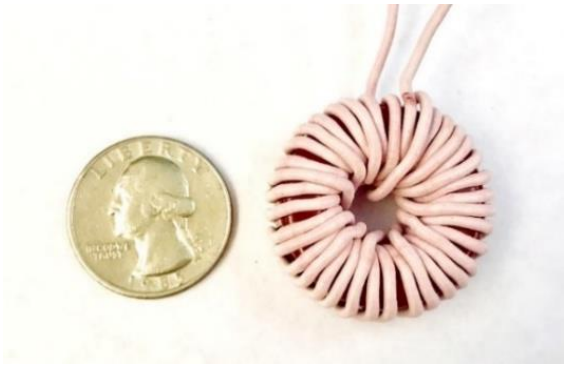


Figure 4.16: Designed boost inductor with core T106-Mix 2 and 350/42 litz wire.

4.4 Control Implementation

4.4.1 Digital-Based Variable On-time Control

To realize the full-line-cycle ZVS, digital-based variable ON-time control is implemented. Figure 4.17 presents the control structure with DSP. The input voltage v_{in}, output voltage V_o, and the inductor positive-to-negative zero current point are sensed through hardware circuits. In the DSP, a PI controller regulates V_o in the outer loop, and generates the ON time T_{on_c} to control the peak inductor current. Meanwhile, switching time intervals are calculated in real time based on the converter model and sensed voltage signals. The zero current detection (ZCD) signal is used as a time reference for the switching actions in each switching cycle. The PWM time-based counter is reset every time the ZCD signal occurs, and switching actions for AS and SS will be conducted after the associated time delays, as shown in (4.19) and Figure 4.18.

$$\begin{cases} \Delta T_{off\_SS} = T_{ex\_SS} \\ \Delta T_{on\_AS} = T_{ex\_SS} + T_{r1} \\ \Delta T_{off\_AS} = \Delta T_{on\_AS} + T_{zvs} + T_{on\_AS} \\ \Delta T_{on\_SS} = \Delta T_{off\_AS} + T_{r2} \end{cases} \tag{4.19}$$

Based on the ZCD time reset, the SS is turned OFF after the extended conduction time at $t = \triangle T_{off\_SS}$, then the AS is turned ON after the resonant time at $t = \triangle T_{on\_AS}$ and turned OFF after the ON time at $t = \triangle T_{off\_AS}$, and the SS is turned ON after a short dead time at $t = \triangle T_{on\_SS}$. In this way, CRM operation and ZVS are maintained in each switching cycle, and i_{valley} is limited by the ZCD signal. Si devices S_3, S_4 operates in line frequency, and the gate signals are determined with the help of a phase locked loop (PLL) in the DSP.

The ZCD signal is important in the control. Figure 4.19 shows the ZCD circuit design based on a current sensing resistor, which is connected in series with the boost inductor. To minimize the additional conduction loss, a small sensing resistor (10 mΩ) is selected. The following circuit includes an amplifier, a high-speed comparator and a digital isolator.

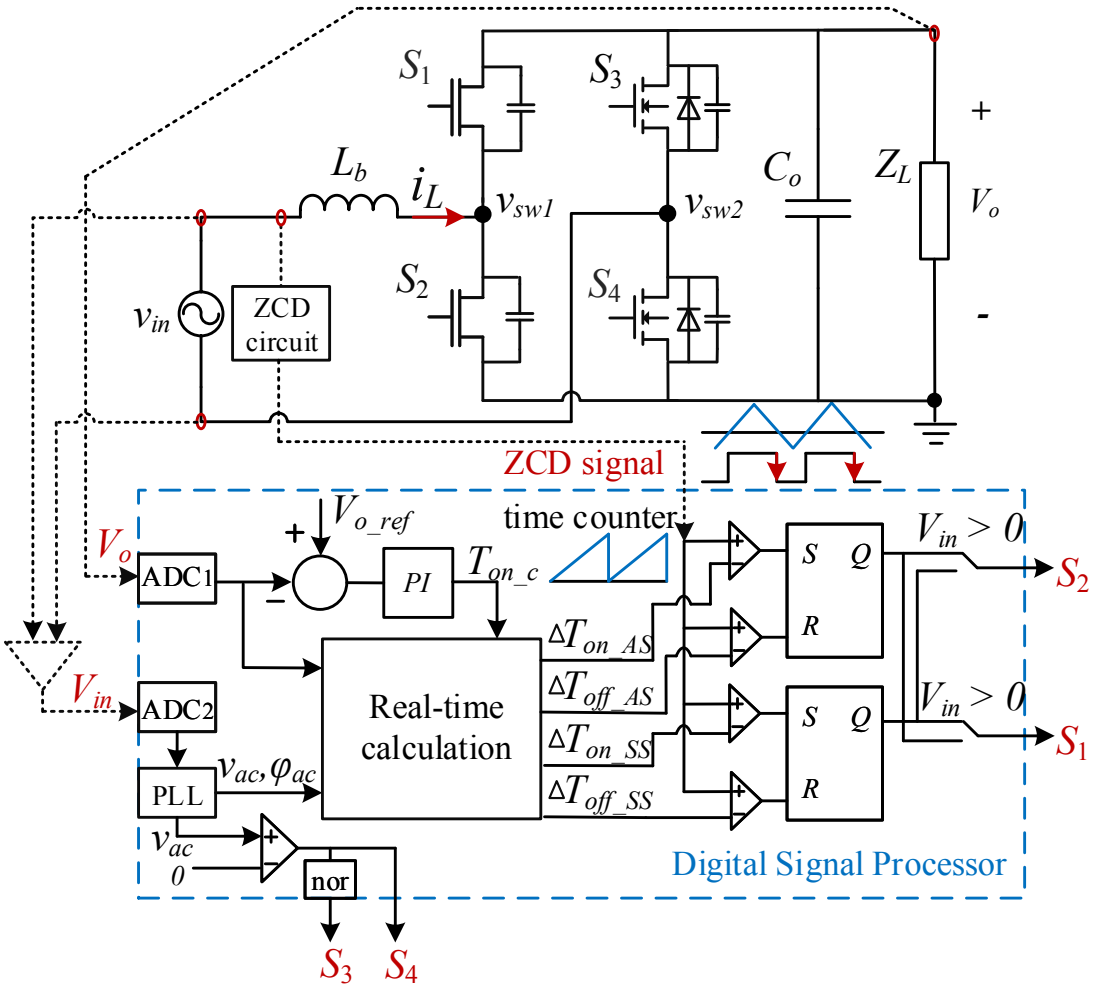


Figure 4.17: Control structure of the CRM totem-pole PFC.

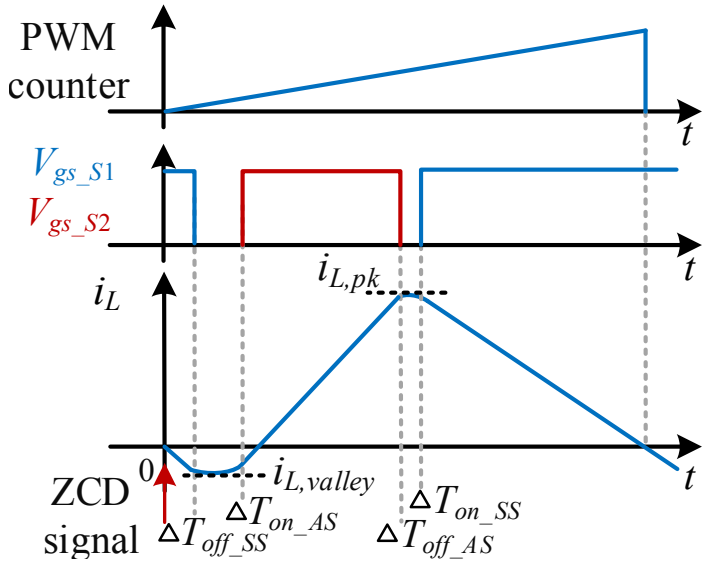


Figure 4.18: GaN device switching sequence in the positive half cycle.

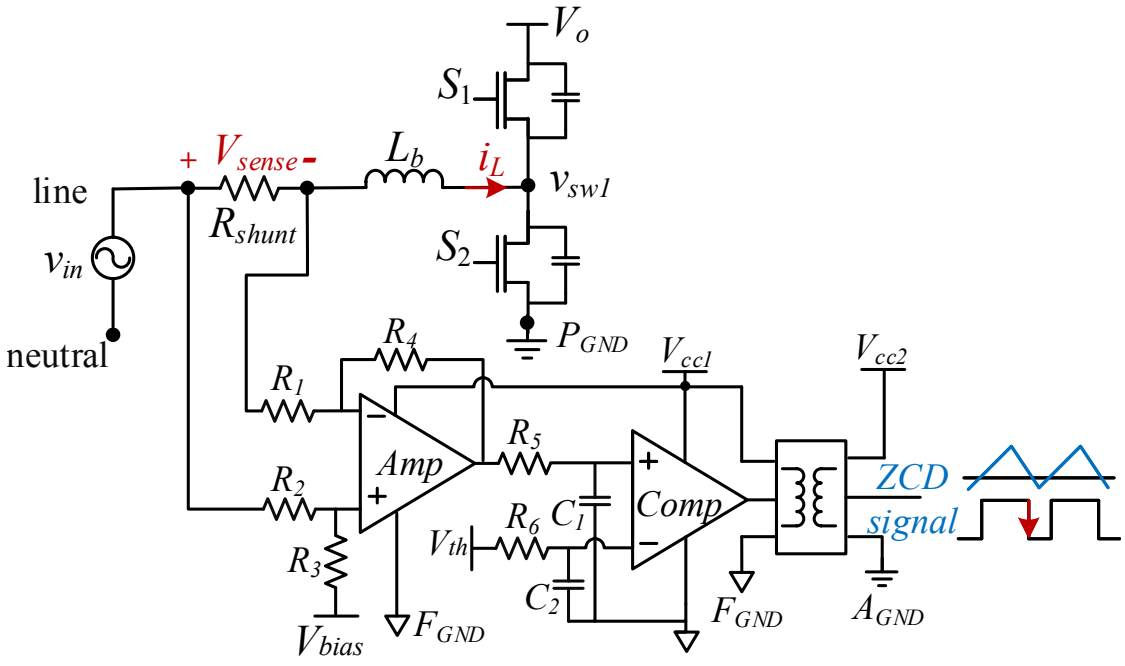


Figure 4.19: ZCD circuit with sensing resistor.

4.4.2 Voltage-Loop Controller Design

As aforementioned, the peak inductor current is controlled by the on time T_{on_AS} which is composed of two parts, $T_{on\_AS} = T_{on\_c} + T_{on\_v}$, where T_{on_c} is the part generated from the low-bandwidth PI controller, and T_{on_v} is the variable part based on the real-time calculation. When $V_{in} > V_{bound}$, $T_{on\_v} = 0$ and $T_{on\_AS} = T_{on\_c}$. Hence, the voltage-loop controller is easier to be designed during the non-natural ZVS region with $V_{in} > V_{bound}$. Here, we pick the peak input voltage point to design the voltage controller.

The ON-time-to-output voltage open-loop transfer function is required for the controller design. Since $|i_{L,valley}| \ll |i_{L,pk}|$, the average inductor current can be simplified as

$$i_{L,ave} \approx \frac{1}{2} i_{L,pk} = \frac{1}{2} \frac{v_{in}}{L_b} T_{on\_c} \tag{4.20}$$

Applying KCL law on the output network, we get

$$C_{dc} \frac{dv_o}{dt} = i_{L,ave} d' - \frac{v_o}{R_L} \tag{4.21}$$

where the duty cycle $d' \approx \frac{v_{in}}{v_o}$ for the boost converter.

Implementing perturbation and linearization on (4.20), (4.21), the small-signal result is

$$\hat{i}_{L,ave} = \frac{V_{in} \hat{t}_{on\_c} + \hat{v}_{in} T_{on\_c}}{2L_b} \tag{4.22}$$

$$C_{dc} V_o \frac{d\hat{v}_o}{dt} = V_{in} \hat{i}_{L,ave} + \hat{v}_{in} I_{L,ave} - \frac{2V_o \hat{v}_o}{R_L} \tag{4.23}$$

Inserting (4.22) into (4.23), and rearranging it in the s domain, we obtain

$$(sC_{dc}V_o + \frac{2V_o}{R_L})\hat{v}_o = \frac{V_{in}^2}{2L_b} \hat{t}_{on\_c} + (I_{L,ave} + \frac{V_{in} T_{on\_c}}{2L_b})\hat{v}_{in} \tag{4.24}$$

Then, the on-time-to-output transfer function is

$$G_{vt} = \left. \frac{\hat{v}_o}{\hat{t}_{on\_c}} \right|_{\hat{v}_{in}=0} = \frac{V_{in}^2 R_L}{4V_o L_b} \frac{1}{1 + s\frac{R_L C_{dc}}{2}} \tag{4.25}$$

To avoid the impact of double-line frequency ripple, the final voltage loop is designed to have 15 Hz control bandwidth with a phase margin of 80°, as shown in Figure 4.20.

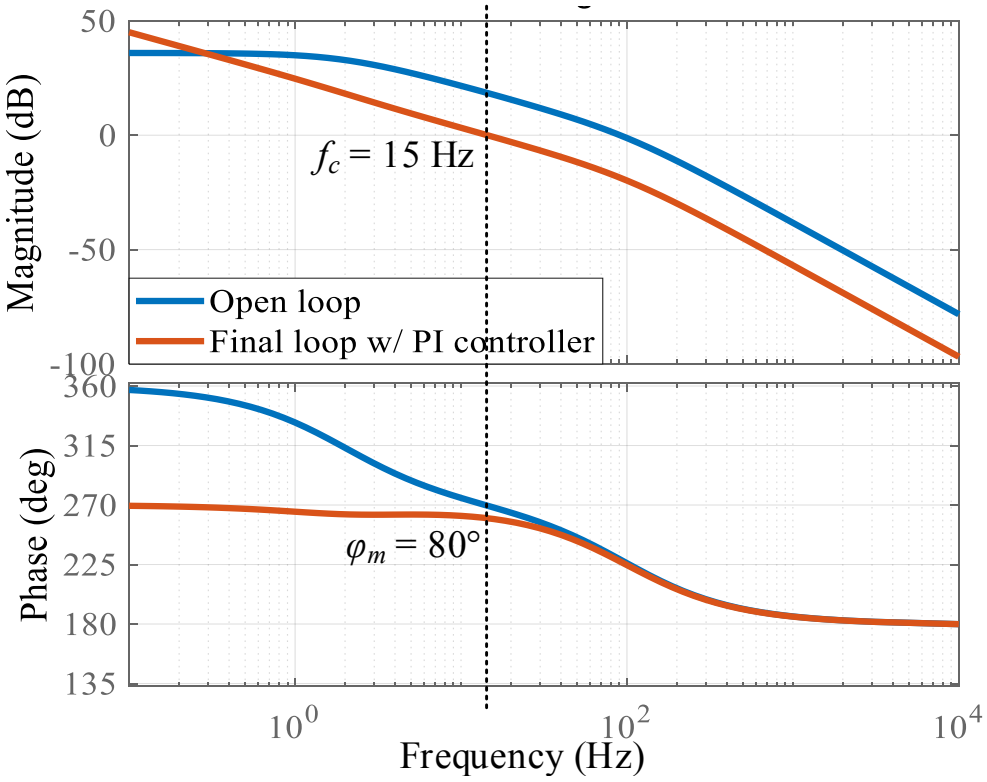


Figure 4.20: Bode diagram of the PFC voltage loop.

4.5 Experimental Verification

To verify the design, a 1.5 kW single-phase GaN-based CRM totem-pole PFC prototype is built and tested. Figure 4.21 shows the physical prototype, and Table 4.5 summarizes the detailed converter design. A TMS320F28377S DSP from Texas Instruments is used as the controller to implement the variable on-time control. In order to avoid the noise disturbance during the ac line zero-crossing, a small blanking time is adopted to shut off all switches [216].

Table 4.6 lists the converter efficiency, PF, and input current THD at different loadings, which are measured by a Yokogawa WT3000E power analyzer. Figure 4.22 and Figure 4.23 present the experimental waveforms of the PFC prototype at full load. As can be seen, the PFC rectifier operates stably with well-regulated inductor current and output voltage at 480 V. With the digital-based variable on-time control, ZVS is achieved within the whole line cycle, as displayed in Figure 4.23. The tested full-load efficiency is 98.8%, and the peak efficiency reaches 98.84%.

However, the input current is severely distorted with current THD $\geq$ 8.6%. As shown in Figure 4.22(a), i_{in} has line-cycle current distortion and large current spike at the ac line zero-crossing. Also, the inductor current i_L has current spike when turning on the GaN devices after the blanking time. Influenced by the current distortion, the PFC power factor is below 0.99.

4.6 Summary

This chapter contains the detailed design of a GaN-based PFC rectifier with v_{in} = 277 V_{ac}, V_o = 480 V_{dc} for data center power supply. Advantageous in simple topology, high device utilization, and capability of ZVS operation, the totem-pole PFC with CRM operation is selected for the rectifier design.

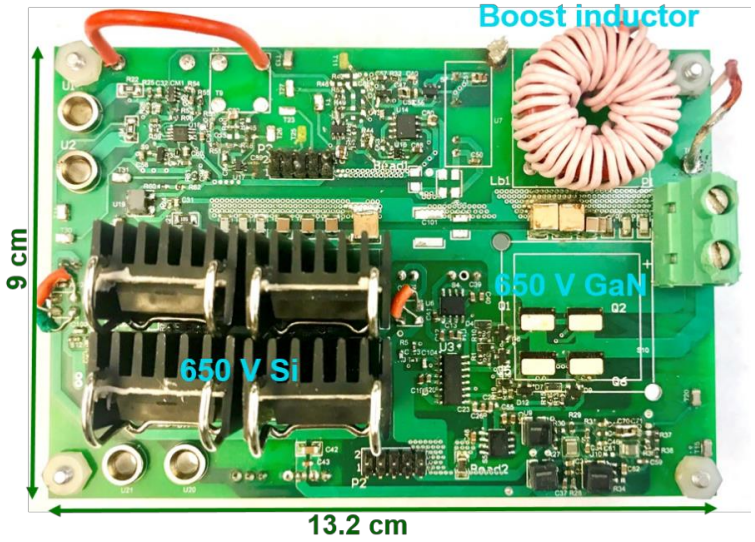


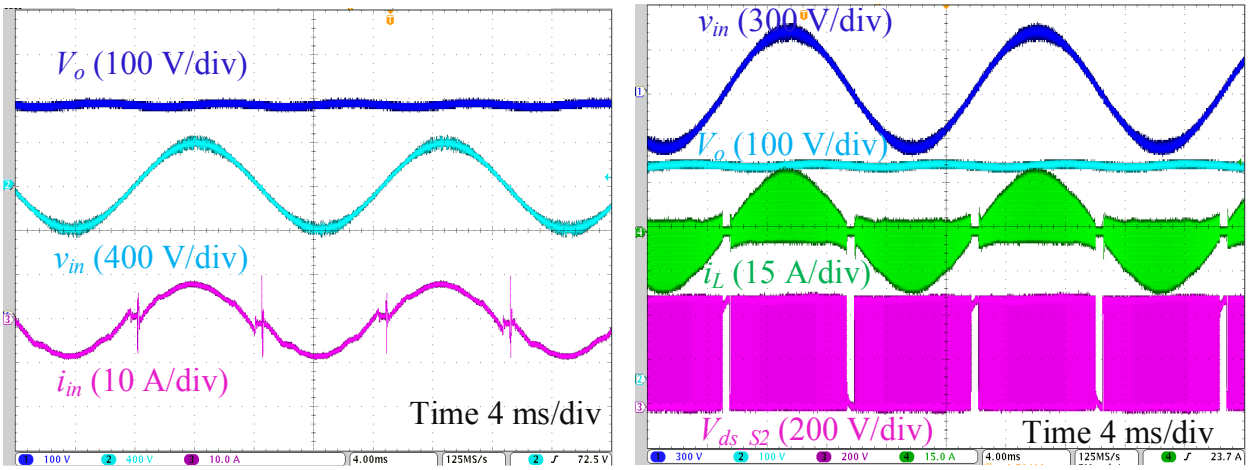
Figure 4.21: Prototype of the 1.5 kW PFC rectifier for data centers.

Table 4.5: Specifications of the PFC converter for data centers.

Parameter	Value
Input voltage v_{in}	277 V_{ac}, 60 Hz
Output voltage V_o	480 V_{dc}
Output power P_o	1.5 kW
Switching frequency f_{sw}	$174 - 508$ kHz
GaN devices S_1, S_2	GS66508T, 650 V
Si devices S_3, S_4	IPW65R019C7, 650 V
Boost inductor	20 µF with core Mix-2-T106 and 350/42 litz wire
Dc-link capacitor	6×B43541B8187M000
ZVS margin	$k_0 = 1.1$, $T_{ZVS,min} = 50$ ns

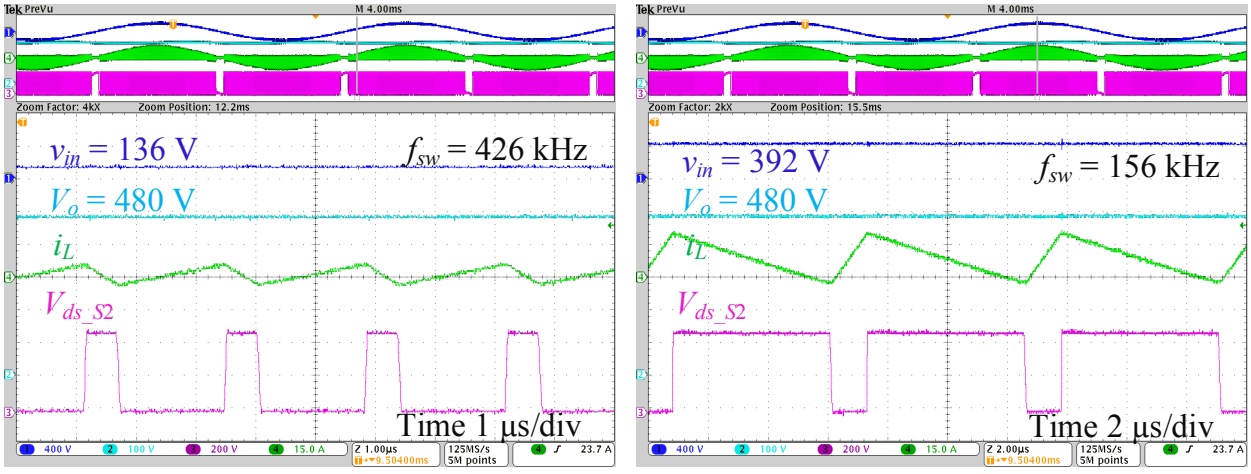
Table 4.6: Tested efficiency, PF, and current THD at various loadings of the PFC prototype.

Output Power P_o	Power Loss	Efficiency η	PF	Current THD
1497 W	18.4 W	98.78 %	0.98	8.6%
1150 W	13.5 W	98.84 %	0.97	11%
750 W	10.5 W	98.62 %	0.95	16.3%



(a) **(b)**

Figure 4.22: Experimental waveforms of the GaN-based CRM totem-pole PFC prototype at full load.



(a) **(b)**

Figure 4.23: Switching waveforms of the GaN-based CRM totem-pole PFC prototype at full load.

The operation principle of the CRM PFC is analyzed, and an adaptive ZVS modulation with ZVS time margin is proposed to achieve soft switching within the whole line cycle. To reduce the power loss and realize high switching frequency, 650 V GaN device is adopted in the fast phase leg. The value of the dc capacitor is selected considering the ripple energy and hold-up time requirement. The boost inductor is designed considering the power loss and inductor volume. To implement the full-line-cycle ZVS, predictive digital-based variable on-time control is employed.

A GaN-based 1.5 kW totem-pole PFC prototype is built. The full-line-cycle ZVS operation is experimentally demonstrated, and $>$ 98.8% peak efficiency is achieved. Nevertheless, the PFC input current has line-cycle current distortion and ac line zero-crossing current spike, which also degrades the PF. Reasons for the current distortion are investigated and the corresponding solutions are developed in the following chapter.

Chapter 5

Mitigation of Current Distortion for GaN-Based Totem-Pole PFC

Current distortion issues of the GaN-based totem-pole PFC rectifier are found in the previous chapter presented in Figure 4.22, where the low-frequency line-cycle current distortion and the ac line zero-crossing current spike are present in the input current. In this chapter, distortion mechanisms are investigated for the purpose of mitigating the PFC current THD and achieving high PF. Research targets in this chapter are:

(1) Determine the two distinct current distortion mechanisms.

(2) Propose effective solutions to mitigate the current distortion.

(3) Investigate the generality of the current distortion issues in a different application.

Research work on this chapter has been published in:

(1) J. Sun, H. Gui, J. Li, X. Huang, N. Strain, D. Costinett, L. M. Tolbert, "Mitigation of current distortion for GaN-based CRM totem-pole PFC rectifier with ZVS control," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 290-303, 2021.

(2) J. Sun, J. Li, D. Costinett, L. M. Tolbert, "A GaN-based CRM totem-pole PFC converter with fast dynamic response and noise immunity for a multi-receiver WPT system," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, 2020, pp. 2555-2562.

(3) J. Sun, N. Strain, D. Costinett, L. M. Tolbert, "Analysis of a GaN-based CRM totem-pole PFC converter considering current sensing delay," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, 2019, pp. 4421-4428.

5.1 Analysis of Current Distortion Issues

The low-frequency line-cycle current distortion is predominantly caused by the ZCD signal time delay, and the ac line zero-crossing current spike typically results from the switching properties of the Si MOSFETs in the line rectifier phase leg.

5.1.1 Line-Cycle Current Distortion

5.1.1.1 ZCD Signal Time Error

The ZCD signal time error is mainly induced by two mechanisms. One is the leading time error arising from the parasitic inductance L_{para} of the sensing resistor R_{shunt}. As shown in Figure 5.1, the series inductance induces offset in the sensed voltage, making the detected zero current point leading to the actual zero current point.

$$V_{sense} = V_R + V_{offset} = i_L R_{shunt} + L_{para}\frac{di_L}{dt} \tag{5.1}$$

where $^{di_L}/_{dt} = {}^{(V_{in} - V_o)}/_{L_b}$ during the positive half-line cycle. The offset voltage varies with the input voltage. Based on the waveform in Figure 5.1, V_{offset} can also be expressed as $V_{offset} = {}^{(di_L R_{shunt} T_{lead})}/_{dt}$. Combined with (5.1), the lead time error is solved as

$$T_{lead} = \frac{L_{para}}{R_{shunt}} \tag{5.2}$$

On the other hand, ZCD signal delay time error is generated along the propagation path. As illustrated in Figure 5.2, the sensed signal is passed through the amplifier, RC filter, comparator, digital isolator to produce the ZCD signal, which is then sent to the DSP for determining the switching signals. In the example implementation, the propagation time delay is around $T_{delay} = 140$ ns. Typically, the lead time error is negligible since L_{para} is very small, and the propagation time delay T_{delay} dominates the ZCD time error.

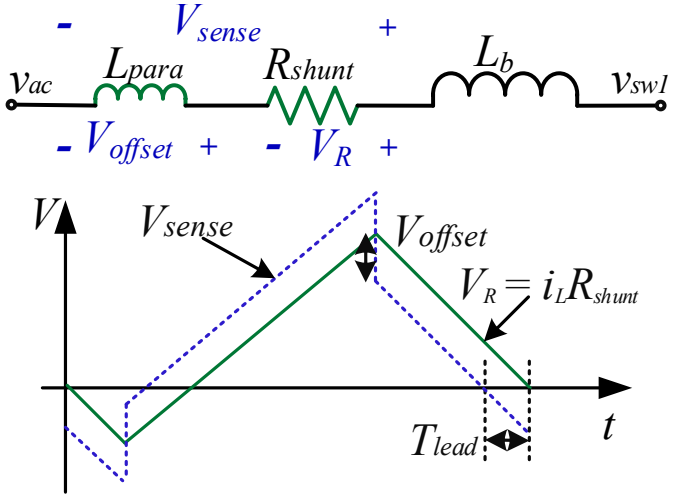


Figure 5.1: Leading time error due to the parasitic inductance of the sensing resistor.

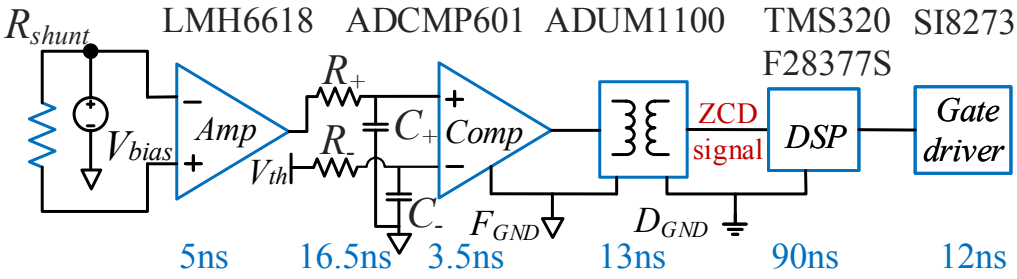


Figure 5.2: Propagation time delay of the ZCD signal.

5.1.1.2 Impact of ZCD Signal Time Delay

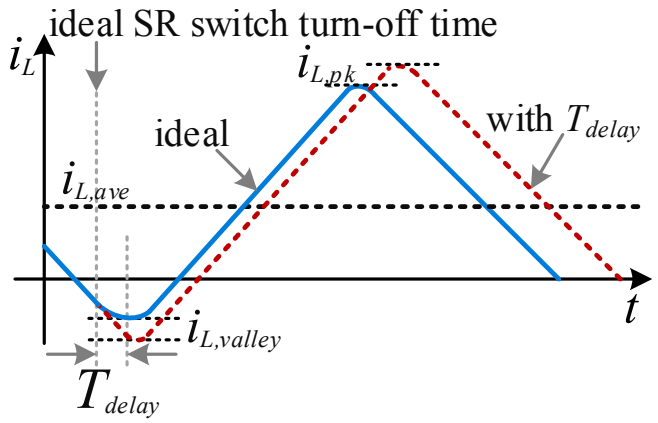
As elaborated in Figure 5.3, the ZCD time delay T_{delay} causes the current to deviate from normal operation. The turn-off moment of the synchronous switch is late by T_{delay}, resulting in a lower inductor valley current $i_{L,valley}$. To maintain the same output power, the PI controller will increase its output T_{on_c} to increase the conduction time of the active switch T_{on_AS} and the inductor peak current $i_{L,pk}$.

According to the variable on-time control, $T_{on\_AS} = T_{on\_c}+T_{on\_v}$, where T_{on_v} is the variable part based on the real-time calculation. When $V_{in} > V_{bound}$ (Figure 5.3(a)), $i_{L,pk}$ is higher with the increased T_{on_c} since $T_{on\_v} = 0$ and $T_{on\_AS} = T_{on\_c}$. However, when $V_{in} \leq V_{bound}$ (Figure 5.3(b)), $T_{on\_v} \neq 0$ and varies instantaneously with the sensed voltages. Although T_{on_c} is increased by the PI controller, T_{on_v} is still calculated based on the ideal model, which is not enough to keep the same peak current. Hence, with ZCD time delay, $i_{L,valley}$ is lower, but $i_{L,pk}$ is higher in the non-natural ZVS region and lower in the natural ZVS region.

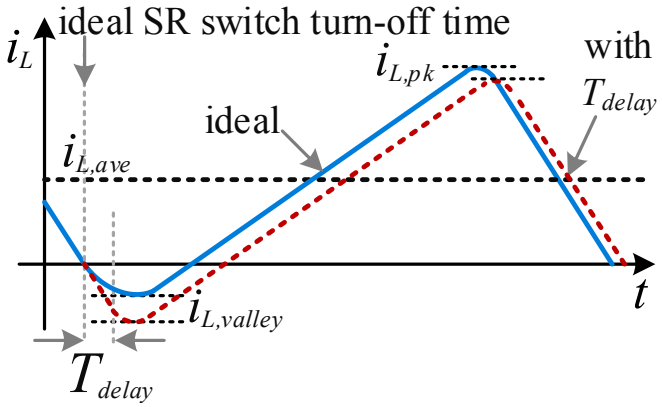
Figure 5.4 illustrates the impacts of the ZCD time delay on the input current of a 1.5 kW CRM PFC rectifier. The average current is severely distorted with the same pattern as the tested result shown in Figure 4.22(a). The inductor current has larger ripple and RMS value (Figure 5.4(a)). The current THD with T_{delay} is two times as high as the normal case at full load, and even worse at light load (Figure 5.4(b)). The ZCD time delay also affects the converter switching frequency and power loss. As shown in Figure 5.4(c), all types of losses are higher compared with the case without T_{delay}, and the total loss is increased from 15.4 W to 18.5 W at full load (Figure 5.4(c)).

5.1.2 Ac Line Zero-Crossing Current Spike

The ac line zero-crossing current spike is a typical issue for the GaN-based totem-pole PFC converter, which is caused by two dominant reasons [217, 216, 162, 163, 161, 140]. One is the asynchronization between the Si device switching and the input voltage zero-crossing due to the Si devices slower commutation, inaccurate zero-crossing detection, or sensing and control time delay. The other one is the high dv/dt noise induced by the drastic voltage change across the Si device.



(a)



(b)

Figure 5.3: Inductor current in one switching cycle with impact of ZCD time delay. (a) i_L when $V_{in} > V_{bound}$; (b) i_L when $V_{in} \leq V_{bound}$

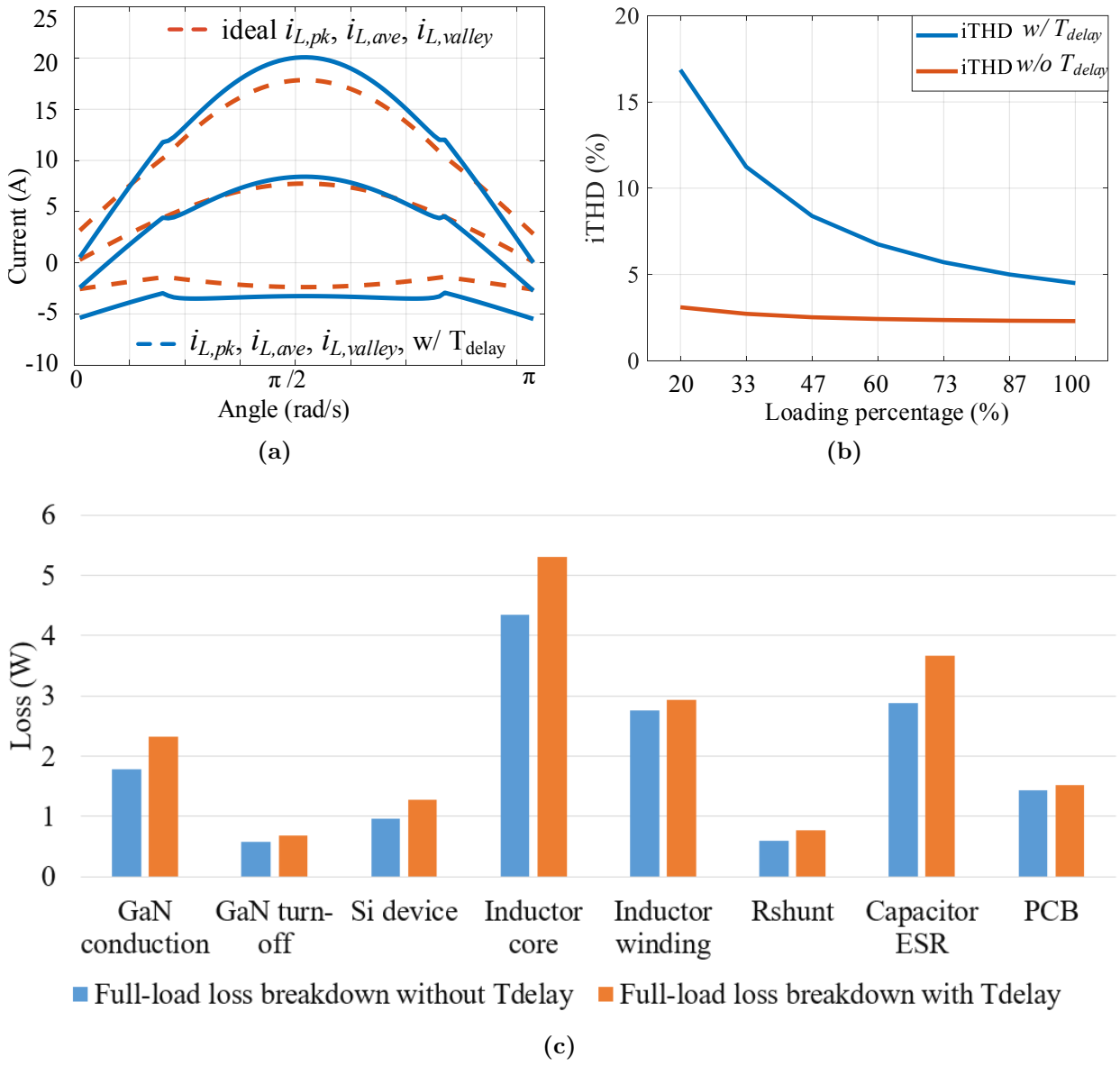


Figure 5.4: Impacts of the ZCD time delay on the PFC with $v_{in} = 277\ \mathrm{V_{ac}}, V_o = 480\ \mathrm{V}, P_o = 1.5\ \mathrm{kW}$. (a) Inductor current; (b) Input current THD.

5.1.2.1 Current Spike due to Slower Transition of Si Devices

Compared to the GaN device with switching speed in excess of 100 V/ns, the commutation speed of the Si MOSFET is much slower [53]. In the practical implementation, small delays, switching noise, limited dv/dt, and input voltage PLL error cause the Si device switching to not be perfectly synchronized to the input voltage zero-crossing, which further results in inductor current spike or instability.

To avoid this, a small blanking time is usually adopted to shut off all switches during the zero-crossing region. As illustrated in Figure 5.5(a), just before the negative-to-positive transition, S_1 and S_3 conduct, and v_{sw1}, v_{sw2} are tied to the high output voltage. During the blanking time, $S_1 - S_4$ are all OFF, and $i_L = 0$ (Figure 5.5(b)). Ideally, after the blanking time, the GaN devices and the Si MOSFETs switch simultaneously with the same speed. S_2 becomes the active switch conducting with large duty cycle, and the inductor current is charged by the small input voltage (Figure 5.5(d)). As shown in Figure 5.6(a), i_L gradually increases with a small slope and no current spike.

However, in practice, Si MOSFETs commutate much slower than the GaN devices. Once the blanking time ends, S_2 turns ON and, due to the smaller C_{oss} and Q_g of the GaN transistors, v_{sw1} drops nearly to zero well before the Si MOSFET commutation completes. During the process (Figure 5.5(c)), the voltage applied on the inductor is $(v_{in} + v_{sw2})$, which gradually decreases from $(v_{in} + V_o)$ to v_{in} as C_{oss} of S_4 discharged. As presented in Figure 5.6(b), the inductor current rises quickly until S_4 is fully ON (Figure 5.5(d)). Consequently, a positive current spike occurs during the negative-to-positive transition. Similarly, a negative current spike occurs during the positive-to-negative transition.

5.1.2.2 Current Spike due to Si Device Switching dv/dt Noise

To avoid the current spike due to slow switching of the Si devices, the Si devices can be purposely turned on earlier during the blanking time. However, current distortion at the voltage zero-crossing cannot be fully eliminated. The second mechanism remains due to the Si device switching dv/dt noise and the parasitic capacitance.

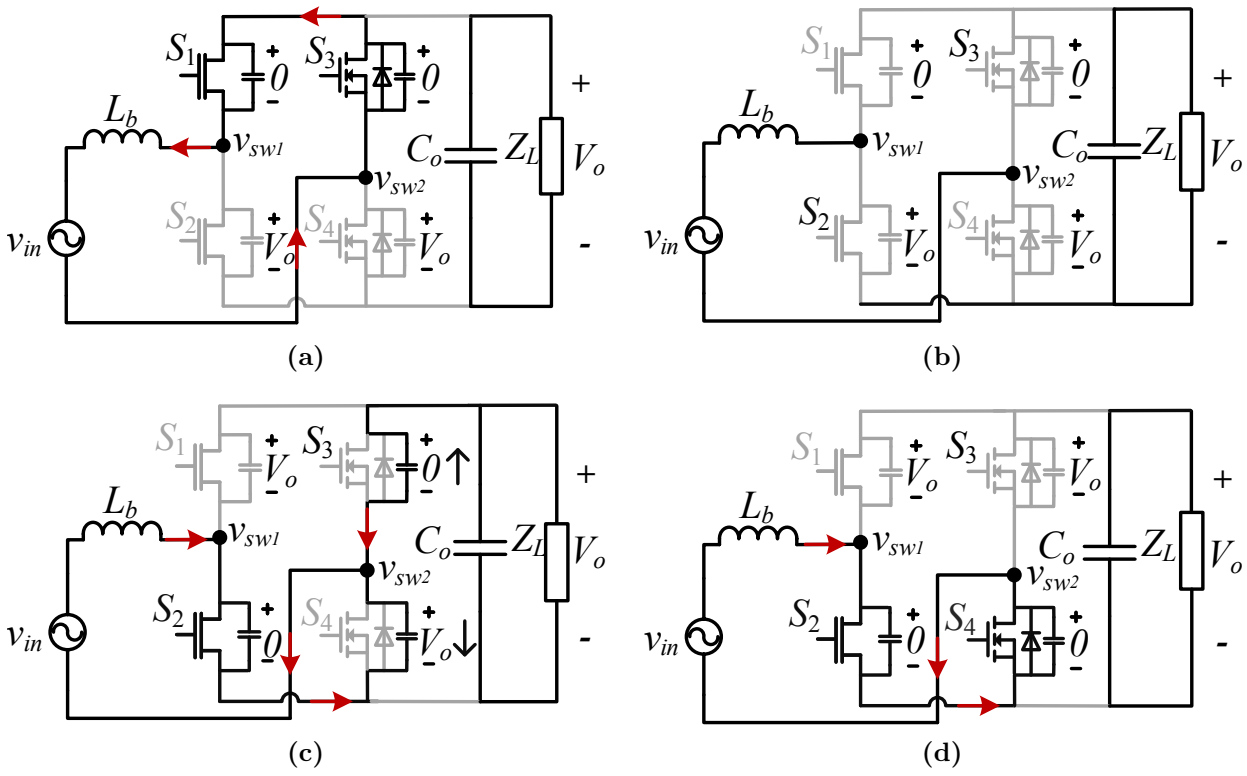


Figure 5.5: Negative-to-positive transition process of the totem-pole PFC.

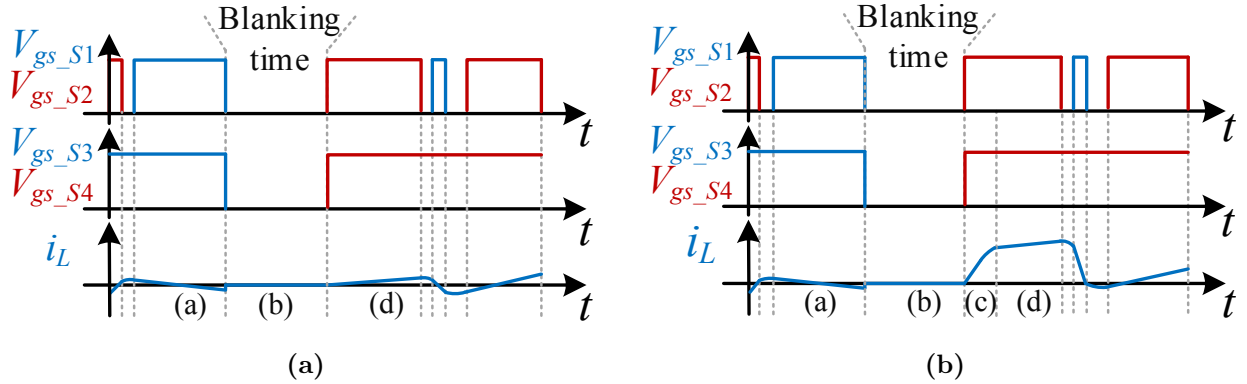


Figure 5.6: Device gate signal and inductor current during the negative-to-positive transition of the GaN-based totem-pole PFC. (a) Ideal case with perfect device synchronization; (b) Practical case with slower Si device commutation.

As illustrated in Figure 5.7. Although Si devices have longer commutation time than GaN devices, the switching speed is still in tens of V/ns [218]. During the negative-to-positive blanking time, $S_1 - S_3$ remain OFF while S_4 turns ON, leading to v_{sw2} decreasing from V_o to 0 with around -10 V/ns slew rate. Since parasitic capacitances C_{p2} and C_{p3} are connected to the common reference ground (E_{GND}), CM noise current is induced and propagates to the input line, resulting in a large current spike in i_{in}.

To analytically understand the CM noise current resulting from v_{sw2} dv/dt noise, an equivalent high-frequency CM noise model is extracted from Figure 5.7, as presented in Figure 5.8(a). During the zero-crossing, the input ac source is approximated as a short circuit, and the input capacitor C_{in} can be ignored. $L_{p,in}$, $R_{p,in}$ are the equivalent inductance and resistance of the input line impedance, $Z_{p,in}$. High-frequency models of C_{p2} and C_{p3} are represented by series RLC circuits. The noise source v_{sw2} is modeled by a line frequency square waveform with 10 V/ns rising and falling slope.

$$v_{sw2}(t) = \big(u(t)-u(t-t_0)\big)\frac{V_o}{t_0}t+V_o\big(u(t-t_0)-u(t-t_1)\big)-\big(u(t-t_1)-u(t-t_0-t_1)\big)\frac{V_o}{t_0}(t-t_0-t_1) \tag{5.3}$$

where t_0 is the voltage rising and falling time, and $t_1 = 1/2f_{line}$ with $f_{line} = 60$ Hz. In the s-domain, the circuit equations based on KVL and KCL laws are

$$\begin{cases} 0 = V_{sw2}(s) + I_{p3}(s)\big(Z_{p3}(s) + \frac{Z_{p2}(s)Z_{p,in}(s)}{Z_{p2}(s)+Z_{in}(s)}\big) \\ I_{CM}(s) = I_{p3}(s)\big(\frac{Z_{p2}(s)}{Z_{p2}(s)+Z_{p,in}(s)}\big) \end{cases} \tag{5.4}$$

where $V_{sw2}(s) = \mathscr{L}(v_{sw2}(t))$, $Z_{p,in}(s) = 2(sL_{p,in} + R_{p,in})$, $Z_{p2}(s) = sL_{p2} + R_{p2} + 1/sC_{p2}$, and $Z_{p3}(s) = sL_{p3} + R_{p3} + 1/sC_{p3}$. Then, the CM noise current is solved by the inverse Laplace transform of $I_{CM}(s)$

$$i_{CM}(t) = \mathscr{L}^{-1}(I_{CM}(s)) = \mathscr{L}^{-1}\left(\frac{-V_{sw2}(s)}{Z_{p3}(s)(1+\frac{Z_{p,in}(s)}{Z_{p2}(s)}) + Z_{p,in}(s)}\right) \tag{5.5}$$

Figure 5.8(b) shows the predicted i_{CM}, which has a significant spike when v_{sw2} changes during the ac line zero-crossing.

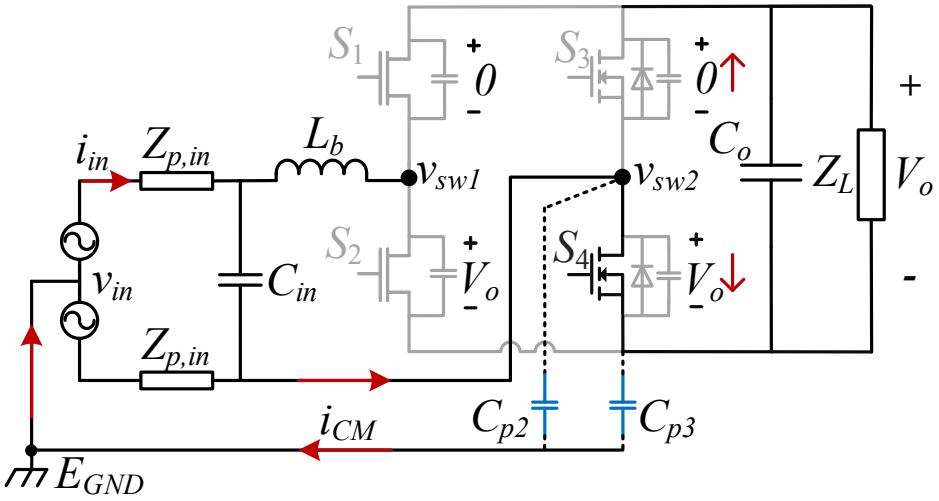
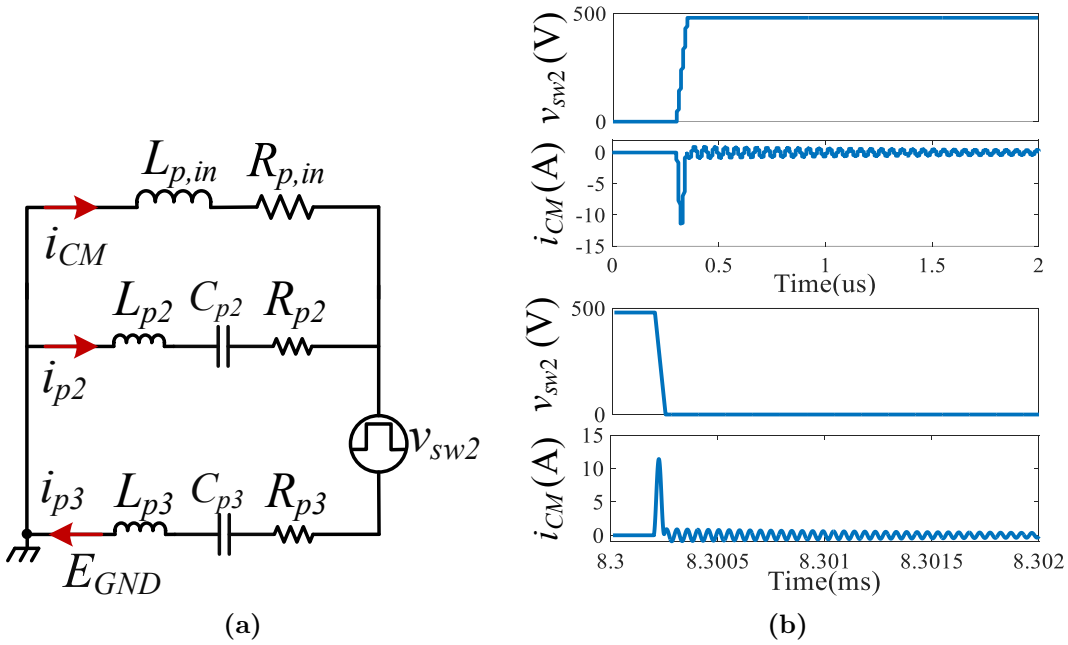


Figure 5.7: Illustration of the current spike due to Si device dv/dt noise during the negative-to-positive transition.



(a) **(b)**

Figure 5.8: Modeling of the current spike due to Si device switching. (a) High-frequency noise model; (b) Predicted i_{CM} when v_{sw2} changes.

5.2 Mitigation Methods for Current Distortion

5.2.1 Delay Compensation for Line-Cycle Current Distortion

To reduce the impact of the current sensing delay, two methods are adopted in the control implementation. On the hardware level, noticing that L_{para} results in ZCD signal leading time error, which is contradictory to the propagation time delay, it can be purposely enlarged to cancel out partial delay time [156]. So instead of using one 10 mΩ sensing resistor, two 5 mΩ sensing resistors are connected in series to enlarge the parasitic inductance.

On the digital programming level, the analytical converter model embedded in the real-time calculation is modified considering the delay time. Because of the ZCD time delay, the actual extended conduction time of the synchronous switch T_{ex_SS} is increased as the sum of T_{delay} and the ideal extension time $T_{ex\_SS,ideal}$, leading to a lower $|i_{L,valley}|$ and distorted input current. In order to maintain the ideal input current, the converter model should be modified considering T_{delay}, and $i_{L,valley}$ should be kept close to the ideal value to limit distortion and/or additional conduction loss.

First, T_{ex_SS} is adjusted close to $T_{ex\_SS,ideal}$. As presented in Figure 5.9(a), when $T_{ex\_SS,ideal} \geq T_{delay}$, compensation can be easily achieved by subtracting T_{delay} from $T_{ex\_SS,ideal}$; when $T_{ex\_SS,ideal} < T_{delay}$, T_{ex_SS} is minimized at T_{delay}, as the switching instant cannot occur before the sensed ZCD signal without significant changes to the control architecture. Thus, the actual extended conduction time is

$$T_{ex\_SS} = \begin{cases} T_{ex\_SS,ideal}, & T_{ex\_SS} \geq T_{delay} \\ T_{delay}, & T_{ex\_SS} < T_{delay} \end{cases} \tag{5.6}$$

Second, the converter model should be modified based on T_{ex_SS} to ensure minimal distortion of i_{in}. Comparing T_{ex_SS} with $T_{ex\_SS,ideal}$, the only difference is the minimum extended conduction time, which is increased from zero to T_{delay} during the natural ZVS region. Hence, letting T_{ex_SS} in (4.6) equal to T_{delay}, we get $k^2 = {}^{(1+(\omega_n)^2(T_{delay})^2)(V_o - V_{in})^2}/_{V_{in}^2}$, and the ZVS

margin k shown in (4.5) is updated as

$$k = \begin{cases} \frac{V_o - V_{in}}{V_{in}} \sqrt{1 + (\omega_n)^2 (T_{delay})^2}, & V_{in} \leq V_{bound} \\ k_0, & V_{in} > V_{bound} \end{cases} \tag{5.7}$$

V_{bound} should also be altered to maintain a smooth transition between the natural ZVS region and non-natural ZVS region.

$$V_{bound} = V_{in}\Big|_{k(V_{in} \leq V_{bound}) = k(V_{in} > V_{bound})} \tag{5.8}$$

$$V_{bound} = \frac{\sqrt{1 + (\omega_n)^2 (T_{delay})^2}}{k_0 + \sqrt{1 + (\omega_n)^2 (T_{delay})^2}} V_o \tag{5.9}$$

Expressions for $i_{L,pk}$, $i_{L,valley}$, T_{on_AS}, T_{r1}, T_{on_SS}, T_{r2}, and T_{ZVS} do not change.

Figure 5.9(b) shows the inductor currents of a 1.5 kW PFC rectifier. With the modified converter model, the average inductor current $i_{L,ave}$ is the same as the ideal case, and inductor current ripple is not enlarged over the majority of the line cycle. The only discrepancy is the slightly increased current ripple during the natural ZVS region, where T_{delay} cannot be fully compensated. However, the impact of such discrepancy is not severe since both the voltage and current are low at this region, and $i_{L,ave}$ is not distorted.

Based on the loss model, the loss breakdown of a 1.5 kW CRM PFC at full load is estimated considering different cases, as shown in Figure 5.10. In the ideal case without ZCD time delay, the PFC power loss at full load is 15.4 W. With the impact of T_{delay}, all types of losses increase, and the full-load power loss is 18.5 W. By adopting the proposed compensation approach, the full-load power loss is reduced to 16.2 W, which is only 0.8 W higher than the ideal case. Therefore, the proposed compensation method can effectively reduce the extra converter loss induced by the current sensing delay.

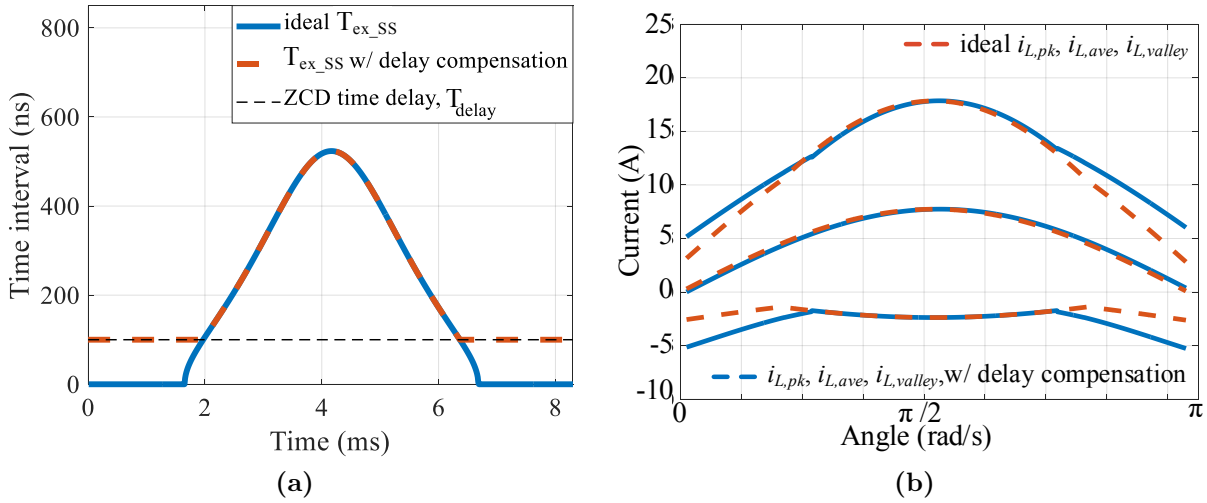


Figure 5.9: (a) Modified extended conduction time of the synchronous switch in the half line cycle for delay compensation; (b) Inductor current in the positive half line cycle of a 1.5 kW PFC rectifier with the modified converter model.

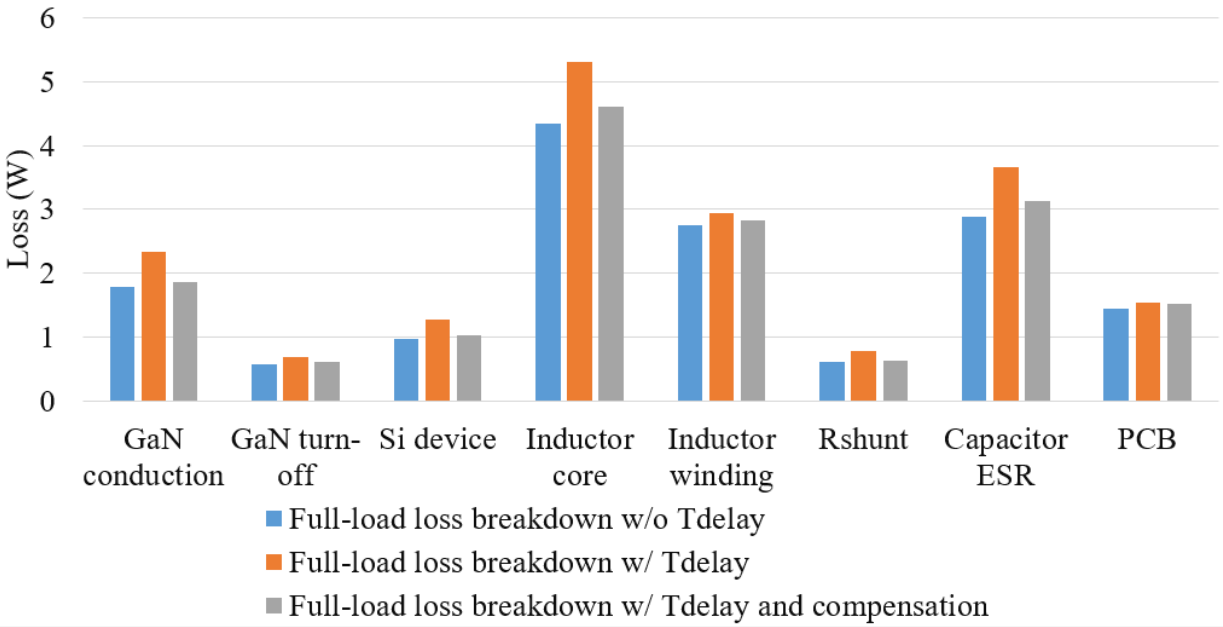


Figure 5.10: Estimated full-load power breakdown of a totem-pole PFC rectifier with $v_{ac} = 277$ V_{ac}, $V_o = 480$ V, $P_o = 1.5$ kW.

5.2.2 Methods for Zero-Crossing Current Spike Elimination

5.2.2.1 Device Switching Sequence

To reduce the current spike after blanking time, a fixed device switching sequence is assigned, as illustrated in Figure 5.11. During the blanking time, the Si MOSFETs are turned off later and turned on earlier than the GaN devices. A sufficient delay time of a few µs is inserted between GaN switching and Si switching to ensure that the Si device is fully turned on when the GaN device turns on after the blanking time. To maintain ZVS in the first switching cycle, the GaN devices are turned on at the beginning of a new period.

5.2.2.2 Auxiliary Circuit for dv/dt Noise Elimination

In order to eliminate the current spike induced by the dv/dt noise of Si device switching, a simple auxiliary circuit consisting of one damping resistor R_{damp} and two Si MOSFETs Q_1, Q_2 is proposed, as shown in Figure 5.12. Q_1 and Q_2 only conduct for a fixed short period during the blanking time (Figure 5.11). In the process of the negative-to-positive transition, Q_2 is turned ON when $S_1 - S_4$ are shut OFF, which provides a current flow path for voltage damping. Then the output capacitance of S_4 and R_{damp} form a R-C circuit, and v_{ds_S4} is smoothly damped to zero. Similarly, during the positive-to-negative transition, Q_1 is turned on within the blanking time to help damp v_{ds_S3}.

To ensure the voltage is completely damped, R_{damp} and the conduction time of Q_1, Q_2 should be selected properly. Small R_{damp} cannot sufficiently slow down the dv/dt, but high R_{damp} requires longer conduction time. During the damping process, the drain-to-source voltage of S_3 or S_4 is

$$v_{ds\_Si} = V_o e^{-\frac{t}{\tau}} \tag{5.10}$$

where time constant $\tau = R_{damp}C_{eq}$, and C_{eq} is the equivalent output capacitance of S_3 and S_4. Typically, the conduction time of Q_1,Q_2 is selected as 3τ to 5τ. Given the Si MOSFET usually has C_{oss} in nF level, R_{damp} of a few kΩ can be used, resulting in a conduction time in tens of µs.

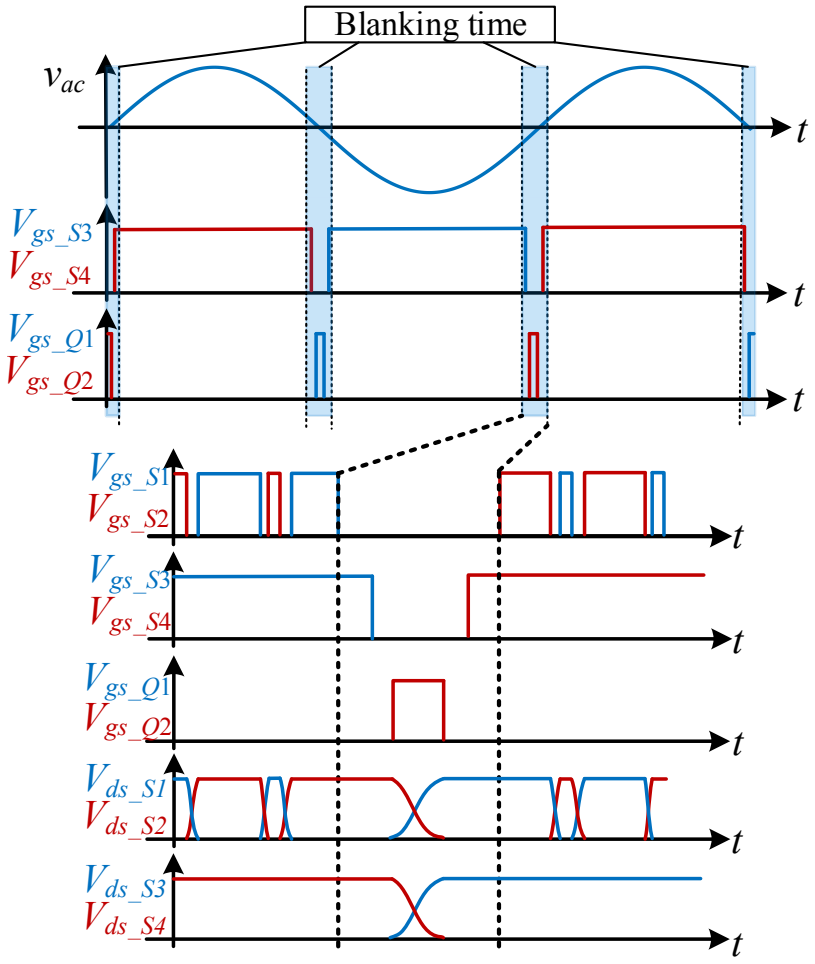


Figure 5.11: Device switching sequence during the ac line zero-crossing.

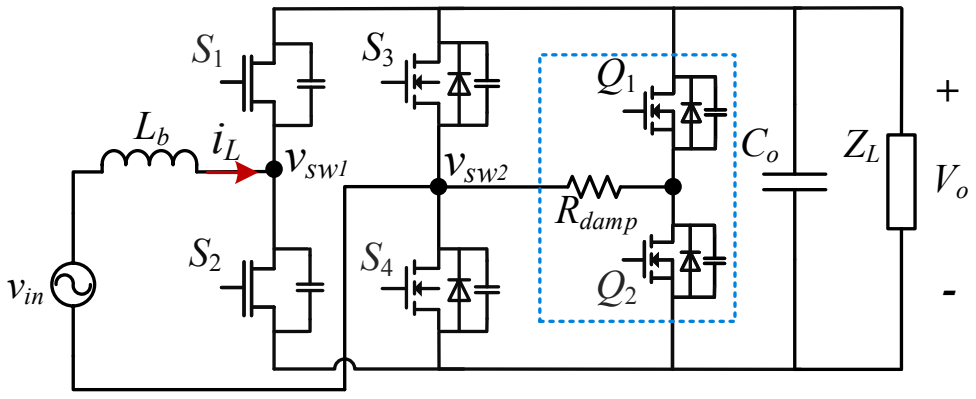


Figure 5.12: Auxiliary circuit for eliminating the dv/dt noise of Si device.

The auxiliary circuit has the benefits of simple topology, low cost, and almost no extra power loss. Since Q_1 and Q_2 switch at the line frequency and their conduction time is short, Si MOSFETs with very low current rating ($< 1A$) are adequate, and the device power consumption is negligible. The only power dissipation comes from the energy stored in the C_{oss} of S_3 and S_4, which is quite small, *e.g.*, $P_{damp} = 0.03$ mW with $f_{line} = 60$ Hz, $C_{eq} = 2.2$ ns, and $V_o = 480$ V.

$$P_{damp} \approx C_{eq} V_o^2 f_{line} \tag{5.11}$$

Implementation of the blanking time and the device switching sequence can be easily achieved through the digital phase-locked loop (PLL) and PWM module within the controller. No extra control resources are required.

5.3 Experimental Verification

The 1.5 kW PFC prototype developed in Chapter 4 is tested again to verify the proposed approaches for mitigating the current distortion. In order to validate the effectiveness of the proposed auxiliary circuit for eliminating the ac zero-crossing current spike due to the voltage change of the Si device, a small board with a damping resistor and two extra Si MOSFETs are designed and fabricated, as shown in Figure 5.13. A 10 kΩ surface-mount resistor is selected as the damping resistor, and 600 V, 1 A STD1NK60T4 Si MOSFET is used as the assisting switch. The auxiliary board can be easily connected to the main power stage through terminal V_{bus}, P_{GND}, and v_{sw2}.

5.3.1 Verification of the Line-Cycle Current Distortion Mitigation

To mitigate the line-cycle current distortion, the 10 mΩ current sensing resistor is formed by two series-connected 5 mΩ resistors for the purpose of increasing the parasitic inductance to cancel out partial T_{delay}. Also, the ZCD signal propagation time delay is compensated by embedding the modified converter model in the real-time calculation. Figure 5.14 shows the testing full-load waveform of the PFC prototype. With the proposed compensation methods, the line-cycle current distortion is almost remedied.

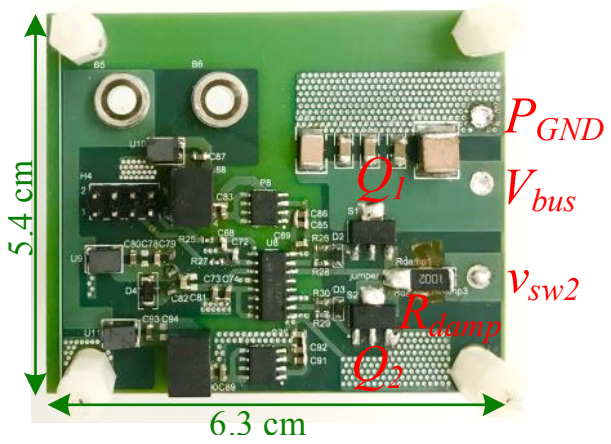


Figure 5.13: Prototype of the auxiliary board for eliminating the ac zero-crossing current spike due to CM noise.

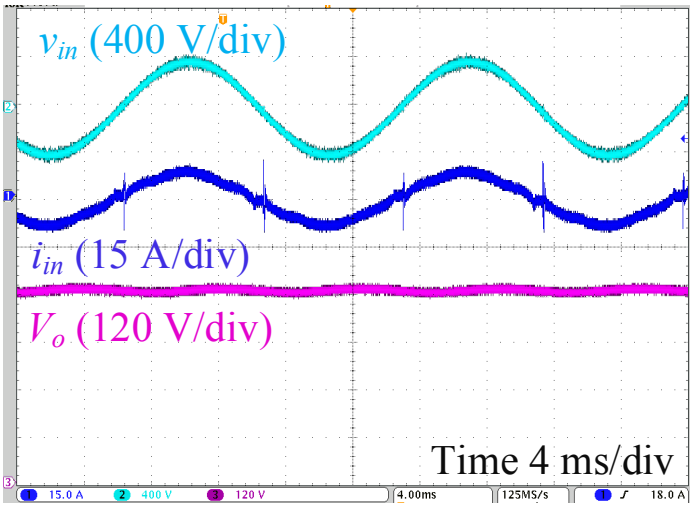


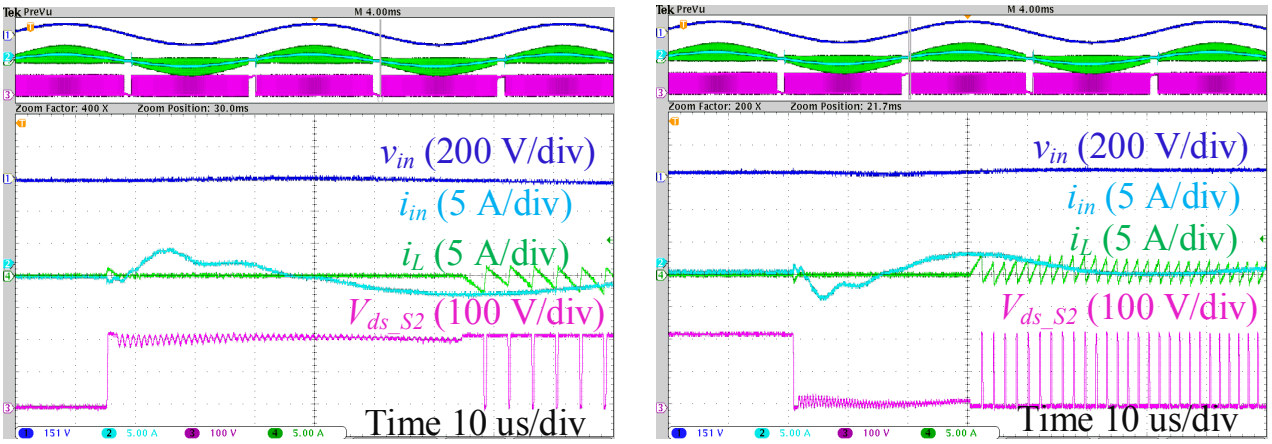
Figure 5.14: Experimental waveforms in line cycle of the 1.5 kW PFC prototype with mitigated line-cycle current distortion at full load.

However, the ac line zero-crossing current spike still exists. Figure 5.15 shows the zoomed-in waveforms during the ac line zero-crossing period. A large current spike is generated on the input current at the high dv/dt point of the drain-to-source voltage. When turning on GaN devices again after the blanking time, large peak inductor current happens in the first switching cycle, as shown in Figure 5.16(a). Also, since the PWM time-based counter still runs during the blanking time, when turning on the GaN device after the blanking time, hard switching happens if the counter is close to the end of the PWM period, as presented in Figure 5.16(b).

5.3.2 Verification of the Ac Line Zero-Crossing Current Spike and Mitigation

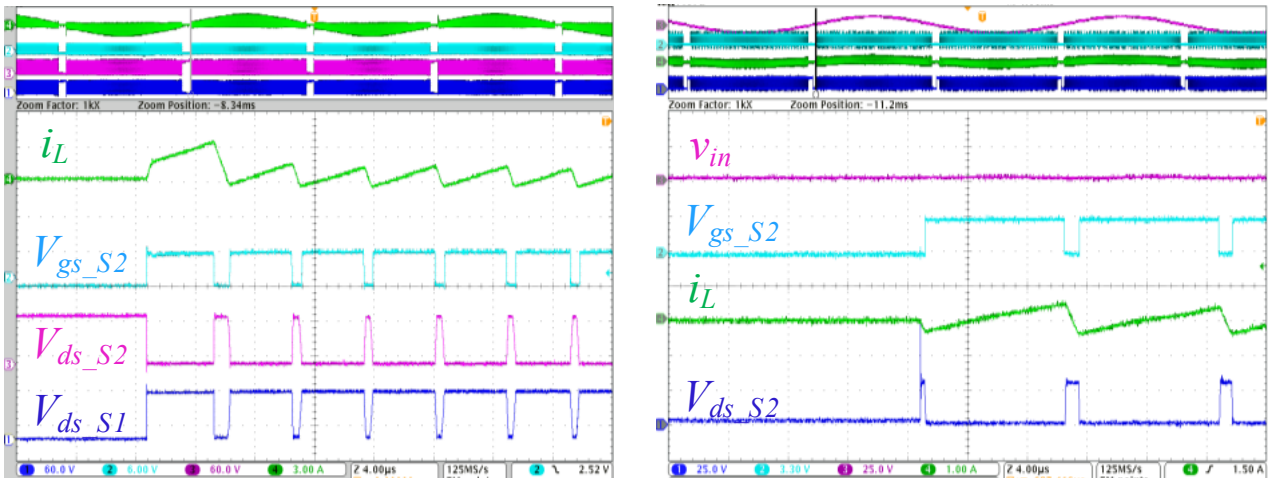
To avoid the inductor current spike and ensure soft switching in each switching cycle, the proposed device switching sequence during the blanking time is implemented. In addition, the proposed auxiliary circuit is adopted to eliminate the current spike induced by the dv/dt noise of Si devices, where Q_1 and Q_2 conduct for 100 µs during the blanking time. Figure 5.17 and Figure 5.18 present the final experimental results of the PFC rectifier at full load. With 277 V_{ac} input, the output voltage is regulated at 480 V_{dc}, and full-line-cycle ZVS is achieved. Thanks to the damping circuit, the drain-to-source voltage gradually changes with low dv/dt, and the input current spike is removed. Meanwhile, the GaN device is turned on with soft switching, and no current spike occurs in the first switching cycle.

The PFC power efficiency, power factor, and the input current THD are measured again by the Yokogawa WT3000E power analyzer. At full-load, the PFC efficiency reaches 98.9% efficiency with current THD $< 5\%$ and PF > 0.99. Figure 5.19 presents the tested efficiency and current THD at different loadings of the PFC prototype. It is clear that, with the proposed mitigation methods, the current THD and the converter efficiency are both improved. The peak efficiency increases to 99%, and the current THD is below 5% in all testing loadings.



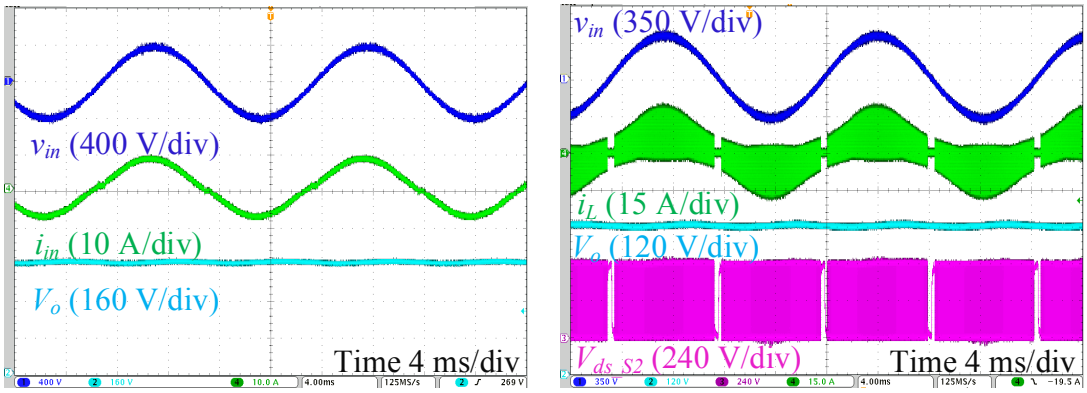
(a) **(b)**

Figure 5.15: Experimental results during the ac line zero-crossing. (a) Positive to negative transition; (b) Negative to positive transition.



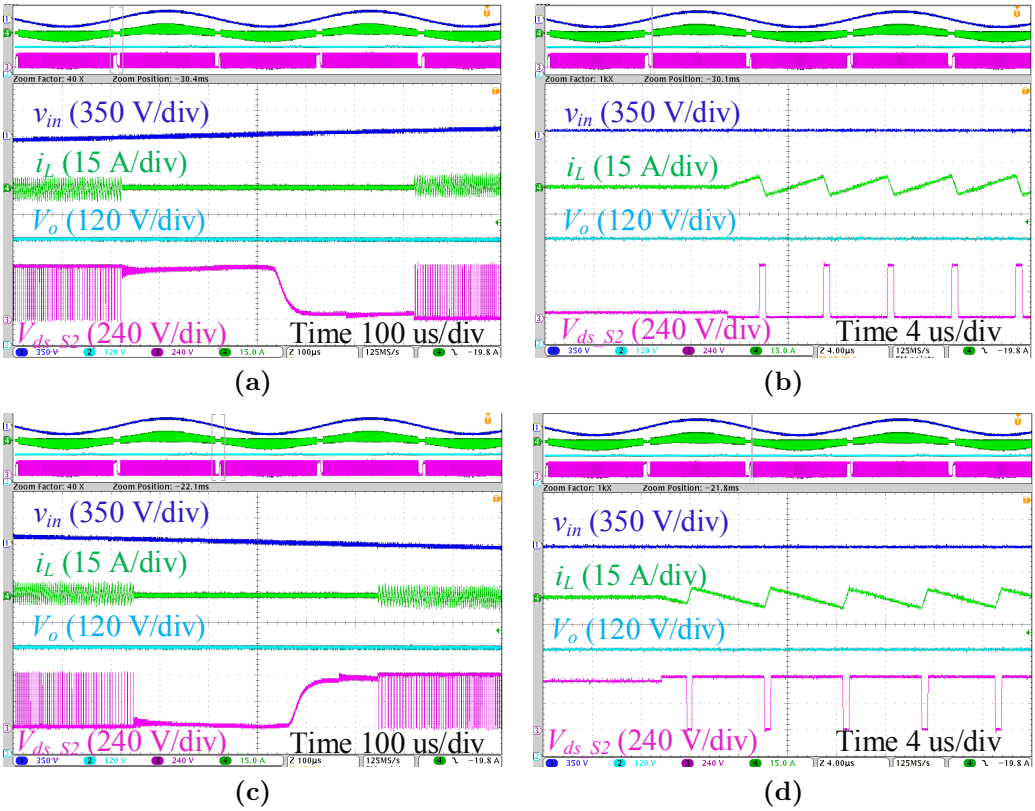
(a) **(b)**

Figure 5.16: Ac line zero-crossing transition with blanking time. (a) Positive current spike during the negative-to-positive transition; (b) Hard switching when turning on devices after the blanking time.



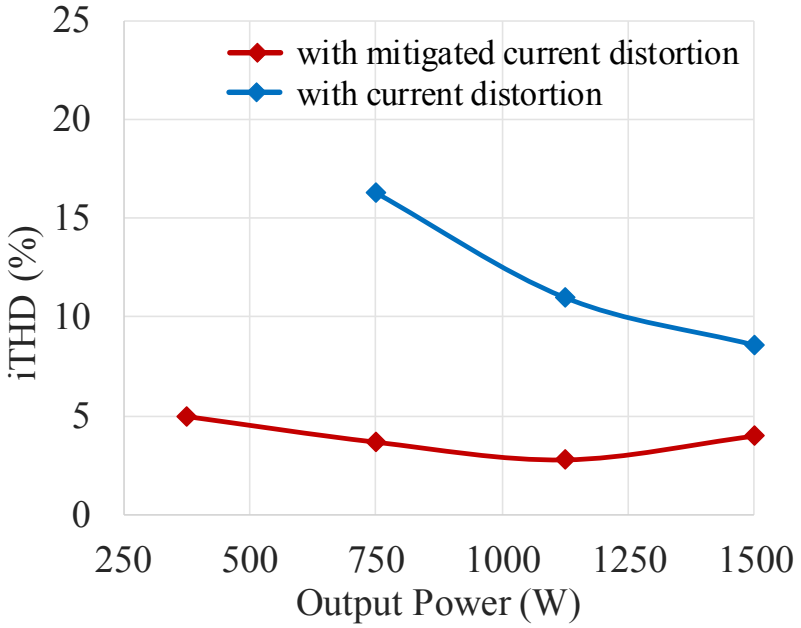
(a) Waveforms of v_{in}, i_{in}, V_o. **(b)** Waveforms of v_{in}, i_L, V_o.

Figure 5.17: Experimental waveforms in line cycle of the PFC prototype at full load with the proposed mitigation methods for current distortion.

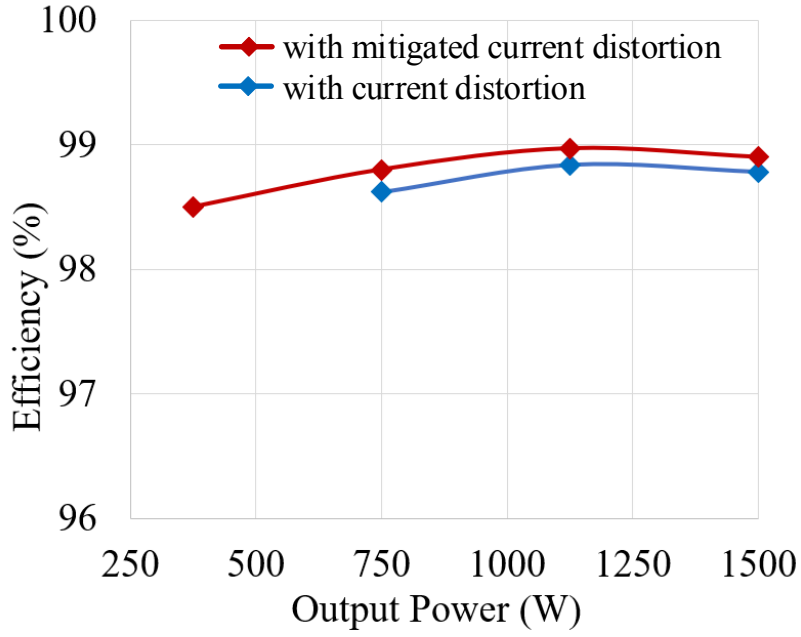


(a) **(b)** **(c)** **(d)**

Figure 5.18: Ac line zero-crossing transition waveforms of the 1.5 kW CRM PFC prototype with the proposed mitigation methods for current distortion. (a) Negative-to-positive transition; (b) Device turn-on waveforms in the positive half line cycle; (c) Positive-to-negative transition; (d) Device turn-on waveforms in the negative half line cycle.



(a)



(b)

Figure 5.19: Measured iTHD and efficiency of PFC prototype at different loads with and without the proposed mitigation methods for current distortion.

5.4 CRM Totem-Pole PFC in MHz WPT System

Wireless power transfer (WPT) based on MHz magnetic resonant coupling has gained increasing attention in applications like consumer electronics and electric vehicles, due to the advantages of spatial freedom, long transfer distance, and high efficiency [219]. In order to maximize the end-to-end efficiency, and also satisfy the power factor and harmonic requirements, a high-efficiency PFC rectifier is required. In this section, a GaN-based CRM totem-pole PFC rectifier is designed for a 100 W 6.78 MHz wireless power supply in consumer electronics. Operation performance of the PFC in the WPT system is evaluated, and the generality of the current distortion issues are investigated.

5.4.1 CRM Totem-Pole PFC for aN All-GaN 6.78 MHz WPT System

Figure 5.20 shows the prototype of a GaN-based 100 W muiti-receiver wireless charging power supply system. The WPT system contains a two-stage transmitter, a 0.5×0.5 m^2 transmitter desk, receiver coils, and two diode receivers. The two-stage transmitter is composed of a front-end CRM totem-pole PFC converter and a 6.78 MHz dc-ac inverter with total volume at $7.4 \times 5.3 \times 1.7$ cm^3. A 100 W CRM totem-pole PFC rectifier is designed as the first stage of the transmitter, which adopts the same ZVS control strategy introduced in Chapter 4. Detailed design specifications of the PFC rectifier are displayed in Table 5.1.

The CRM PFC converts 120 V_{ac} input voltage to a 200 V dc voltage, which is further inverted to a 6.78 MHz ac voltage by the inverter. Figure 5.21 presents the topology of the transmitter second stage, which is a half-bridge inverter with ZVS operation. An impedance matching network (IMN) consisting of L_{IMN} and C_{IMN} is used to allow the coil current fundamental magnitude to be independent of the loading impedance. Detailed coil design is provided in [24].

Table 5.1: Specifications of the CRM PFC for the 100 W WPT system.

Parameter	Value
Input voltage v_{in}	120 V_{ac}, 60 Hz
Output voltage V_o	200 V_{dc}
Output power P_o	100 W
Switching frequency f_{sw}	$187 - 725$ kHz
GaN devices $S_1 - S_4$	GS66508B, 650 V
Boost inductor	28 µH with core Mix-2 T94 and AWG 20 wire
Dc capacitor	UCY2E121MHD9, 120 µF, 250 V_{dc}
ZVS margin	$k_0 = 1.1$, $T_{ZVS,min} = 50$ ns

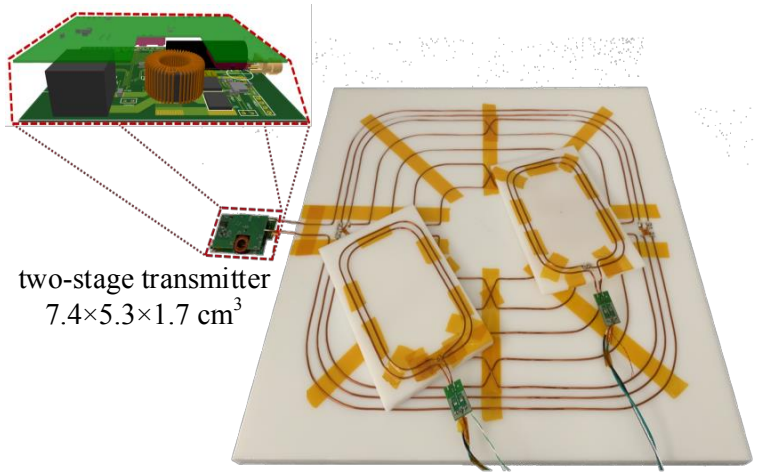


Figure 5.20: Prototype of the 100 W GaN-based WPT system [23, 24].

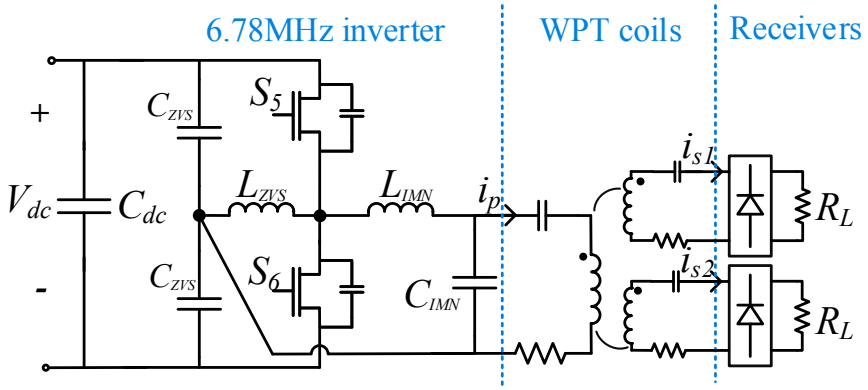


Figure 5.21: Topology of the 6.78 MHz dc-dc stage in the WPT system.

For the WPT system allowing multiple devices to charge simultaneously, fast dynamic response is indispensable. In order to improve the transient response, higher bandwidth of the voltage control is desired. To avoid the impact of the double-line frequency ripple, digital notch filters are applied on the output voltage feedback loop. Because the whole circuit operates with 60 Hz ac line input, notch filters with stop bands at 60 Hz and 120 Hz are implemented. As depicted in Figure 5.22(a), assuming the analog-to-digital (A/D) conversion gain and the PWM modulation gain are cancelled out, the final loop gain of the voltage control loop is

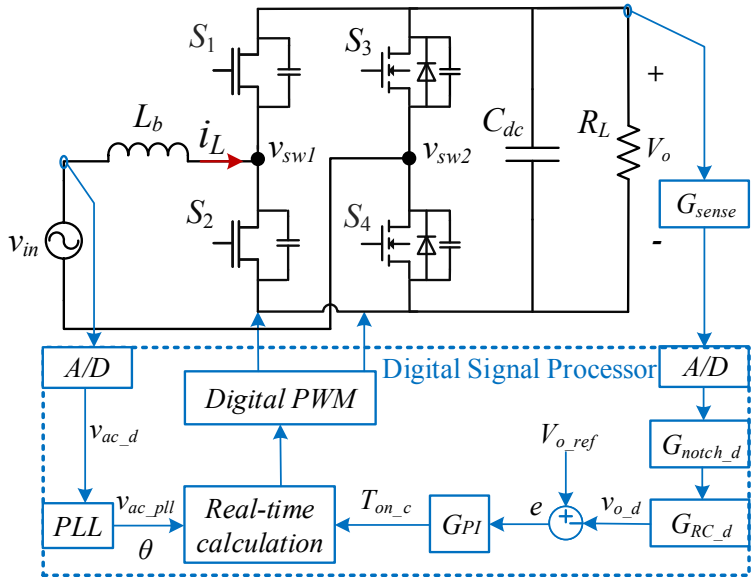
$$T_v = G_{sense} G_{notch\_d} G_{RC\_d} G_{PI} G_{vt} \tag{5.12}$$

where G_{RC_d} is the digital low-pass filter for noise suppression, G_{vt} is the on-time-to-control transfer function derived in (4.25). Figure 5.22(b) shows the bode plot of the PFC loop gain at the peak input voltage. The PI compensator is designed to have 160 Hz control bandwidth with a phase margin of 65°.

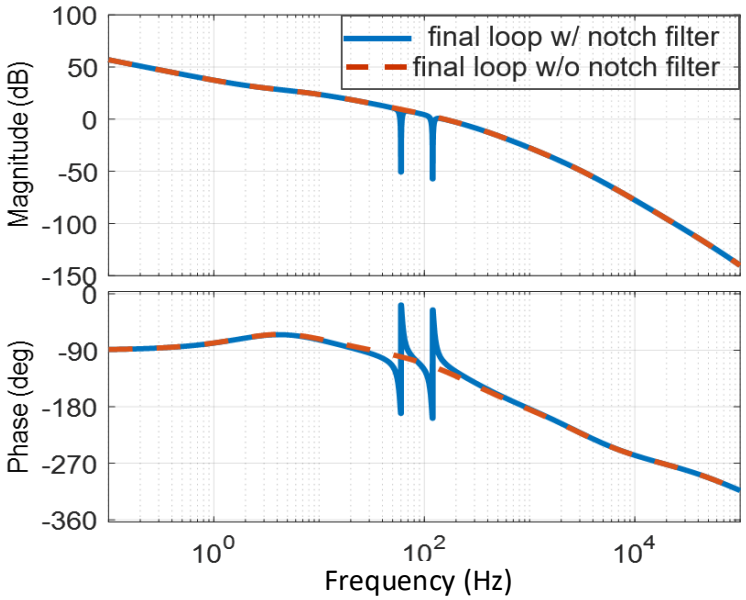
However, when operating in the 6.78 MHz WPT system, the PFC stage operates unstably with severe current distortion, as shown in Figure 5.23. Apart from the previously discussed line-cycle current distortion and ac line zero-crossing current spike, ZVS control becomes unstable with current runaway, and the PFC cannot operate at the target voltage and power.

5.4.2 Noise Impact on Current Distortion

For wireless charging power supplies, the transmitter and receiver coils are loosely-coupled with magnetic resonance [24]. In GaN-based high-frequency power supply systems, CM noise, especially the high dv/dt noise from the 6.78 MHz WPT stage is significant, which impacts the operation of the front-end PFC stage. Figure 5.24 shows the CM noise sources and propagation paths of the WPT power supply system. High dv/dt noise is generated by the switching nodes v_{sw1}, v_{sw2}, and v_{sw3}, and the resulting noise currents flow to E_{GND} through parasitic capacitance C_{p1}-C_{p4}. C_{p5} and C_{p6} are the parasitic capacitance between the WPT coils and E_{GND}, which cannot be neglected since WPT coils have large area.



(a)



(b)

Figure 5.22: (a) Control loop with notch filters of the CRM totem-pole PFC; (b) Bode diagram of the CRM PFC voltage loop gain with and without notch filters.

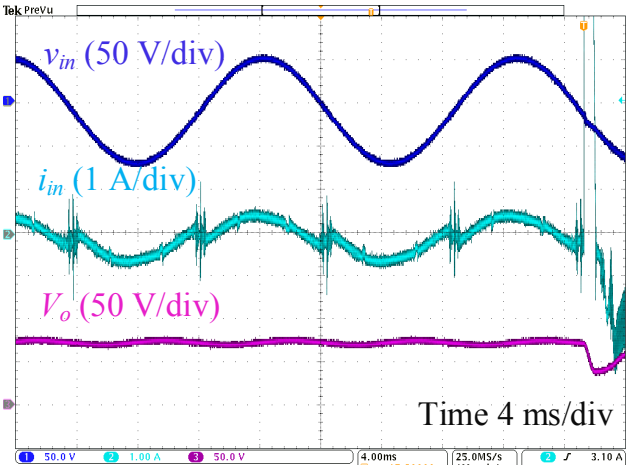


Figure 5.23: Experimental waveforms in line cycle of the 100 W GaN-based CRM PFC in the 6.78 MHz WPT system.

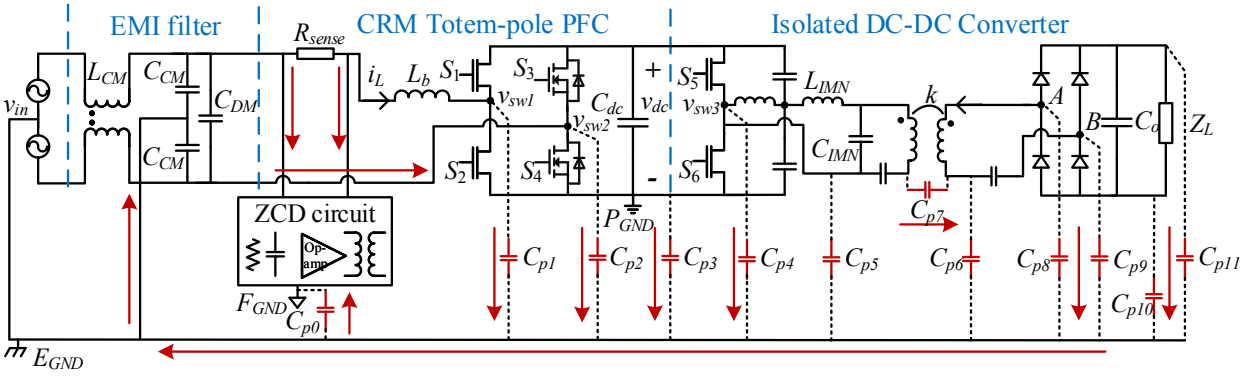


Figure 5.24: CM Noise propagation path within a GaN-based ac-dc power supply system.

Bridging parasitic capacitance C_{p7} between the transmitter coil and receiver coils transfers the noise current from the primary side to the secondary side. Parasitic capacitances C_{p8} and C_{p9} exist between the diode switching nodes A, B and E_{GND}. Given the distances between A, B and E_{GND} are the same, and the dv/dt waveforms generated at A, B have 180° phase shift, noise currents flowing through C_{p8} and C_{p9} are canceled out. The noise current is finally injected into the ground via load parasitic capacitance C_{p10} and C_{p11}.

The noise currents propagate to the input side and flow back forming a conduction loop. Even with the input EMI filter, CM noise current still flows into the ZCD circuit through the current sensing terminals or parasitic capacitance C_{p0}, which can impact the ZCD signal. Figure 5.25 presents the simulation of the WPT power supply system (Figure 5.24), including the low-side drain-to-source voltages $v_{ds,S2}, v_{ds,S6}$, the inductor current i_L, the differential input signal v_d of the amplifier, the amplifier output signal v_{amp}, and the ZCD signal v_{ZCD}. ZVS turn-on is achieved in all GaN-based active switches.

Figure 5.25(a) shows the ideal case without the parasitic capacitance and noise propagation path. v_{amp} is a clean waveform following the inductor current, and the comparator generates the clean ZCD signal with small delay time at 35 ns. Figure 5.25(b) presents the case with the parasitic capacitance and noise propagation. The amplifier differential input v_d is coupled with large amount of switching noise, and v_{amp} has resonant ripples at 6.78 MHz. The ZCD signal is hence noisy and has much longer time delay, at 279 ns. The increased ZCD time delay leads to line-cycle current distortion. The erroneous ZCD signal results in false switching demands and control instability as displayed in Figure 5.23.

5.4.3 Noise Immunity Approaches

To prevent CM noise from distorting the sensed ZCD signal, the noise should be attenuated in the path of the ZCD circuit. In general, efforts can be made in two aspects. First, the CM impedance within the power stage can be increased. In the WPT power supply system (Figure 5.25), a CM filter can be placed on the dc bus so that the high-frequency noise from the WPT stage will not propagate to the PFC stage. Also, increasing the CM impedance of the WPT inverter LC network helps suppress the CM noise.

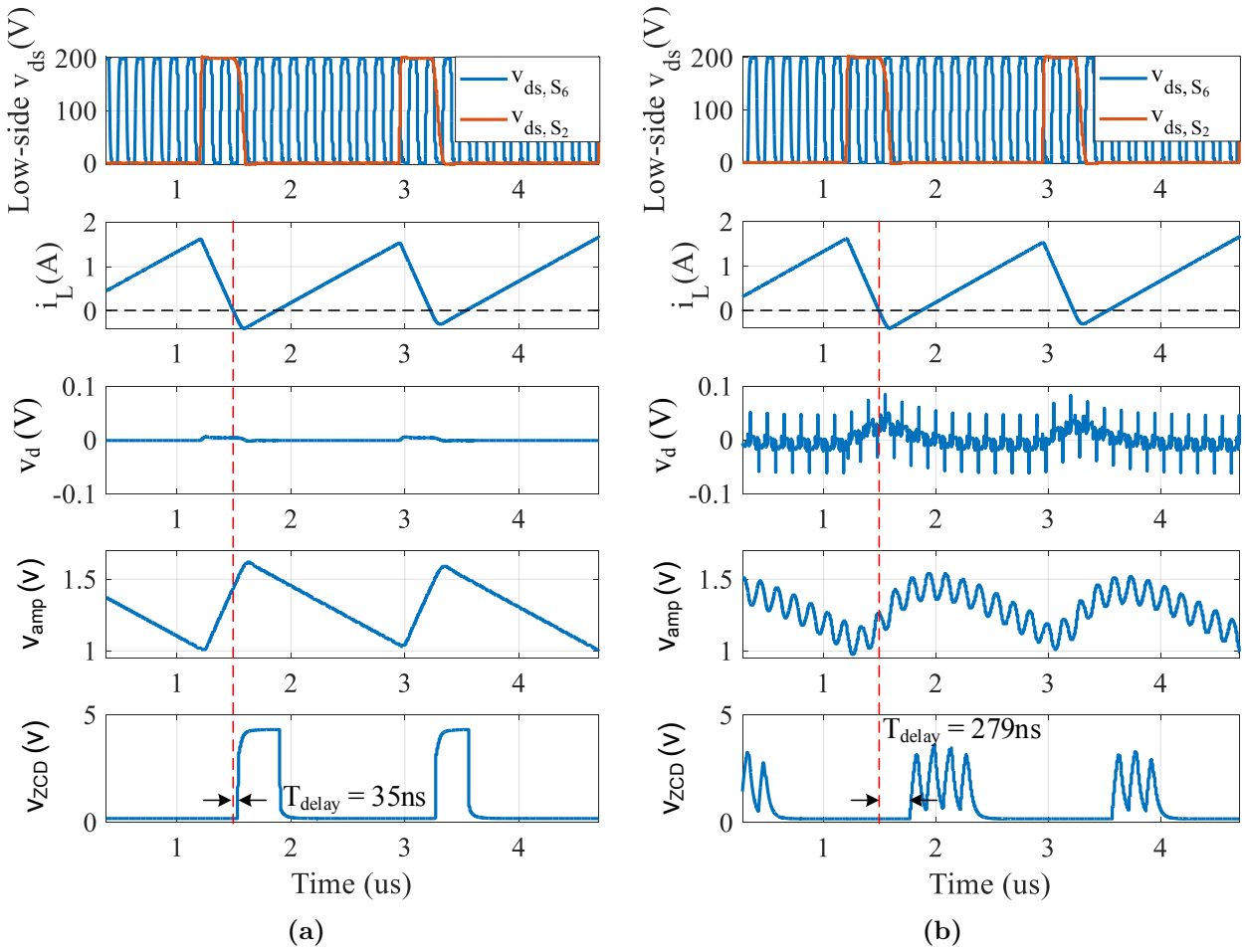


Figure 5.25: Simulated waveforms of the ZCD circuit at V_{in} = 70 V in the WPT power supply systems. (a) Normal case with no parasitic capacitance and noise propagation; (b) Noise case with parasitic capacitance and noise propagation.

Figure 5.26 shows the simulation waveforms of the ZCD circuit with attenuated noise based on the same 6.78 MHz WPT system. In Figure 5.26(a), a CM choke is added in the inverter LC network. As a result, the ZCD amplifier output has smaller noise ripple, the ZCD signal is much cleaner, and T_{delay} reduces to 65 ns. Adding a CM filter on the dc bus is more effective. As presented in Figure 5.26(b), v_{amp} is nearly distortion-free, and the ZCD signal is almost ideal.

As a second alternative, the common noise rejection level of the ZCD circuit can be increased. For the differential amplifier used in the ZCD circuit (Figure 4.19), the common mode rejection rate (CMRR) highly depends on the precision of the feedback resistors $R_1 - R_4$. Figure 5.27 shows the equivalent circuit of the differential amplifier, where $A(s)$ is the open-loop gain and represented by a multi-pole transfer function. Based on the model, the DM closed-loop gain $G_{DM} = {}^{v_{amp}}/_{v_{DM}}$ and CM closed-loop gain $G_{CM} = {}^{v_{amp}}/_{v_{CM}}$ are

$$\begin{aligned} G_{DM}(s) &= \frac{v_{amp}}{v_{DM}} \\ &= \frac{1}{2}\left(\frac{R_4}{R_1}\cdot f_{A1}(s) + \frac{R_3}{R_1 + f_{A2}(s)}\cdot\frac{R_1+R_4}{R_2+R_3}\right) \end{aligned} \tag{5.13}$$

$$\begin{aligned} G_{CM}(s) &= \frac{v_{amp}}{v_{CM}} \\ &= -\frac{R_4}{R_1}\cdot f_{A1}(s) + \frac{R_3}{R_1 + f_{A2}(s)}\cdot\frac{R_1+R_4}{R_2+R_3} \end{aligned} \tag{5.14}$$

where $f_{A1}(s), f_{A2}(s)$ are functions of $A(s)$. Since R_{in} and $A(s)$ gain are very large in low-frequency range, $|f_{A1}(s)| \approx 1, |f_{A2}(s)| \approx 0$, and $G_{DM} = {}^{R_4}/_{R_1}, G_{CM} = 0$ with $R_1 = R_2, R_3 = R_4$.

$$f_{A1}(s) = \frac{\frac{A(s)}{R_o} - \frac{1}{R_4}}{\frac{A(s)}{R_o} + \frac{R_o+R_L}{R_oR_L} + \frac{R_1+R_{in}}{R_1R_{in}}\left(1 + \frac{R_4(R_o+R_L)}{R_oR_L}\right)} \tag{5.15}$$

$$f_{A2}(s) = \frac{R_o\left(1+\frac{R_o}{R_L}\right)\left(R_{in} + R_3 + \frac{R_1R_4}{R_1+R_4} - \frac{R_3}{R_2+R_3}\right)}{A(s)\frac{R_{in}}{R_1+R_4} + \frac{R_1R_o}{(R_1+R_4)^2}} \tag{5.16}$$

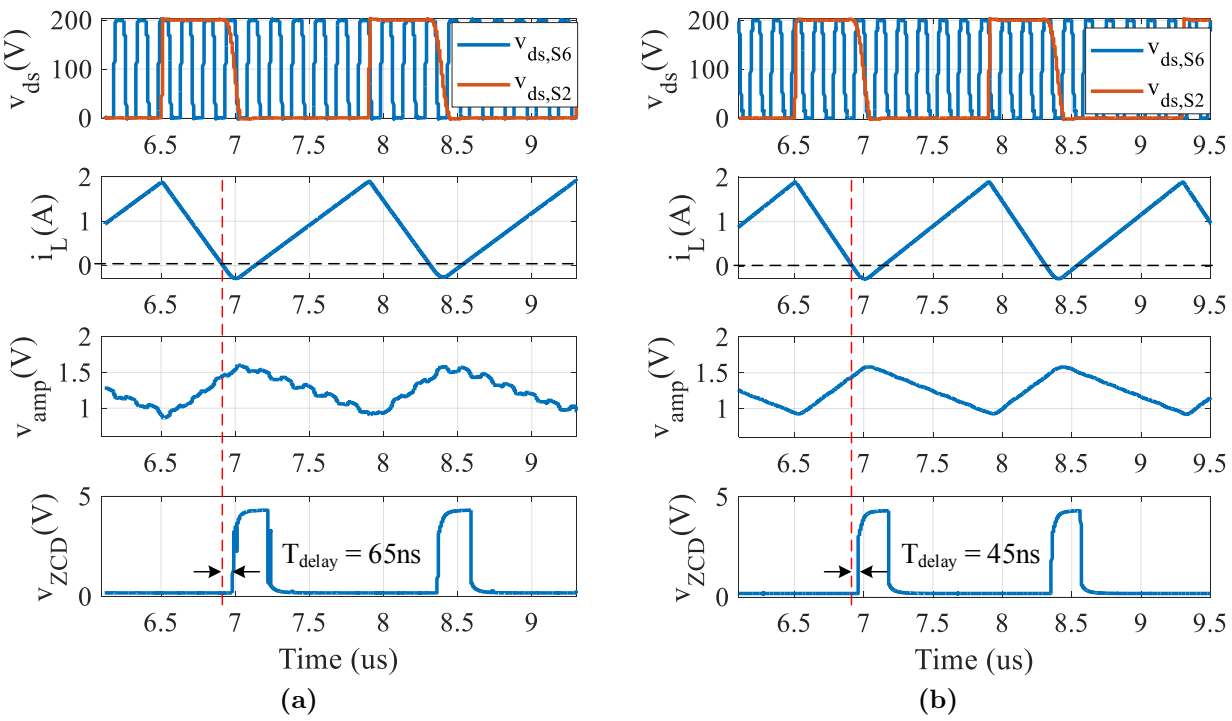


Figure 5.26: Simulated waveforms of the ZCD circuit with noise attenuation. (a) With CM choke in the inverter LC network; (b) With CM filter on dc bus between the PFC stage and the inverter.

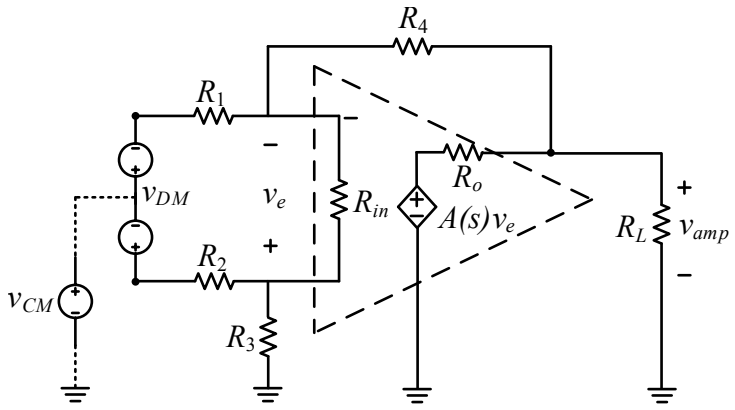


Figure 5.27: Equivalent circuit of a typical differential amplifier.

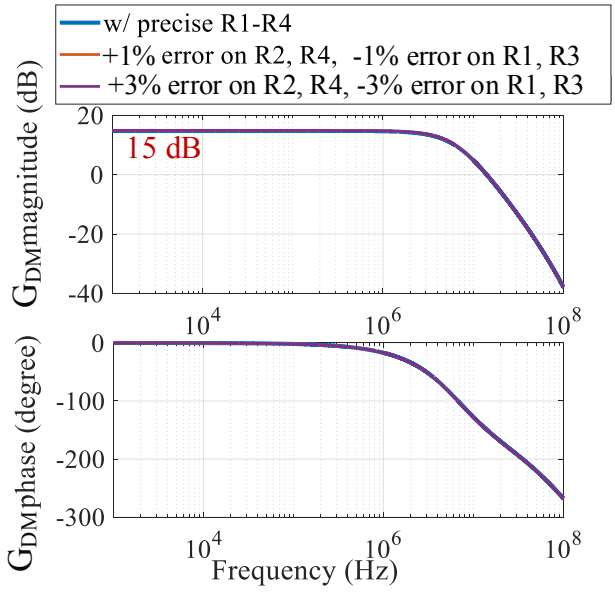
Figure 5.28 displays the bode plots of G_{DM} and G_{CM} in three cases: a nominal case with precise resistances for $R_1 - R_4$, an error case with 1% error in resistance, and an error case with 3% error in resistance. In all cases, G_{DM} is nearly identical with 15 dB low-frequency gain. However, G_{CM} changes, with low-frequency gain increased from -98 dB in the nominal case to -29 dB in the 1% error case and to -19 dB in the 3% error case. Consequently, the amplifier CMRR is reduced from 113 dB to 34 dB. Therefore, resistors with higher precision should be used in the amplifier circuit to maintain high CMRR. In addition, for the ZCD circuit (Figure 4.19), balanced RC filters with $R_5 = R_6$, $C_1 = C_2$ between the amplifier and the comparator filter out the coupled noise on v_{amp} and v_{th}. These filters must be selected carefully to provide adequate noise attenuation without contributing significant propagation delay.

5.4.4 Experimental Verification

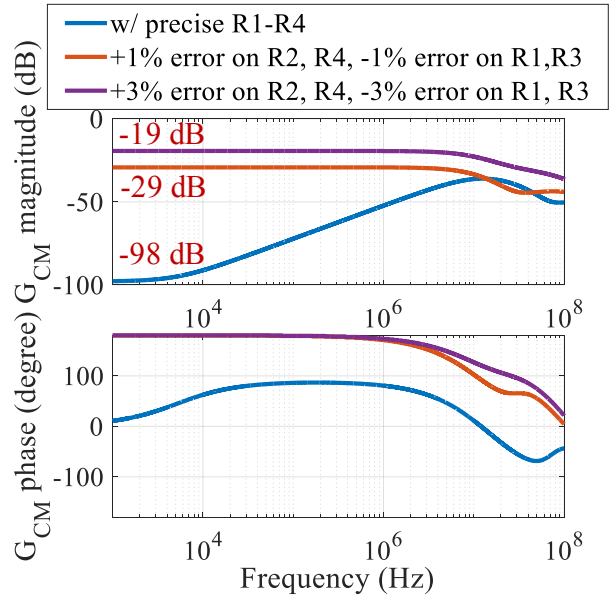
5.4.4.1 Verification of the Line-Cycle Current Distortion and Mitigation

To mitigate the line-cycle current distortion, the ZCD signal propagation delay is first compensated by embedding the modified converter model in the real-time calculation. Figure 5.29 presents the tested waveforms. The inductor current is still severely distorted due to the noise impact. Figure 5.29(b) presents zoomed-in waveforms and the measured ZCD signal time delay of PFC prototype in the WPT system. The ZCD signal is coupled with high-frequency noise, and has large and varying time delay within a line cycle (Figure 5.29(c)).

To reduce the noise impact on the ZCD signal, system CM impedance and the ZCD circuit noise rejection level should be improved. Considering the limited converter space of the high-density power supply, an additional CM filter or CM choke is not desired. For the WPT system, the CM impedance can be increased by adjusting the IMN network to an L-C-L configuration instead of an L-C structure. As illustrated in Figure 5.30, L_{IMN} is modified from a single inductor to a coupled inductor with the same inductance in the DM loop.



(a)



(b)

Figure 5.28: Bode plot of the closed-loop gains in the differential amplifier, with $R_1 = R_2 = 1$ kΩ, $R_3 = R_4 = 6$ kΩ, $R_{in} = 10^{12}$ Ω, $R_o = 10$ Ω, output RC filter $R_5 = 50$ Ω, $C_1 = 330$ pF. (a) DM closed-loop gain; (b) CM closed-loop gain.

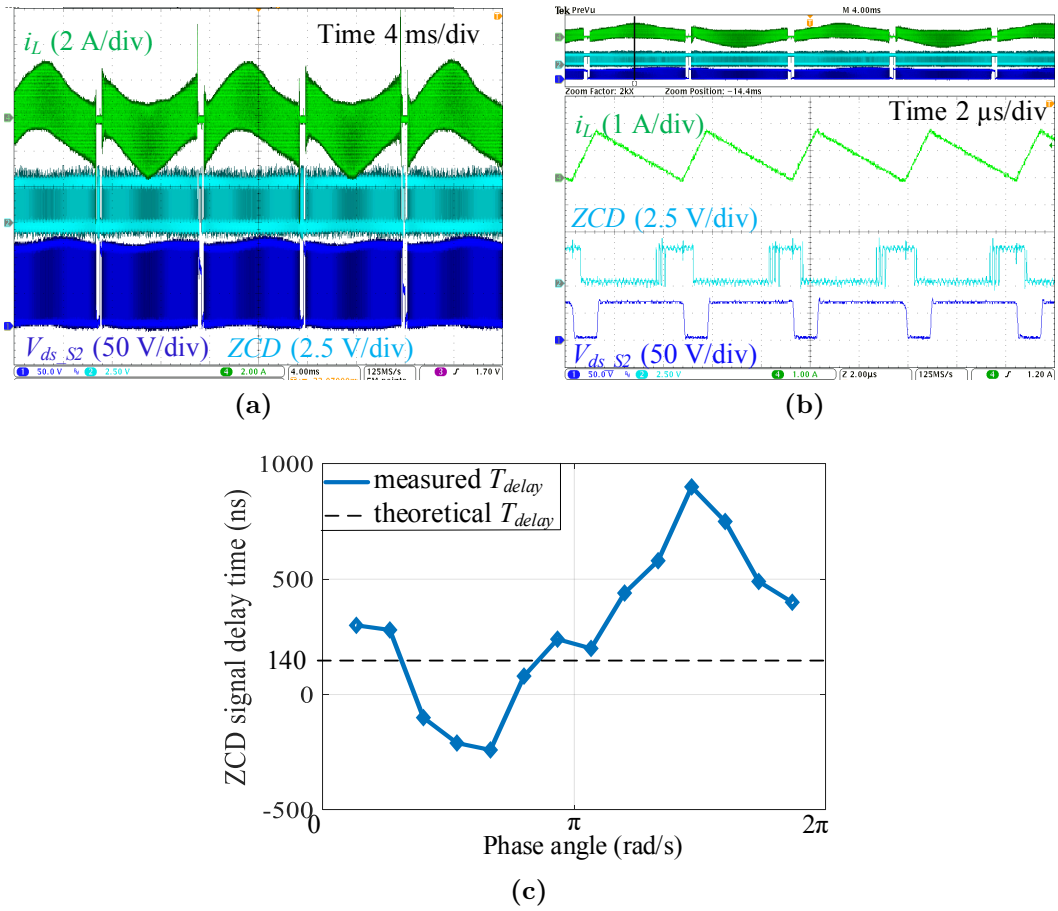


Figure 5.29: Experimental waveforms of the 100 W PFC in WPT system with compensated ZCD signal time delay. (a) Line-cycle waveform; (b) Noise on ZCD signal; (c) Large and varying ZCD time delay within one cycle.

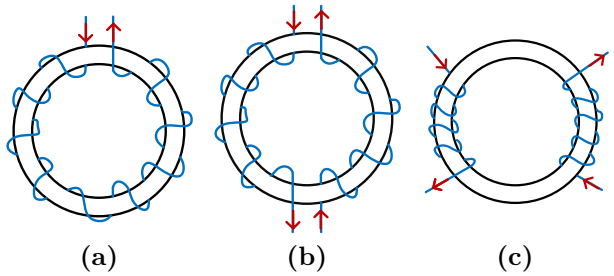


Figure 5.30: IMN inductor. (a) Original single L_{IMN}; (b) Coupled L_{IMN}; (c) Coupled L_{IMN} with higher CM impedance.

To achieve higher CM impedance, a lower coupling coefficient k is realized by separating the windings to opposite ends of the low-permeability core (Figure 5.30(c)). As listed in Table 5.2, with the same core and winding wire, the CM impedance varies widely among different winding structures. In the ZCD circuit, feedback resistors measured with lower than 1% error are selected for the amplifier to keep high CMRR, and the RC filters are carefully enlarged and balanced to help suppress the noise impact.

Figure 5.31 displays the testing waveforms of PFC in the WPT system with the noise mitigation. The inductor current is balanced and distortion-free along the line cycle, and the ZCD signal is clean without varying time delay. As shown in Figure 5.31(c), the PFC converter is able to operate at full load with target voltage and power. Apart from the ac line current spike, the line-cycle current distortion is removed from the input ac current.

5.4.4.2 Verification of the Ac Line Zero-Crossing Current Spike and Mitigation

Similar with the 1.5 kW PFC prototype for data centers, to avoid the inductor current spike and ensure soft switching in each switching cycle, the proposed device switching sequence during the blanking time is implemented in the WPT transmitter PFC stage. For the high-density transmitter of the WPT system, adding an auxiliary circuit is not preferable. Hence, the CM choke of the EMI filter is built with a nanocrystalline core and high CM impedance to stop the noise current from distorting the input source.

Figure 5.32 - Figure 5.34 show the full-load experimental results of the PFC rectifier in the 6.78 MHz WPT system. With 120 V_{ac} input, the output voltage is regulated at 200 V_{dc} with reliable ZVS control. The ac line zero-crossing current spike is significantly attenuated with the heavy CM filter, but cannot be completely removed. As shown in Figure 5.34, the high dv/dt still exists in v_{ds} when the Si devices switch, but no large inductor peak current or hard switching occurs when GaN devices are turned on.

The tested full-load end-to-end efficiency of the WPT power supply system is 90.16%. Figure 5.35 presents the measured efficiency and current THD of the PFC rectifier. With the proposed mitigation methods for current distortion, the PFC efficiency is increased and the current THD is reduced. At full load, the PFC efficiency reaches 98.5%, PF = 0.994, and current THD = 6.6%.

Table 5.2: Impedance of different IMN inductors in Figure 5.30

L_{IMN}	a	b	c
L_{DM}	1.68 uH	1.68 uH	1.68 uH
L_{CM1}	1.68 uH	0.55 uH	0.73 uH
L_{CM2}	0 uH	0.57 uH	0.7 uH
k	0	0.4822	0.1816

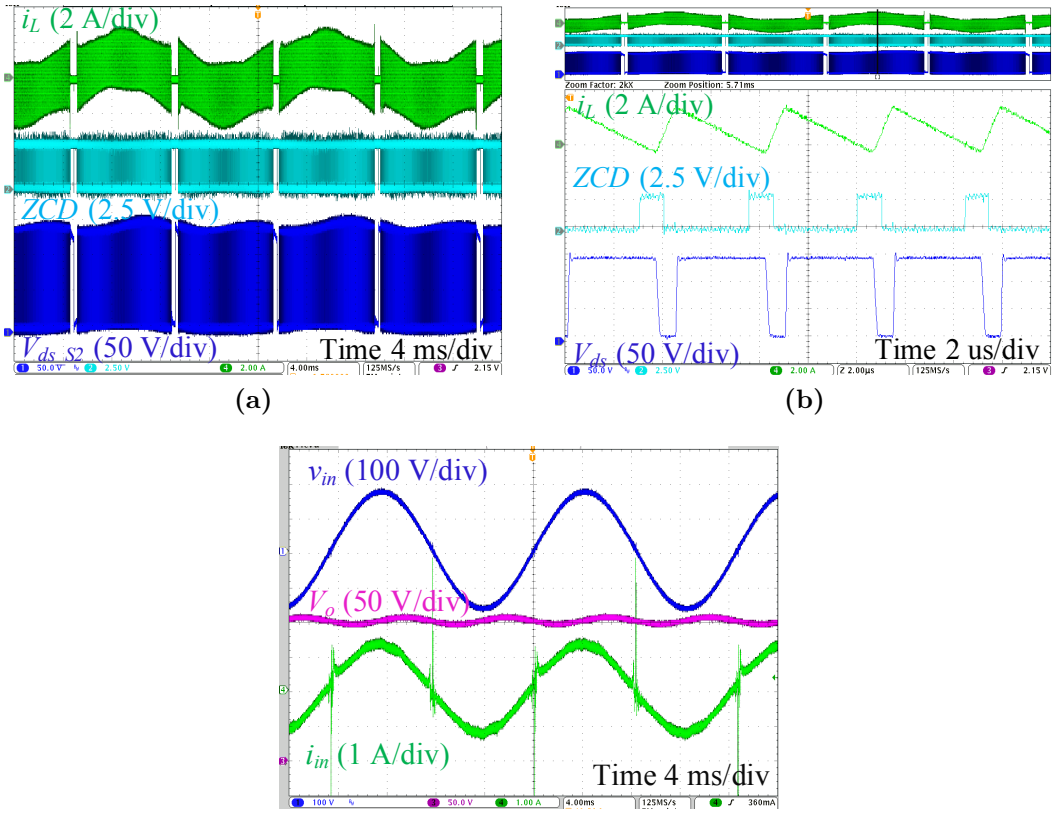
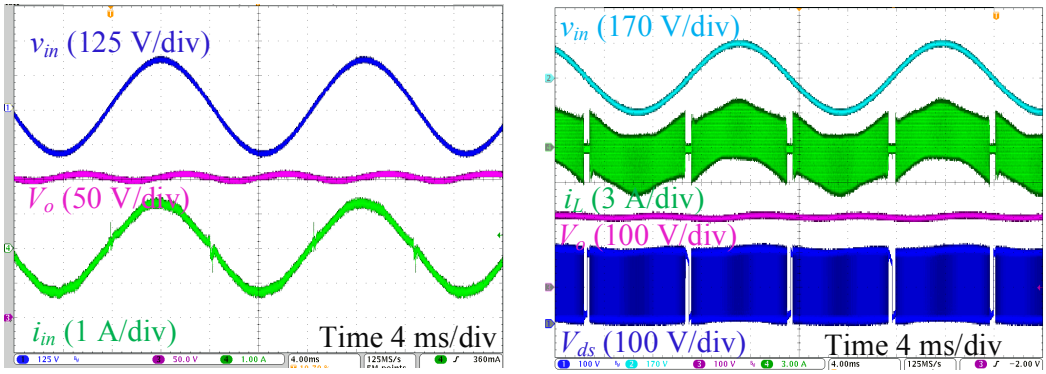
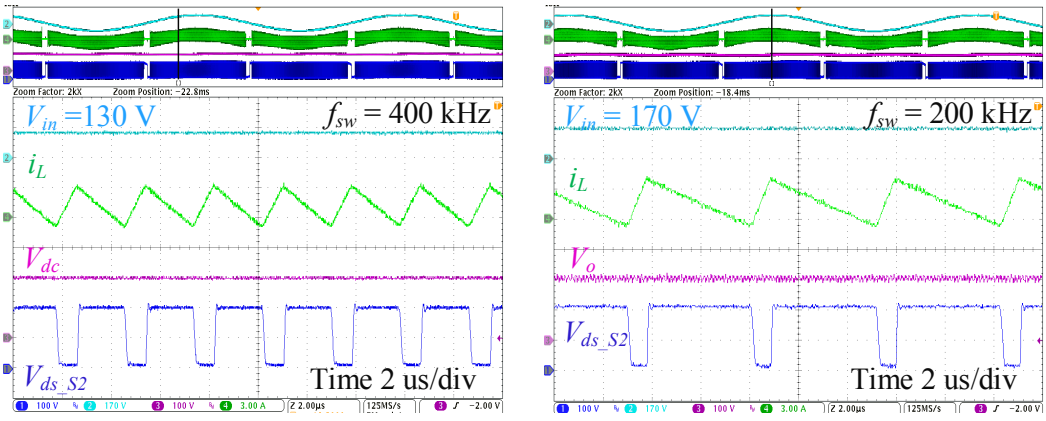


Figure 5.31: Experimental waveforms of the PFC prototype in WPT system with mitigated noise. (a) Waveforms of iL, ZCD signal, and $V_{ds,S2}$; (b) Zoom-in waveforms of iL, ZCD signal, and $V_{ds,S2}$; (c) Full-load operation wavefroms of v_{in}, V_o, i_{in}.



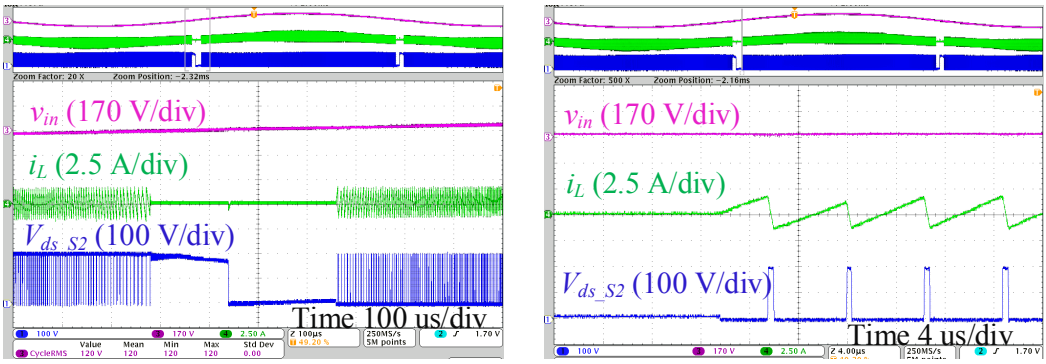
(a) Wavefroms of v_{in}, V_o, i_{in}. **(b)** Wavefroms of v_{in}, V_o, i_L.

Figure 5.32: Experimental line-cycle waveforms of the PFC rectifier at 100 W in the 6.78 MHz WPT system with the mitigation methods for current distortion.



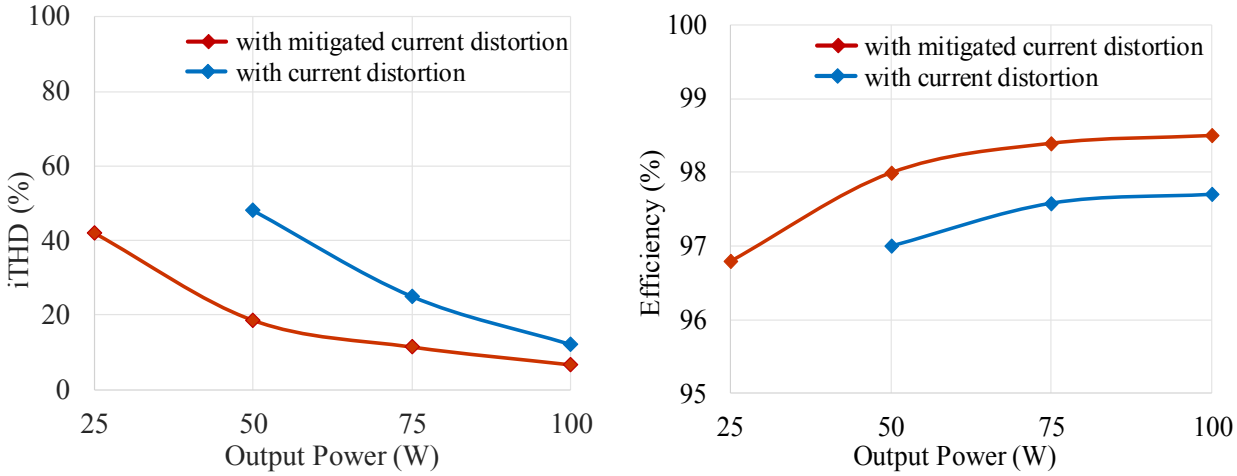
(a) Switching wavefroms at $V_{in} = 130\ V$. **(b)** Switching wavefroms at $V_{in} = 170\ V$

Figure 5.33: Experimental switching waveforms of the PFC rectifier at 100 W in the 6.78 MHz WPT system with the mitigation methods for current distortion.



(a) (b)

Figure 5.34: AC line zero-crossing transition waveforms of PFC_WPT with the proposed mitigation methods for current distortion. (a) Negative-to-positive transition; (b) Device turn-on waveforms in the positive half line cycle.



(a) (b)

Figure 5.35: Measured iTHD and efficiency of the PFC rectifier for the WPT system at different loads with and without the proposed mitigation methods for current distortion.

5.4.4.3 Verification of the Fast Dynamic Response During Load Change

To validate the capability of fast dynamic response, a load transient is conducted by removing one of the receivers in the WPT system. Figure 5.36 and Figure 5.38 display the tested waveforms of the CRM PFC during the transition between full load and half load. Figure 5.37 shows the transmitter coil current during the load transient. As can be seen, fast transient response is achieved with very small dc bus voltage fluctuation, and the 6.78 MHz transmitter coil current is not influenced during the process.

5.5 Summary

This chapter explores the current distortion issues of the GaN-based CRM totem-pole PFC rectifier. Detailed analysis is provided, and effective solutions are proposed. The root cause for the line-cycle current distortion is the current sensing time delay, which leads to larger current ripple, higher current THD, and increased power loss. In order to reduce the delay impact, parasitic inductance of the sensing resistor is purposely enlarged to cancel partial delay time. Also, a modified analytical converter model considering the delay time is implemented in the controller real-time calculation.

The ac line zero-crossing current spike is induced by two mechanisms. One is the asynchronization between the Si device switching and the ac voltage zero-crossing, and the other one is the high dv/dt noise induced by the voltage change of the Si device. To reduce the current spike, a fixed device switching sequence with a small blanking time is implemented during the ac line zero-crossing. And a simple auxiliary circuit is proposed to slow down the switching node voltage commutation and eliminate the current spike due to high dv/dt.

The current distortion and mitigation methods are experimentally validated on the 1.5 kW GaN-based PFC prototype. With the proposed solutions, both the current THD and the converter efficiency are improved. The peak efficiency increases to 99%, and the current THD is reduced below 5% in all testing loadings.

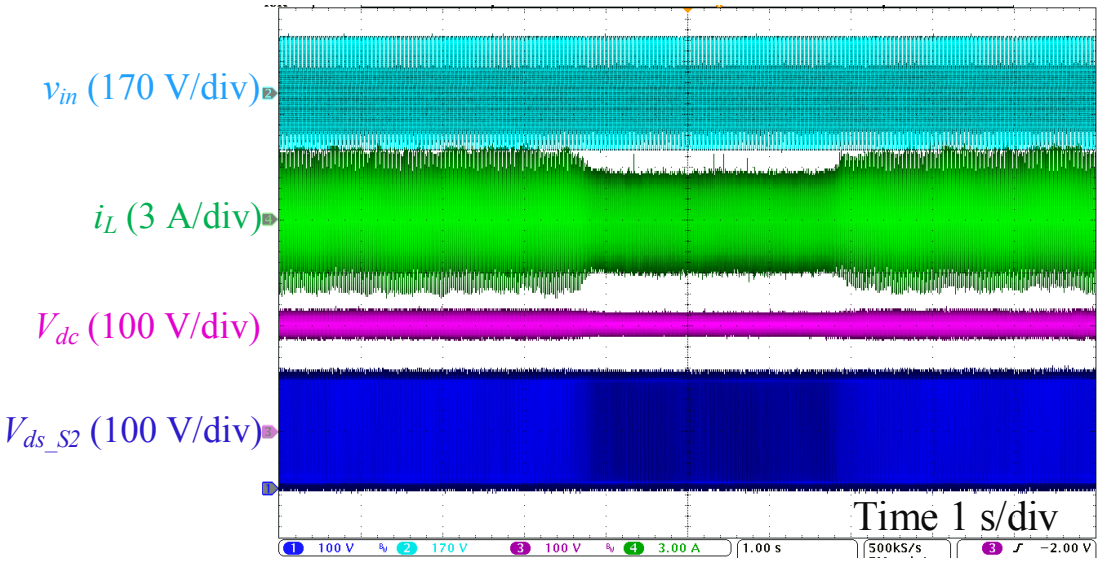
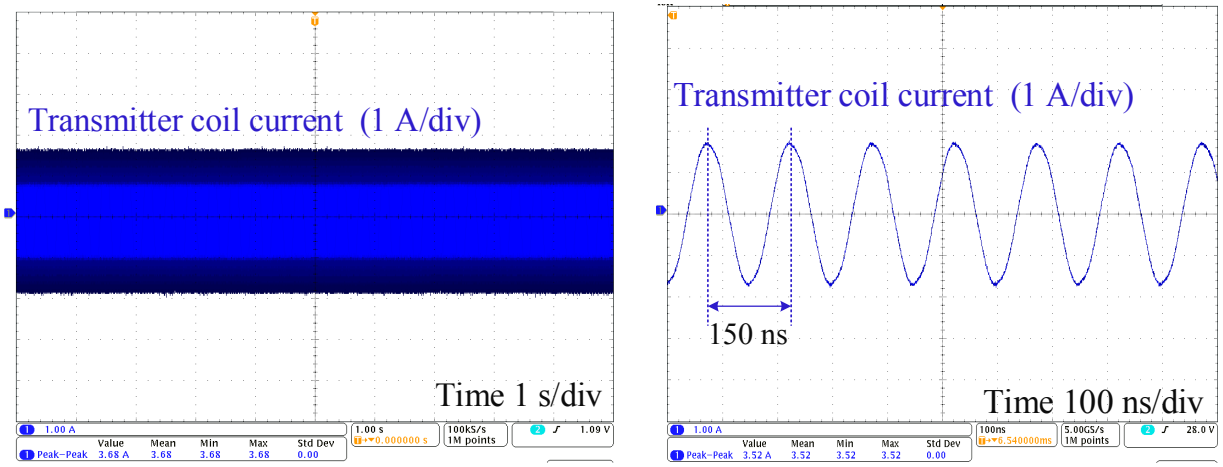
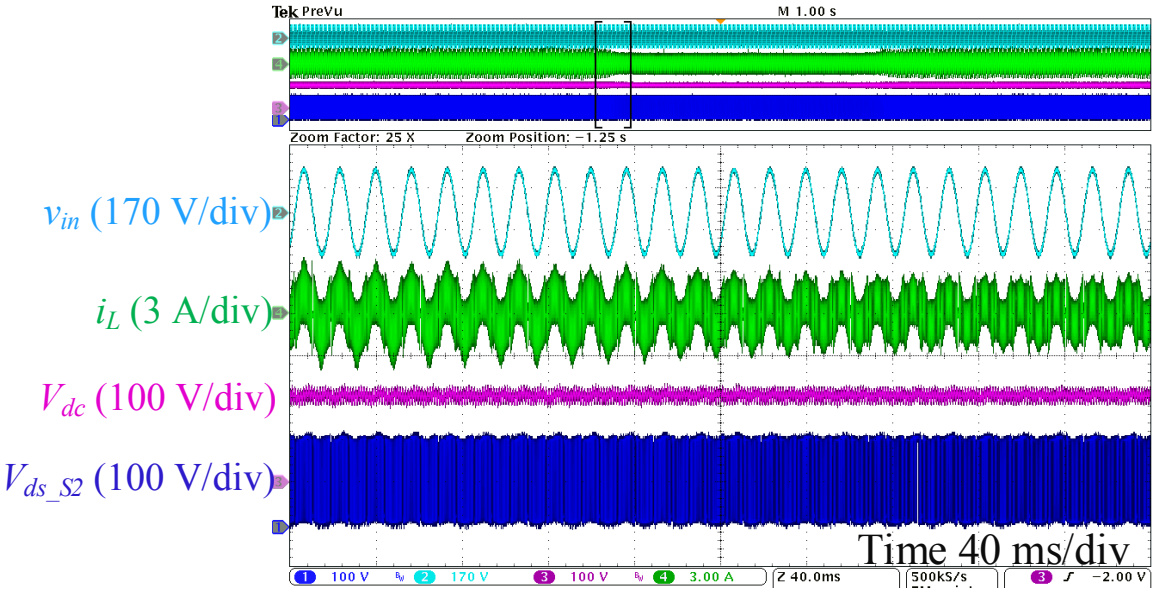


Figure 5.36: Experimental transition waveforms of the CRM PFC in the 6.78 MHz WPT system during load variation between full load and half load.

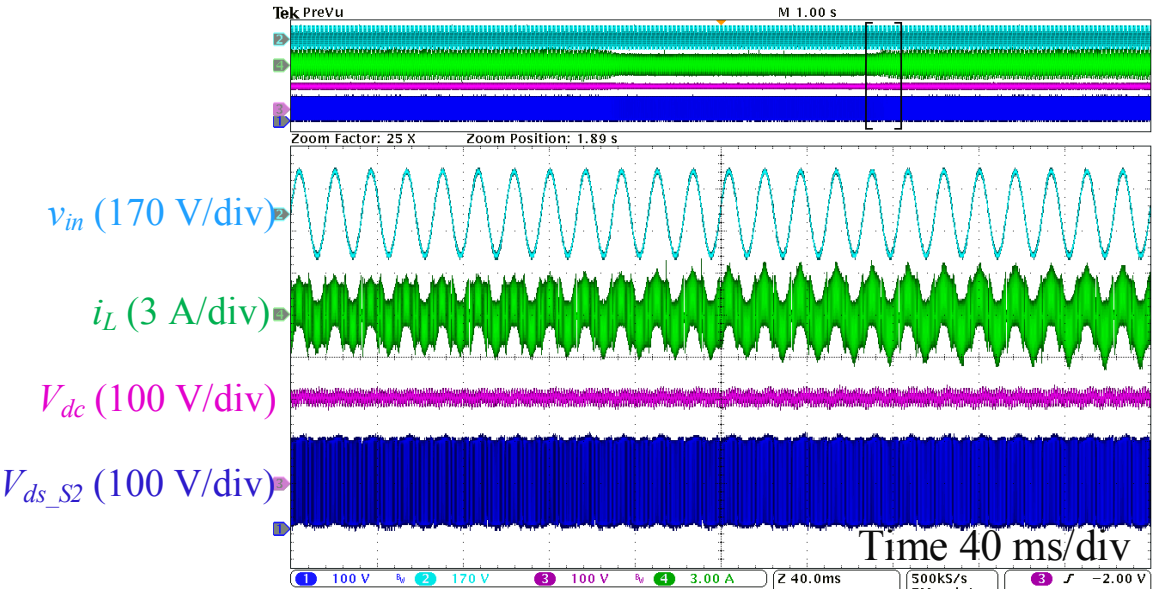


(a) **(b)**

Figure 5.37: Experimental transmitter coil current during load variation between full load and half load (a) Long-scale waveform; (b) Zoom-in waveform.



(a)



(b)

Figure 5.38: Experimental transition waveforms of the CRM PFC in the 6.78 MHz WPT system. (a) From full load to half load; (b) From half load to full load.

Similar current distortion issues also occur in the front-end PFC rectifier of a GaN-based 100 W 6.78 MHz wireless charging power supply system. Apart from the aforementioned current distortion, the ZCD signal is disturbed by high-frequency noise, leading to more severe line-cycle current distortion and unstable ZVS control. In order to avoid the noise impact and maintain stable ZVS control in the noise susceptible environment, system CM impedance is enlarged by configuring the WPT IMN network as balanced structure with coupled inductor, and precise resistors are employed in the ZCD circuit to improve CMRR. Effectiveness of the proposed noise immunity methods are verified experimentally, where the power supply system is able to operate stably with 90.16% end-to-end full-load efficiency and fast dynamic response during load change.

In summary, maintaining low current distortion and reliable ZVS control of the GaN-based CRM totem-pole PFC is challenging, especially in high-frequency noise-susceptible environment. The proposed mitigation methods for current distortion are effective and advantageous in straightforward implementation without the need for extra control resources.

Chapter 6

GaN-Based Rectifier with Reactive Power Regulation

The GaN-based CRM totem-pole PFC rectifier has been demonstrated to achieve 99% peak efficiency with full-line-cycle ZVS control. Compared to the traditional boost PFC rectifier with efficiency usually lower than 97% [220], more than 60% of the converter loss is reduced. However, commercial high-voltage GaN transistors are expensive in the current market, which sabotages the profit gained from the high-efficiency performance.

On the other hand, a large amount of reactive power is generated within a data center, especially from the cooling system. To satisfy grid interconnection regulations, the reactive power needs to be compensated so that the power factor (PF) on the gird terminal is close to 1. A traditional centralized power compensator results in significant power loss and increases the system cost. Since server rack rectifiers are directly connected to the grid terminal during the normal operation mode, reactive power can also be compensated by the front-end rectifiers. If GaN-based high-efficiency rectifiers are used, the power loss in processing the reactive power can be significantly reduced, and centralized power compensator is not required.

In this chapter, the idea of regulating reactive power on GaN-based front-end rectifiers is proposed, in order to further improve the data center power usage efficiency and help reduce the system cost.

(1) Evaluate the advantages of using GaN-based front-end rectifiers for reactive power compensation in data centers to achieve unity PF on the point of common coupling (PCC).

(2) Propose full-range ZVS modulation with non-unity PF for GaN-based CRM rectifier.

(3) Compare and select a suitable rectifier topology to overcome the control challenges.

(4) Propose control strategy to implement the full-line-cycle ZVS modulation and reactive power regulation.

6.1 Advantages of Reactive Power Compensation by Front-End Rectifiers

In order to investigate the benefits of using GaN-based front-end rectifiers for reactive power compensation, data center systems with different reactive power compensation methods and front-end rectifiers are evaluated. A 10 MW data center is defined to quantify and compare the system power loss and cost, as shown in Table 6.1. Two loading condition with server utilization $u = 100\%$ and $u = 50\%$ are considered, and three system configurations are

- Data center system 1: centralized STATCOM is used for reactive power compensation; traditional Si-based boost PFC rectifiers are used on server racks.
- Data center system 2: centralized STATCOM is used for reactive power compensation; GaN-based totem-pole PFC rectifiers are used on server racks.
- Data center system 3: GaN-based totem-pole rectifier is adopted for the front-end rectifiers on server racks, which also compensate the reactive power.

In order to assess the system cost and power loss, the traditional boost PFC rectifier and GaN-based CRM totem-pole rectifier are designed with $V_{in} = 277\ \mathrm{V_{ac}}, V_o = 480\ \mathrm{V_{dc}}, P_{rate} = 1.5$ kW. Table 6.2 and Table 6.3 present the detailed design and the rectifier capital cost. Because of the high cost of GaN devices, the totem-pole rectifier is twice as expensive as the traditional boost PFC rectifier.

Table 6.1: Defined 10 MW data center system.

Parameter	w/ server $u = 100\%$			w/ server $u = 50\%$		
P_t(MW)	10			6.875		
Q_t(MVAr)	2.506			2.058		
PF	0.97			0.958		
P_{IT}(MW)	6.740			3.629		
N_{rec}	4500			4500		
Parameter	system 1	system 2	system 3	system 1	system 2	system 3
$N_{STATCOM}$	21	21	0	21	21	0
$Q_{STATCOM}$(MVAr)	-2.506	-2.506	0	-2.058	-2.058	0
Q_{rec}(MVAr)	0	0	-2.506	0	0	-2.058

* ABB STATCOM PCS100 is adopted as the STATCOM, which can deliver 125 kVAr reactive power per module with peak efficiency at 97% [46].
* N_{rec} represents the total number of the front-end rectifiers.
* **System 1** has centralized STATCOM and Si-based boost PFC rectifiers.
* **System 2** has centralized STATCOM and GaN-based CRM totem-pole PFC rectifiers.
* **System 3** has GaN-based CRM totem-pole rectifiers.

Table 6.2: Design of Si-based boost PFC rectifier.

Component	Part No.	Price
Diode bridge	2-paralleled GSIB2580, 800 V	2×\$2
Si MOSFET	IPW65R019C7, 650 V	\$11.73
SiC diode	IDH16G65C5, 650 V	\$5
Gate drive	gate driver SI8271AB-IS	\$1.45
	LDO BD60GC0MEFJ	\$0.57
Boost inductor L_b	600 μH, Kool Mu 77083A7	\$3
DC capacitor C_{dc}	6×B43541B8187M000, 180 μF, 600 V	6×\$6.17
Input capacitor C_{in}	B32924B4105K000, 350 V_{ac}, 1 μF	\$1.87
Controller	UCD3138A	\$12.06
Low-speed	hall sensor ACS723LLCTR-40AB-T	\$1.9
current sensing	linear regulator LP2985-50DBVRG4	\$0.187
Total		\$78.79

Table 6.3: Design of GaN-based CRM totem-pole PFC rectifier.

Component	Part No.	Price
GaN devices S_1, S_2	2-paralleled GS66508T, 650 V	$4 \times \$12.45$
Si Mosfets S_3, S_4	IPW65R019C7, 650 V	$2 \times \$11.73$
Gate drive	gate driver 2×SI8273AB-IS1-2	$2 \times \$2.18$
	LDO Rohm 4×BD60GC0MEFJ	$4 \times \$0.57$
Boost inductor L_b	20 μH, powder core Mix-2-T157	\$1.5
DC capacitor C_{dc}	6×B43541B8187M000, 180 μF, 600 V	6×\$6.17
Input capacitor C_{in}	B32924A4335M000, 350 V_{ac}, 3.3 μF	\$4
Controller	DSP TMS320F28377S	\$15
High-speed	10 mΩ R_{shunt} LVK25R010FER	\$0.84
current sensing	comparator ADCMP601	\$2.35
	digital isolator ADUM1100	\$2.5
Total		\$143.11

Table 6.4 summarizes the predicted cost and power loss of the three data center systems. $P_{rec}, Q_{rec}, S_{rec}$ are the operation power of a single rectifier. Power loss of a single rectifier is calculated based on the loss model in Appendix A, and the total rectifiers' loss is calculated by multiplying with the number of rectifiers. STATCOMs'loss is estimated based on the reactive power capacity to be compensated and the STATCOM's efficiency [46]. For each system, the total power loss include the rectifiers' loss, STATCOMs'loss, and the server room cabling loss which is estimated as 0.5% of the IT equipment power. Electricity bill of the total power loss is calculated, and the data center system cost is defined as the sum of the initial costs of rectifiers and STATCOMs, and the electricity bill over years.

As shown in Figure 6.1, for both $u = 100\%$ and $u = 50\%$, System 2 and System 3 have lower power loss compared to that in System 1, and System 3 with GaN-based front-end rectifiers for reactive power compensation has the lowest power loss. Figure 6.1(b) shows the system cost over two years. System 2 has the highest cost because of the high cost of commercial GaN devices and centralized STATCOM. By utilizing GaN-based front-end rectifiers for reactive power compensation in System 3, the total system cost is reduced to be less than System 1. For data centers, the average lifespan is 10-15 years and the computing hardware should be replaced around every five years [221]. Hence, the total costs in five years of the three data center systems are also compared, as shown in Figure 6.1(c). In five years, the reduced cost in System 3 is more significant, where at 100% server loading, 27% cost is saved compared to System 1, and 32% cost is reduced compared to System 2.

Therefore, by using GaN-based rectifiers to provide reactive power compensation, the data center system cost can be reduced significantly, and more profit can be obtained. Meanwhile, implemented with reactive power operation, the data center rack-level rectifiers can be used for grid reactive power support to gain more profit and revenue source. In summary, the advantages of implementing reactive power operation on the GaN-based front-end rectifiers on server racks include:

(1) Reduce the data center power consumption and system cost.

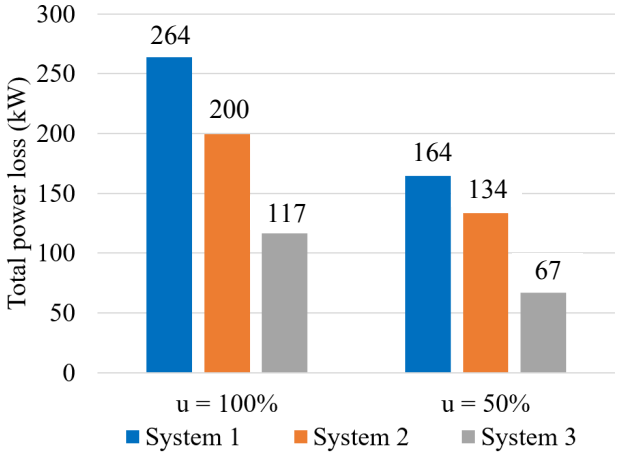
(2) Allow practical adoption of GaN-based front-end rectifiers in data centers.

(3) Gain more profit by providing grid reactive power support.

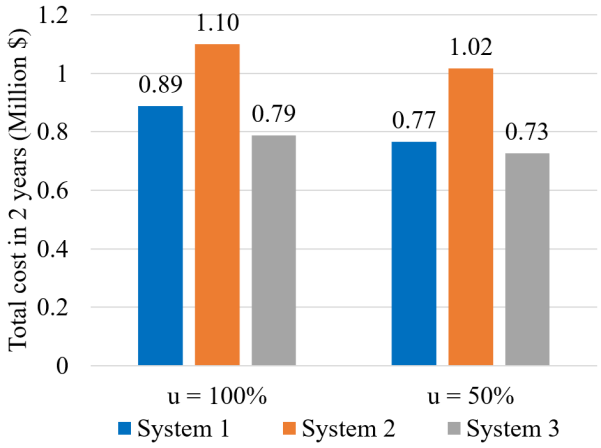
Table 6.4: Predicted cost and power loss of data center systems.

Parameter	w/ server $u = 100\%$			w/ server $u = 50\%$		
	system 1	system 2	system 3	system 1	system 2	system 3
P_{rec}(kW)	1.498	1.498	1.498	0.807	0.807	0.807
Q_{rec}(kVAr)	0	0	-0.557	0	0	-0.457
S_{rec}(kVA)	1.498	1.498	1.598	0.807	0.807	0.9271
Rectifiers loss(kW)	139.19	75.15	80.55	71.55	40.86	46.327
STATCOMs loss(kW)	90.9	90.9	0	74.64	74.64	0
Cable loss(kW)	33.7	33.7	35.96	18.16	18.16	20.86
Electricity bill/year	\$161,756	\$122,487	\$71,444	\$100,779	\$81,954	\$41,088
Rectifiers initial cost	\$354,542	\$643,950	\$643,950	\$354,542	\$643,950	\$643,950
STATCOMs initial cost	\$210,000	\$210,000	\$0	\$210,000	\$210,000	\$0

* It is assumed that both active power and reactive power are evenly distributed on each STATCOM module and front-end rectifiers.
* Server room cable loss is estimated as 0.5% of the IT equipment power.
* The U.S. average industrial price of electricity is \$ 0.07/kWh since 2010 [222].
* STATCOMs cost \$ 60/kVAr to \$ 100/kVAr [223]. The average cost at \$ 80 per kVAr is used here.
* **System 1** has centralized STATCOM and Si-based boost PFC rectifiers.
* **System 2** has centralized STATCOM and GaN-based CRM totem-pole PFC rectifiers.
* **System 3** has GaN-based CRM totem-pole rectifiers.



(a)



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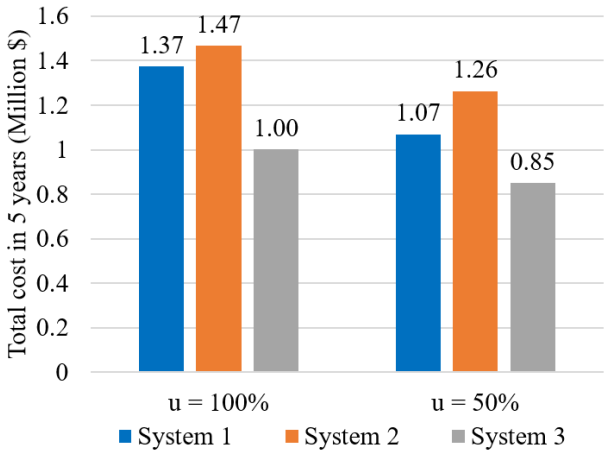


(c)

Figure 6.1: Data center power loss and cost as defined in Table 6.4. (a) Power loss; (b) Cost in two years; (c) Cost in five years.

6.2 CRM Totem-Pole Rectifier with Reactive Power

6.2.1 Effect of Reactive Power on Dc Capacitance

The dc capacitance required in the single-phase rectifier is influenced by the reactive power operation. Assuming the input voltage is $v_{in}(t) = \sqrt{2}V_{rms}\sin\omega t$ and the input current is $i_{in}(t) = \sqrt{2}I_{rms}\sin(\omega t - \theta)$, the instantaneous ac input power is

$$\begin{aligned} p_{ac}(t) &= v_{in}(t)i_{in}(t) = 2V_{rms}I_{rms}\sin\omega t\sin(\omega t-\theta) \\ &= V_{rms}I_{rms}\cos\theta - V_{rms}I_{rms}\cos(\omega t-\theta) \end{aligned} \tag{6.1}$$

The instantaneous power absorbed by the boost inductor is

$$\begin{aligned} p_L(t) &= v_L(t)i_{L,ave}(t) \approx v_L(t)i_{in}(t) = L_b\frac{di_{in}}{dt}i_{in} \\ &= L_b \times \sqrt{2}I_{rms}\omega\cos(\omega t-\theta) \times \sqrt{2}I_{rms}\sin(\omega t-\theta) \\ &= \omega L_b I_{rms}^2\sin(2\omega t - 2\theta) \end{aligned} \tag{6.2}$$

Hence, the power transferred to the output is

$$\begin{aligned} p_o(t) &= p_{ac}(t) - p_L(t) \\ &= V_{rms}I_{rms}\cos\theta - V_{rms}I_{rms}\cos(\omega t-\theta) - \omega L_b I_{rms}^2\sin(2\omega t-2\theta) \end{aligned} \tag{6.3}$$

The dc component $P = V_{rms}I_{rms}\cos\theta$ is the active power consumed by the rectifier. The rest of the equation represents the ac double-line frequency ripple power, which can be rearranged as

$$p_{ripple}(t) = P_{ripple}\cos(2\omega t + \beta) \tag{6.4}$$

$$\begin{aligned} P_{ripple} &= \sqrt{(V_{rms}I_{rms})^2 + (\omega L_b I_{rms}^2)^2 - 2\omega L_b V_{rms}I_{rms}^3\sin\theta} \\ &= \sqrt{S^2 + (\omega L_b\frac{S^2}{V_{rms}^2})^2 - 2\omega L_b\frac{S^2V_{rms}^2}{Q}} \end{aligned} \tag{6.5}$$

$$\beta = \arctan\left(\frac{V_{rms}I_{rms}\sin\theta + \omega L_b I_{rms}^2\cos 2\theta}{-V_{rms}I_{rms}\cos\theta + \omega L_b I_{rms}^2\sin 2\theta}\right) \tag{6.6}$$

where $S = V_{rms}I_{rms}$ is the rectifier apparent power, $Q = V_{rms}I_{rms}\sin\theta$ is the reactive power.

Figure 6.2 illustrates the double-line frequency ripple power of the single-phase rectifier. The dc capacitor should be large enough to store the ripple energy and balance the power transfer. The ripple energy that needs to be processed can be obtained by integrating the ripple power waveform, as

$$\begin{aligned} E_{ripple} &= 2\int_{t_{min}}^{t_{zero}} |p_{ripple}(t)|\, dt = \frac{P_{ripple}}{\omega} \\ &= \frac{1}{\omega}\sqrt{S^2 + (\omega L_b \frac{S^2}{V_{rms}^2})^2 - 2\omega L_b \frac{S^2 V_{rms}^2}{Q}} \end{aligned} \tag{6.7}$$

The maximum energy that can be stored in the dc capacitor is

$$\begin{aligned} \triangle E_{max} &= \frac{1}{2}C_{dc}(V_{o,max}^2 - V_{o,min}^2) \\ &= \frac{1}{2}C_{dc}(V_{o,max} - V_{o,min})(V_{o,max} + V_{o,min}) \\ &= C_{dc}\triangle V_o V_o \end{aligned} \tag{6.8}$$

where $V_{o,max}, V_{o,min}$ are the maximum value and minimum value of the output voltages, $\triangle V_o$ is the peak-to-peak output voltage ripple. To buffer the ripple energy, $\triangle E_{max}$ cannot be less than E_{ripple}. Combining (6.7) and (6.8), the required minimum dc capacitance is

$$C_{dc} \geq \frac{\sqrt{S^2 + (\omega L_b \frac{S^2}{V_{rms}^2})^2 - 2\omega L_b \frac{S^2 V_{rms}^2}{Q}}}{\omega \triangle V_o V_o} \tag{6.9}$$

In addition, dc capacitance of the data center power supply is required to maintain the hold-up time as shown in (4.18). Considering both the ripple energy and hold-up time, the minimum dc capacitance of a 1.6 kVA rectifier with 1.5 kW output power at full load is illustrated in Figure 6.3. When the allowable ripple voltage is $\triangle V_o = 10$ V, the minimum dc capacitance is dominated by the ripple energy requirement. With unity PF operation, $C_{dc,min} = 830\ \mu$F is sufficient to meet the requirements. However, when the rectifier operates with reactive power at $Q = 600$ VAr, $C_{dc,min} = 895\ \mu$F is required. The required capacitance increases with larger reactive power capacity.

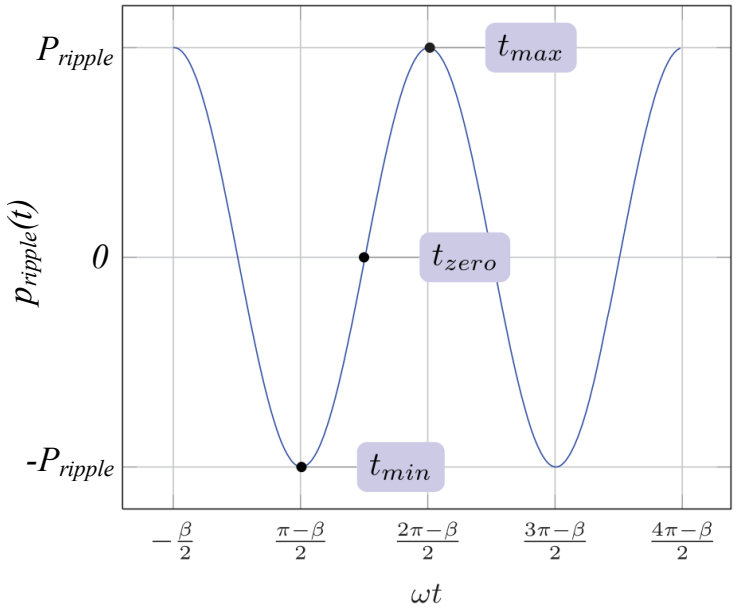


Figure 6.2: Instantaneous double-line frequency ripple power of the single-phase rectifier.

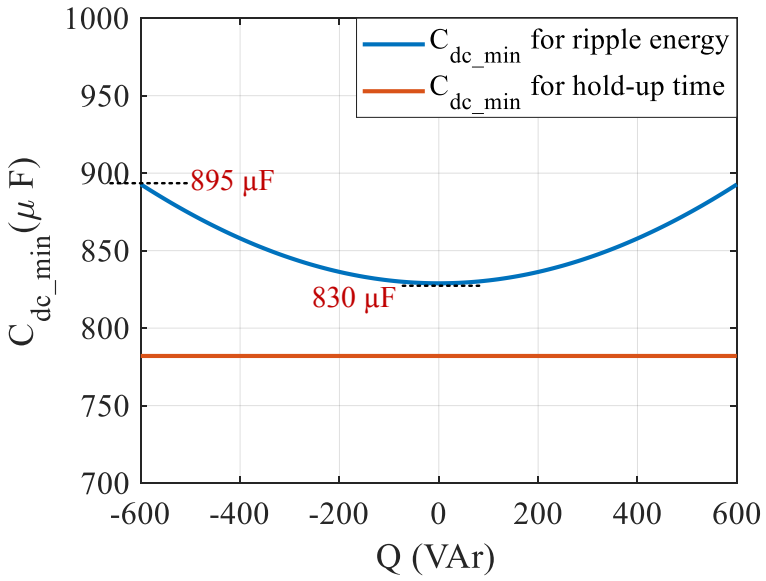


Figure 6.3: Effect of reactive power on the minimum dc capacitance required for energy buffer and hold-up time when $V_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}, $\triangle V_o = 10$ V, $P = 1.5$ kW.

6.2.2 ZVS Modulation with Non-Unity PF

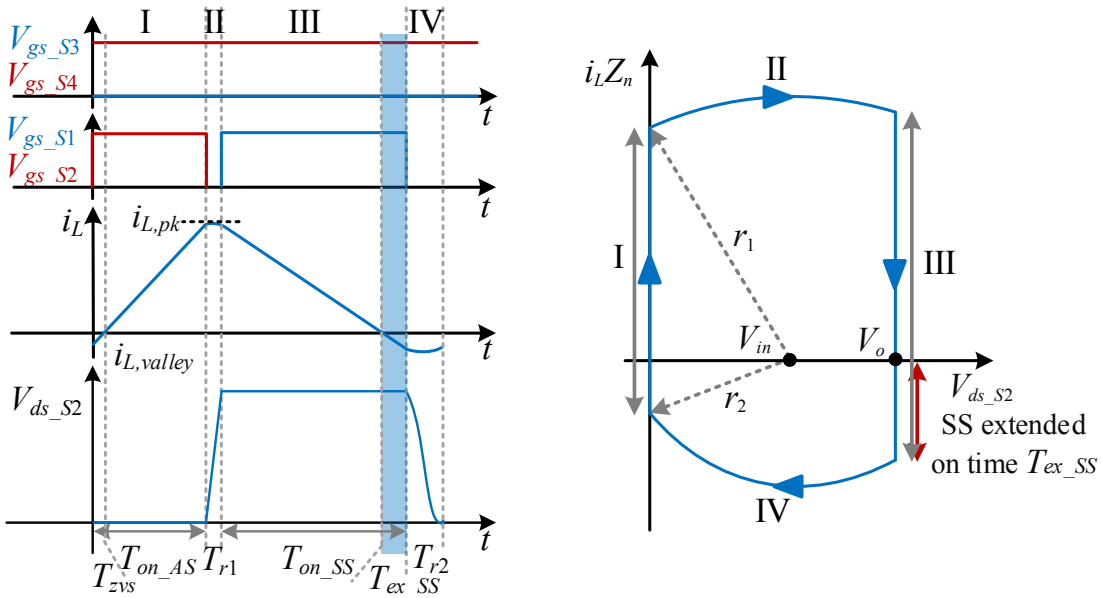
The full-line-cycle ZVS modulation of the CRM totem-pole PFC rectifier has been illustrated in Chapter 4. In this section, ZVS modulation with non-unit PF operaiton is proposed. Due to the symmetrical characteristic, discussion on the ZVS modulation will only consider the positive half-line cycle of the input voltage, and assumes that the input voltage remains nearly constant within one switching cycle.

For the CRM totem-pole rectifier during v_{in} positive half line cycle, Si device S_4 is ON and S_3 is OFF , S_2 is the active switch (AS), and S_1 is the synchronous rectification switch (SS). With unipolar modulation, the inductor current is charged with V_{in} when S_2 conducts, and discharged with $(V_{in}-V_o)$ when S_1 is ON. The rectifier waveforms and state-plane trajectory within one switching cycle are shown in Figure 6.4. For the state-plane trajectories, the characteristic impedance Z_n is defined as $Z_n^2 = {}^{L_b}/_{(2C_{oss})}$, where C_{oss} is the equivalent drain-to-source capacitance of S_1 and S_2, assuming $C_{oss,S1} = C_{oss,S2} = C_{oss}$.

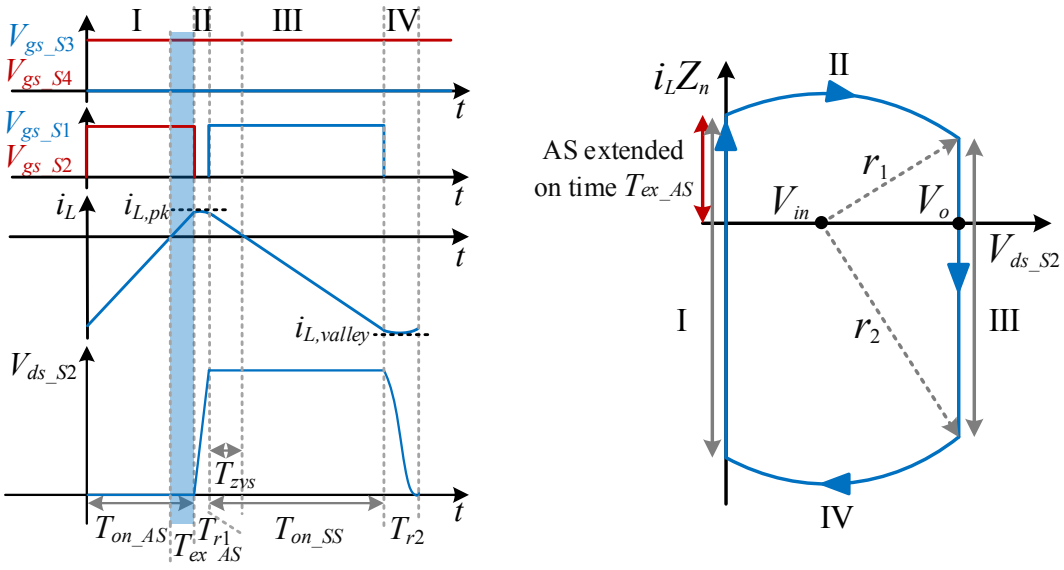
In Figure 6.4(a) when $V_{in} > 0, I_{in} > 0$, the ZVS operation is the same as that in the unity PF case. S_1 achieves ZVS turn-ON naturally since $i_{L,pk}$ discharges $C_{oss,S1}$ during a deadtime before S_1 turns ON. However, S_2 can only achieve natural ZVS turn-ON when $V_{in} \leq V_{bound}$. When $V_{in} > V_{bound}$, $i_{L,valley}$ is not enough to fully discharge $C_{oss,S2}$ before S_2 turns ON, leading to valley switching. To also realize ZVS when $V_{in} > V_{bound}$, the conduction time of S_1, T_{on_SS}, is extended by T_{ex_SS} to have a lower $i_{L,valley}$, so that V_{ds_S2} is able to resonate to zero before S_2 turns ON.

When $V_{in} > 0, I_{in} < 0$, S_2 achieves ZVS turn-ON passively since $|i_{L,valley}|$ is large enough to discharge $C_{oss,S2}$. However, S_1 only realizes valley switching when $V_{in} > V_{bound}$, as shown in Figure 6.4(b). To achieve S_1 ZVS turn-ON, the conduction time of AS device S_2, T_{on_AS}, is extended by T_{ex_AS} for achieving a larger $|i_{L,pk}|$.

Table 6.5 summarizes the key parameters for ZVS operation in the four quadrants of V_{in} and I_{in}. Figure 6.5 shows the waveforms of input voltage, inductor currents, switching frequency, and time intervals of a CRM totem-pole rectifier with and without reactive power. Compared with the unity-PF operation, the rectifier exhibits larger inductor current ripple and higher peak switching frequency.



(a)



(b)

Figure 6.4: ZVS waveforms and state plane trajectories of the CRM totem-pole rectifier in the positive half line cycle with (a) $V_{in} > 0, I_{in} > 0$; (b) $V_{in} > 0, I_{in} < 0$.

Table 6.5: Full-line-cycle ZVS operation principle of the CRM totem-pole rectifier.

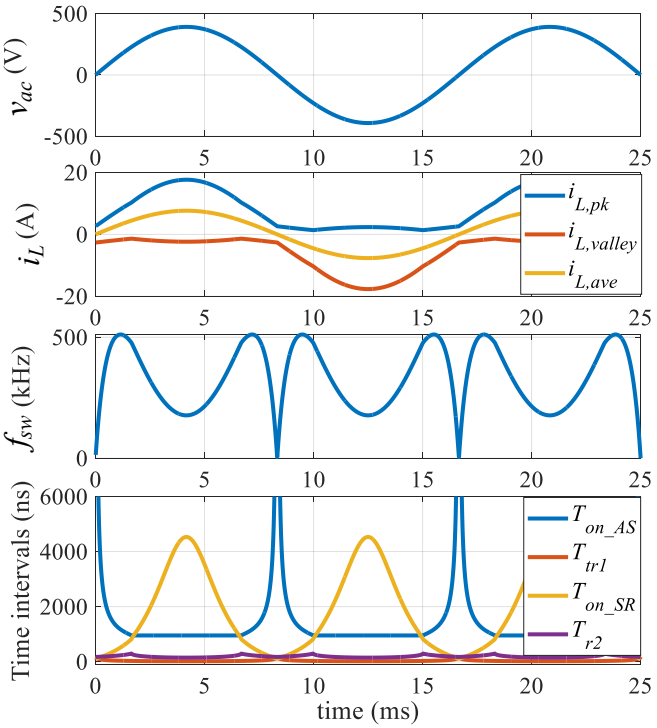
Positive half-line cycle of the input voltage

Parameter	$\mathbf{V_{in}} > \mathbf{0}, \mathbf{I_{in}} > \mathbf{0}$	$\mathbf{V_{in}} > \mathbf{0}, \mathbf{I_{in}} < \mathbf{0}$
Active switch	S_2	S_2
Synchronous switch	S_1	S_1
AS natural ZVS region	$V_{in} \leq V_{bound}, \quad V_{bound} = \frac{V_o}{k_0+1}$	all range
SS natural ZVS region	all range	$V_{in} \geq V_{bound}, \quad V_{bound} = \frac{k_0 V_o}{k_0+1}$
Full-range ZVS constraint	$k = \begin{cases} \frac{V_o - V_{in}}{V_{in}}, & V_{in} \leq V_{bound} \\ k_0, & V_{in} > V_{bound} \end{cases}$	$k = \begin{cases} \frac{V_{in}}{V_o - V_{in}}, & V_{in} \geq V_{bound} \\ k_0, & V_{in} < V_{bound} \end{cases}$
Extended conduction time	$T_{ex\_SS} = \frac{\sqrt{(k^2-1)V_{in}^2 - V_o^2 + 2V_o V_{in}}}{w_r(V_o - V_{in})}$	$T_{ex\_AS} = \frac{\sqrt{(k^2-1)V_{in}^2 + V_o^2 - 2V_o V_{in}}}{w_r V_{in}}$

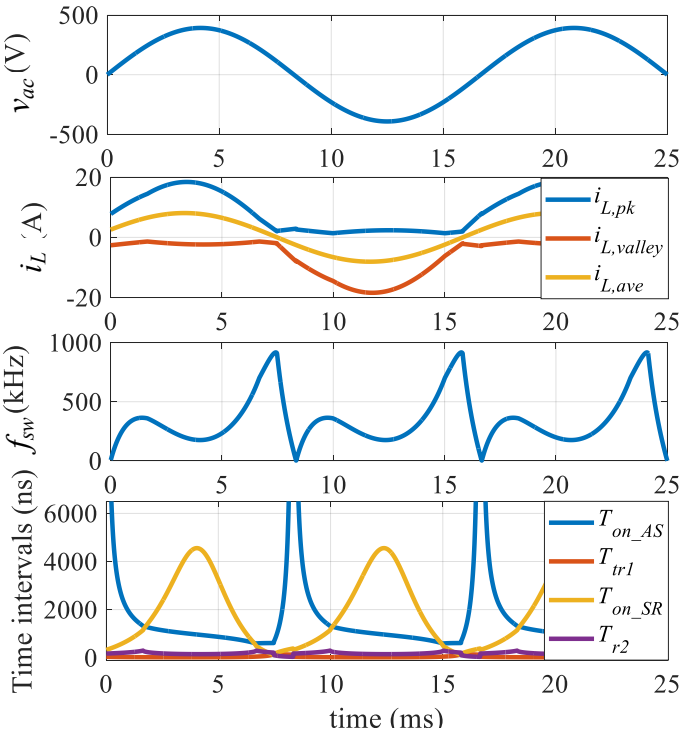
Negative half-line cycle of the input voltage

Parameter	$\mathbf{V_{in}} < \mathbf{0}, \mathbf{I_{in}} > \mathbf{0}$	$\mathbf{V_{in}} < \mathbf{0}, \mathbf{I_{in}} < \mathbf{0}$
Active switch	S_1	S_1
Synchronous switch	S_2	S_2
AS natural ZVS region	all range	$-V_{in} \leq V_{bound}, \quad V_{bound} = \frac{V_o}{k_0+1}$
SS natural ZVS region	$-V_{in} \geq V_{bound}, \quad V_{bound} = \frac{k_0 V_o}{k_0+1}$	all range
Full-range ZVS constraint	$k = \begin{cases} \frac{-V_{in}}{V_o + V_{in}}, & -V_{in} \geq V_{bound} \\ k_0, & -V_{in} < V_{bound} \end{cases}$	$k = \begin{cases} \frac{V_{in} + V_o}{-V_{in}}, & -V_{in} \leq V_{bound} \\ k_0, & -V_{in} > V_{bound} \end{cases}$
Extended conduction time	$T_{ex\_SS} = \frac{\sqrt{(k^2-1)V_{in}^2 + V_o^2 + 2V_o V_{in}}}{-w_r V_{in}}$	$T_{ex\_AS} = \frac{\sqrt{(k^2-1)V_{in}^2 - V_o^2 - 2V_o V_{in}}}{w_r(V_o + V_{in})}$

* ω_r is the resonance angular frequency, designated as $w_r^2 = {}^1/_{(2C_{oss}L_b)}$;



(a)



(b)

Figure 6.5: Ideal waveforms of the CRM totem-pole rectifier with (a) unity PF; (b) 0.948 leading PF with $Q = -500$ VAr, when $V_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}, $P = 1.5$ kW.

6.2.3 Ac Line Zero-Crossing Challenges

6.2.3.1 Frequency Limitation at Ac Current Zero-Crossing

One issue of the the CRM totem-pole rectifier with non-unity PF operation is the high peak switching frequency f_{sw} during the ac current zero-crossing. This is because the zero-crossing points of i_{in} and v_{in} are no longer at the same moment. During the ac current zero-crossing, v_{in} is not zero, leading to very high switching frequency to maintain the CRM operation. The peak switching frequency further increases with higher reactive power and lower PF. Such high switching frequency would result in higher switching loss and gate drive loss.

A frequency limitation method is proposed to reduce the peak frequency by modifying the ZVS margin constraint k. To simplify the calculation of switching period t_{sw}, the inductor current is approximated as a triangular waveform with linear increase from $i_{L,valley}$ to $i_{L,pk}$ and linear decrease from $i_{L,pk}$ to $i_{L,valley}$. Thus, the switching period is expressed as

$$t_{sw} = \frac{1}{f_{sw}} \approx L_b \frac{i_{L,pk} - i_{L,valley}}{v_{L,rise}} + L_b \frac{i_{L,pk} - i_{L,valley}}{-v_{L,fall}} \tag{6.10}$$

where $v_{L,rise} > 0, v_{L,fall} < 0$ are the voltages applied on the inductor during i_L rising and falling, *e.g.,* during the positive half-line cycle, $v_{L,rise} = V_{in}, v_{L,fall} = V_{in} - V_o$. Assume f_{smax} is the allowable maximum switching frequency, f_s should be lower than f_{smax}, that is

$$t_{sw} \geq \frac{1}{f_{smax}} \tag{6.11}$$

Combining (6.10) and (6.11), the required inductor current ripple is

$$i_{L,pk} - i_{L,valley} \geq \frac{-v_{L,rise} v_{L,fall}}{L_b f_{smax} (v_{L,rise} - v_{L,fall})} \tag{6.12}$$

Since $i_{L,pk} + i_{L,valley} = 2i_{L,ave} \approx 2i_{in}$, together with (6.12), the inductor current limit is

$$i_{L,pk} \geq i_{in} + \frac{-v_{L,rise} v_{L,fall}}{2L_b f_{smax} (v_{L,rise} - v_{L,fall})} \tag{6.13}$$

or

$$i_{L,valley} \leq i_{in} - \frac{-v_{L,rise}v_{L,fall}}{2L_b f_{smax}(v_{L,rise} - v_{L,fall})} \tag{6.14}$$

When $i_{in} > 0$, $i_{L,valley} = {}^{-kv_{rise}}/_{Z_n}$. Inserting $i_{L,valley}$ into (6.14), the ZVS constraint k for frequency limitation is solved as

$$k \geq k_{lim} = (i_{in} + \frac{v_{L,rise}v_{L,fall}}{2L_b f_{smax}(v_{L,rise} - v_{L,fall})})\frac{Z_n}{-v_{L,rise}}, \qquad for\ i_{in} > 0 \tag{6.15}$$

Similarly, when $i_{in} < 0$, $i_{L,pk} = {}^{-kv_{fall}}/_{Z_n}$. Inserting $i_{L,pk}$ into (6.13), the ZVS constraint k for frequency limitation is solved as

$$k \geq k_{lim} = (i_{in} - \frac{v_{L,rise}v_{L,fall}}{2L_b f_{smax}(v_{L,rise} - v_{L,fall})})\frac{Z_n}{-v_{L,fall}}, \qquad for\ i_{in} < 0 \tag{6.16}$$

To limit the switching frequency below f_{smax}, k cannot be lower than k_{lim}. Similar analysis is also applied for the negative half cycle, and Table 6.6 shows the values of k_{lim} in the four quadrants of V_{in}, I_{in} for the frequency limitation.

Figure 6.6 show the operation waveforms of the CRM totem-pole rectifier at non-unity PF, where the peak frequency is limited below 800 kHz.

6.2.3.2 Current Distortion at Ac Voltage Zero-Crossing

Another issue of the non-unity PF operation is the current distortion during ac voltage zero-crossing. As shown in Figure 6.6, the conduction time T_{on_AS} becomes very long and f_{sw} decreases to almost zero during v_{ac} zero-crossing. This is because with the unipolar modulation, the voltage applied on the inductor is v_{in} when the active switch is on, and this voltage is extremely low near the zero-crossing region, leading to a long conduction time. Also, Si devices need to be switched exactly at v_{in} zero-crossing point, and the GaN device duty cycle shifts from almost 100% to nearly 0%.

Table 6.6: ZVS constraint k with frequency limitation of the CRM totem-pole rectifier.

Positive half-line cycle of the input voltage		
	$\mathbf{V_{in} > 0, I_{in} > 0}$	$\mathbf{V_{in} > 0, I_{in} < 0}$
V_{rise}	V_{in}	V_{in}
V_{fall}	$V_{in} - V_o$	$V_{in} - V_o$
k_{lim}	$(I_{in} + \frac{V_{L,rise}V_{L,fall}}{2L_b f_{smax}(V_{L,rise}-V_{L,fall})})\frac{Z_n}{-V_{L,rise}}$	$(I_{in} - \frac{V_{L,rise}V_{L,fall}}{2L_b f_{smax}(V_{L,rise}-V_{L,fall})})\frac{Z_n}{-V_{L,fall}}$
Negative half-line cycle of the input voltage		
	$\mathbf{V_{in} < 0, I_{in} > 0}$	$\mathbf{V_{in} < 0, I_{in} < 0}$
V_{rise}	$V_{in} + V_o$	$V_{in} + V_o$
V_{fall}	V_{in}	V_{in}
k_{lim}	$(I_{in} - \frac{V_{L,rise}V_{L,fall}}{2L_b f_{smax}(V_{L,rise}-V_{L,fall})})\frac{Z_n}{-V_{L,fall}}$	$(I_{in} + \frac{V_{L,rise}V_{L,fall}}{2L_b f_{smax}(V_{L,rise}-V_{L,fall})})\frac{Z_n}{-V_{L,rise}}$

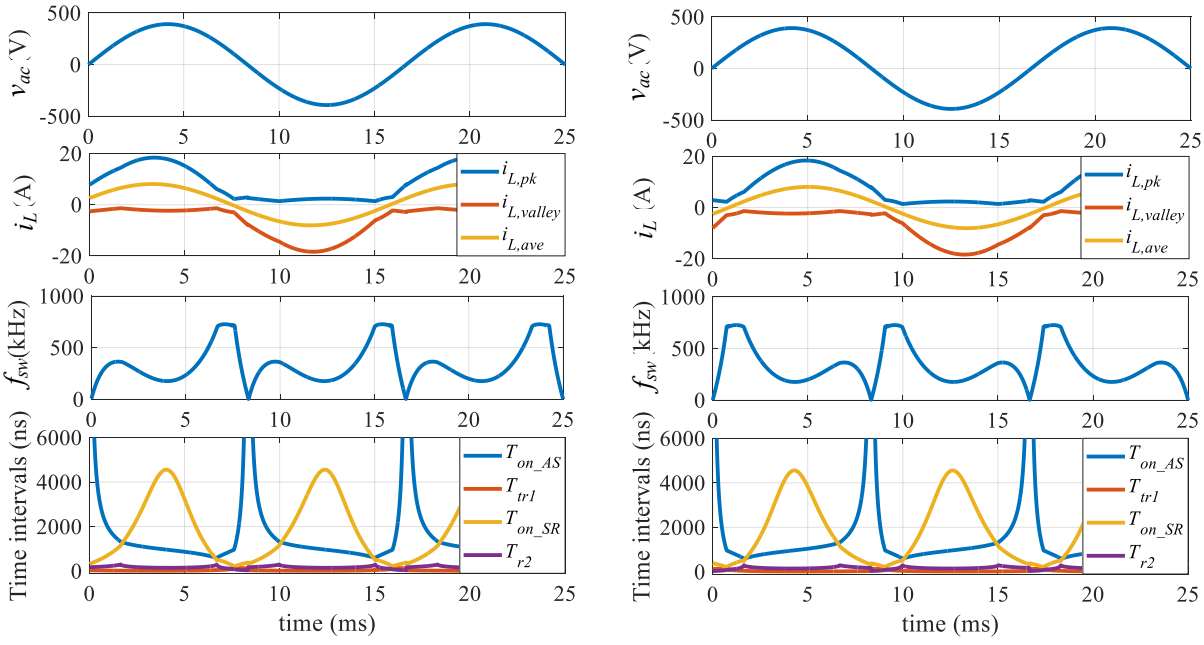


Figure 6.6: Ideal waveforms of the CRM totem-pole rectifier with peak frequency limitation at (a) 0.948 leading PF with $Q = -500$ VAr; (b) 0.948 lagging PF with $Q = 500$ VAr, when $V_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}, $P = 1.5$ kW.

Practical implementation of accurate devices' switching during the ac voltage zero-crossing is difficult. As discussed in Chapter 5, small delays, switching noise, limited dv/dt, and input voltage PLL error cause the Si device switching to not be perfectly synchronized to the input voltage zero-crossing. Consequently, the inductor voltage cannot be controlled following the unipolar modulation, and large inductor current spike or instability occurs when the polarity of the input voltage is not matched to the Si device switching state. To achieve a stable zero-crossing transition, a specified device switching sequence with a blanking time is adopted in the totem-pole PFC rectifier.

Nevertheless, the blanking-time approach is not applicable in the case with reactive power operation. Figure 6.7 shows the simulation results of the CRM totem-pole rectifier with leading PF, and the blanking time is implemented during the voltage zero-crossing. Since the input current is not zero, during the blanking time, inductor current suddenly drops to zero and the input current abruptly changes to be equal to the current flowing through the input capacitor, leading to observable input current distortion.

Figure 6.8 shows the input current THD of the CRM totem-pole rectifier with blanking time during the voltage zero-crossing. When the blanking time is set to 200 μs, the current THD with reactive power exceeds the standard significantly, as shown in Figure 6.8(a). One approach to remedy the current THD is decreasing the blanking time. As presented in Figure 6.8(b), the current THD with blanking time at 30 μs remains below the standard at all loadings. However, it is difficult to implement such small blanking time, hindered by the voltage sensing accuracy and the device switching performance with parasitic parameters. Advanced voltage sensing circuit with precise detection of small signal during the zero-crossing region and wide-range signal detection over the line cycle is required, which increases the design complexity and cost. Also, even if the small banking time is implemented, current spike or instability during the voltage zero-crossing cannot be avoided due to the non-ideal switching performance with parasitic parameters. Therefore, an alternative solution is required to overcome the voltage zero-crossing issue of the GaN-based CRM totem-pole rectifier during non-unity PF operation.

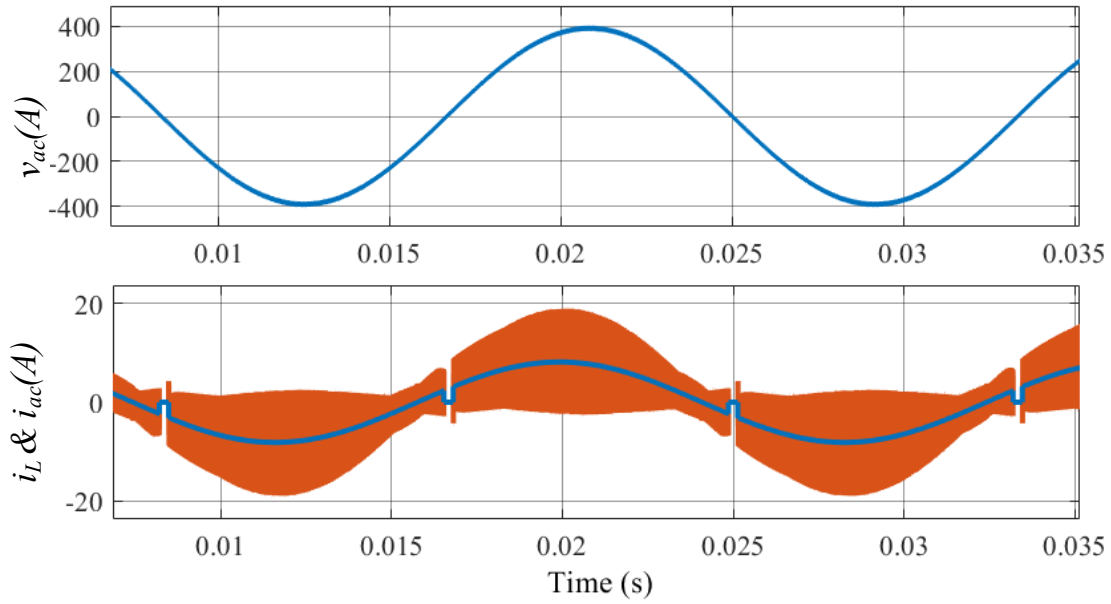


Figure 6.7: Simulation waveforms of the CRM totem-pole rectifier at 0.948 leading power factor with 200 μs blanking time during the input voltage zero-crossing when $v_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}, $P = 1.5$ kW, $Q = -500$ VAr.

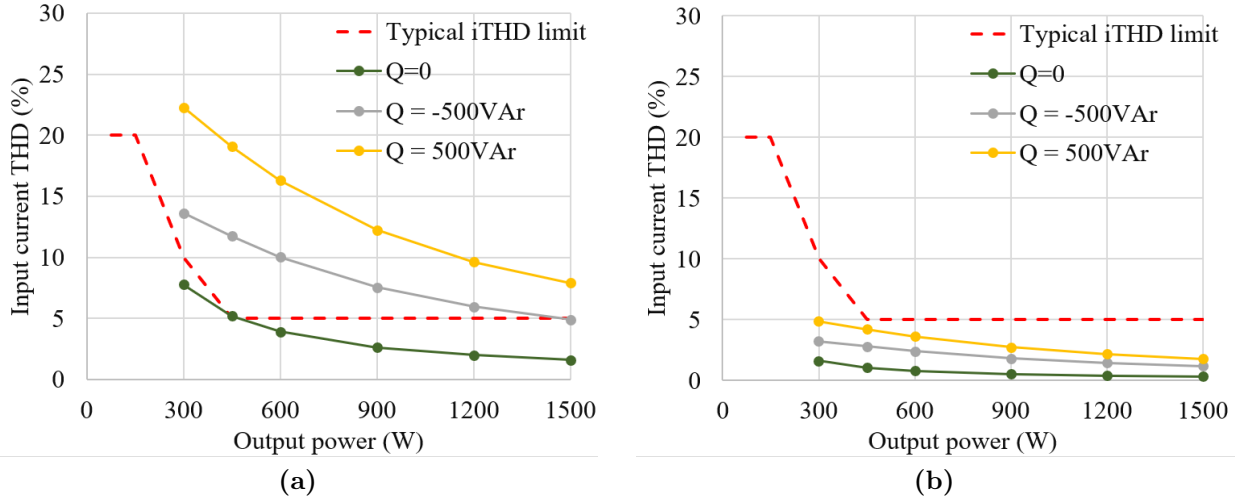


Figure 6.8: Input current THD of the CRM totem-pole rectifier at various power levels with (a) 200 μs blanking time; (b) 30 μs blanking time, when $V_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}.

6.3 Rectifier Topology Selection

For the CRM totem-pole rectifier in unipolar modulation, large current spike or instability occurs during the voltage zero-crossing, and severe current distortion is caused with blanking time approach. If the Si MOSFETs' switching is independent of the input voltage zero-crossing and the inductor voltage is controlled, the instability and current distortion issue will be eliminated. Therefore, changing the modulation method of the rectifier is one way to overcome the voltage zero-crossing challenge. In this section, two rectifier topologies with different modulations are evaluated. One is the CRM dual boost full-bridge (DBFB) rectifier with bipolar modulation, the other is the CRM T-type totem-pole rectifier which changes the modulation only during the voltage zero-crossing region.

6.3.1 Dual Boost Full-Bridge (DBFB) Rectifier

Figure 6.9 shows the dual-boost full-bridge (DBFB) rectifier, which splits the full-bridge rectifier into two identical boost phases by using high-frequency input capacitors $C_1 - C_4$. The two boost inductors are symmetrical with $L_{b1} = L_{b2} = 0.5L_b$. The first boost phase's input voltage v_{inL} is the differential voltage between the grid line terminal v_{Line} and the power ground P_{GND}. Thus, it is named as the Line boost phase. Similarly, the second boost phase is called the Neutral boost phase.

Assume $v_{Line} = 0.5(v_{in} + V_o)$, $v_{Neutral} = 0.5(V_o - v_{in})$, then $v_{in} = v_{Line} - v_{Neutral}$. During v_{in} positive half-line cycle, S_2, S_3 are AS devices, S_1, S_4 are SS devices, and $v_{inL} = v_{Line} = 0.5(v_{in} + V_o), v_{inN} = V_o - v_{Neutral} = 0.5(v_{in} + V_o)$. During the negative half-line cycle, S_1, S_4 are AS devices, S_2, S_3 are SS devices, and $v_{inL} = V_o - v_{Line} = 0.5(V_o - v_{in}), v_{inN} = v_{Neutral} = 0.5(V_o - v_{in})$. Therefore, input voltages of the two boost phases are the same within the whole line cycle, which are always higher than $0.5V_o$, as shown in Figure 6.10.

Different from the unipolar modulated totem-pole rectifier, the DBFB rectifier operates with bipolar modulation, where $S_1 - S_4$ are all fast-switched devices, and $S_1\&S_4$ have the same switching actions as well as $S_2\&S_3$. When $S_1\&S_4$ conduct, $v_L = 0.5(v_{in} - V_o) < 0$, the inductor is discharged. When $S_2\&S_3$ are ON, $v_L = 0.5(v_{in} + V_o) > 0$, the inductor is charged.

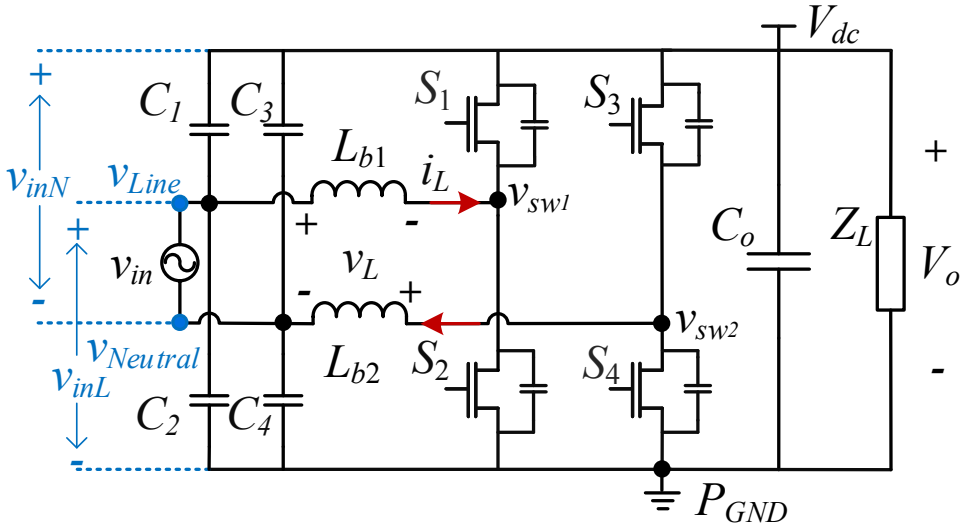


Figure 6.9: Topology of the dual-boost full-bridge (DBFB) rectifier.

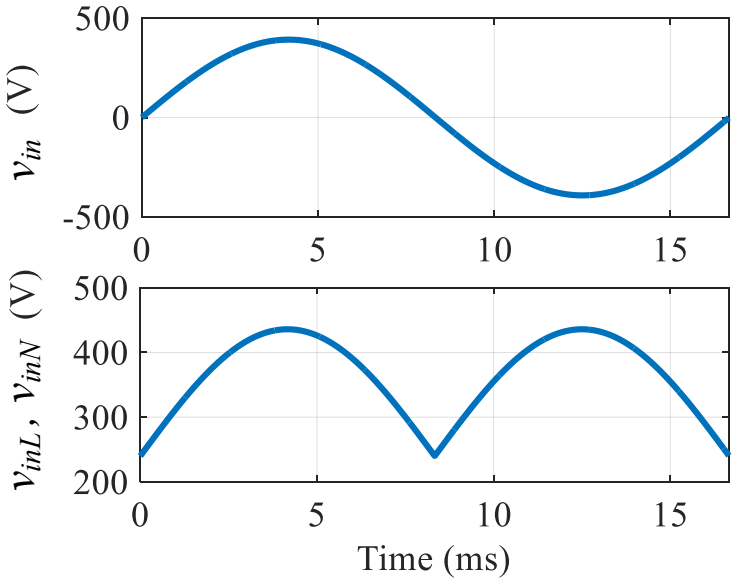


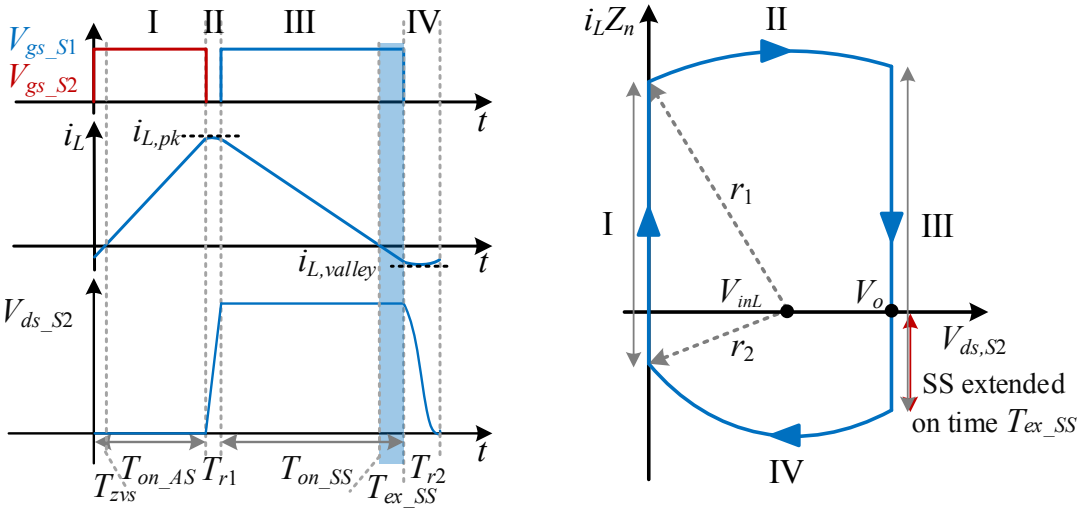
Figure 6.10: Input voltage of the DBFB rectifier with $v_{in} = 277$ V_{ac}, 60 Hz, $V_o = 480$ V.

Because of the symmetrical characteristics between the two boost phases and between the two half-line cycles, ZVS operation is analyzed based on the Line boost phase during the positive half line cycle. In order to analyze the state-plane trajectories, the characteristic impedance Z_n is defined as $Z_n^2 = {}^{0.5L_b}/_{(2C_{oss})}$, where C_{oss} is the equivalent drain-to-source capacitance of S_1 and S_2, assuming $C_{oss,S1} = C_{oss,S2} = C_{oss}$. The resonant angular frequency is designated as $\omega^2 = {}^{1}/_{C_{oss}L_b}$.

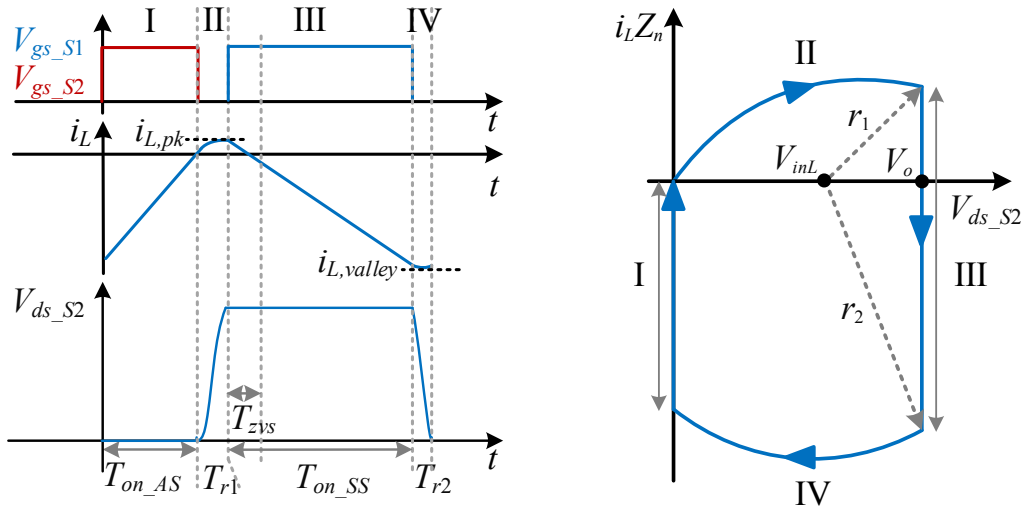
Figure 6.11 shows the switching waveforms and state-plane trajectories of the DBFB rectifier with ZVS operation during the positive half-line cycle. The dc solution of the state plane for ZVS analysis is $(V_{inL}, 0)$, where $V_{inL} = 0.5(V_o + V_{in}) \geq 0.5V_o$. When $V_{in} > 0, I_{in} > 0$ (Figure 6.11(a)), the SS device S_1 achieves ZVS naturally, but AS device S_2 can only realize valley switching since $V_{inL} \geq 0.5V_o$. To realize ZVS turn-ON, conduction time of the SS device is extended to obtain a lower negative current, and the ZVS margin constraint is defined as $k = {}^{r_2}/_{V_{inL}} = k_0 > 1$. When $V_{in} > 0, I_{in} < 0$ (Figure 6.11(b)), both AS and SS devices achieve ZVS naturally. ZVS extension is not required, and $k = {}^{r_2}/_{V_{inL}} = 1$. To be more clear, Table 6.7 summarizes the ZVS modulation principle of the CRM DBFB rectifier. Compared with the bipolar totem-pole rectifier, the ZVS extension is only required when V_{in}, I_{in} have the same polarity.

Figure 6.12 presents the ideal waveforms of the DBFB rectifier with unity PF and leading PF. Similarly, peak switching frequency occurs at the current zero-crossing. To limit the maximum frequency, the proposed frequency limitation method by modifying the ZVS coefficient k is adopted, and Figure 6.13 displays the waveforms with peak frequency at 800 kHz.

Because of the bipolar modulation, issues like extreme low frequency and current instability are avoided during the voltage zero-crossing region, and blanking time is not needed, resulting in a better current THD. However, due to higher average frequency and inductor current ripple, the bipolar DBFB rectifier usually suffers from higher power loss in comparison to the unipolar totem-pole rectifier. To enable fast switching frequency and reduce the converter loss, GaN devices are required for all switches, which increases the converter cost.



(a)



(b)

Figure 6.11: ZVS waveforms and state plane trajectories of the DBFB rectifier in the positive half line cycle with (a) $V_{in} > 0, I_{in} > 0$; (b) $V_{in} > 0, I_{in} < 0$.

Table 6.7: Full-line-cycle ZVS principle of the CRM DBFB rectifier.

Positive half-line cycle of the input voltage

Parameter	$\mathbf{V_{in} > 0, I_{in} > 0}$	$\mathbf{V_{in} > 0, I_{in} < 0}$
Active switch	S_2, S_3	S_2, S_3
Synchronous switch	S_1, S_4	S_1, S_4
AS natural ZVS region	no range	all range
SS natural ZVS region	all range	all range
Full-range ZVS constraint	$k = k_0$	$k = 1$
Extended conduction time	$T_{ex\_SS} = \frac{\sqrt{k^2(V_{in}+V_o)^2-(V_o-V_{in})^2}}{w_r(V_o-V_{in})}$	$T_{ex\_AS} = 0$

Negative half-line cycle of the input voltage

Parameter	$\mathbf{V_{in} < 0, I_{in} > 0}$	$\mathbf{V_{in} < 0, I_{in} < 0}$
Active switch	S_1, S_4	S_1, S_4
Synchronous switch	S_2, S_3	S_2, S_3
AS natural ZVS region	all range	no range
SS natural ZVS region	all range	all range
Full-range ZVS constraint	$k = 1$	$k = k_0$
Extended conduction time	$T_{ex\_AS} = 0$	$T_{ex\_SS} = \frac{\sqrt{k^2(-V_{in}+V_o)^2-(V_o+V_{in})^2}}{w_r(V_o+V_{in})}$

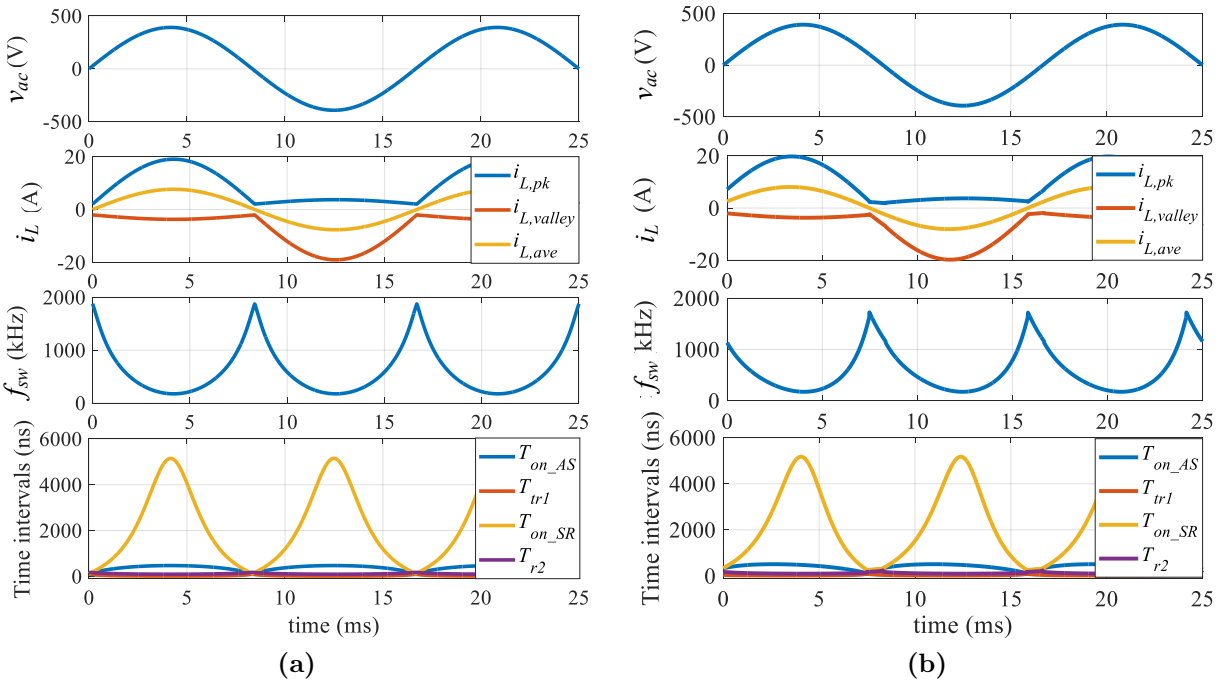


Figure 6.12: Waveforms of the CRM DBFB rectifier at (a) unity PF; (b) 0.948 leading PF with $Q = -500$ VAr, when $V_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}, $P = 1.5$ kW.

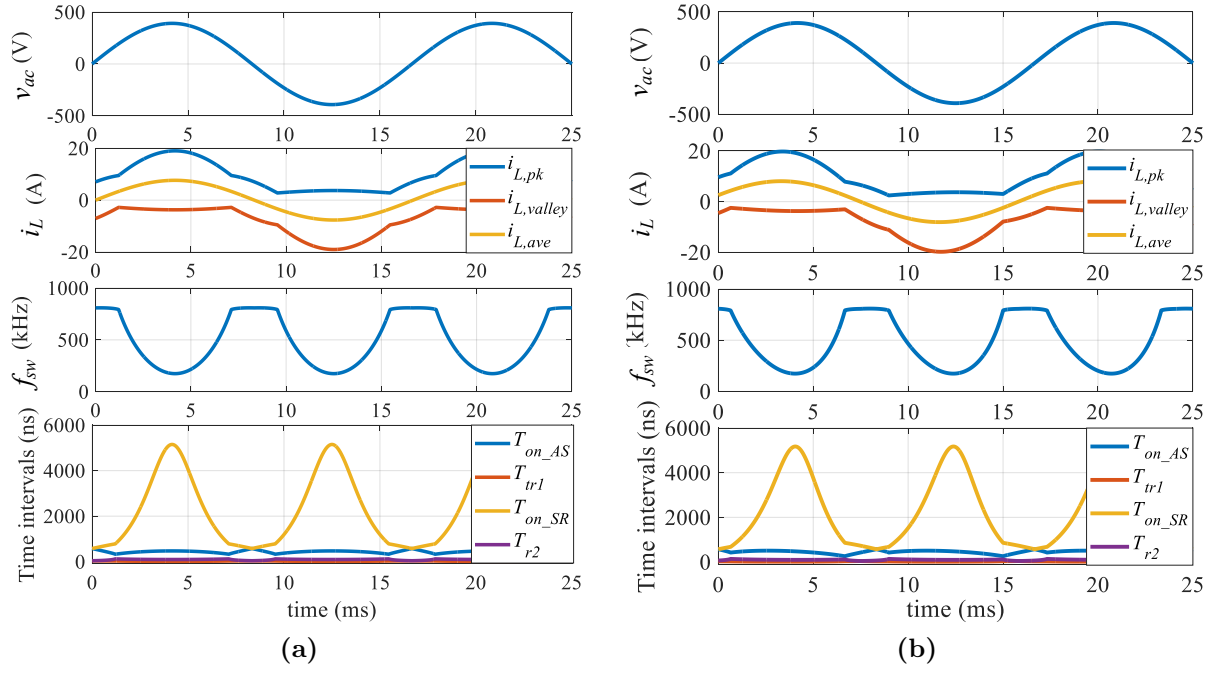


Figure 6.13: Waveforms of the CRM DBFB rectifier with peak frequency limitation at (a) unity PF; (b) 0.948 leading PF with $Q = -500$ VAr, when $V_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}, $P = 1.5$ kW.

6.3.2 T-Type Totem-Pole Rectifier

To overcome the voltage zero-crossing issue, a modified totem-pole rectifier is proposed, as shown in Figure 6.14. A bidirectional switch that is composed of two anti-series connected Si MOSFETs is inserted between the Si phase leg switching node and the dc capacitor middle point. Since a T-type structure is constructed, the topology is called T-type totem-pole rectifier. During the voltage zero-crossing region, Si devices S_3, S_4 are turned OFF, and the bidirectional switch S_5 is turned ON.

Figure 6.15 illustrates the device switching pattern of the T-type totem-pole rectifier. An intermediate boundary voltage V_{boun} is defined to distinguish the two operation modes. When $|V_{in}| > V_{boun}$, the rectifier operates in the normal totem-pole mode with unipoloar modulation. Bidirectional switch S_5 remains OFF, S_3 conducts during the negative half cycle, and S_4 conducts during the positive half cycle. S_1, S_2 switch at high frequency with the same ZVS modulation in the CRM totem-pole rectifier as shown in Table 6.5. When $|V_{in}| \leq V_{boun}$, the rectifier switches to T-type mode. S_5 is ON and S_3, S_4 are OFF. S_1, S_2 are still high switching devices. Since T-type mode is only adopted during the voltage zero-crossing region, V_{boun} is typically small, *e.g.,* $V_{boun} \leq 0.25V_o$. Hence, during the T-type mode, the inductor is charged when S_2 conducts with $v_L = V_{in} + 0.5V_o > 0$, and the inductor is discharged when S_1 is ON with $v_L = V_{in} - 0.5V_o < 0$.

To maintain the full-range ZVS operation, ZVS modulation during the T-type mode is investigated. Figure 6.16 shows the equivalent circuit during the resonance in the T-type mode, where the voltage across the dc capacitor is represented by a constant voltage source equal to $0.5V_o$, and $2C_{oss}$ is the equivalent output capacitance of S_1, S_2. When $V_{boun} \geq V_{in} > 0$, S_2 is the AS device, and the dc voltage applied on $2C_{oss}$ is $V_{dc} = V_{in} + 0.5V_o > 0.5V_o$. When $-V_{boun} \leq V_{in} < 0$, S_1 is the AS device, and the dc voltage across $2C_{oss}$ is $V_{dc} = -V_{in} + 0.5V_o > 0.5V_o$. Therefore, the dc solution of the state plane for ZVS analysis is $(|V_{in}| + 0.5V_o,\ 0)$.

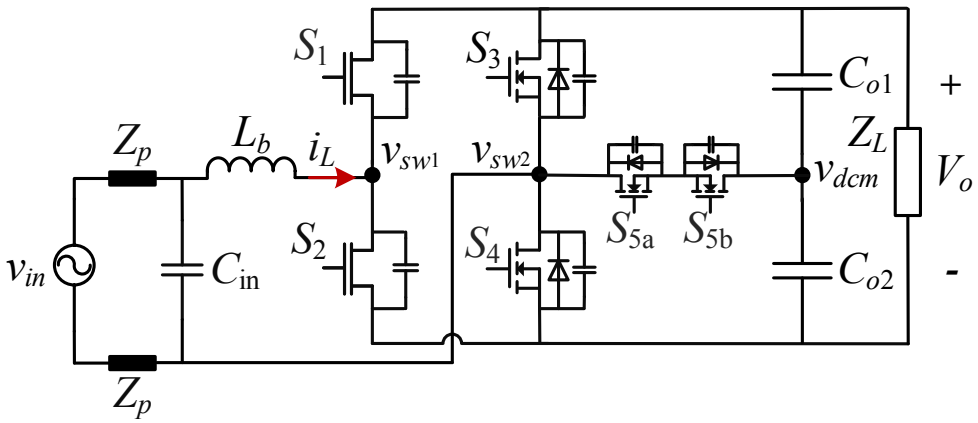


Figure 6.14: Topology of the T-type totem-pole rectifier.

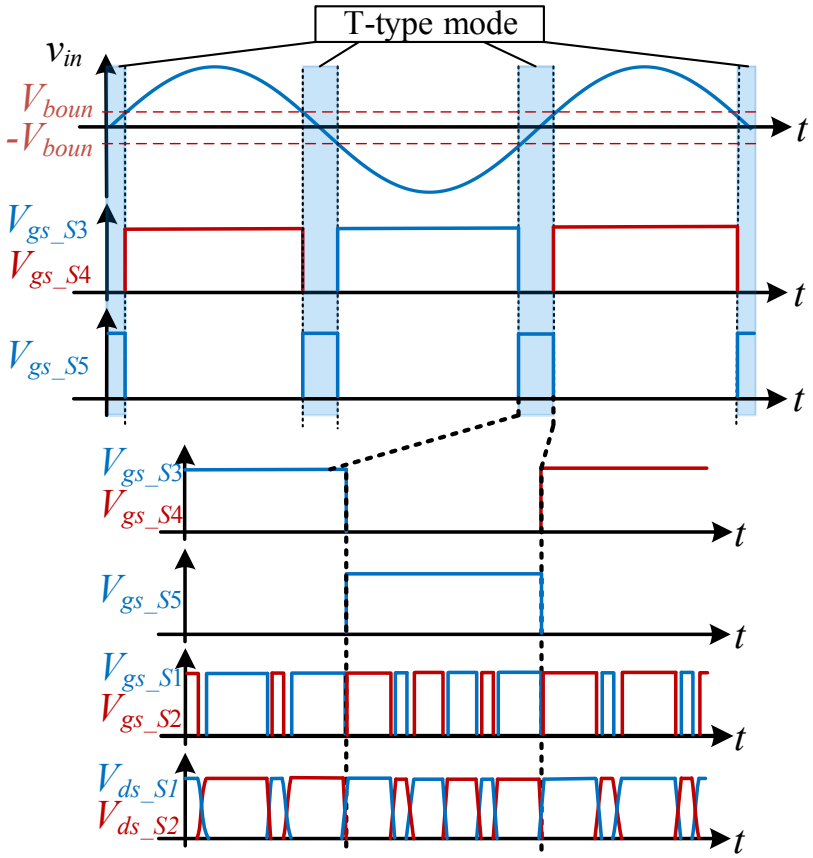


Figure 6.15: Device switching sequence of the T-type totem-pole rectifier.

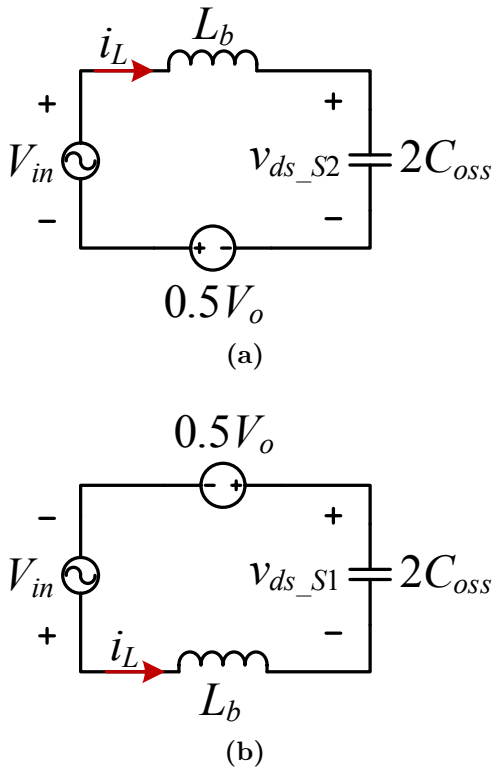


Figure 6.16: Resonant equivalent circuits of the T-type totem-pole rectifier during the T-type mode when (a) $V_{boun} \geq V_{in} > 0$; (b) $-V_{boun} \leq V_{in} < 0$.

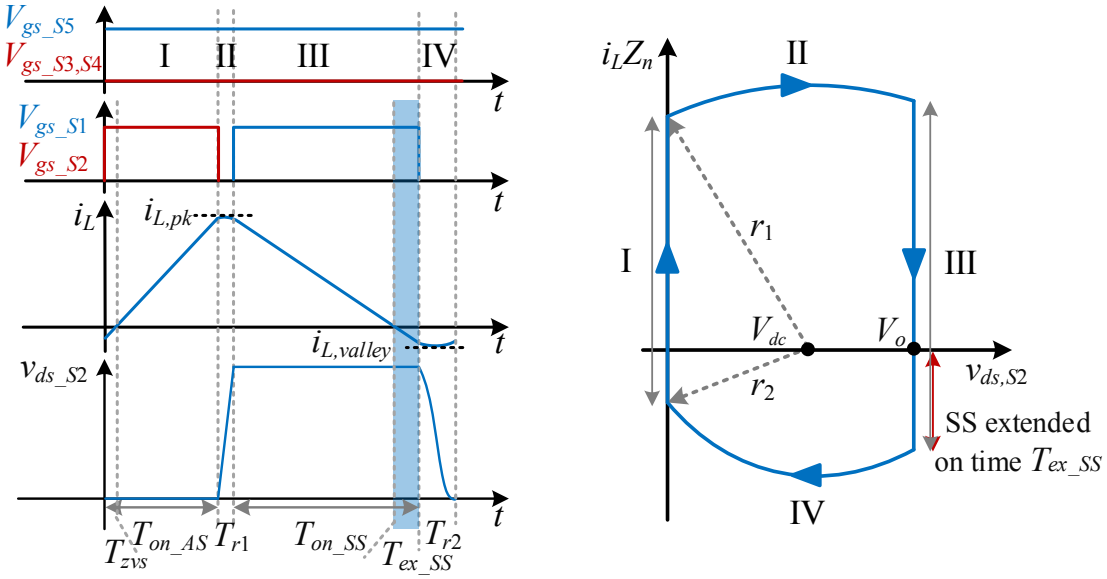
Figure 6.17 presents the switching waveforms and state-plane trajectories of the T-type totem-pole rectifier during the T-type mode with positive V_{in}, where $Z_n^2 = {}^{L_b}/_{(2C_{oss})}$, $w_r^2 = {}^{1}/_{(2C_{oss}L_b)}$. Similar with the DBFB rectifier, when $V_{in} > 0, I_{in} > 0$ (Figure 6.17(a)), SS device realizes ZVS naturally, but AS device can only achieve valley switching because $V_{dc} = |V_{in}| + 0.5V_o \geq 0.5V_o$. Therefore, ZVS extension is required by increasing the conduction time of the SS device. When $V_{in} > 0, I_{in} < 0$ (Figure 6.17(b)), both AS device and SS device can achieve ZVS turn-ON without ZVS extension.

Considering the peak frequency limitation, ZVS operation principle during the T-type mode of the rectifier is summarized in Table 6.8. Figure 6.18 shows the line-cycle waveforms of the T-type totem-pole rectifier under unity PF and leading PF. With the intermediate boundary voltage V_{boun}, T-type mode operation time can be set much longer than traditional blanking time. Also, during the T-type mode, the inductor voltage is dominated by the output voltage and is always under control. Hence, v_{ac} zero-crossing detection is not required and the ac voltage zero-crossing issue of the totem-pole rectifier is avoided.

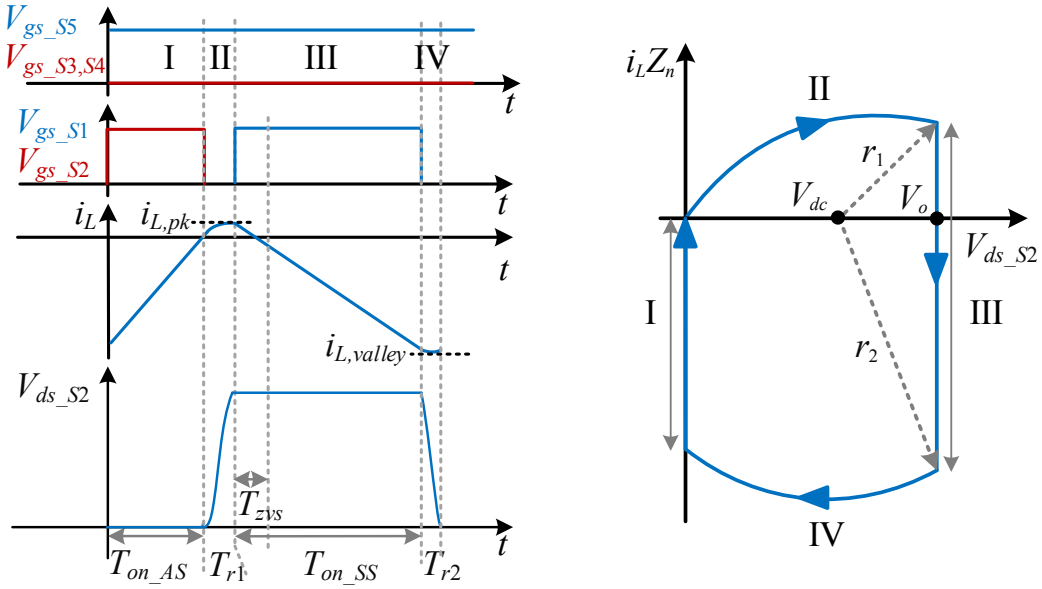
6.3.3 Performance Comparison

To compare the topologies discussed above, converter cost and power loss are predicted. Table 6.9 and Table 6.10 present the design of the GaN-based CRM DBFB rectifier and the GaN-based CRM T-type totem-pole rectifier with $V_{in} = 277$ $\mathrm{V_{ac}}, V_o = 480$ $\mathrm{V_{dc}}, S_{rate} =$ 1.6 kVA. Converter cost is estimated based on the major components, including GaN and Si devies, gate drive circuits, inductor, capacitors, controller, and current sensing circuit. The DBFB rectifier has higher total cost mainly because more GaN devices are required.

Based on the power loss model (Appendix A), the full-load power losses of the CRM totem-pole rectifier, CRM DBFB rectifier, and the CRM T-type totem-pole rectifier with various reactive power are calculated. As shown in Figure 6.19, the DBFB rectifier exhibits the highest loss in all cases. Although the totem-pole rectifier has the lowest loss, the voltage zero-crossing issue hinders the practical implementation. The proposed T-type totem-pole rectifier has slightly higher power loss than the totem-pole rectifier, however, it remedies the voltage zero-crossing problem. Therefore, the T-type totem-pole topology is selected for the rectifier to perform the reactive power regulation in data centers.



(a)



(b)

Figure 6.17: ZVS waveforms and state-plane trajectories of the T-type totem-pole rectifier during the T-type mode when (a) $V_{boun} \geq V_{in} > 0, I_{in} > 0$; (b) $V_{boun} \geq V_{in} > 0, I_{in} < 0$.

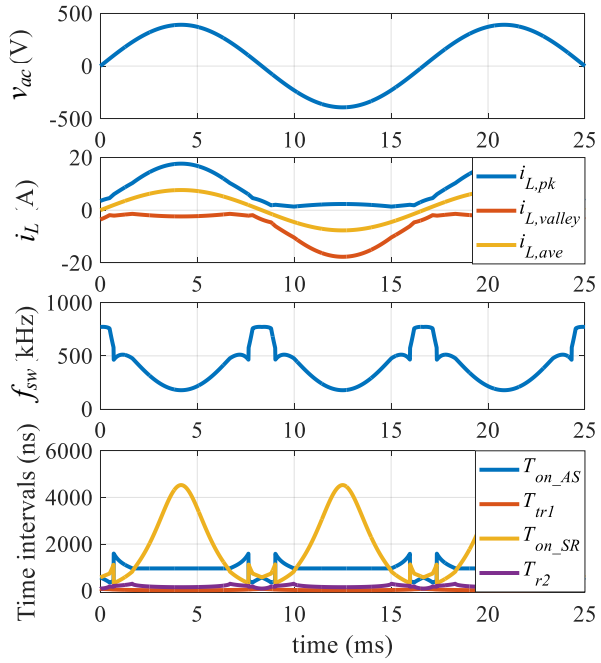
Table 6.8: ZVS principle of the CRM T-type totem-pole rectifier during T-type mode.

Positive half-line cycle of the input voltage

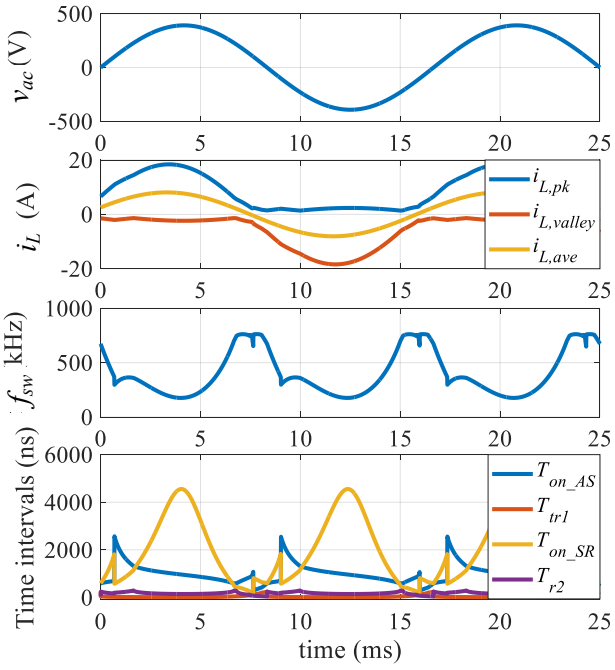
Parameter	$\mathbf{V_{boun} \geq V_{in} > 0, I_{in} > 0}$	$\mathbf{V_{boun} \geq V_{in} > 0, I_{in} < 0}$
Active switch (AS)	S_2	S_2
Synchronous switch (SS)	S_1	S_1
AS natural ZVS region	no range	all range
SS natural ZVS region	all range	all range
ZVS constraint	$k = \max\{k_0, k_{lim}\}$	$k = \max\{1, k_{lim}\}$
Extended on time	$T_{ex\_SS} = \frac{\sqrt{k^2(V_{in}+0.5V_o)^2-(0.5V_o-V_{in})^2}}{w_r(0.5V_o-V_{in})}$	$T_{ex\_AS} = 0$

Negative half-line cycle of the input voltage

Parameter	$\mathbf{-V_{boun} \leq V_{in} < 0, I_{in} > 0}$	$\mathbf{-V_{boun} \leq V_{in} < 0, I_{in} < 0}$
Active switch (AS)	S_1	S_1
Synchronous switch (SS)	S_2	S_2
AS natural ZVS region	all range	no range
SS natural ZVS region	all range	all range
ZVS constraint	$k = \max\{1, k_{lim}\}$	$k = \max\{k_0, k_{lim}\}$
Extended on time	$T_{ex\_SS} = 0$	$T_{ex\_AS} = \frac{\sqrt{k^2(-V_{in}+0.5V_o)^2-(0.5V_o+V_{in})^2}}{w_r(0.5V_o+V_{in})}$



(a)



(b)

Figure 6.18: Ideal waveforms of the CRM T-type totem-pole PFC rectifier with peak frequency limitation at (a) unity PF; (b) 0.948 leading PF with $Q = -500$ kVAr, when $V_{in} = 277$ $\mathrm{V_{ac}}$, $V_o = 480$ $\mathrm{V_{dc}}$, $V_{boun} = 100$ V, $P = 1.5$ kW.

Table 6.9: Design of CRM dual boost full-bridge (DBFB) rectifier.

Component	Part No.	Price
GaN devices $S_1 - S_4$	2-paralleled GS66508T, 650 V	$8 \times \$12.45$
Gate drive	gate driver 2×SI8273AB-IS1-2	$2 \times \$2.18$
	LDO 4×BD60GC0MEFJ	$4 \times \$0.57$
Boost inductor L_b	20 μH, powder core Mix-2-T157	\$1.5
DC capacitor C_{dc}	6×ELH687M400AT4AA, 680 μF, 400 V	$6 \times \$3.57$
Input capacitor $C_1 - C_4$	B32924B4105K000, 350 V_{ac}, 1 μF	$4 \times \$1.87$
Controller	DSP TMS320F28377S	\$15
High-speed	10 mΩ R_{shunt} LVK25R010FER	\$0.84
current sensing	comparator ADCMP601	\$2.35
	digital isolator ADUM1100	\$2.5
Low-speed	hall sensor ACS723LLCTR-40AB-T	\$1.9
current sensing	linear regulator LP2985-50DBVRG4	\$0.187
Total		\$159.42

Table 6.10: Design of CRM T-type totem-pole rectifier.

Component	Part No.	Price
GaN devices S_1, S_2	2-paralleled GS66508T, 650 V	$4 \times \$12.45$
Si devices S_3, S_4	IPW65R019C7, 650 V	$2 \times \$11.73$
Si device S_{5a}, S_{5b}	IPW60R040CFD7XKSA1, 600 V	$2 \times \$1.32$
Gate drive	gate driver 3×SI8273AB-IS1-2	$3 \times \$2.18$
	LDO 6×BD60GC0MEFJ	$6 \times \$0.57$
Boost inductor L_b	20 μH, powder core Mix-2-T157	\$1.5
DC capacitor C_{dc}	6×ELH687M400AT4AA, 680 μF, 400 V	$6 \times \$3.57$
Input capacitor C_{in}	B32924A4335M000, 350 V_{ac}, 3.3 μF	\$4
Controller	DSP TMS320F28377S	\$15
High-speed	10 mΩ R_{shunt} LVK25R010FER	\$0.84
current sensing	comparator ADCMP601	\$2.35
	digital isolator ADUM1100	\$2.5
Low-speed	hall sensor ACS723LLCTR-40AB-T	\$1.9
current sensing	linear regulator LP2985-50DBVRG4	\$0.187
Total		\$135.56

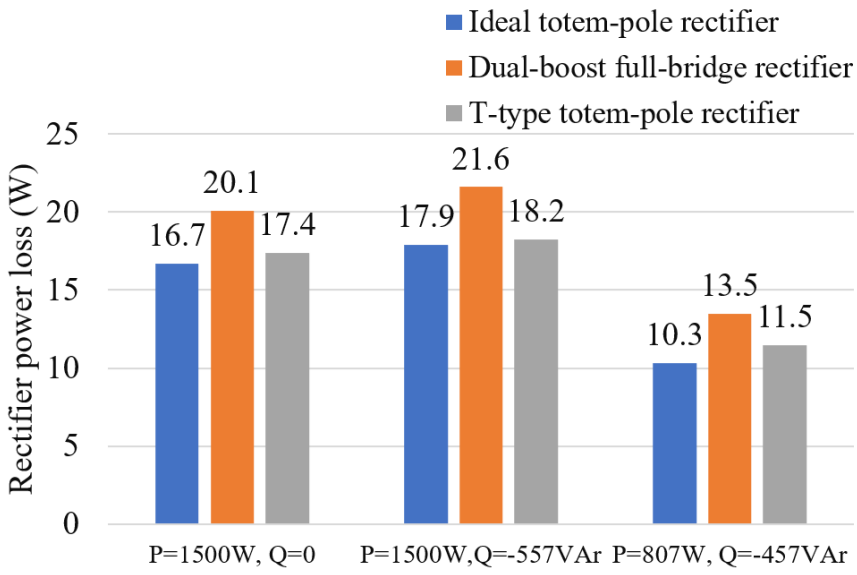


Figure 6.19: Loss comparison of the rectifiers with different reactive power at $V_{in} = 277\ \mathrm{V_{ac}}, V_o = 480\ \mathrm{V_{dc}}, V_{boun} = 100\ \mathrm{V}, S = 1.6\ \mathrm{kVA}$.

6.4 Control Implementation

6.4.1 Control Strategy

To achieve reactive power operation as well as the full-range ZVS, the current reference embedded in the model-based calculation should be adjustable according to the demanded reactive power, and a controller is required to accurately control the reactive power.

Figure 6.20 shows the proposed control strategy for the T-type totem-pole rectifier, where the active power and reactive power are decoupled and controlled in dq rotating frame. First, the single-phase input current and voltage are sensed and converted into $\alpha\beta$ frame through a second-order generalized integrator (SOGI) based orthogonal signal generator (OSG). Assuming $v_\alpha = v_{in} = \sqrt{2}V_{rms}\cos\omega t$, $i_\alpha = i_{in} = \sqrt{2}I_{rms}\cos(\omega t - \phi)$, the ideal orthogonal signals are $v_\beta = \sqrt{2}V_{rms}\sin\omega t$, $i_\beta = \sqrt{2}I_{rms}\sin(\omega t - \phi)$. Then, $\overrightarrow{v_{\alpha\beta}}$ and $\overrightarrow{i_{\alpha\beta}}$ are converted into dq rotating frame through Park transformation.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = T_{\alpha\beta-dq}\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \sqrt{2}V_{rms} \\ 0 \end{bmatrix} \tag{6.17}$$

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = T_{\alpha\beta-dq}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \sqrt{2}I_{rms}\cos\phi \\ -\sqrt{2}I_{rms}\sin\phi \end{bmatrix} \tag{6.18}$$

where $T_{\alpha\beta-dq}$ is the Park transformation with $\theta = \omega t$.

$$T_{\alpha\beta-dq} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \tag{6.19}$$

Based on $\overrightarrow{v_{dq}}$, $\overrightarrow{i_{dq}}$, the average active power P and reactive power Q are calculated in a power estimator, as

$$P = \frac{1}{2}(v_d i_d + v_q i_q) = V_{rms}I_{rms}\cos\phi \tag{6.20}$$

$$Q = \frac{1}{2}(v_q i_d - v_d i_q) = V_{rms}I_{rms}\sin\phi \tag{6.21}$$

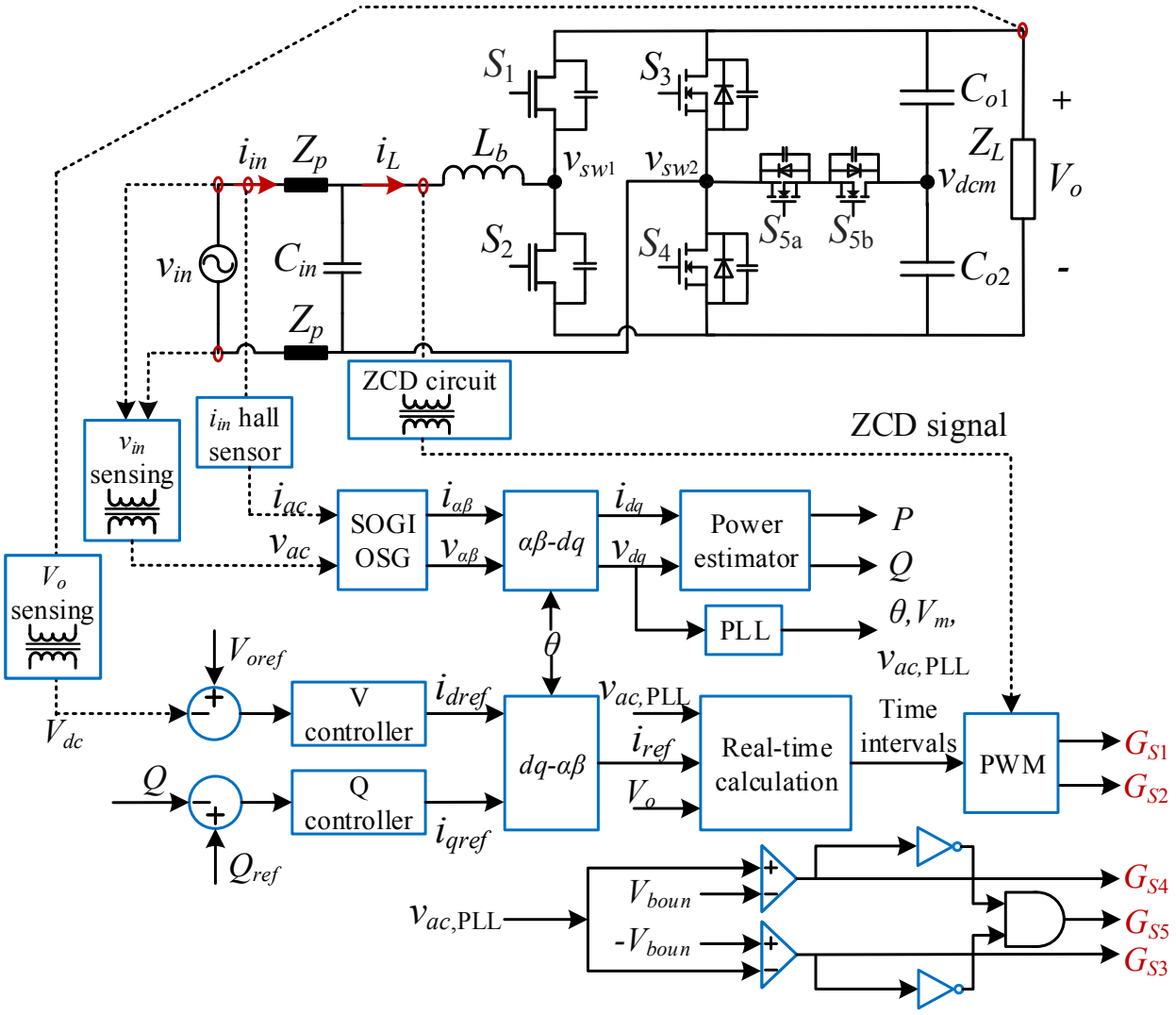


Figure 6.20: Control diagram of the T-type totem-pole rectifier with reactive power operation.

The input voltage magnitude V_m and phase angle θ are detected in a PLL, and a locked input voltage signal $v_{in,PLL}$ is generated with $v_{in,PLL} = V_m \cos\theta$ for the following control actions. Outer voltage loop is maintained in the d axis to regulate the output voltage and active power. Instead of generating the switch ON time, the voltage controller produces the d-axis current reference i_{dref}. In the q axis, the conditioned reactive power Q is used to form a reactive power loop. Q is adjusted to follow the power reference Q_{ref} by a controller, which generates the q-axis current reference i_{qref}. In order to obtain the single-phase current reference i_{ref}, i_{dref} and i_{qref} are converted back to $\alpha\beta$ frame via the inverse Park transform. Then, the current reference together with the conditioned input and output voltages are transmitted to the real-time calculation, where instantaneous switching time intervals are calculated based on the extended analytical model for full-range ZVS with reactive power operation. Synchronized with the sensed ZCD signal, gate signals of the fast-switching GaN devices S_1, S_2 are generated.

On the other hand, line-cycle switched Si MOSFETs are controlled according to the value of the conditioned input voltage $v_{in,PLL}$. A boundary voltage V_{boun} is defined to distinguish the totem-pole mode and T-type mode. When $|V_{in,PLL}| \leq V_{boun}$, S_5 is turned ON and S_3, S_4 are turned OFF to conduct the T-type mode. Otherwise, the rectifier operates in totem-pole mode with S_3 ON during the negative half-line cycle when $v_{in,PLL} < -V_{boun}$ and S_4 ON during the positive half-line cycle when $v_{in,PLL} > V_{boun}$.

6.4.2 Controller Design

As illustrated in Figure 6.20, a voltage-loop controller and a reactive power controller are required to regulate the rectifier output voltage and reactive power. Accordingly, the d-axis current-to-voltage open-loop transfer function G_{id_v} and the q-axis current-to-reactive power open-loop transfer function G_{iq_Q} need to be derived for the controller design.

Since the T-type mode is only adopted during the input voltage zero-crossing region, the rectifier can still be regarded as two boost converters working alternatively during the positive and negative half-line cycles. During the positive half-line cycle, the rectifier is

modeled as

$$\begin{cases} L_b \frac{d\bar{i}_L}{dt} = d \cdot \bar{v}_{in} + d'(\bar{v}_{in} - \bar{v}_o) \\ C_{dc} \frac{d\bar{v}_o}{dt} = d \cdot (-\frac{\bar{v}_o}{R_L}) + d'(\bar{i}_L - \frac{\bar{v}_o}{R_L}) \end{cases} \tag{6.22}$$

where $\bar{i}_L$ is the average inductor current, and $\bar{i}_L \approx \bar{i}_{in}$. d is the instantaneous duty cycle, and R_L is the load resistor. With the generated orthogonal signals, the average model is converted into $\alpha\beta$ frame as

$$\begin{cases} L_b \frac{d\overrightarrow{i_{\alpha\beta}}}{dt} = \overrightarrow{v_{\alpha\beta}} - \overrightarrow{d'_{\alpha\beta}} \bar{v}_o \\ C_{dc} \frac{d\bar{v}_o}{dt} = -\frac{\bar{v}_o}{R_L} + \overrightarrow{d'_{\alpha\beta}}^T \overrightarrow{i_{\alpha\beta}} \end{cases} \tag{6.23}$$

Further transform (6.23) into the dq frame by multiplying $T_{\alpha\beta-dq}$, the average model is

$$\begin{cases} L_b \frac{di_d}{dt} = v_d - d'_d \bar{v}_o + \omega L_b i_q \\ L_b \frac{di_q}{dt} = v_q - d'_q \bar{v}_o - \omega L_b i_d \\ C_{dc} \frac{d\bar{v}_o}{dt} = -\frac{\bar{v}_o}{R_L} + \overrightarrow{d'_{dq}}^T \overrightarrow{i_{dq}} \end{cases} \tag{6.24}$$

Implementing small-signal perturbation and linearization on (6.24), the small-signal model is

$$\begin{cases} L_b \frac{d\hat{i}_d}{dt} = \hat{v}_d - V_o \hat{d}'_d - \hat{v}_o D'_d + \omega L_b \hat{i}_q \\ L_b \frac{d\hat{i}_q}{dt} = \hat{v}_q - V_o \hat{d}'_q - \hat{v}_o D'_q - \omega L_b \hat{i}_d \\ C_{dc} \frac{d\hat{v}_o}{dt} = -\frac{\bar{v}_o}{R_L} + D'_d \hat{i}_d + \hat{d}'_d I_d + D'_q \hat{i}_q + \hat{d}'_q I_q \end{cases} \tag{6.25}$$

where $V_d, V_q, I_d, I_q, D'_d, D'_q$ are dc solutions at steady state. Based on (6.17) and (6.18), $V_d = \sqrt{2} V_{rms}$, $V_q = 0$, $I_d = \sqrt{2} I_{rms} \cos\phi$, $I_q = -\sqrt{2} \sin\phi$. D'_d, D'_q can be solved with (6.24) by setting the differential items to zero, and $D'_d = 1 - (\sqrt{2}V_{rms} - \sqrt{2}\omega L_b I_{rms} \sin\phi)/V_o$, $D'_q = 1 + (\sqrt{2}\omega L_b I_{rms} \cos\phi)/V_o$. Convert (6.25) into the s domain, and the d-axis current-to-voltage open-loop transfer function is solved as

$$G_{v\_id} = \frac{\hat{v}_o}{\hat{i}_d}|_{\hat{v}_{dq}=\hat{d}'_{dq}=0} = \frac{sR_L L_b D'_q + \omega R_L L_b D'_d}{sC_{dc} R_L \omega L_b + \omega L_b - R_L D'_d D'_q} \tag{6.26}$$

On the other hand, applying small-signal perturbation and linearization on (6.21), the small-signal model of the reactive power is

$$\hat{Q} = \frac{1}{2}(V_q\hat{i}_d + I_d\hat{v}_q - V_d\hat{i}_q - I_q\hat{v}_d) \tag{6.27}$$

Combining with (6.25) and removing $\hat{i}_d$, $\hat{v}_q$, $\hat{v}_d$ in (6.27), the q-axis current-to-reactive power open-loop transfer function is

$$G_{i_{qQ}} = \frac{1}{2}(sL_bI_d + \omega L_bI_q - V_d) \tag{6.28}$$

PI controllers are designed to compensate the voltage loop and the reactive power loop. Figure 6.21 shows the bode plots of the final voltage loop and reactive power loop.

6.4.3 Simulation Verification

A Simulation model of the T-type totem-pole rectifier with closed-loop control is built in Matlab Simulink. Figure 6.22 shows the simulation waveforms, including the input voltage v_{in}, inductor current i_L, output voltage V_o, active and reactive power P, Q of the T-type totem-pole rectifier at full load with reactive power variations. The reactive power is controlled in the pattern of 0 VAr $\rightarrow -500$ VAr $\rightarrow$ 0 VAr $\rightarrow$ 500 VAr, corresponding to the rectifier PF at 1 $\rightarrow$ leading 0.948 $\rightarrow$ 1 $\rightarrow$ lagging 0.948. With the reactive power control, Q follows the reference demand accurately and achieves a fast dynamic response. Also, the output voltage is well regulated at 480 V and the active power levels at 1.5 kW. The input current and inductor current are well shaped with full-range ZVS operation.

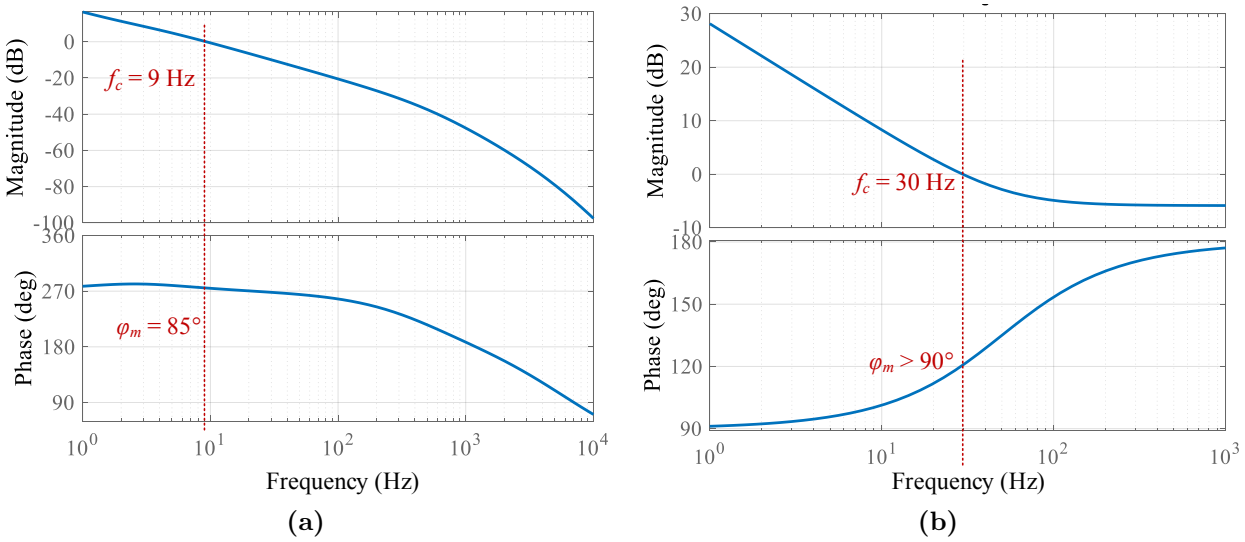


Figure 6.21: Bode plot of (a) final voltage loop gain; (b) final reactive power loop gain.

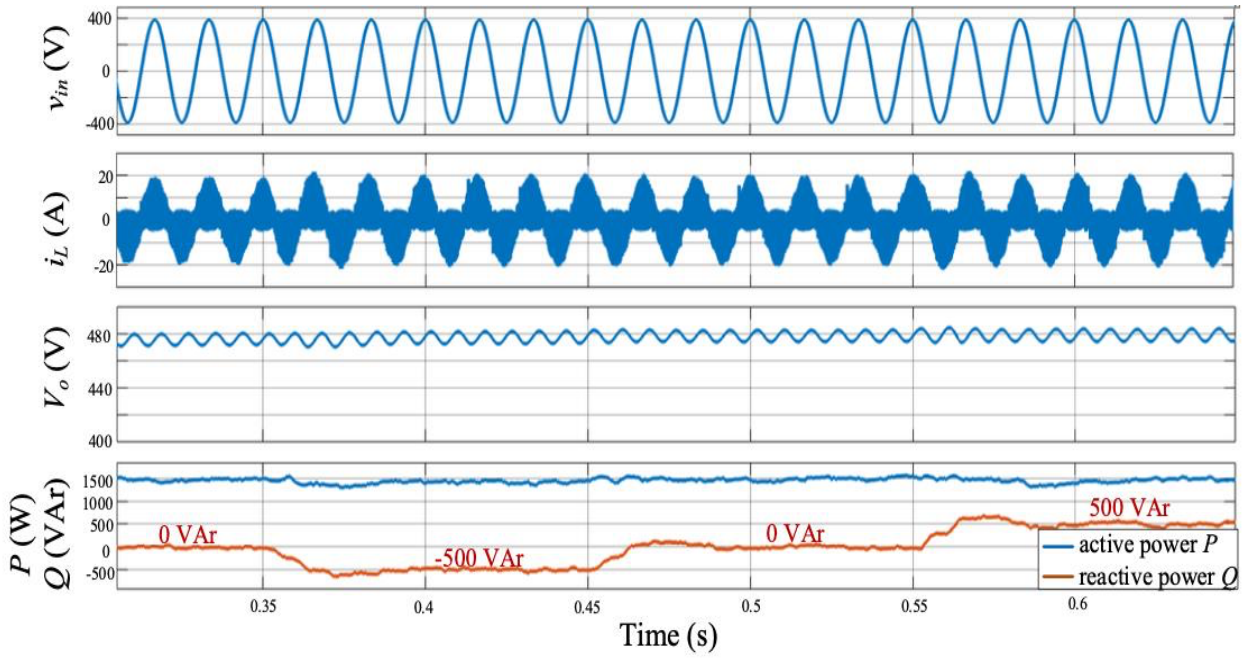


Figure 6.22: Simulation waveforms of the T-type totem-pole rectifier with reactive power operation when $v_{in} = 277$ V_{ac}, $V_o = 480$ V, $P_o = 1.5$ kW, $V_{boun} = 100$ V.

To verify the extended full-range ZVS modulation, detailed switching waveforms at the steady state with $P_o = 1.5$ kW, $Q = -500$ VAr are presented in Figure 6.23, where device gate-to-source voltages $V_{gs,GaN}, V_{gs,Si}$ and drain-to-source voltages $V_{ds,GaN}$ are monitored. The inductor current is well regulated, except for a small current spike appearing during the transition from the T-type mode to the totem-pole mode. As illustrated in Figure 6.23(b), the current spike is caused by inductor voltage change due to the topology change during the mode transition. Although the peak current is higher, ZVS turn-on is maintained, and the input current THD is not influenced since the current spike only occurs in one switching cycle. Figure 6.23(c) and Figure 6.23(d) show the zoomed-in switching waveforms during the totem-pole mode with $V_{in} > 0, I_{in} > 0$ and the T-type mode with $V_{in} < 0, I_{in} < 0$. In both moments, ZVS turn-on of the switches is achieved, which validates the proposed full-range ZVS control.

6.5 Summary

This chapter proposes the idea of using GaN-based rack-level front-end rectifiers for reactive power compensation in data centers. To identify the practical benefits, data center system cost and power loss are estimated. It is indicated that performing reactive power compensation with the GaN-based front-end rectifier can reduce data center's power consumption, allow practical usage of GaN-based front-end rectifiers, and gain more profit.

Detailed analysis of designing the GaN-based front-end rectifiers with reactive power regulation is provided. Effect of reactive power transfer on the dc capacitance is first discussed. The required capacitance for buffering the ripple energy increases with higher reactive power and apparent power. Then, operation principle of the GaN-based CRM totem-pole rectifier with reactive power and full-range ZVS is discussed. ZVS modulation is expanded to allow non-unity PF operation, and ac-line zero-crossing issues are discussed. To restrict the peak switching frequency during the ac current zero-crossing, a frequency limitation method is proposed. However, ac voltage zero-crossing is a challenge in practical implementation, and the previously used blanking time results in distorted input current under non-unity PF operation.

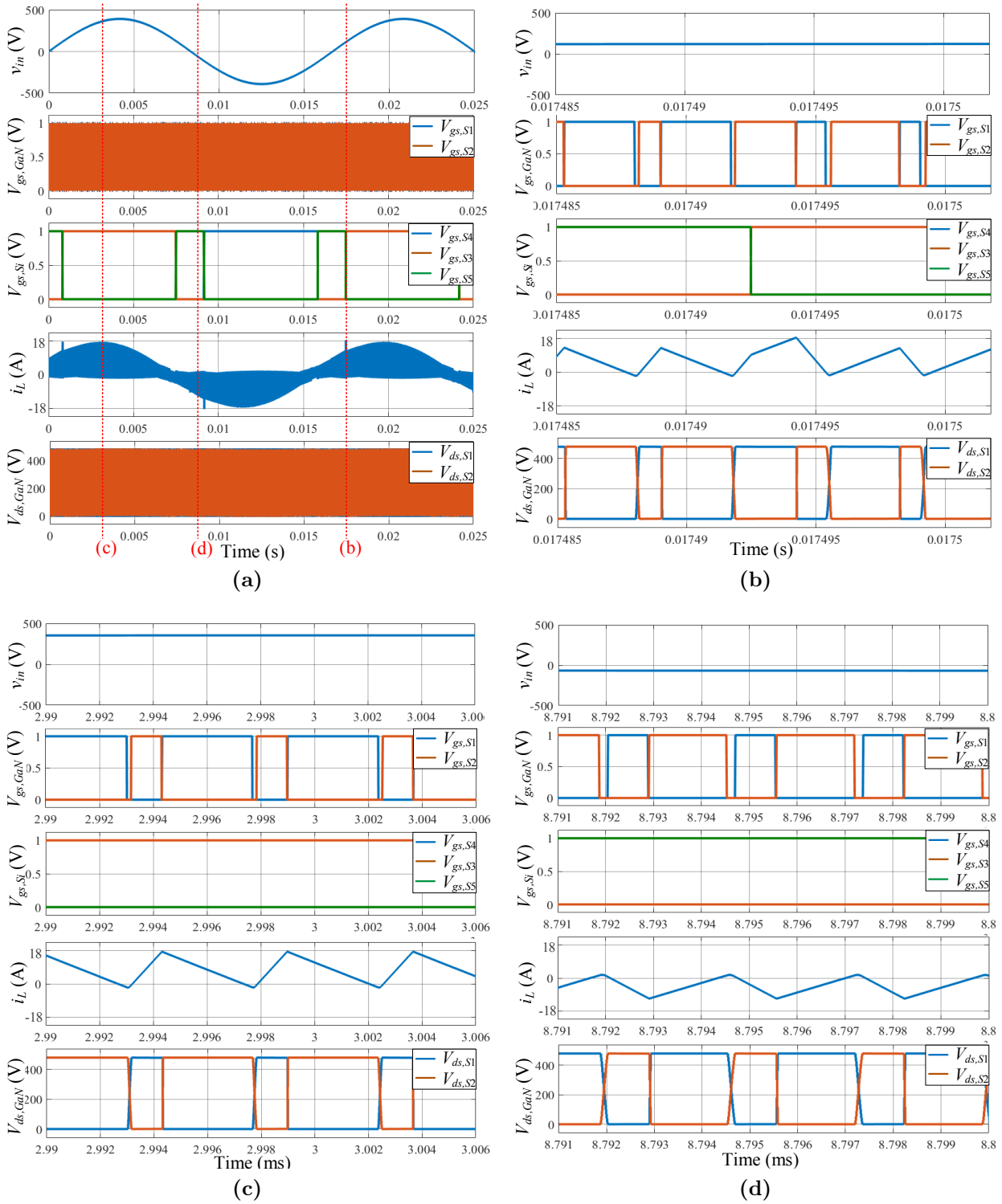


Figure 6.23: Simulation waveforms of the T-type totem-pole rectifier at leading PF with $Q = -500$ VAr when $v_{in} = 277$ V_{ac}, $V_o = 480$ V, $P_o = 1.5$ kW, $V_{boun} = 100$ V. (a) Line-cycle waveforms; (b)-(d) Switching-cycle waveforms.

To overcome the voltage zero-crossing issue, two rectifier topologies, the DBFB rectifier and the proposed T-type totem-pole rectifier, are investigated. For each topology, full-range ZVS modulation and operation waveforms are analyzed. The two rectifiers are designed with the same voltage and power rating, and the converter cost and loss are estimated. By comparison, the T-type totem-pole rectifier exhibits lower capital cost and power loss. Therefore it is selected as the front-end rectifier topology.

A control strategy containing the output voltage control, reactive power control, and model-based real-time calculation for full-range ZVS operation is proposed for the T-type totem-pole rectifier. The small-signal model is derived, and voltage and reactive power controllers are designed. A simulation model is established, and the rectifier design is validated with full-range ZVS, stable reactive power operation, and smooth dynamic response.

Chapter 7

Rectifier Verification and Data Center System Emulation with Reactive Power Regulation

Chapter 6 has proposed the design of the GaN-based T-type totem-pole rectifier and evaluated the advantages of the data center system with reactive power regulation. In order to validate the theory, a hardware prototype of the GaN-based T-type totem-pole rectifier is built, and a data center power emulator with reactive power regulation is developed in this chapter. Experiments are demonstrated to verify:

(1) High-efficiency performance of the rectifier with full-line-cycle ZVS strategy

(2) Steady-state and dynamic operations of the rectifier with flexible reactive power regulation

(3) Capability of compensating and regulating the grid terminal reactive power of the data center power system emulator

7.1 Verification of the T-type Totem-Pole Rectifier

7.1.1 Hardware Prototype Design

To verify the rectifier design, a single-phase GaN-based CRM T-type totem-pole rectifier prototype is built and tested. Figure 7.1 shows the physical prototype, and Table 7.1 summarizes the detailed converter design. The main circuit of the rectifier is composed of the input EMI filter, boost inductor, GaN and Si devices, gate drive circuits, sensing circuits, auxiliary power supply, and the dc-link capacitors. Figure 7.2 shows the two daughter cards of the rectifier prototype. One is the device daughter card containing the GaN devices, Si MOSFETs, the associated gate drive circuits, and the dc-link decoupling capacitors; the other one is the auxiliary power supply card for powering the gate driver and device gate-to-source voltages. Sensing circuits are also designed on the board, including the v_{ac} sensing circuit, i_{ac} sensing circuit, the inductor zero current detection (ZCD) circuit, and V_{dc} sensing circuit. The size of the total power stage is 90 mm $\times$ 200 mm $\times$ 43 mm, which is compatible with the $1U \times 2U$ form factor of the typical data center PSU form factor. A TMS320F28379D DSP launchpad from Texas Instruments is used as the controller to implement the control.

7.1.2 Experimental Verification

The rectifier prototype is tested at steady-state operation and dynamic operation with reactive power variations. Power analyzer Yokogawa WT3000E is used to measure the converter performance.

7.1.2.1 Steady-State Operation

The prototype is first tested at steady-state with unity PF. Figure 7.3 shows the measured efficiency, and the full-load efficiency is 98.9% at unity PF. The rectifier efficiency and power loss at each loading are also calculated based on the loss model, and the testing results match well with the model prediction. Loss breakdown including the GaN devices' conduction loss and turn-off switching loss, Si MOSFETs loss, inductor loss, ac and dc capacitors'loss, and the PCB conduction loss is analyzed.

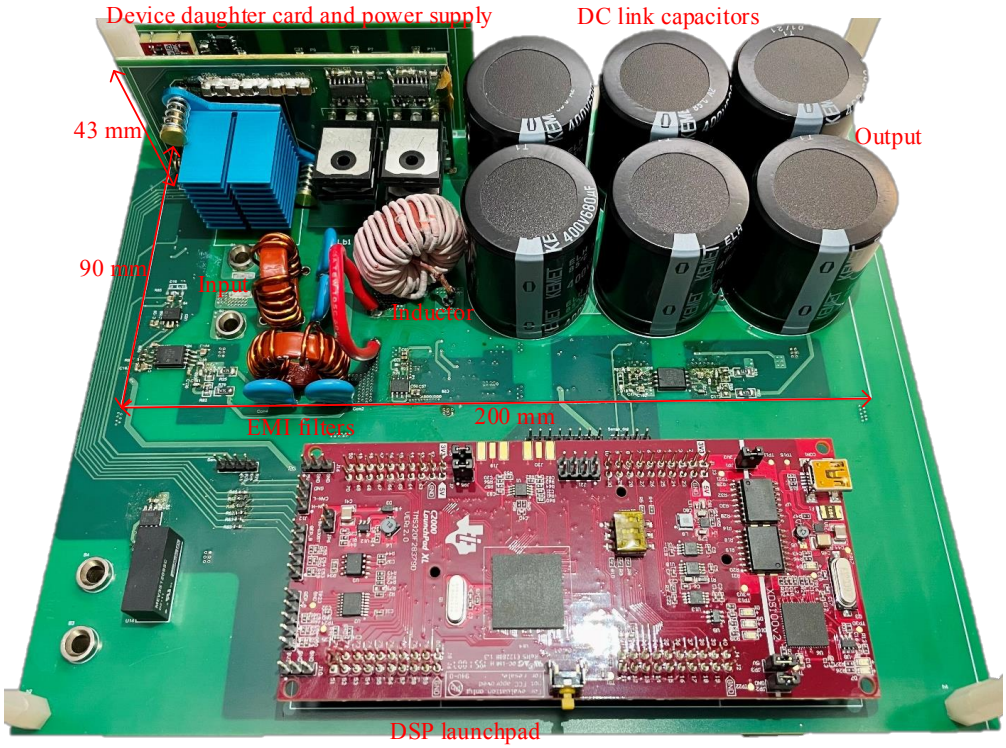
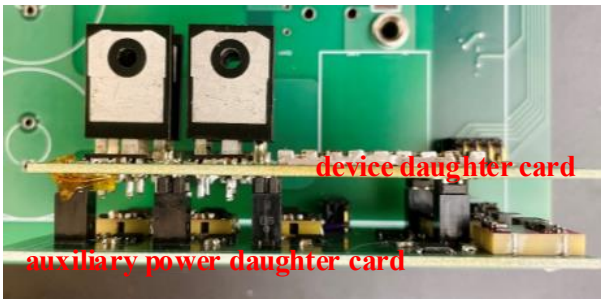


Figure 7.1: Prototype of the GaN-based T-type totem-pole rectifier.

(a) front side view.



(b) Top side view.

Figure 7.2: Daughter cards of the T-type totem-pole rectifier prototype.

Table 7.1: Specifications of the GaN-based T-type totem-pole rectifier prototype.

Parameter	Value
Input voltage v_{in}	277 V_{ac}, 60 Hz
Output voltage V_o	480 V_{dc}
Active power rating P_o	1.5 kW
Apparent power rating S	1.6 kVA
Switching frequency f_{sw}	$170 - 800$ kHz
GaN devices S_1, S_2	GS66516T, 650 V, 60 A
Si devices S_3, S_4, S_5	IPW65R019C7, 650 V
Boost inductor	21 µF with core Mix-2-T106 and 350/42 litz wire
Dc-link capacitor	6×ELH687M400AT4AA, 680 μF, 400 V
ZVS margin	$k_0 = 1.1$, $T_{ZVS,min} = 50$ ns

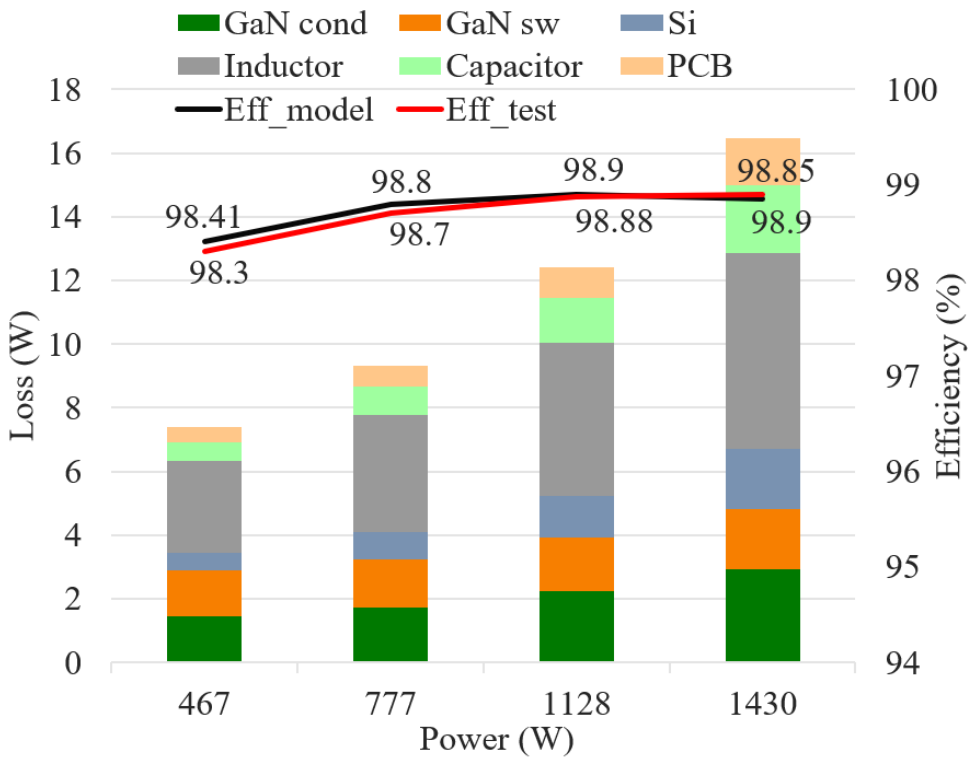


Figure 7.3: Tested efficiency of the rectifier at different loading with unity PF.

Steady-state operation with different PFs is also demonstrated on the prototype. Table 7.2 summarizes the measured operation performance at full load, and Table 7.3 lists the measured operation performance at half load. The tested efficiency at full load and half load is above 98.5%, and the input current THD is below 5%.

Figure 7.4 and Figure 7.5 show the detailed experimental waveforms of the GaN-based T-type totem-pole rectifier prototype at full load in unity PF. Both the line-cycle waveforms and switching-cycle waveforms are presented. The input current is well regulated in phase with the input voltage, and the output voltage is converted stably at 480V. The inductor current is regulated in CRM, and full-range ZVS operation is achieved in both the totem-pole mode and T-type mode.

Figure 7.6 and Figure 7.7 present the experimental waveforms of the GaN-based T-type totem-pole rectifier prototype at full load in 0.94 leading PF and 0.94 lagging PF. Specified at 1.6 kVA power rating, 0.94 is the lowest PF of the rectifier prototype that can be achieved at full load with $P = 1.5$ kW and $Q = 500$ VAr. With the reactive power closed-loop control, the reactive power and phase shift between v_{in} and i_{in} are regulated accurately.

Figure 7.8 displays the experimental waveforms of the GaN-based CRM T-type totem-pole rectifier prototype at half load in unity PF, 0.79 leading PF, and 0.87 lagging PF. With the same power rating, the rectifier can generate or absorb more reactive power at light load. With separate control loops of the output voltage and reactive power, the output voltage is regulated stably at 480 V_{dc} regardless of the reactive power level.

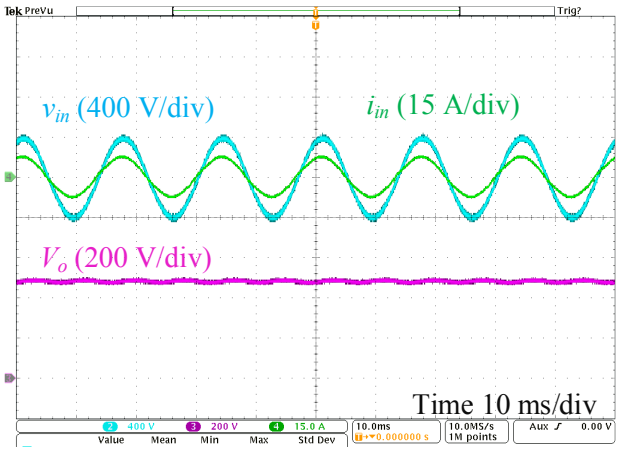
There are inductor current spikes during the mode transition between the totem-pole mode and T-type mode. This is because of the implementation limitation of DSP for PWM generation. Since the CRM rectifier has variable switching frequency with wide frequency range, the PWM generation at switching frequency cannot be synchronized with the period of model-based calculation of switching time intervals in the DSP. Therefore, device switching actions cannot be controlled accurately at the desired instant within one switching cycle during the mode transition. The resulting inductor current spike occurs in one switching period and has little impact on the input current THD and rectifier efficiency.

Table 7.2: Operation performance of the T-type totem-pole rectifier prototype at full load.

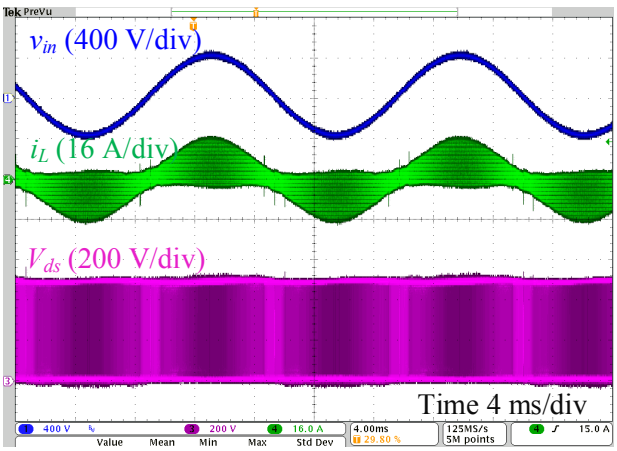
	P (W)	S (W)	Q (W)	PF	Efficiency η	iTHD
Unity PF	1430	1439	-166	> 0.99	98.9%	3.2%
Leading PF	1437	1521	-499	0.94	98.8%	2.3%
Lagging PF	1435	1525	516	0.94	98.6%	4.7%

Table 7.3: Operation performance of the rectifier prototype at half load.

	P (W)	S (W)	Q (W)	PF	Efficiency η	iTHD
Unity PF	777	783	-93	> 0.99	98.7%	4.9%
Leading PF	782	986	-600	0.79	98.6%	3%
Lagging PF	779	890	431	0.87	98.54%	4.9%

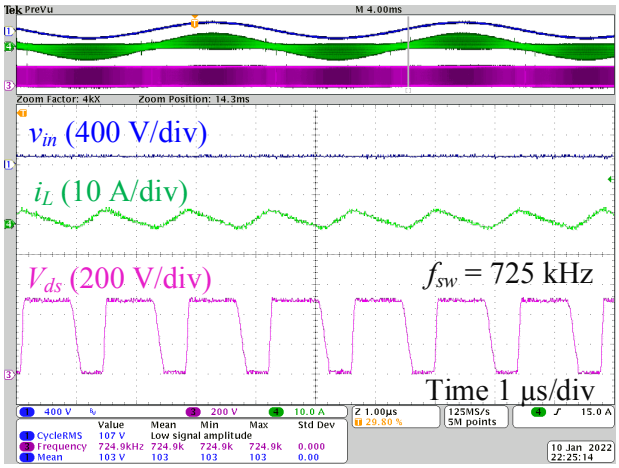


(a) Waveforms of v_{in}, i_{in}, V_o.

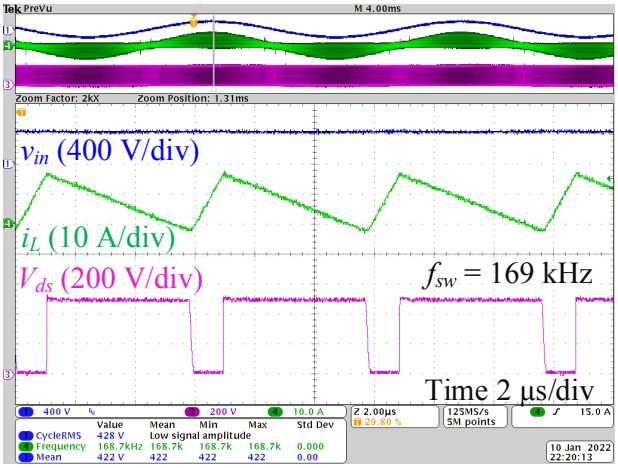


(b) Waveforms of v_{in}, i_L, V_{ds}.

Figure 7.4: Full-load experimental waveforms in line cycle of the GaN-based CRM T-type totem-pole rectifier prototype at unity PF when $v_{in} = 277$ $\mathrm{V_{ac}}$, $V_o = 480$ $\mathrm{V_{dc}}$.

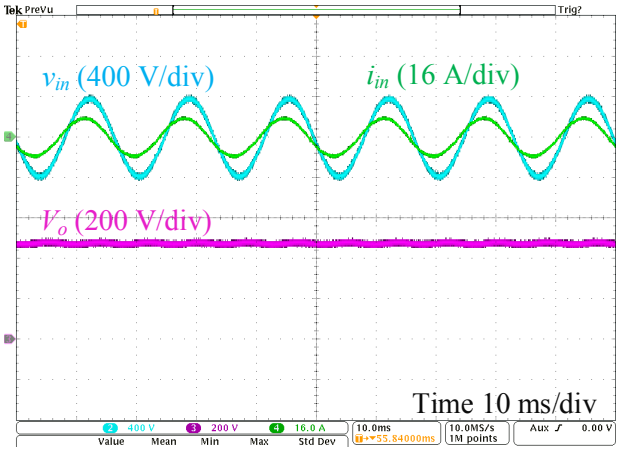


(a) Waveforms of v_{in}, i_L, V_{ds} at during T-type mode.

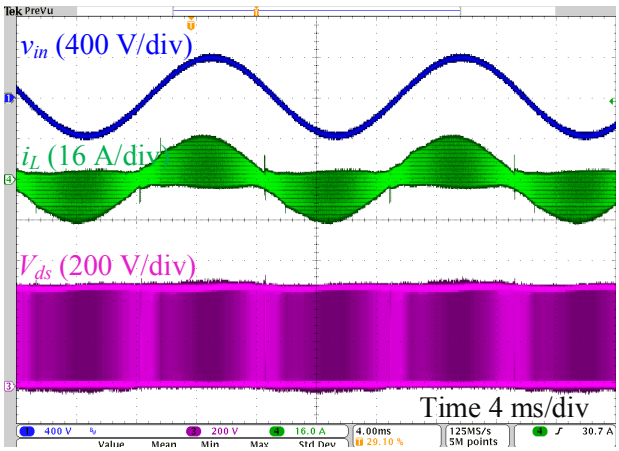


(b) Waveforms of v_{in}, i_L, V_{ds} during totem-pole mode.

Figure 7.5: Full-load experimental waveforms in switching cycle of the GaN-based CRM T-type totem-pole rectifier prototype at unity PF when $v_{in} = 277$ $\mathrm{V_{ac}}$, $V_o = 480$ $\mathrm{V_{dc}}$.

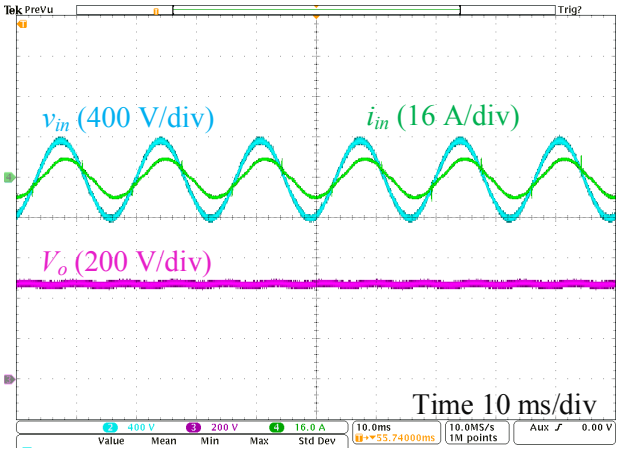


(a) Waveforms of v_{in}, i_{in}, V_o.

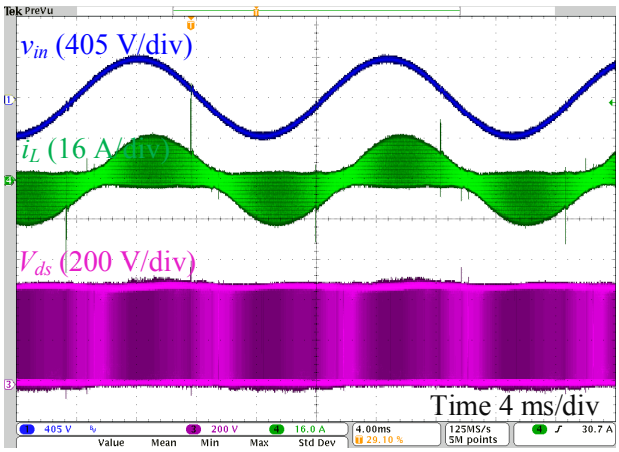


(b) Waveforms of v_{in}, i_L, V_{ds}.

Figure 7.6: Full-load experimental waveforms in line cycle of the GaN-based CRM T-type totem-pole rectifier prototype at 0.94 leading PF when $v_{in} = 277$ $\mathrm{V_{ac}}$, $V_o = 480$ $\mathrm{V_{dc}}$.

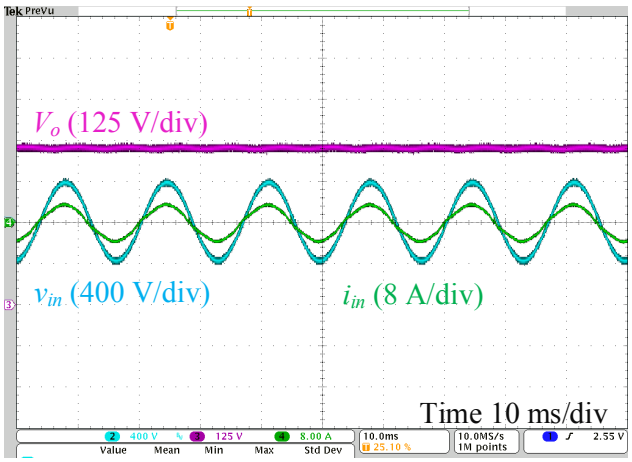


(a) Waveforms of v_{in}, i_{in}, V_o.

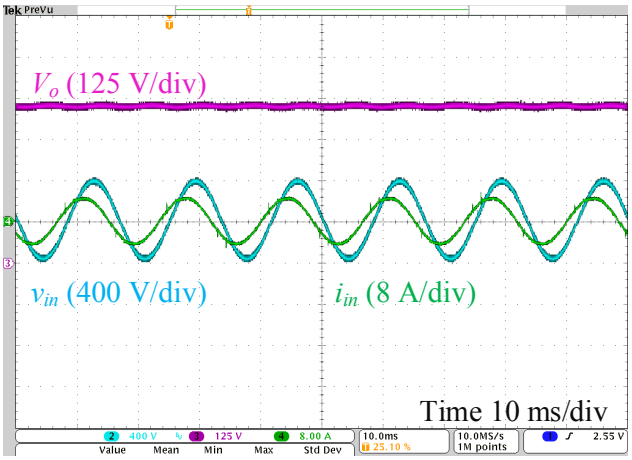


(b) Waveforms of v_{in}, i_L, V_{ds}.

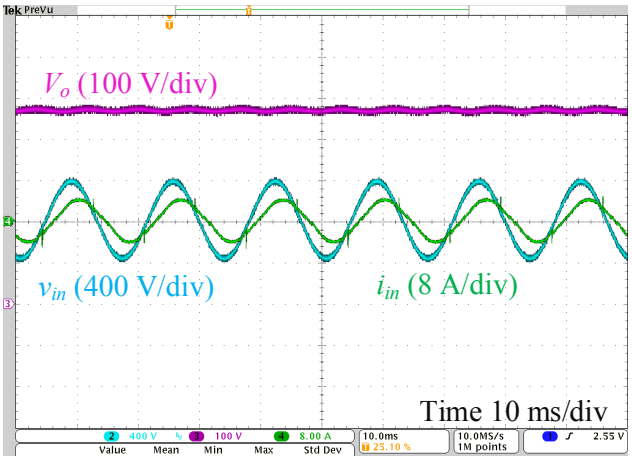
Figure 7.7: Full-load experimental waveforms in line cycle of the GaN-based CRM T-type totem-pole rectifier prototype at 0.94 lagging PF when $v_{in} = 277$ $\mathrm{V_{ac}}$, $V_o = 480$ $\mathrm{V_{dc}}$.



(a) Waveforms of v_{in}, i_{in}, V_o at unity PF.



(b) Waveforms of v_{in}, i_{in}, V_o at 0.79 leading PF.



(c) Waveforms of v_{in}, i_{in}, V_o at 0.87 lagging PF.

Figure 7.8: Half-load experimental waveforms of the GaN-based CRM T-type totem-pole rectifier prototype when $v_{in} = 277$ $\mathrm{V_{ac}}$, $V_o = 480$ $\mathrm{V_{dc}}$.

7.1.2.2 Dynamic Operation

To compensate the reactive power in a data center, the GaN-based front-end rectifiers should be able to transfer reactive power flexibly based on the reactive power reference Q_{ref} and achieve a smooth transient response during Q_{ref} variations. Therefore, the rectifier prototype is demonstrated at dynamic operation among different PFs.

Figure 7.10 - Figure 7.12 present the experimental waveforms at full-load when the rectifier transitions among unity PF, 0.94 leading PF, and 0.94 lagging PF. It is designed that the reactive power reference linearly changes within four line cycles. As can be seen, the phase shift between v_{in} and i_{in} is adjusted gradually in four line cycles, and there is no current overshoot during the transition.

Dynamic operation of the rectifier is also demonstrated at half load. Figure 7.13 shows the dynamic operation from 0.87 lagging PF to unity PF, and Figure 7.14 presents the transient response from unity PF to 0.79 leading PF. The reactive power reference is given a step change, and the dynamic response of the rectifier lasts for two line cycles, which is limited by the reactive power loop bandwidth at 30 kHz. Faster dynamic response can be achieved by designing the reactive power control loop with higher bandwidth. Still, the rectifier performs a smooth dynamic response without current overshoot during transitions among various PFs.

Therefore, the capability of flexible reactive power regulation with smooth dynamic response is validated in the GaN-based T-type totem-pole rectifier prototype.

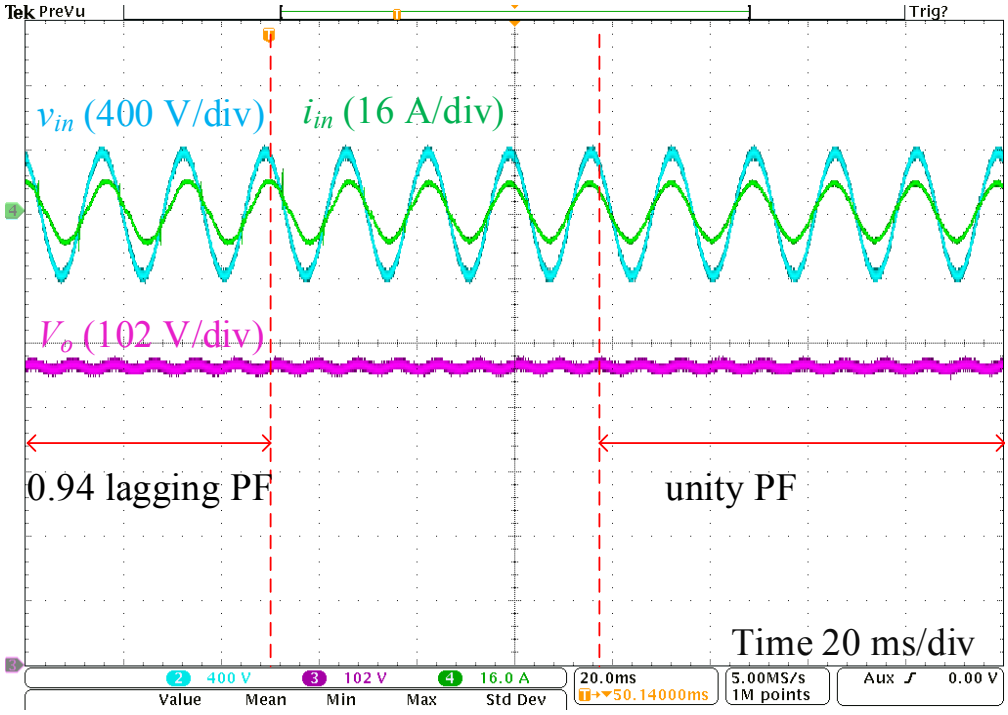


Figure 7.9: Dynamic experimental waveform of the rectifier prototype from 0.94 lagging PF to unity PF at full load when $v_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}.

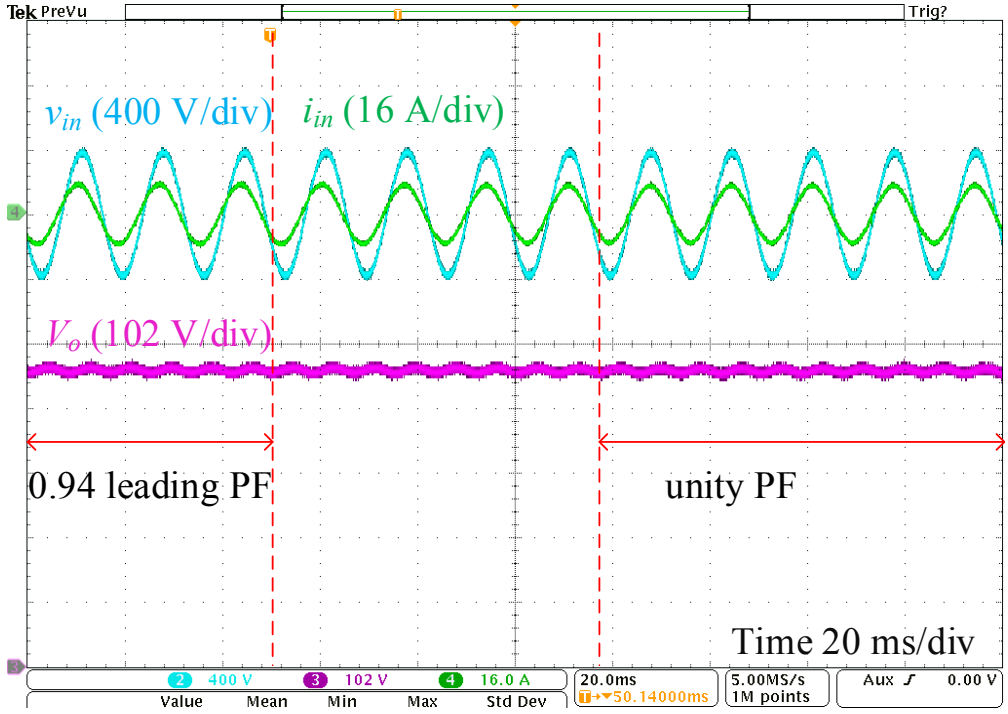


Figure 7.10: Dynamic experimental waveform of the rectifier prototype from 0.94 leading PF to unity PF at full load when $v_{in} = 277$ V_{ac}, $V_o = 480$ V_{dc}.

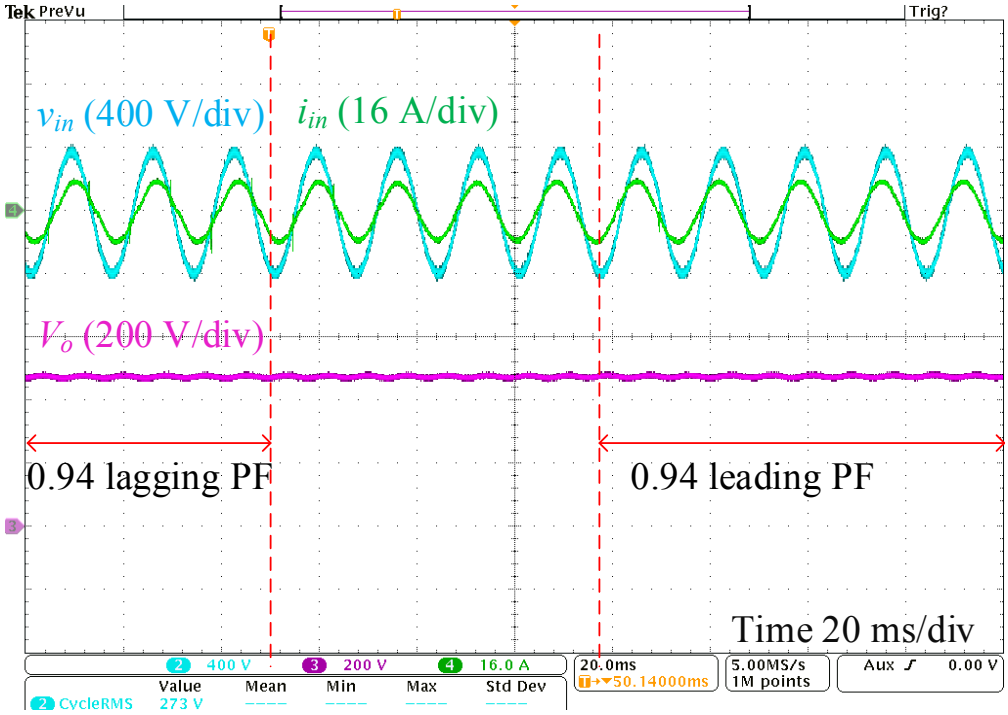


Figure 7.11: Dynamic experimental waveform of the rectifier prototype from 0.94 lagging PF to 0.94 leading PF at full load when $v_{in} = 277$ $\mathrm{V_{ac}}$, $V_o = 480$ $\mathrm{V_{dc}}$.

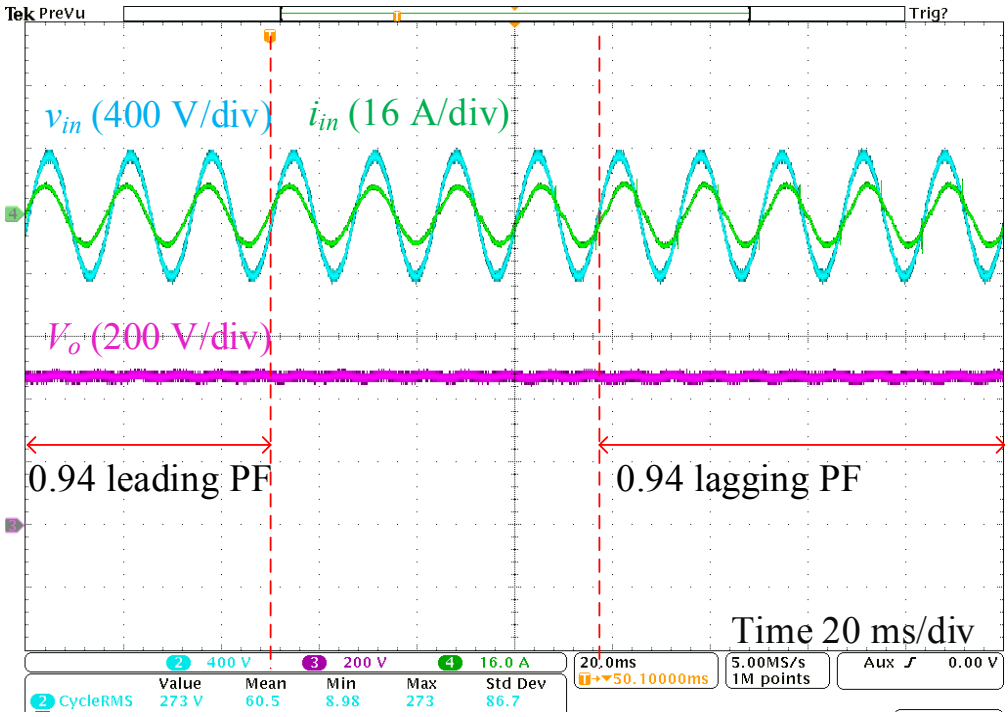


Figure 7.12: Dynamic experimental waveform of the rectifier prototype from 0.94 leading PF to 0.94 lagging PF at full load when $v_{in} = 277$ $\mathrm{V_{ac}}$, $V_o = 480$ $\mathrm{V_{dc}}$.

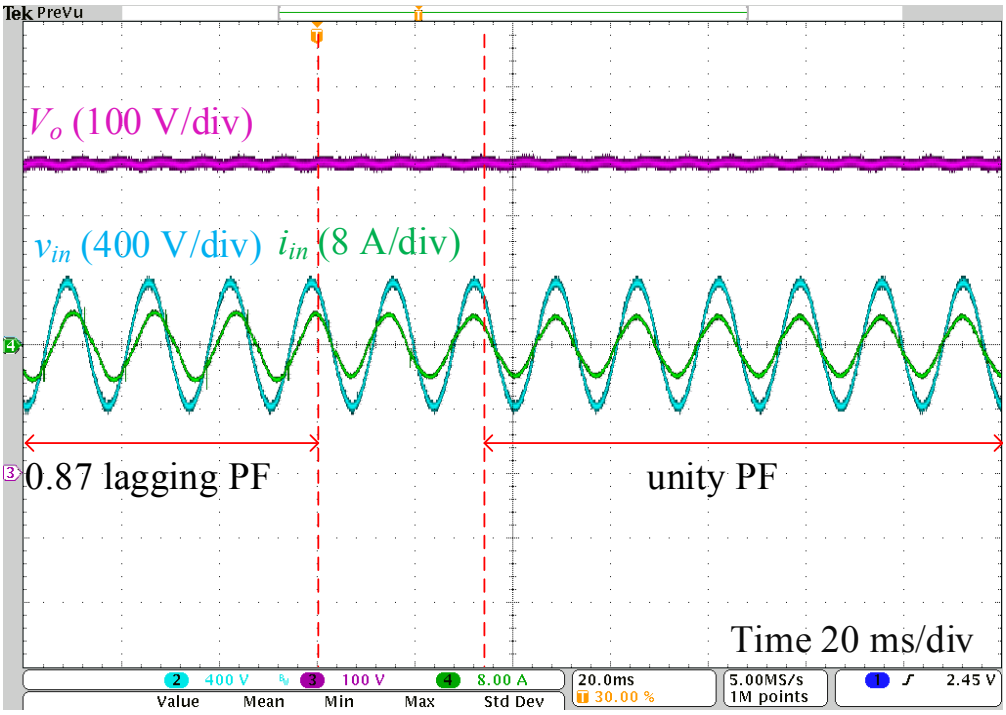


Figure 7.13: Dynamic experimental waveform of the rectifier prototype from 0.87 lagging PF to unity PF at half load when $v_{in} = 277$ $\mathrm{V_{ac}}$, $V_o = 480$ $\mathrm{V_{dc}}$.

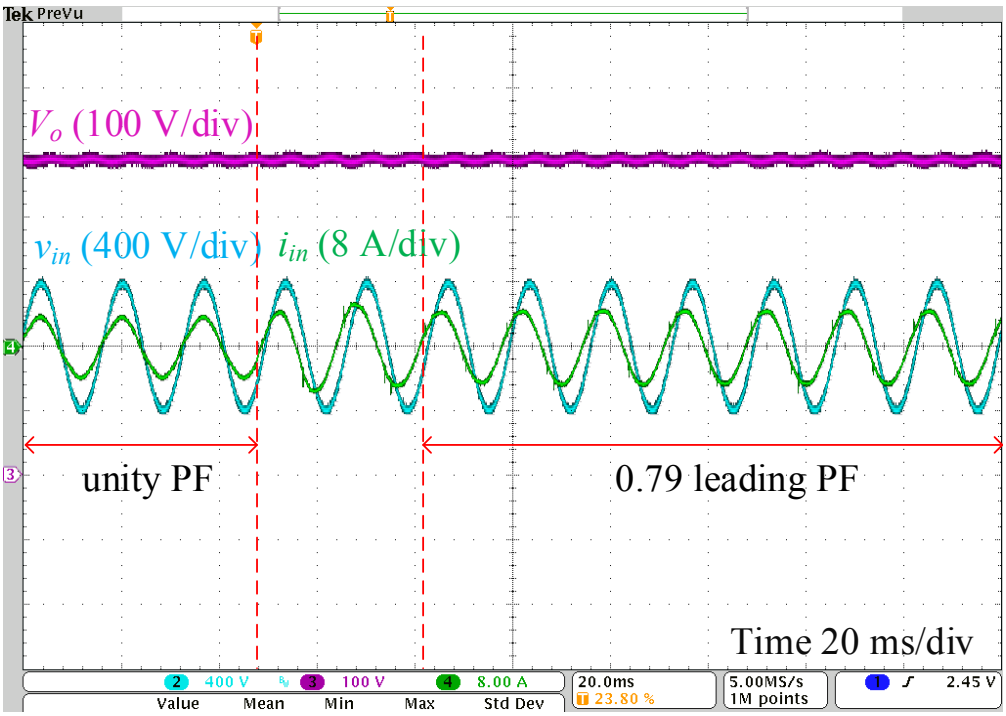


Figure 7.14: Dynamic experimental waveform of the rectifier prototype from unity PF to 0.79 leading PF at half load when $v_{in} = 277$ $\mathrm{V_{ac}}$, $V_o = 480$ $\mathrm{V_{dc}}$.

7.2 Emulation of the Data Center Power System

7.2.1 Data Center Power System with Reactive Power Regulation

7.2.1.1 System Circuit and Operation

By replacing the traditional boost PFC rectifier with the proposed GaN-based T-type totem-pole rectifier, the data center system is able to regulate the grid terminal reactive power and provide the point-of-load server power simultaneously. Figure 7.15 shows the data center system structure with reactive power regulation during the normal eco mode. The rack-level front-end rectifiers are directly connected to the grid and are used to compensate the reactive power as well as supplying the active power for the server loads. The grid terminal voltage and current are sensed, and the instantaneous power is estimated. A supervisory central controller will decide the required reactive power that is assigned to the front-end rectifiers.

7.2.1.2 Modeling of the T-type Totem-Pole Rectifier

To implement the function of reactive power regulation in the the data center power system, modeling of the T-type totem-pole rectifier is required. Since only the line-cycle dynamic performance is of interest, specific switching pattern and the short-time T-type mode operation can be ignored. As shown in Figure 7.16(a), the rectifier is modeled as a boost-type converter with current-programmed control and a controlled voltage source $\bar{v}_d$ that represents the pulsating voltage between the ac source and the ground.

Recalling the rectifier control strategy presented in Figure 6.20 in Chapter 6, the dc voltage loop and reactive power loop generate i_{dref} and i_{qref} respectively, and the current reference i_{ref} is composed through the inverse Park transformation. Then, i_{ref} is used in the real-time calculation to generate the instantaneous switching time intervals. Neglecting the high-frequency switching and online calculation, the average inductor current equals to the current reference approximately, that is $\bar{i}_{Lb} = \bar{i}_{ref} = \bar{i}_{ac,rec}$. Hence, the rectifier average

model can be expressed as

$$\begin{cases} \bar{i}_{ac,rec} \approx \bar{i}_{Lb} \approx \bar{i}_{ref} = \bar{i}_{dref}\cos\theta - \bar{i}_{qref}\sin(\theta) \\ \bar{v}_d = \begin{cases} 0, v_{ac} \geq 0 \\ \bar{v}_{dc,rec}, v_{ac} < 0 \end{cases} \\ C_{dc,rec}\frac{d\bar{v}_{dc,rec}}{dt} = \bar{i}_{dc,rec} - \bar{i}_{load,rec} \\ \bar{i}_{dc,rec} = \frac{\bar{v}_{ac,rec}\bar{i}_{ac,rec}}{\bar{v}_{dc,rec}} \end{cases} \tag{7.1}$$

where θ is the phase angle of $v_{ac,rec}$.

Figure 7.16(b) shows the output voltage control and the reactive power control used in the model. To estimate the reactive power, the single-phase ac voltage and current are converted into $\alpha\beta$ frame through a second-order generalized integrator (SOGI) based orthogonal signal generator (OSG), and then transformed into dq frame via Park transformation. The rectifier reactive power is calculated as

$$\bar{q}_{rec} = \frac{1}{2}(\bar{v}_q\bar{i}_d - \bar{v}_d\bar{i}_q) \tag{7.2}$$

$$\begin{cases} \bar{v}_d = \bar{v}_\alpha\cos\theta + \bar{v}_\beta\sin\theta \\ \bar{v}_q = -\bar{v}_\alpha\sin\theta + \bar{v}_\beta\cos\theta \\ \bar{i}_d = \bar{i}_\alpha\cos\theta + \bar{i}_\beta\sin\theta \\ \bar{i}_q = -\bar{i}_\alpha\sin\theta + \bar{i}_\beta\cos\theta \end{cases} \tag{7.3}$$

$\bar{v}_\alpha, \bar{v}_\beta, \bar{i}_\alpha, \bar{i}_\beta$ are obtained through SOGI with the closed-loop transfer function as

$$\begin{cases} H_\alpha(s) = \frac{x_\alpha(s)}{x(s)} = \frac{k\omega s}{s^2+k\omega s+\omega^2} \\ H_\beta(s) = \frac{x_\beta(s)}{x(s)} = \frac{k\omega^2}{s^2+k\omega s+\omega^2} \end{cases} \tag{7.4}$$

where k is the coefficient that determines the frequency width for the second order integrator, ω is the fundamental angular frequency.

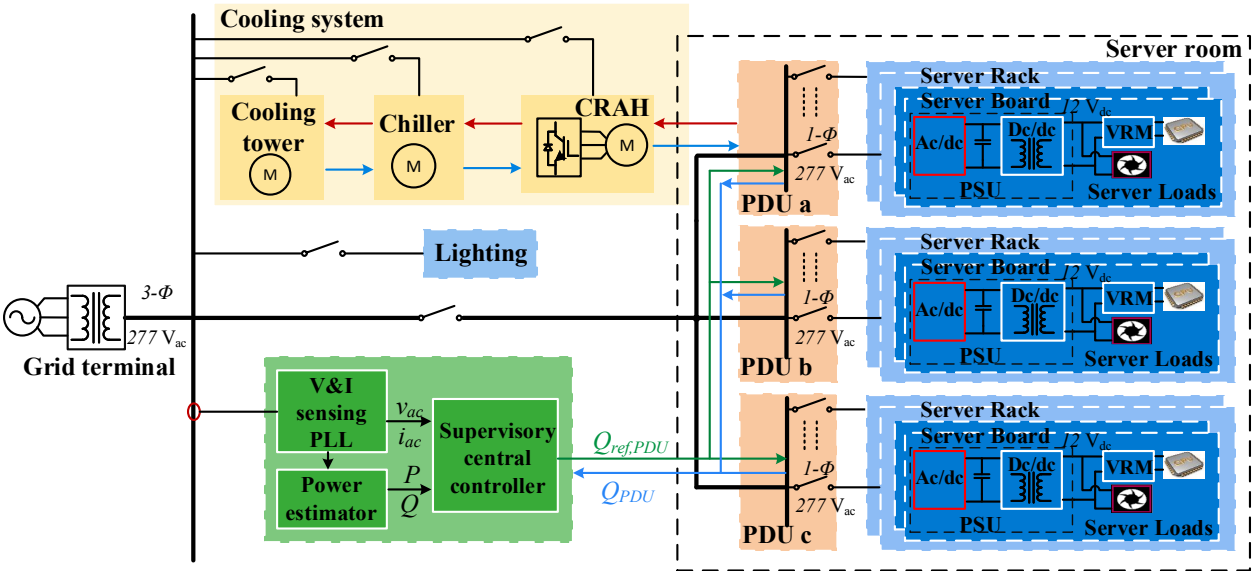


Figure 7.15: Data center power system structure with reactive power regulation.

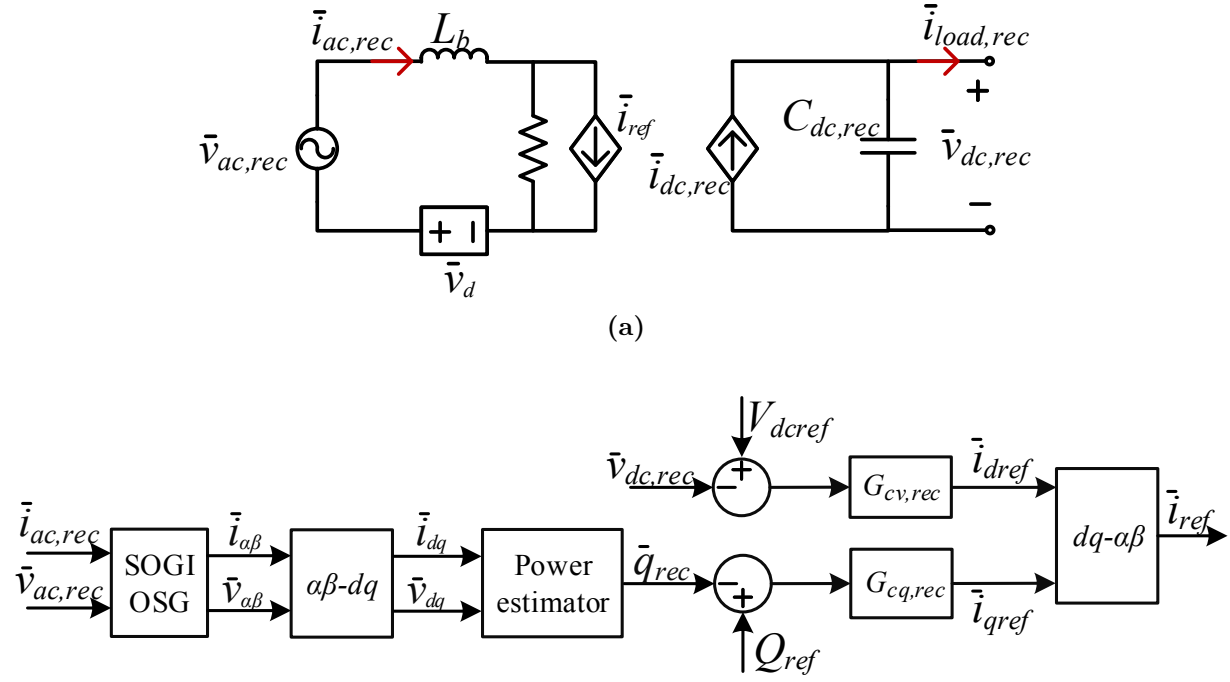


Figure 7.16: Modeling of the T-type totem-pole rectifier. (a) Average model; (b) Control loops of the dc voltage and reactive power.

7.2.2 Experimental Emulation

7.2.2.1 Emulator Implementation

To validate the function of reactive power regulation, the data center power emulator developed in Chapter 3 is modified by updating the front-end rectifier model in the VSI DSP. Therefore, digitized model of the proposed T-type totem-pole rectifier is derived, as shown below.

Dc voltage loop with PI controller in pu in discrete-time equation is given as:

$$\begin{cases} e_{v,rec}[x] = V^{pu}_{dcref,rec}[x] - \bar{v}^{pu}_{dc,rec}[x-1] \\ \bar{i}^{pu}_{dref}[x] = k_{p\_v,rec} e_{v,rec}[x] + \sum_{0}^{x} k_{i\_v,rec} e_{v,rec}[x] T_s \end{cases} \tag{7.5}$$

Reactive power loop with PI controller in discrete-time equation is as follows:

$$\begin{cases} e_{q,rec}[x] = Q^{pu}_{ref,rec}[x] - \bar{q}^{pu}_{rec}[x-1] \\ \bar{i}^{pu}_{qref}[x] = k_{p\_q,rec} e_{q,rec}[x] + \sum_{0}^{x} k_{i\_q,rec} e_{q,rec}[x] T_s \end{cases} \tag{7.6}$$

Rectifier average model in discrete-time equation is:

$$\begin{cases} \bar{i}_{ac,rec}[x] = \bar{i}_{ref}[x] = \bar{i}_{dref}[x]\cos\theta[x] - \bar{i}_{qref}[x]\sin(\theta[x]) \\ \bar{v}_{dc,rec}[x] = \bar{v}_{dc,rec}[x-1] + \frac{T_s}{C_{dc,rec}}\left(\frac{\bar{v}_{ac,rec}[x]\bar{i}_{ac,rec}[x]}{\bar{v}_{dc,rec}[x-1]} - \bar{i}_{load,rec}[x]\right) \\ \bar{q}_{rec}[x] = \frac{1}{2}(\bar{v}_q[x]\bar{i}_d[x] - \bar{v}_d[x]\bar{i}_q[x]) \end{cases} \tag{7.7}$$

Based on the grid frequency ω ($2\pi 60$ rad/s) and sampling frequency f_s (5 kHz), trapezoidal approximation is used to obtain the discrete transfer function for SOGI, and the discrete equations for generating $\alpha\beta$ parameters are:

$$\begin{cases} X_\alpha[x] = a_1 X_\alpha[x-1] + a_2 X_\alpha[x-2] + b_0 X[x] + b_2 X[x-2] \\ X_\beta[x] = a_1 X_\beta[x-1] + a_2 X_\beta[x-2] + qb_0 X[x] + qb_1 X[x-1] + qb_2 X[x-2] \end{cases} \tag{7.8}$$

where $b_0 = \frac{c}{c+d+4}, b_2 = -b_0, a_1 = \frac{2(4-d)}{c+d+4}, a_2 = \frac{c-d-4}{c+d+4}, qb_0 = \frac{kd}{c+d+4}, qb_1 = 2q_{b0}, qb_2 = qb_0, c = 2k\omega T_s, d = (\omega T_s)^2$. Then, $\bar{v}_d[x], \bar{v}_q[x], \bar{i}_d[x], \bar{i}_q[x]$ are calculated based on (7.3).

The data center power emulator is implemented on the HTB and verified in a local network consisting of three VSIs in one cabinet, as presented in Figure 3.23.

7.2.2.2 Emulator Testing Results

Figure 7.17 and Figure 7.18 present the experimental emulation results of the data center power emulator with reactive power regulation, including waveforms of the grid terminal voltage $V_{t,pu}$, the grid terminal current $I_{dq,pu}$, the grid terminal active power $P_{t,pu}$ and reactive power $Q_{t,pu}$, and the dc output voltage of the front-end rectifier $V_{dc\_rec,pu}$. Table 7.4 lists the grid terminal power and PF in different cases.

Figure 7.17 shows the emulation results of the data center power system with reactive power compensation. In case (a) during $t = 0 - 1$ s, the data center operates in normal eco mode with server utilization at $u = 100\%$, and the reactive power from the cooling system is not compensated. As a result, the grid terminal power $Q_{t,pu} = 0.15, P_{t,pu} = 0.85$ and PF is 0.985 lagging. At $t = 1$ s, the function of reactive power compensation is enabled in the central controller, and the front-end rectifiers start to generate reactive power to help regulate the grid terminal PF. Consequently, during case (b) from $t = 1$ s to $t = 2$ s, $Q_{t,pu}$ decreases to 0, $P_{t,pu}$ is unchanged, and grid terminal PF is regulated at 1. For case (c) after $t = 2$ s, the data center server load decreases to $u = 40\%$, and $P_{t,pu}$ drops to 0.49. During the load change, $V_{dc\_rec,pu}$ is regulated with small transient fluctuation, but the terminal current and active power have significant transient change mainly because of the slow dynamic response and large inertia of the cooling system. Since reactive power compensation is still enabled, unity PF is maintained on the grid terminal.

The front-end rectifiers can also generate or consume more reactive power to achieve a flexible PF regulation on the grid terminal and help support the power system. As demonstrated in Figure 7.18, starting from case (d) without reactive power compensation, the front-end rectifiers generate more reactive power to the grid terminal during case (e) ($t = 1 - 2$s), and the PF is regulated at 0.973 leading with $P_{t,pu} = 0.85, Q_{t,pu} = -0.2$. Then, in case (f) during $t = 2 - 3$s, the terminal reactive power is regulated at zero and

unity PF is realized. After $t = 3$ s, the front-end rectifiers absorb more reactive power to achieve a 0.973 lagging PF, and the terminal reactive power is regulated at 0.2. In all cases, the server load remains the same, and terminal active power is unchanged.

Because of the separate power controls in the front-end rectifier, regulation of the reactive power does not influence supplying the active power for the server load in the data center system. However, since line impedance exists between the grid generator and data center load, the point of common coupling (PCC) voltage V_t fluctuates to some degree when the reactive power changes.

7.3 System Cost and Loss Evaluation

Since the proposed T-type totem-pole rectifier has slightly higher power loss and cost than the totem-pole rectifier, it is necessary to reevaluate data center system's total loss and cost. To further verify the advantages of using the proposed rectifier for reactive power regulation, a 10 MW data center system's power loss and cost are evaluated in the way shown in Section 6.1. For server rack front-end rectifiers, traditional boost PFCs and GaN-based CRM totem-pole PFCs are used in system 1 and system 2, respectively, and the proposed GaN-based T-type totem-pole rectifier is used in system 3 for reactive power compensation. Table 7.5 shows the predicted cost and power loss of the 10 MW data center system that is defined in Table 6.1. Figure 7.19 compares the three data center systems in terms of the power loss and total cost.

With the high-efficiency GaN-based rectifiers, System 2 and System 3 have much lower power loss than the loss in System 1, as shown in Figure 7.19(a). However, due to the expensive commercial GaN devices, System 2 cost is higher than System 1 cost (Figure 7.19(b), Figure 7.19(c)). By providing reactive power compensation from the GaN-based T-type totem-pole rectifiers in System 3, the system cost is significantly reduced compared to System 2 cost and even lower than System 1 cost in two years. As presented in Figure 7.19(c), the saved system cost in System 3 is more substantial in five years. Therefore, same as before, System 3 has the lowest power loss and cost by using the GaN-based rectifiers for both server power and reactive power compensation.

Table 7.4: Emulated data center terminal power and PFs corresponding to Figure 7.17 and Figure 7.18.

Case No.	$P_{t,pu}$	$Q_{t,pu}$	PF
(a)	0.85	0.15	0.985 lagging
(b)	0.85	0	1
(c)	0.49	0	1
(d)	0.85	0.15	0.985 lagging
(e)	0.85	-0.2	0.973 leading
(f)	0.85	0	1
(g)	0.85	0.2	0.973 lagging

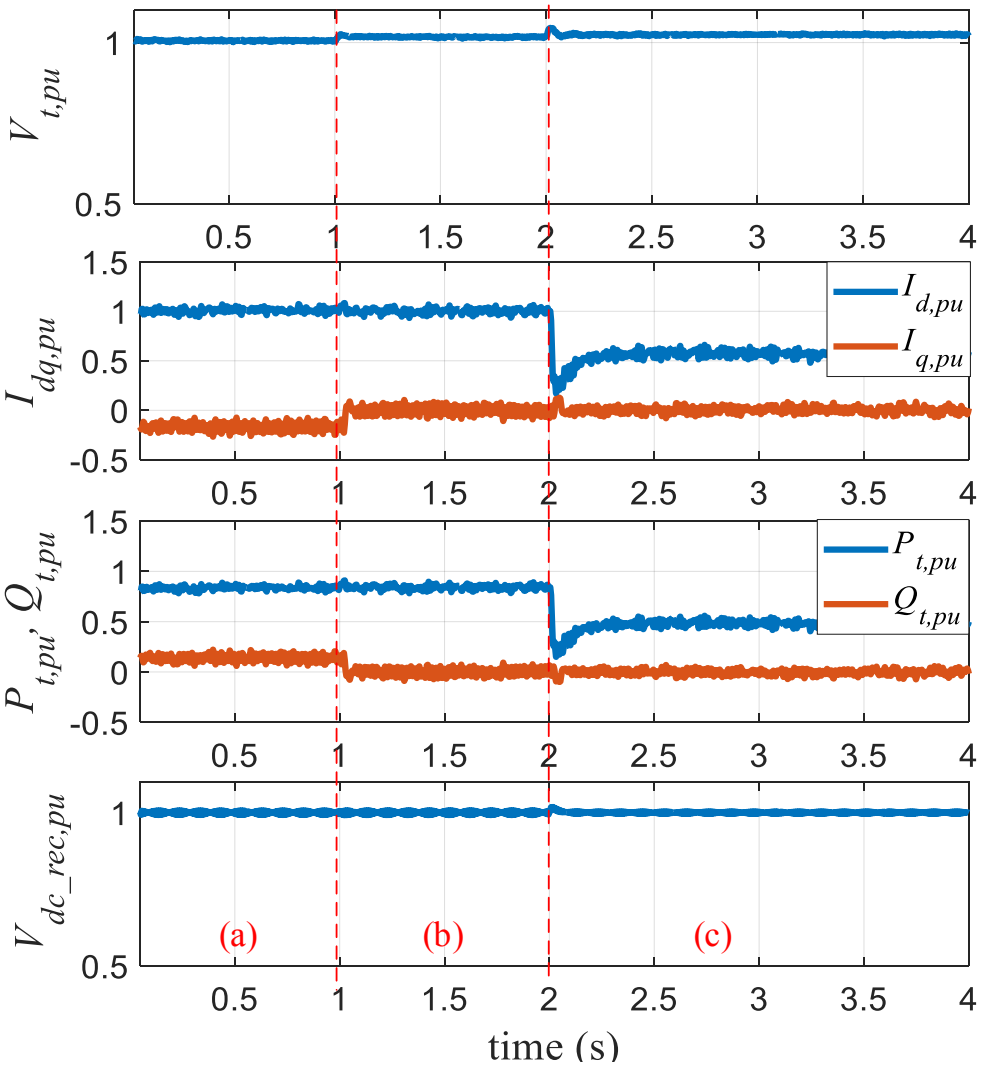


Figure 7.17: Experimental emulation waveforms of the data center power system with reactive power compensation.

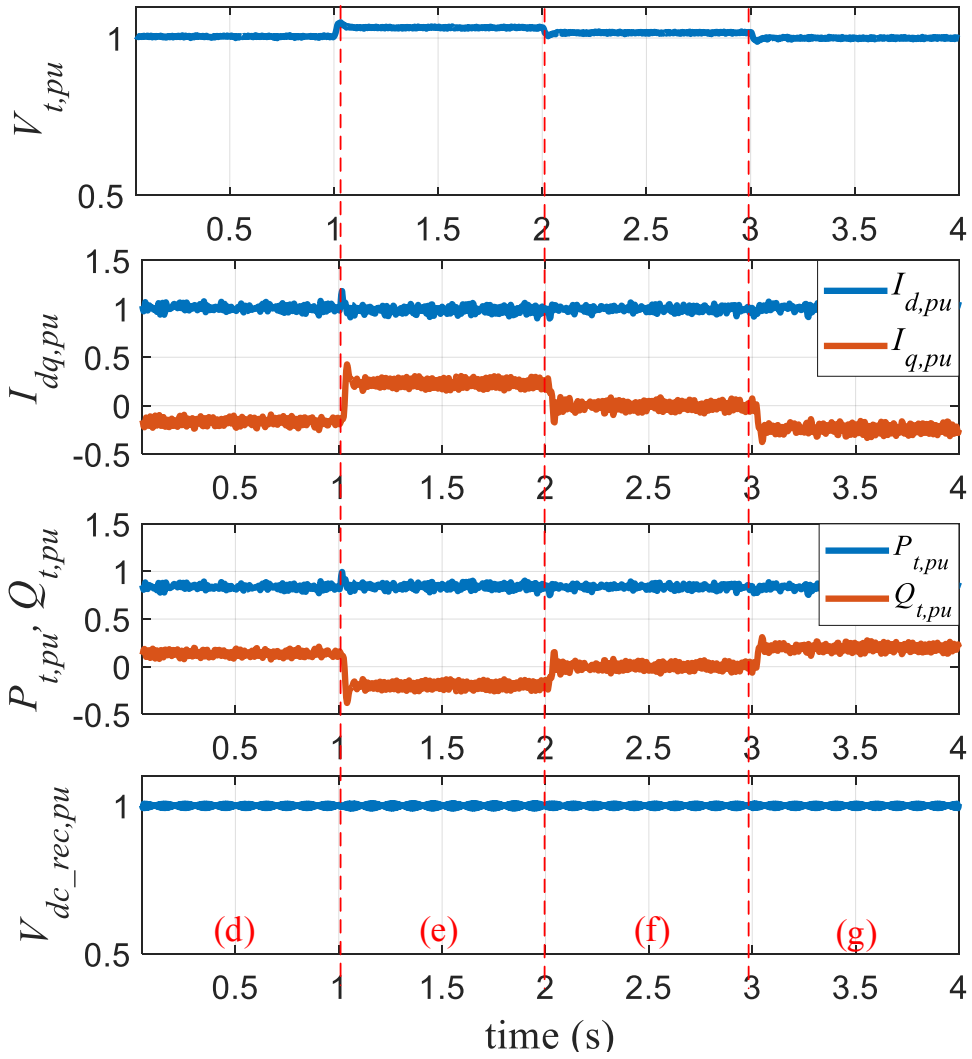
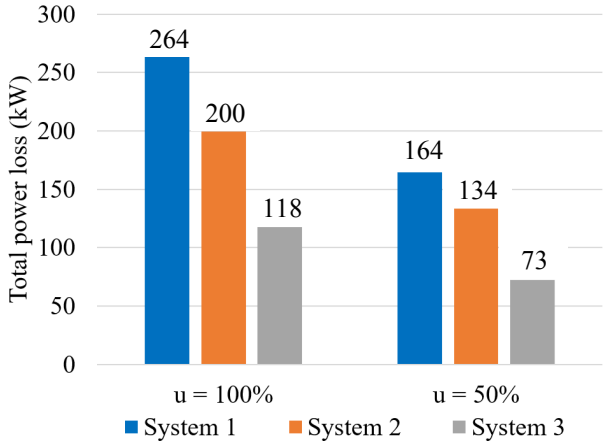


Figure 7.18: Experimental emulation waveforms of the data center power system with reactive power regulation.

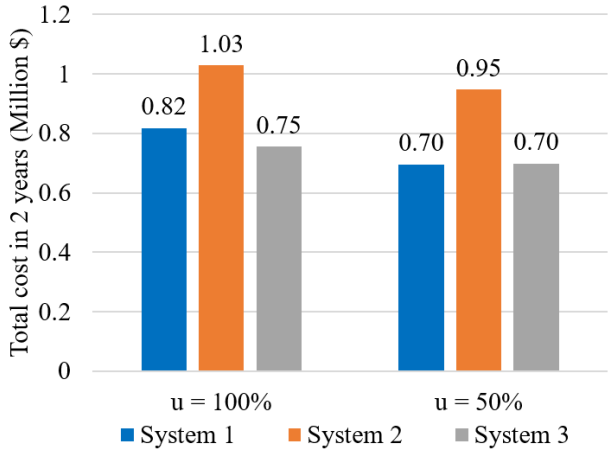
Table 7.5: Predicted cost and power loss of 10 MW data center systems.

Parameter	w/ server $u = 100\%$			w/ server $u = 50\%$		
	system 1	system 2	system 3	system 1	system 2	system 3
P_{rec}(kW)	1.498	1.498	1.498	0.807	0.807	0.807
Q_{rec}(kVAr)	0	0	-0.557	0	0	-0.457
S_{rec}(kVA)	1.498	1.498	1.598	0.807	0.807	0.9271
Rectifiers loss(kW)	139.19	75.15	81.9	71.55	40.86	51.75
STATCOMs loss(kW)	90.9	90.9	0	74.64	74.64	0
Cable loss(kW)	33.7	33.7	35.96	18.16	18.16	20.86
Rectifiers cost	$ 284,355	$ 573,795	$ 610,020	$ 284,355	$ 573,795	$ 610,020
STATCOMs cost	$ 210,000	$ 210,000	$ 0	$ 210,000	$ 210,000	$ 0
Electricity bill/year	$ 161,756	$ 122,487	$ 72,272	$ 100,779	$ 81,960	$ 44,530

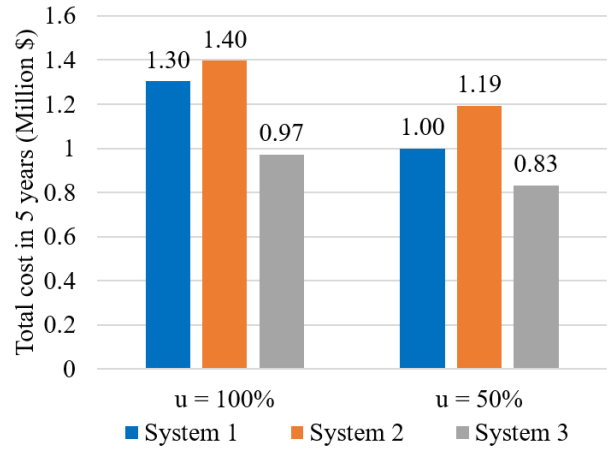
* It is assumed that both active power and reactive power are evenly distributed on each STATCOM module and front-end rectifiers.
* Server room cable loss is estimated as 0.5% of the IT equipment power.
* The U.S. average industrial price of electricity is $ 0.07/kWh since 2010 [222].
* STATCOMs cost $ 60/kVAr to $ 100/kVAr [223]. The average cost at $ 80 per kVAr is used here.
* **System 1** has centralized STATCOM and Si-based boost PFC rectifiers.
* **System 2** has centralized STATCOM and GaN-based CRM totem-pole PFC rectifiers.
* **System 3** has GaN-based CRM T-type totem-pole rectifiers.



(a)



(b)



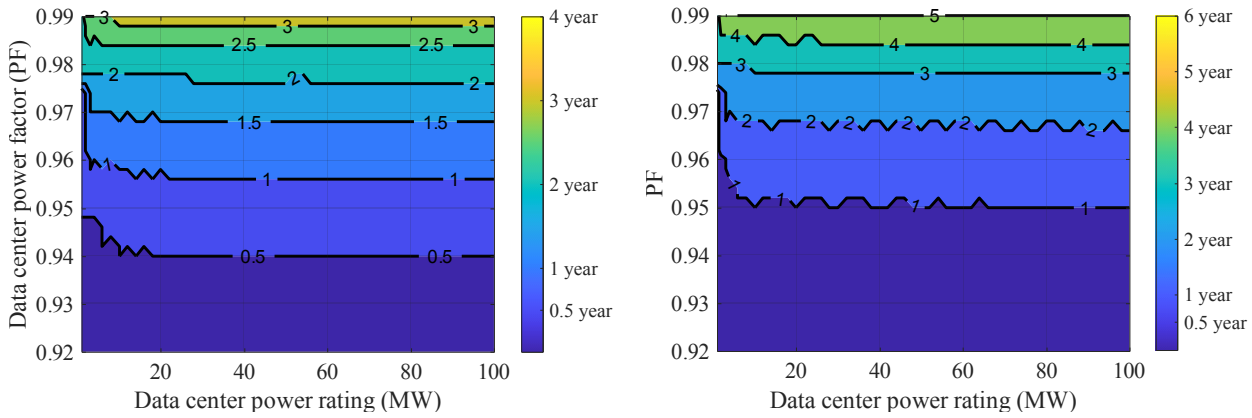
(c)

Figure 7.19: Comparison of data center power loss and cost as defined in Table 7.5. (a) Power loss; (b) Cost in two years; (c) Cost in five years.

To better analyze the profit gained by implementing reactive power compensation on the GaN-based T-type totem-pole rectifiers, the number of years to pay back of the data center System 3 compared to the traditional data center System 1 is plotted versus data center power factor, data center system power rating, electricity price, and GaN device price. Figure 7.20 illustrates the number of years to payback of data centers with power rating from 1 MW to 100 MW and PF from 0.92 to 0.99 at server utilization $u = 100\%$ and $u = 50\%$ when current market prices of electricity bill and GaN device are used. The lower the original data center power factor is, the shorter the payback time is, and more profit can be obtained. When data center server loading decreases, the profit gained by regulating reactive power on front-end rectifiers becomes lower, and longer time is required for paying off. Data center power rating has slight impact on the required payback time, especially when the power capacity is above 20 MW. Also, with the current market prices of electricity bill and GaN device, all data centers can gain profit within five years by conducting reactive power compensation on the front-end rectifiers.

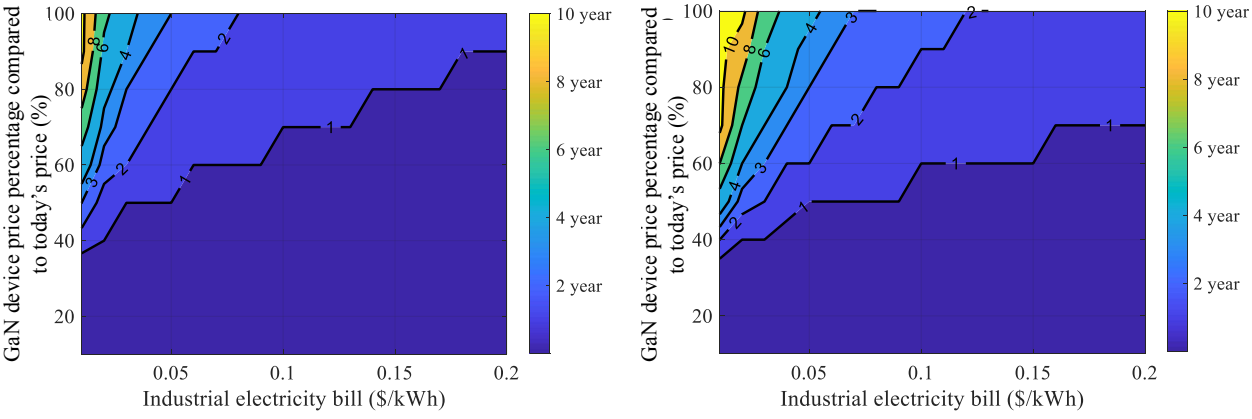
Figure 7.21 presents the number of years to pay back of data center System 3 compared to System 1 with various electricity prices and GaN device prices at server utilization $u = 100\%$ and $u = 50\%$ when data center original PF is 0.98 lagging and power rating is 50 MW. Generally, data centers can gain more profit and pay back earlier with higher electricity price and less expensive GaN device. For a data center power system with PF=0.98, it is recommended to adopt the GaN-based T-type totem-pole rectifiers whenever electricity price is above \$ 0.05/kWh since profit can be gained within four years. The data center is encouraged to use the traditional Si-based PFC rectifiers only if electricity price is below \$ 0.04/kWh and GaN device price remains above 70% of the current level.

In conclusion, providing reactive power compensation by the GaN-based T-type totem-pole rectifiers reduces data center power loss and system cost. More profit can be gained for data centers with lower original PF, higher server utilization rate, lower GaN device price and higher electricity price.



(a) (b)

Figure 7.20: Number of years to pay back of data center System 3 compared to System 1 with various PFs and power ratings at (a) $u = 100\%$; (b) $u = 50\%$ when electricity price is \$ 0.07/kWh and GaN device GS66508T price is \$ 12.45.



(a) (b)

Figure 7.21: Number of years to pay back of data center System 3 compared to System 1 with various electricity prices and GaN device price rates at (a) $u = 100\%$; (b) $u = 50\%$ when PF is 0.98 lagging and power rating is 50 MW.

7.4 Summary

In this chapter, hardware prototypes are designed and implemented to verify the idea of using GaN-based rack-level front-end rectifiers for reactive power regulation in data centers. To validate the design of the GaN-based T-type totem-pole rectifier, a 1.6 kVA rectifier prototype is built and tested. Experimental results show that the rectifier is able to regulate reactive power and realize full-range ZVS operation. The measured steady-state efficiency reaches 98.9% at full load and 98.7% at half load. Transient operations during reactive power variations are also demonstrated. The rectifier prototype achieves smooth dynamic response with flexible reactive power regulation.

In order to validate the capability of reactive power regulation in a data center power system, the data center power emulator is modified with the modeling of GaN-based T-type totem-pole front-end rectifiers. A supervisory central controller is added to determine the reactive power reference assigned to the front-end rectifiers. The data center power emulator is implemented on the HTB with a regional power network. Experimental emulation results show that the front-end rectifiers are able to compensate the system reactive power and correct the grid terminal power factor. Also, the front-end rectifiers can generate or consume more reactive power to achieve flexible PF regulation and support the power grid.

In addition, system cost and power loss of data centers are evaluated. By employing the GaN-based T-type totem-pole rectifier for reactive power compensation, data center achieves lower power loss and system cost. It is more profitable by using the front-end rectifiers for reactive power compensation in data centers with lower original PF, higher server utilization, lower GaN device price, and higher electricity price.

Chapter 8

Conclusion and Future Work

8.1 Conclusion

8.1.1 Summary of the Work

In this thesis, methods of characterizing the data center power performance and improving the data center energy usage efficiency are proposed.

In terms of evaluating the system power performance, power load modeling and hardware-based emulation are two effective approaches. The existing research efforts on data center power modeling and emulation have limitations in completeness, precision, capability of dynamic performance prediction, and accessibility. There is a lack of a accurate data center dynamic load model and flexible converter-based data center power emulator.

In order to investigate data centers' load characteristics, a dynamic data center power model is proposed. The data center power model is able to predict the dynamic performance for two reasons: (1) it includes complete models of the power supply system, cooling system, server load and thermal load; (2) it contains detailed modeling of power converters and control loops. Based on the data center model and the HTB platform, a data center power emulator is developed to perform realistic grid power test and assess the grid dynamic performance. A generalized discrete model is proposed to implement the emulator in two VSIs, serving as an all-in-one power load. The data center emulator is validated in a regional power network in the HTB, and transient characteristics during voltage sags and server load

variations are demonstrated. The proposed data center power model and emulator provide an effective and easy-to-use tool to investigate the data center internal operation as well as to conduct grid-related experiments.

For improving the data center energy usage efficiency, the main research efforts are made on advancing the design of the rack-level front-end rectifier. Bridgeless PFC converters are attractive for the front-end rectifier owing to the simple topology and low power loss. High-voltage GaN device and ZVS control strategies provide more opportunities to achieve higher power efficiency and power density of the front-end rectifier. A GaN-based CRM PFC rectifier is designed for the data center power supply. A totem-pole PFC topology is employed to achieve simple structure and low part count. Full-line-cycle ZVS control is implemented to realize high efficiency. A 1.5 kW CRM PFC rectifier prototype is built and demonstrated with $> 98.8\%$ peak efficiency.

One challenge of the GaN-based CRM totem-pole PFC with model-based ZVS control is the current distortion issue. To realize low current THD and high PF, current distortion mechanisms including the line-cycle current distortion and ac line zero-crossing current spike are analyzed. Effective methods are proposed to mitigate each kind of current distortion. Implemented with the mitigation approaches, the measured current THD of the 1.5 kW PFC prototype at full load is decreased from 8.6% to 3.2%, and PF is increased from 0.98 to 0.993. Also, the peak efficiency is improved from 98.8% to 99% with current THD below 5% in all tested power loads. The effectiveness of the current distortion mitigation methods are also verified in a GaN-based 100 W 6.78 MHz WPT system. In addition, the impact of high-frequency noise on the ZVS control of the PFC rectifier is explored in the WPT system, and noise immunity methods are proposed to achieve stable operation of the WPT system with fast dynamic response during load change.

Another important aspect of improving the data center energy usage efficiency is to reduce the power loss and system cost in reactive power compensation. Instead of using conventional centralized power compensators, the idea of using GaN-based front-end rectifiers for data center reactive power compensation is proposed, which is advantageous in achieving lower power loss, reducing system cost, and helping popularize the usage of commercial GaN devices in data centers. To achieve the idea, full-line-cycle ZVS modulation of the CRM

rectifier is extended to both unity and non-unity PF conditions. Challenges of reactive power operation occur during ac-line zero-crossing, including the high peak switching frequency at ac current zero-crossing and current distortion at ac voltage zero-crossing. To restrict the switching frequency during the ac current zero-crossing, a frequency limitation method is proposed. Also, a GaN-based CRM T-type totem-pole rectifier is proposed to overcome the ac voltage zero-crossing issue, which also realizes full-range ZVS and flexible reactive power regulation. In addition, a control strategy is proposed to implement the ZVS control and reactive power regulation. A 1.6 kVA prototype of the GaN-based T-type totem-pole rectifier is built and demonstrated with 98.9% full-load peak efficiency and flexible reactive power regulation.

The capability of reactive power regulation by front-end rectifiers is also validated through the data center power emulator, which is updated by replacing the front-end rectifier model with the model of the GaN-based T-type totem-pole rectifier. Experimental emulation within a regional power system is conducted with flexible reactive power regulation on the grid terminal, and the according dynamic performance is analyzed. Based on the evaluation of data center system cost and power loss, it is concluded that, performing reactive power operation on the front-end GaN-based T-type totem-pole rectifiers is an efficient and profitable alternative to conventional centralized power compensators for data centers.

8.1.2 Contributions

The contributions of this work are summarized as follows:

(1) A dynamic data center power model is proposed to predict the data center load characteristics. The model is advantageous in complete modeling, capability of predicting dynamic performance, and achieving reactive power regulation via rack-level front-end rectifiers. The corresponding converter-based data center power emulator is developed, which acts as an all-in-one load in the HTB and can be used to evaluate the power grid dynamic performance.

(2) A full-line-cycle ZVS modulation for both unity PF operation and non-unity PF operation is proposed for GaN-based CRM rectifiers. A ZVS margin constraint is

proposed to ensure full-line-cycle ZVS with a time margin, and a frequency limitation method is proposed to limit the peak switching frequency.

(3) Current distortion mitigation methods for the GaN-based CRM totem-pole PFC rectifier are proposed. A specified device switching sequence with a blanking time and an auxiliary circuit are proposed to eliminate the input voltage zero-crossing current spike. A current sensing delay compensation method and noise immunity approaches are proposed to mitigate the line-cycle current distortion and ensure control stability in noise-susceptible environment.

(4) A GaN-based CRM T-type totem-pole rectifier is proposed and the associated control strategy with reactive power operation and full-range ZVS operation is developed.

8.1.3 Publication List

Journal Papers

(1) **J. Sun**, L. Zhu, D. Costinett, L. M. Tolbert, "Design of a GaN-based T-type totem-pole rectifier with full-range ZVS control and reactive power regulation", *IEEE Transactions on Power Electronics*, in review.

(2) **J. Sun**, S. Wang, J. Wang, L. M. Tolbert, "Dynamic model and converter-based emulator of a data center power distribution system," *IEEE Transactions on Power Electronics*, early access, Jan. 2022.

(3) **J. Sun**, H. Gui, J. Li, X. Huang, N. Strain, D. Costinett, L. M. Tolbert, "Mitigation of current distortion for GaN-based CRM totem-pole PFC rectifier with ZVS control," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 290-303, 2021.

(4) J. Li, R. Qin, **J. Sun**, D. Costinett, "Systematic design of a 100 W 6.78 MHz wireless charging station covering multiple devices and a large charging area," *IEEE Transactions on Power Electronics*, vol. 37, no. 4, pp. 4877-4889, 2022.

(5) H. Gui, **J. Sun**, L. M. Tolbert, "Charge pump gate drive to reduce turn-ON switching loss of SiC MOSFETs," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13136-13147, Dec. 2020.

(6) S. Ji, X. Huang, **J. Sun**, W. Giewont, F. Wang, L. M. Tolbert, "Short-circuit characterization and protection of 10-kV SiC MOSFET," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1755-1764, Feb. 2019.

Conference Papers

(1) **J. Sun**, L. Zhu, R, Qin, D. Costinett, L. M. Tolbert, D. Costinett, "A GaN-based T-type totem-pole rectifier with ZVS control and reactive power regulation," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, 2022, in review.

(2) **J. Sun**, S. Wang, L. M. Tolbert, D. Costinett, "Emulation of voltage sag event for a data center power distribution system," in *IEEE Applied Power Electronics Conference (APEC)*, Phoenix, AZ, 2021, pp. 126-133.

(3) **J. Sun**, R. Qin, J. Li, D. Costinett, L. M. Tolbert, "Design of a resonant reactive shielding coil for wireless power transfer system," in *IEEE Applied Power Electronics Conference (APEC)*, Phoenix, AZ, 2021, pp. 1565-1572.

(4) **J. Sun**, J. Li, D. Costinett, L. M. Tolbert, "A GaN-based CRM totem-pole PFC converter with fast dynamic response and noise immunity for a multi-receiver WPT system," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, 2020, pp. 2555-2562.

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8.2 Future Work

8.2.1 Microgrid Emulation with Data Center Load

As a large electric load, data centers consume significant energy and emit a large amount of CO_2 annually. To reduce the CO_2 emission and achieve more reliable power distribution infrastructure, green data centers with renewable energy integration has drawn increased attention and became more popular [224, 225].

Typically, a data center is located within a mircogrid with renewable energy resources like wind farm and photovoltaic (PV) system [226, 61]. As shown in Figure 8.1, the data center works as a critical load within the microgrid, which can be powered by either the grid terminal, the PV energy, or the microgrid generator.

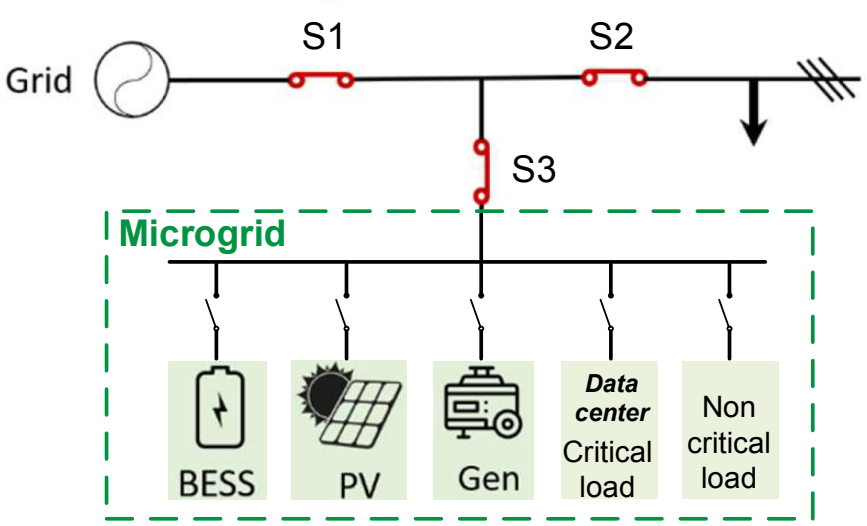


Figure 8.1: Typical microgrid with data center as critical load.

In terms of improving the grid transient stability and better designing the microgrid with data center load, dynamic performance during possible scenarios need to be investigated and evaluated. These scenarios include but are not limited to the following cases:

(1) Black start when the PV and battery begin to pick up the data center load and lead the microgrid to islanded mode;

(2) Islanding process when transitioning from grid-connected mode to islanded mode;

(3) During steady-state islanded operation, the power source of the data center load changes among battery, PV, and generator;

(4) Reconnection when transitioning from islanded mode to grid-connected mode;

(5) During steady-state islanded mode or grid-connected mode, data center server loading has large variations;

(6) Data center generates or absorbs extra reactive power to support the nearby load and help regulate the voltage;

Based on the CURENT HTB platform, the data center power emulator has been developed in this work, and [227] has developed a microgrid emulator. Future work can combine them together to develop a microgrid power emulator with data center load, and investigate the dynamic performances during potential scenarios.

8.2.2 Data Center Power Management System with Reactive Power Control

Since data center is a complicated system with power hierarchy and a diverse set of workloads, power management system is very important for achieving efficient power usage and ensuring power safety and reliability. The data center power management system should have the capabilities of centralized control, scalability, remote access, security, and flexibility [228, 229]. For example, Facebook developed a data center wide power management system named "Dynamo" that monitors the entire power hierarchy and makes

coordinated control decisions to safely and efficiently use provisioned data center power [230]. Dynamo is not a single supervisory central controller, but has a hierarchy of controllers that target different power stages.

If reactive power regulation is implemented in data center rack front-end rectifiers, the power management system should be updated to monitor the reactive power on the grid terminal and determine the reactive power assigned on each front-end rectifier. Also, given the versatile availability of the front-end rectifiers, assignment of the reactive power needs to be adjusted based on the server load distribution in order to obtain a high power usage efficiency. Figure 8.2 shows an example loss map of a data center front-end rectifiers, where the total power loss of the rectifiers with different Q assignments is predicted in possible server load distributions. Power rating of the rectifier is set as 1.6 kVA with $P_{rate} = 1.5$ kW, $Q_{rate} = 1.5$ kVA. The blanking area represents the operation range that the rectifier is overloaded, and the red dots stand for the operation points with minimum total power loss at different server load distributions. Based on the loss map, the central controller could assign reactive power reference instantaneously to achieve a lower system power loss.

Here, it is assumed that the power is evenly distributed within the front-end rectifiers. In practice, power distribution in a data center is more complicated with a diverse set of workloads and control strategies. Future efforts need to be made on the power management system to intelligently monitor the reactive power, conduct reactive power assignment with an efficiency optimization algorithm, and maintain the power safety and reliability.

8.2.3 Harmonic Current Compensation with Rack-Level Front-End Rectifiers

As aforementioned, reactive power generated within the data center is composed of displacement reactive power and distortion reactive power. The proposed GaN-based T-type totem-pole rectifier is only implemented with the function of reactive power regulation. It is also possible and necessary to implement harmonic current compensation on the front-end rectifiers to further improve the grid terminal power quality [231, 232].

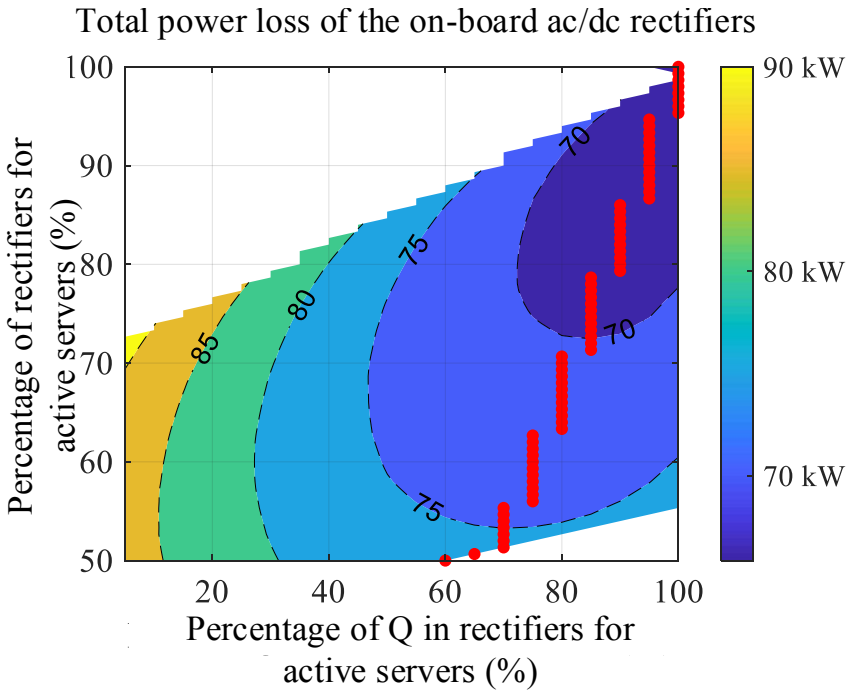
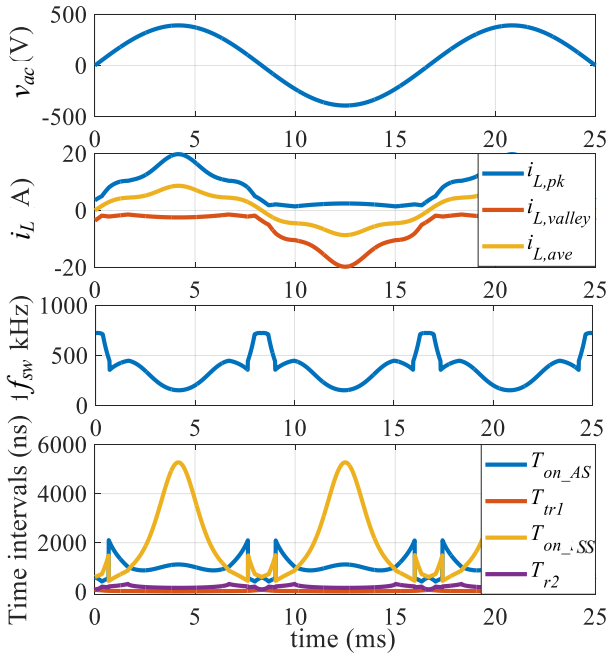


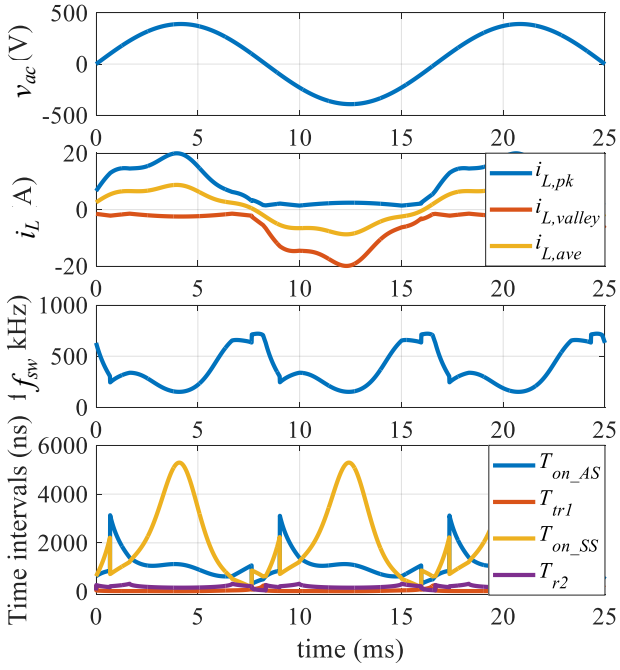
Figure 8.2: Total power loss of the front-end rectifiers with reactive power compensation in a 10 MW data center system at $u = 50\%$ as defined in Table 6.1, assuming power is evenly distributed within the rectifiers for active servers and within the rectifiers for idle servers.

Typically, a passive filter is used to filter high order harmonics, and the active filter cleans up the residual low-order harmonics (*i.e.,* up to 13_{th}). Similarly, in data center power system, the front-end rectifiers can act as parallel-distributed active filters, injecting certain harmonic current to compensate the original harmonic current. In order to achieve harmonic current compensation in a GaN-based CRM rectifier, the current reference for real-time calculation needs to be modified. i_{ref} should be composed of the fundamental current reference i_{ref_f} and the harmonic current reference i_{ref_h}, *i.e.,* $i_{ref} = i_{ref\_f} + i_{ref\_h}$. i_{ref_f} determines the rectifier power control, which is produced by the output voltage loop and reactive power loop. i_{ref_h} regulates the rectifier input current harmonics, which is from a top-level control in the data center. Figure 8.3 shows the example waveforms of the GaN-based T-type totem-pole rectifier with the 5_{th} order harmonic current compensation.

Specific implementation of the current reference needs to be addressed in the future work. A closed harmonic current control loop may be added to accurately control the input harmonic current [233]. Also, top-level control of determining the harmonic current reference for the individual front-end rectifier need to be designed, which may coordinate with the power management system to monitor and assign the harmonic current reference.



(a)



(b)

Figure 8.3: Analytical waveforms of the CRM T-type totem-pole rectifier with 5_{th} order harmonic current compensation at (a) unity PF; (b) 0.948 leading PF with $Q = -500$ kVAr, when $V_{in} = 277$ $\mathrm{V_{ac}}$, $V_o = 480$ $\mathrm{V_{dc}}$, $k_0 = 1.1$, $V_{boun} = 100$ V, $P = 1.5$ kW.

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Appendices

A Power Loss Model

The main principles for loss calculation in this part come from [127, 214, 215, 234]

A.1 Power Loss of CRM Rectifiers with ZVS Operation

For the CRM rectifiers with ZVS turn-on of GaN devices, major loss mechanisms include the device conduction loss, GaN device turn-off switching loss, inductor core loss and winding loss, and capacitor loss.

A.1.1 Device Conduction Loss

If approximating the inductor current as a triangular waveform with the maximum value at $i_{L,pk}$ and the minimum value at $i_{L,valley}$, the inductor RMS current is

$$i_{L,rms}(t) \approx \sqrt{\frac{1}{3}\left(i_{L,pk}(t)^2 + i_{L,valley}(t)^2 + i_{L,pk}(t)i_{L,valley}(t)\right)} \tag{1}$$

Since the two devices in one phase leg conduct alternatively, the total conduction loss in one phase leg is equivalent to one switch conducting all the time if neglecting the small dead times. Hence, the equivalent RMS currents of the GaN device and the Si device are $i_{L,rms\_GaN} \approx i_{L,rms\_Si} \approx i_{L,rms}$. The total GaN device conduction loss over the ac line cycle is

$$P_{cond,GaN} = \frac{2}{T_{line}} \int_0^{T_{line}/2} i_{L,rms\_GaN}(t)^2 R_{on\_GaN} dt \tag{2}$$

And the Si device conduction loss over the line cycle is

$$P_{cond,Si} = \frac{2}{T_{line}} \int_0^{T_{line}/2} i_{L,rms\_Si}(t)^2 R_{on\_Si} dt \tag{3}$$

where R_{on_GaN} and R_{on_Si} are the on resistances of the GaN device and Si MOSFET respectively.

A.1.2 GaN Device Switching Loss

Given soft-switching turn ON of the GaN devices is achieved, the dominant switching loss is the GaN device turn-OFF loss. The total GaN device turn-OFF loss over the line cycle is

$$P_{off,GaN} = \frac{2}{T_{line}} \int_0^{T_{line}/2} f_{sw}(t)\big(E_{off\_AS}(t) + E_{off\_SR}(t)\big)dt \tag{4}$$

where E_{off_AS}, E_{off_SR} are the turn-OFF energies for active and synchronous switches, and $E_{off\_AS}(t) = E_{off}(|i_{L,pk}(t)|)$, $E_{off\_SR}(t) = E_{off}(|i_{L,valley}(t)|)$ in the positive half cycle, $E_{off\_AS}(t) = E_{off}(|i_{L,valley}(t)|)$, $E_{off\_SR}(t) = E_{off}(|i_{L,pk}(t)|)$ in the negative half cycle. E_{off} is the simulated turn-OFF energy of the GaN deviece at different current levels.

The other part of the switching loss is the gate charge loss, which can be calculated as

$$P_g = Q_{gs} V_{gs} f_{sw} \tag{5}$$

where V_{gs} is the device gate-to-source voltage, and Q_{gs} is the gate charge.

A.1.3 Inductor Power Loss

Traditional Steinmetz Equation (SE) is not accurate for core loss calculation of the CRM operation with large current ripple. Instead, the generalized Steinmetz equation (GSE) proposed in [214] is adopted to estimate the core loss. The core loss density in each switching cycle is

$$p_v(t) = f_{sw}(t) \int_0^{t_{sw}(t)} k_1 \left|\frac{dB(t)}{dt}\right|^{\alpha} |B(t)|^{\beta-\alpha} dt \tag{6}$$

And the total core loss over the line cycle is

$$P_{core} = \frac{2}{T_{line}} \int_0^{T_{line}/2} p_v(t) V_{core} dt \tag{7}$$

where $B(t)$ is the instantaneous flux density derived by inductor current, V_{core} is the core volume, α, β, k_{loss} are Steinmetz coefficients of the specific core material, and k_1 is calculated as $k_1 = {k_{loss}}/{((2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} |\sin\theta|^{\beta-\alpha} d\theta)}, \theta = 0 - 2\pi$.

The winding loss includes the low-frequency dc copper loss and the high-frequency eddy current related losses. The dc winding loss is calculated based on the copper resistance.

$$P_{winding\_dc} = \frac{2}{T_{line}} \int_0^{T_{line}/2} i_{L,rms}(t)^2 R_{winding\_dc} dt \tag{8}$$

For the high-frequency CRM rectifier, litz wire is typically used to reduce the eddy current related loss. However, the commercial finite element analysis (FEA) tools cannot be used to directly simulate the ac winding loss due to the large number of litz wire strands. Instead, the square-field-derivative (SFD) method combining the FEA simulation and analytical calculation is adopted [215]. The ac winding loss over the line cycle is

$$\begin{aligned} P_{winding\_ac} &= \frac{2}{T_{line}} \int_0^{T_{line}/2} p_{winding\_ac}(t) dt \\ &= \frac{2}{T_{line}} \int_0^{T_{line}/2} \left(f_{sw}(t) \int_0^{t_{sw}(t)} \gamma \langle B_b^2 \rangle \left(\frac{d_{i_L(t)}}{dt}^2 dt \right) \right) dt \end{aligned} \tag{9}$$

where B_b is the normalized flux with 1 A current obtained from the static field, γ is determined by parameters of the specific litz wire [215]. Hence, the total inductor loss is

$$P_{loss,L} = P_{core} + P_{winding\_dc} + P_{winding\_ac} \tag{10}$$

A.1.4 Capacitor Power Loss

Capacitor loss of the CRM rectifier occurs at the input capacitor and the output capacitor due to the equivalent series resistance (ESR) R_{Cin}, R_{Co}. Since the capacitors absorb the high-frequency current ripples, RMS values of the ripple currents are required for the loss calculation. The instantaneous RMS currents of input and output capacitors are

$$\begin{cases} i_{Cin,rms}(t) = \sqrt{\frac{T_{on\_AS}(t)}{3t_{sw}(t)} \left((i_{L,valley}(t) - I_o)^2 + (i_{L,pk}(t) - I_o)^2 + (i_{L,pk}(t) - I_o)(i_{L,valley}(t) - I_o) \right)} \\ i_{Co,rms}(t) = \sqrt{\frac{T_{on\_SS}(t)}{3t_{sw}(t)} \left((i_{L,valley}(t) - i_{in}(t))^2 + (i_i(t) - i_{in}(t))^2 + (i_{L,pk}(t) - i_{in}(t))(i_{L,valley}(t) - i_{in}(t)) \right)} \end{cases} \tag{11}$$

where $T_{on\_AS}(t)$, $T_{on\_SS}(t)$ are the conduction time of the active and synchronous switches, and I_o is the dc output current that is $I_o = {}^{P_o}/_{V_o}$. Hence, the capacitor ESR losses are

calculated as

$$\begin{cases} P_{esr,Cin} = \frac{2}{T_{line}} \int_0^{T_{line}/2} i_{Cin,rms}(t)^2 R_{Cin} dt \\ P_{esr,Co} = \frac{2}{T_{line}} \int_0^{T_{line}/2} i_{Co,rms}(t)^2 R_{Co} dt \end{cases} \tag{12}$$

A.2 Power Loss of CCM Boost PFC Rectifier

Traditional boost PFC rectifier operates in continuous conduction mode (CCM) with hard switching. Major components of the PFC include the front-end diode rectifier, boost inductor L_b, active switch S, boost diode D, and the dc-link capacitor C_{dc}. Assuming the input current waveform is sinusoidal and the PFC power factor is unity, the input RMS current is calculated as $I_{rms} = {}^{P_o}/_{(\eta V_{rms})}$, where V_{rms} is the input voltage RMS value, P_o is the output power, and η is the converter efficiency. Then the instantaneous input current is $i_{in}(t) = \sqrt{2} I_{rms} \sin(\omega t)$, with given input voltage $v_{in}(t) = \sqrt{2} V_{rms} \sin(\omega t)$, and $\omega = 2\pi f_{line}$.

A.2.1 Bridge Rectifier Power Loss

Conduction loss is the dominant power loss of the ac line diode rectifier, which is

$$P_{loss,B} = \frac{2}{T_{line}} \int_0^{T_{line}/2} 2 i_{in}(t) V_{f,bridge} dt \tag{13}$$

where $V_{f,bridge}$ is the forward voltage drop of the bridge rectifier diode, typically $V_{f,diode} = 0.7 - 1$ V.

A.2.2 Boost Inductor Power loss

Assuming the average inductor current $i_{L,ave} = i_{in}$ and the peak-to-peak inductor current ripple is $\triangle I_{L,ripple}$, *e.g.,* $\triangle I_{L,ripple} = 25\%$ in CCM operation, the minimum and maximum inductor currents are represented as $i_{L,min}(t) = i_{in}(t)(1 - 0.5\triangle I_{L,ripple})$ and $i_{L,max}(t) = i_{in}(t)(1 + 0.5\triangle I_{L,ripple})$. Then the inductor RMS current is

$$i_{L,rms}(t) = \sqrt{\frac{1}{3}\big(i_{L,min}(t)^2 + i_{L,max}(t)^2 + i_{L,min}(t) i_{L,max}(t)\big)} \tag{14}$$

The inductor loss is composed of inductor copper loss and core loss. For the CCM boost PFC with small current ripple, the copper loss is

$$P_{L,copper} = \frac{2}{T_{line}} \int_0^{T_{line}/2} i_{L,rms}(t)^2 DCR dt \tag{15}$$

where DCR is the dc resisitance of the copper wire.

Core loss is generated by the changing magnetic flux field within the core material. So the instantaneous ac flux swing is required for estimating the core loss. For a toroidal core with given path length l_e and N winding turns, the minimum and maximum magnetic forces H_{min}, H_{max} are

$$\begin{cases} H_{min}(t) = \frac{N i_{L,min}(t)}{l_e} \\ H_{max}(t) = \frac{N i_{L,max}(t)}{l_e} \end{cases} \tag{16}$$

Then, the minimum and maximum ac flux densities B_{min}, B_{max} can be predicted according to the curve-fitted $B-H$ function [234]. For example, the flux density of 60 μ Kool core material is

$$B = \left(\frac{a + bH + cH^2}{a + dH + eH^2}\right)^x \tag{17}$$

where a, b, c, d, e, x are the related coefficients. For 60 μ Kool core material, $a = 1.658 \times 10^{-2}$, $b = 1.831 \times 10^{-3}$, $c = 4.621 \times 10^{-3}$, $d = 4.7 \times 10^{-3}$, $e = 3.833 \times 10^{-5}$, $x = 0.5$. Based on the curve-fitted $B-H$ function, the minimum and maximum flux densities B_{min}, B_{max} are solved, and the instantaneous ac flux swing is

$$\triangle B(t) = \frac{B_{max}(t) - B_{min}(t)}{2} \tag{18}$$

Hence, the core loss density can be estimated based on the Steinmetz equation with

$$p_v(t) = k \triangle B(t)^\alpha f_{sw}^\beta \tag{19}$$

where k, α, β are Steinmetz coefficients of the core material which can be determined from curve fitting. The average core loss along the line cycle is

$$P_{L,core} = \frac{2}{T_{line}} \int_0^{T_{line}/2} p_v(t) V_e dt \tag{20}$$

where V_e is the core volume. The total inductor loss is the sum of the copper loss and the core loss, as

$$P_{loss,L} = P_{L,copper} + P_{L,core} \tag{21}$$

A.2.3 MOSFET Power Loss

MOSFET loss includes the conduction loss and switching on/off loss. For the boost PFC, the MOSFET RMS current is

$$i_{S,rms}(t) = i_{L,rms}(t)\sqrt{d(t)} \tag{22}$$

where $d(t)$ is the instantaneous duty cycle that is $d(t) = 1 - {}^{v_{in}(t)}/_{V_o}$. Thus, the conduction loss of the MOSFET is

$$P_{cond,S} = \frac{2}{T_{line}} \int_0^{T_{line}/2} i_{S,rms}(t)^2 R_{on,S} dt \tag{23}$$

where $R_{on,S}$ is the on-resistance of the MOSFET, usually assuming $R_{on,S(100^\circ)} = 1.8 R_{on,S(25^\circ)}$.

Switching loss of the MOSFET is predominantly composed of the $i - v$ overlap loss during turning on/off, the loss dissipated on the output capacitance C_{oss} during charging/discharging, and the gate charge loss. The $i - v$ overlap loss is

$$P_{ivloss,S} = \frac{2}{T_{line}} \int_0^{T_{line}/2} \frac{1}{2}\big(i_{L,min}(t) V_o t_{on} + i_{L,max}(t) V_o t_{off}\big) dt \tag{24}$$

where t_{on}, t_{off} are the turn-on time and turn-off time, which are functions of gate voltage V_g, gate resistance R_g, threshold voltage V_{th}, junction capacitance C_{iss}, C_{rss}, etc. The output capacitance loss is

$$P_{coss,S} = \frac{1}{2} C_{eq} V_o^2 f_{sw} \tag{25}$$

where C_{eq} is the equivalent output capacitance at V_o based on the charge balance. The gate charge loss is

$$P_{g,S} = Q_{gs} V_{gs} f_{sw} \tag{26}$$

where V_{gs} is the gate-to-source voltage of the MOSFET, and Q_{gs} is the gate charge. The final MOSFET power loss is

$$P_{loss,S} = P_{ivloss,S} + P_{coss,S} + P_{g,S} \tag{27}$$

A.2.4 Boost Diode Power Loss

Power loss of the diode mainly consists of the conduction loss and the reverse recovery loss. To calculate the conduction loss, RMS current of the power diode is

$$i_{D,rms}(t) = i_{L,rms}(t)\sqrt{1 - d(t)} \tag{28}$$

The conduction loss is then calculated as

$$P_{cond,D} = \frac{2}{T_{line}} \int_0^{T_{line}/2} i_{D,rms}(t) V_{f,diode} dt \tag{29}$$

where $V_{f,diode}$ is the forward voltage drop of the diode.

Diode reverse recovery loss occurs during the turn-off process, which is

$$P_{rr,D} = \frac{1}{2} V_o Q_{rr} f_{sw} \tag{30}$$

where Q_{rr} is the is the reverse recovery change of the diode. The final diode loss is

$$P_{loss,D} = P_{cond,D} + P_{rr,D} \tag{31}$$

A.2.5 Capacitor loss

Similar with the GaN-based CRM rectifier, capacitor loss of the boost PFC includes the input capacitor and output capacitor ERS losses. The instantaneous RMS currents of input

and output capacitors are

$$\begin{cases} i_{Cin,rms}(t) = \sqrt{\frac{1}{3}d(t)\big((i_{L,min}(t)-I_o)^2+(i_{L,max}(t)-I_o)^2+(i_{L,max}(t)-I_o)(i_{L,min}(t)-I_o)\big)} \\ i_{Co,rms}(t) = \sqrt{\frac{1}{3}(1-d(t))\big((i_{L,min}(t)-i_{in}(t))^2+(i_i(t)-i_{in}(t))^2+(i_{L,max}(t)-i_{in}(t))(i_{L,min}(t)-i_{in}(t))\big)} \end{cases} \tag{32}$$

And the capacitor ESR losses are

$$\begin{cases} P_{esr,Cin} = \frac{2}{T_{line}}\int_0^{T_{line}/2} i_{Cin,rms}(t)^2 R_{Cin}dt \\ P_{esr,Co} = \frac{2}{T_{line}}\int_0^{T_{line}/2} i_{Co,rms}(t)^2 R_{Co}dt \end{cases} \tag{33}$$

Vita

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