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Acoustoelectric Amplification in Piezoelectric-Silicon Micromachined Lamb Wave Devices

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ACOUSTOELECTRIC AMPLIFICATION IN PIEZOELECTRIC-SILICON MICROMACHINED LAMB WAVE DEVICES

by

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ABSTRACT

In this dissertation, heterostructured micro-acoustic devices are explored that leverage the interactions between acoustic phonons and electrons to enable radio frequency (RF) signal amplification or attenuation. Thin films of piezoelectric and semiconductor material are tailored into a heterostructure that allows for a strong acoustoelectric (AE) effect due to the combination of high electromechanical coupling and high electron drift velocity in said films respectively. In such devices, the relative electron drift and acoustic velocities could determine whether the RF signal undergoes AE gain or loss, rendering the device non-reciprocal. This is a highly sought-after property for building isolators and circulators which facilitate full-duplex communication and interference cancellation in forthcoming generations of telecommunication. The AE effect attracted a great deal of attention during the mid-twentieth century, ultimately leading to the invention of interdigital transducers for excitation of surface acoustic waves as the preferred enabler of such effect which is still being investigated. However, the widespread application of such class of AE components is hindered by their poor performance metrics such as low power efficiency and limited frequency scaling. In this dissertation, by taking advantage of the superior properties of Lamb waves, namely, higher frequency scaling and lower insertion loss at larger available bandwidth, power-efficient and high power-handling AE devices are realized in a lithium niobate on silicon micromachined platform. Through this platform in this work, at few milliwatts of bias power, more than 30 dB of AE gain with larger than 40 dB nonreciprocal transmission is realized in a sub-millimeter form factor. This novel platform enables single-chip realization of frequency-disperse high power-handling ultrasonic signal processors with numerous functionalities such as gain, non-reciprocal behavior, tunable attenuation, insertion delay, and

switching. This could significantly reduce the number of components in an RF frontend module, shrink their footprints, and facilitate packaging.

To Julia, Nana, Baba, and my furry buddy Remy

ACKNOWLEDGMENTS

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LIST OF ABBREVIATIONS

ADS	Advanced Design System
AE	Acoustoelectric
AlN	Aluminum Nitride
AlScN	Aluminum Scandium Nitride
Ar	Argon
Au	Gold
BAW	Bulk Acoustic Wave
BOE	Buffered Oxide Etchant
BOX	Buried Oxide Layer
CdS	Cadmium Sulfide
CMOS	Complementary Metal-Oxide-Semiconductor
Cr	Chromium
DRIE	Deep Reactive Ion Etching
DUT	Device Under Test
EM	Electromagnetic
FBAR	Film Bulk Acoustic Resonator
FBW	Fractional Bandwidth
FDD	Frequency Division Duplex
FEA	Finite Element Analysis
GHz	Gigahertz
HD	Half-Duplex

HF	Hydrofluoric acid
IBFD	In-Band Full-Duplex
IC	Integrated Circuit
ICP	Inductive Coupled Plasma
IDT	Interdigital Transducer
IL	Insertion Loss
LFE	Lateral Field Excitation
LiF	Lithium Fluoride
LNA	Low Noise Amplifier
LNoSi	Lithium Niobate on Silicon
MEMS	Micro-Electro-Mechanical System
MHz	Megahertz
MIS	Metal-Insulator-Semiconductor
Mo	Molybdenum
NTR	Non-Reciprocal Transmission Ratio
PECVD	Plasma Enhanced Chemical Vapor Deposition
Q	Quality Factor
RF	Radio Frequency
RIE	Reactive Ion Etch
SAW	Surface Acoustic Wave
SCS	Single Crystalline Silicon
SEM	Scanning Electron Micrograph

SF$_6$	Sulfur Hexafluoride
SFIT	Slanted-Finger Interdigital Transducer
Si	Silicon
SiC	Silicon Carbide
SIC	Self-Interference Cancellation
SiO$_2$	Silicon Oxide
SMR	Solidly Mounted Resonator
SNR	Signal to Noise Ratio
SOI	Silicon on Insulator
TCF	Temperature Coefficient of Frequency
TDD	Time Division Duplex
TFE	Thickness Field Excitation
Ti	Titanium
TPoS	Thin-Film Piezoelectric-on-Substrate
UWB	Ultra-Wideband

CHAPTER 1: INTRODUCTION

Ultrasonic waves – acoustic waves having a frequency higher than 20 KHz – have been widely adopted as a powerful platform for radio frequency (RF) analog signal processing by enabling lower loss relative to electromagnetic (EM) waves as well as significant device size reduction. Since the acoustic velocity is a few orders of magnitude smaller than that of the EM waves, for applications with size constraints, ranging all the way up to super high frequencies (~30 GHz), the acoustic domain is preferred. Acoustic resonators operating in KHz range, traditionally made of Quartz [1] and more recently demonstrated in silicon (Si) with extreme size reduction [2, 3], are commercially used as the frequency selective component of the real-time clocks. Alternatively, MHz and GHz range acoustic resonators along with frequency divider circuitry are utilized for this purpose [4]. The same scheme is leveraged to realize resonant sensors in which respective to a change of a targeted physical parameter, the resonance frequency shifts. By tracking the resonance frequency, the variation of the targeted physical parameter is obtained. A system at resonance is most sensitive to such physical changes, thus, resonant sensors could offer superior sensitivity. Additionally, the readout interface and circuitry are much simpler for reliable tracking of the frequency rather than that of the electric voltage or current. Countless number of ultrasonic resonant sensors in the form of resonant gyroscopes [5, 6], accelerometers [7, 8], pressure sensors [9, 10], mass sensors [11, 12], chemical sensors [13, 14], to name a few, have been reported. Acoustic resonators, furthermore, in the forms of surface acoustic wave (SAW) resonators, film bulk acoustic resonators (FBAR), and solidly mounted resonators (SMR) are currently omnipresent in RF frontend modules for analog filtering purposes. A few comprehensive surveys have been published on this class of filters [15, 16].

Driven by the increased connectivity, the internet of things paradigm, increased data rate, and the subsequent need for better spectral efficiency, full-duplex communication seems inevitable. While today's wireless systems rely on separating the transmit and receive in either the time or frequency domain (i.e., half-duplex), full-duplex could be realized by separating signals based on their propagation direction. This would require augmenting the frontend modules, made of predominantly reciprocal components, with non-reciprocal components such as isolators and circulators. However, currently, most of such non-reciprocal devices are ferrite based [17] which are bulky, lossy, and most importantly, not compatible with integrated circuits (IC); therefore, other solutions for breaking the reciprocity are essential. In the acoustic domain, because of the interactions between acoustic phonons and charge carriers, also known as the acoustoelectric (AE) effect [18], acoustic waves could be amplified or attenuated depending on some properties of the charge carriers. Such phenomenon has been demonstrated for SAW propagating on a piezoelectric substrate with a thin semiconductor layer deposited on its propagation path [19] or held at its proximity with a small air-gap via spacers [20]. The inherent problem with the former approach is that deposited film if too thick would be detrimental to the SAW; conversely, attaining a high carrier mobility in deposited ultra-thin films is challenging. The latter approach, on the other hand, suffers from reduced AE coupling and challenging fabrication process with limited scalability. In addition, SAW practically has a limited operation frequency, well below what is required for covering the sub-6 GHz bands of the new radio. Therefore, solutions with higher frequency scalability are needed that if efficiently implemented, could enable numerous highly sought-after functionalities such as non-reciprocity, signal amplification, amplitude tuning, to name but a few, through the AE effect.

In this dissertation, it is experimentally demonstrated that by taking advantage of the high coupling between the piezoelectrically generated Lamb waves and electrons propagating laterally within micromachined piezoelectric-silicon waveguides, the AE effect and the subsequent non-reciprocal transmission can be efficiently realized. The organization of the rest of this dissertation is as follows. In chapter two, a background is presented on the subject of piezoelectricity, which enables the transduction between the acoustic waves and RF signals as well as the AE interactions with the semiconductor; in addition, Lamb waves are briefly described as the targeted acoustic waves in this dissertation. This is followed by a short description of thin-film piezoelectric-on-substrate (TPoS) technology as the platform used for exploring the AE effect and finally the need for non-reciprocity in today's microwave communication and some of the solutions that are proposed to attain so. In Chapter three, the AE effect is described and a literature review on this phenomenon is presented. In chapter four, the initial feasibility studies and proof-of-concept experiments are described using aluminum nitride (AlN) on Si micro-acoustic cavities. Chapter five introduces lithium niobate (LN) on Si micro-acoustic waveguides as a promising platform for realizing the AE effect and the main experimental results are presented in this chapter. The fabrication process for the introduced AlN-based and LN-based devices is elaborated in chapter six. The final chapter, chapter seven, is dedicated to a short discussion on the applications of the developed AE signal processing scheme and its performance metrics compared to the state-of-the-art AE SAW platforms.

CHAPTER 2: BACKGROUND

2.1   Piezoelectricity

An electrical signal can be transduced to acoustic or mechanical waves – and vice versa – by different means such as electrostatic, thermal, or piezoelectric schemes. The latter is believed to offer the highest coupling between the two domains, thus, lower transduction loss and better device performance. Piezoelectricity was discovered for the first time by Curie brothers in 1880 and is exhibited by almost all non-centrosymmetric crystal materials. In a piezoelectric crystal, subject to a mechanical deformation, electrical charge is developed; conversely, an electrical field induced therein causes a mechanical deformation. This is illustrated in Figure 1. Such couplings are defined by the general constitutive equations of piezoelectricity as follows

$$D = dT + \varepsilon^T E \tag{2-1}$$

$$S = d^t E + s^E T \tag{2-2}$$

where D is the electrical displacement, d is piezoelectric constant, T is stress, ε^T is permittivity at a constant stress, E is electric field, S is strain and s^E is compliance at a constant electric field and the superscript t stands for matrix transposition. In the most general form, the stress, strain, and electric fields are Cartesian vectors while the coefficients are tensors. Using this generalized form, (2-1) can be written as

$$\begin{bmatrix} D_1 \\ D_2 \\ D_3 \end{bmatrix} = \begin{bmatrix} d_{11} d_{12} d_{13} d_{14} d_{15} d_{16} \\ d_{21} d_{22} d_{23} d_{24} d_{25} d_{26} \\ d_{31} d_{32} d_{33} d_{34} d_{35} d_{36} \end{bmatrix} \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} + \begin{bmatrix} \varepsilon_{11} & \varepsilon_{12} & \varepsilon_{13} \\ \varepsilon_{21} & \varepsilon_{22} & \varepsilon_{23} \\ \varepsilon_{31} & \varepsilon_{32} & \varepsilon_{33} \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \tag{2-3}.$$
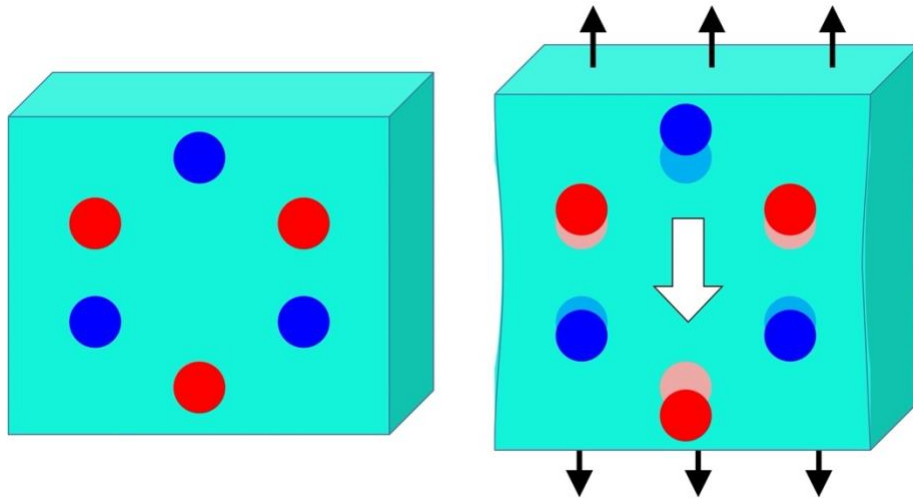
Figure 1. A piezoelectric crystal is neutral once there is no mechanical stress. Upon application of the stress, the deformation voids charge neutrality and a dipole moment appear. Conversely, application of a voltage results in mechanical deformation.

By exerting electric fields along the desired piezoelectric coefficient, electromechanical transduction takes place, exciting acoustic waves within the piezoelectric media. The excited acoustic waves could be trapped to form a resonant cavity, guided within a waveguide, or radiated into surrounding, with each category having vast applications for timing, signal processing, communication, sensing, and actuating, to name but a few. The transduction of the targeted acoustic waves is often realized by deposition of conductive electrodes on one side or both sides of the piezoelectric material, leading to lateral field excitation (LFE) and thickness field excitation (TFE) schemes, respectively. The piezoelectric materials used in this dissertation are AlN which is a CMOS compatible widely adopted piezoelectric and LN which is a promising material for realization of opto-electro-mechanical platforms. Table 1 and Figure 2, respectively show the physical properties and crystal structure of AlN and LN.

Table 1. Select material properties of AlN and LN used as the piezoelectric material herein.

	AlN	LN	Units
Density	3260	4700	kg/m^3
Acoustic Velocity (Longitudinal)	11300	6550	m/s
Acoustic Velocity (Shear)	6000	3590	m/s
Piezoelectric Coefficient (e_{31})	-0.58	0.3	C/m^2
Piezoelectric Coefficient (e_{33})	1.55	1.77	C/m^2
Piezoelectric Coefficient (e_{15})	-0.48	3.69	C/m^2
Relative Permittivity	8.3	30 to 40	-
Temperature Coefficient of Frequency	-25	-60 to -90	ppm/°C
Thermal Conductivity	280	5.6	W/mK
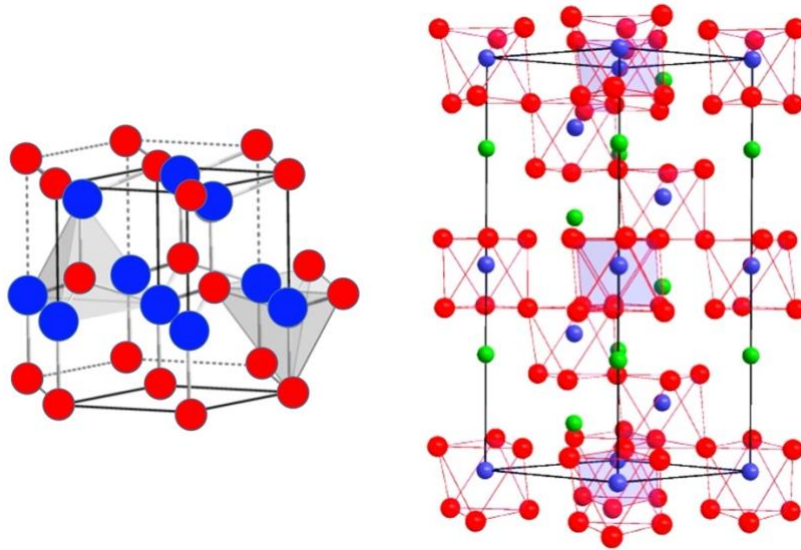
Figure 2. Crystalline structure of AlN (left) and LN (right).

2.2   Thin-Film Piezoelectric-on-Substrate Technology

Micro-acoustic resonators that are widely used for timing and filtering applications are mainly realized through either the electrostatic or the piezoelectric transduction mechanism. In the electrostatic scheme, the conductive resonant body is driven by electrostatic forces between parallel plates that are formed by narrow dielectric gaps which define the boundary of the resonant body. This class of micro-resonators, if fabricated from low acoustic loss materials such as polysilicon and single crystal Si (SCS), typically have very high quality factors (Q) of up to a few hundred thousand in vacuum [21, 22]. Therefore, this type of resonator is an excellent solution to replace quartz resonators in reference clock circuits [3, 23, 24]. The drawback of the electrostatic resonators, however, is that their electromechanical coupling is usually small, which also causes a very large motional impedance, up to several thousand ohms. This would increase the power consumption and makes interfacing the device with 50-ohm systems for RF filtering applications very challenging. In contrast with the electrostatic transduction, the electromechanical coupling of piezoelectric transduction is much larger. As a result, the motional impedance of piezoelectric micro-resonators is inherently lower than the electrostatic counterparts, especially at higher frequencies where the later becomes less efficient. Although, the values of Q reported for piezoelectric micro-resonators are not as high as the values obtained from electrostatic devices, piezoelectric micro-resonators have outperformed their electrostatic counterparts at high frequencies and particularly in applications with relaxed Q requirements such as filtering. By merging the high Q of electrostatic micro-resonators with the high electromechanical coupling of piezoelectric ones, despite some compromises in such performance metrics, TPoS micro-resonators have been developed [25]. The resonant micro-cavity in the TPoS platform comprises

a thin piezoelectric film with at least two metallic electrodes on both sides (TFE case) or one side (LFE case) of the film and stacked on top of a substrate (Figure 3). The free-standing device stack is usually suspended by a few anchors connected to the resonant body at displacement nodal points. This is to minimize the distortion of the mode-shape and the acoustic energy leakage known as the anchor loss. The substrate is chosen from martials with very low acoustic loss such as SCS, SiC, or diamond, enabling high Q resonance. In addition, the superior power-handling of the substrate compared to commonly used piezoelectric materials makes this class of micro-resonators more robust against thermally induced issues, ranging from non-linearities to device destruction at high drive power levels. The piezoelectric layer is actuated by applying an alternating electric field between the set of electrodes which should conform to the polarization induced in the device at a targeted resonance mode. This is to achieve the highest electromechanical coupling, although, such value would still be lower than that of pure piezoelectric micro-resonators due to the substrate presence in TPoS.
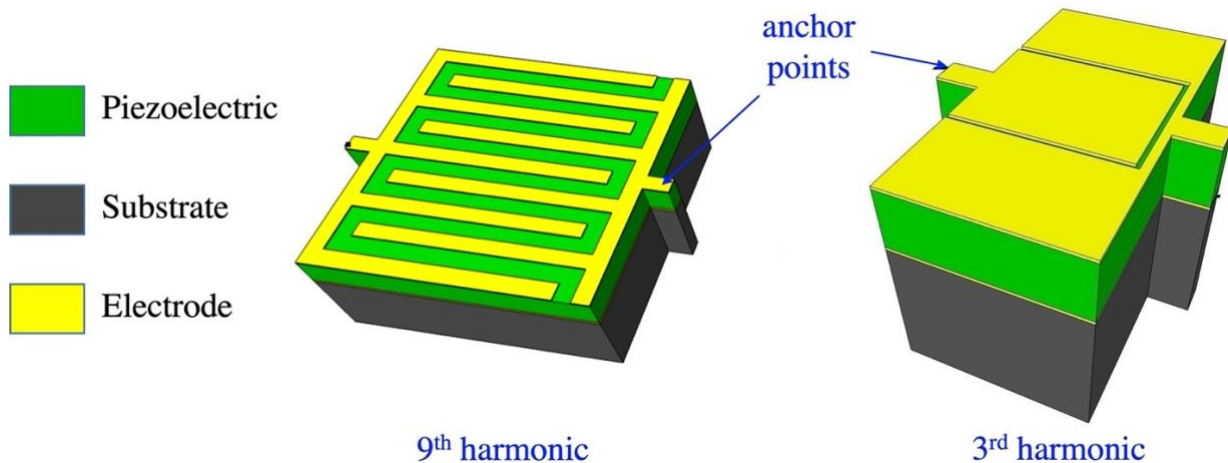
Figure 3. Schematic of TPoS resonators having lithographically-defined resonance frequency.

2.3   Lamb Waves

In a thin-film piezoelectric, once the acoustic waves are launched, for example by the interdigital transducer (IDT), Lamb waves can be formed as a result of the interference of waves reflected between the upper and lower boundaries of the film. Lamb waves could exhibit symmetric (S) and antisymmetric (A) modes and for lower frequencies when the wavelength is much larger than the film thickness, the vibrational elastic energy is mostly contained within the fundamental symmetric (S_0) and antisymmetric (A_0) modes. These two modes, shown in Figure 4, are also respectively referred as contour or extensional modes and flexural modes and the latter exhibits lower wave velocity and higher dispersion. Higher-order S and A modes are characterized by nodal planes in parallel to and within the film and appear only above a certain frequency. Lamb waves could offer high electromechanical coupling due to the highly overlapped confinement of elastic and electric fields in thin film. In addition, they practically enable operation frequencies beyond the limit of SAW because of having higher phase velocities which is influenced by the film thickness.
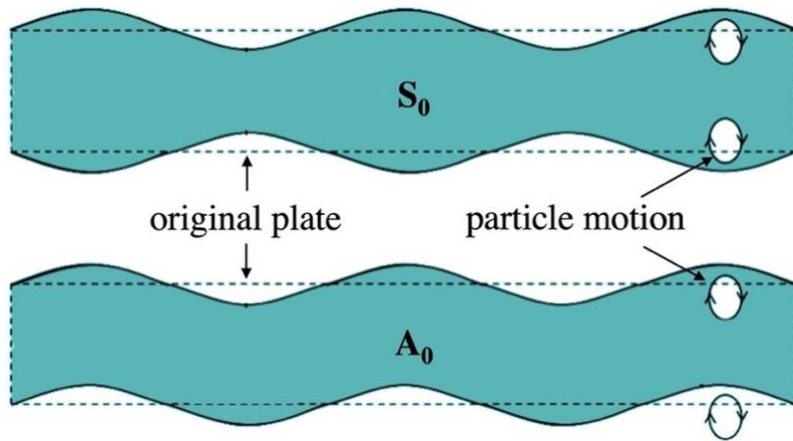
Figure 4. Cross-sectional view of thin films supporting S_0 (top) and A_0 (bottom) Lamb modes.

2.4 The Need for Non-Reciprocity

The rapidly growing connectivity and data rate calls for a larger number of filters, mainly acoustic, and amplifiers, mainly transistor based, to be integrated in the frontend modules. This increased complexity and congestion also calls for improving the spectral efficiency. Among the various methods that are considered to increase the spectral efficiency in wireless communication, in-band full-duplex (IBFD) operation has been attracted a great deal of attention as it could double the spectral efficiency in the physical layer [26, 27]. Most communication systems include terminals such as cell phones that function as both transmitters and receivers. Conventionally, almost all current systems operate in a half-duplex (HD) or out-of-band full-duplex manner. The 3G and 4G networks handle uplink versus downlink signals through two configurations of frequency division duplexing (FDD) and time division duplexing (TDD). With FDD, the transmit and receive signals are in different frequency bands with a wide separation. In other words, the uplink signal is sent in one block of the spectrum and the downlink is sent in another block. With TDD, the uplink is separated from the downlink by using different time slots in the same frequency band. As such, uplink signals will connect for a few seconds, and then downlink signals will connect for a few seconds. On the other hand, in IBFD protocol, a wireless terminal is allowed to transmit and receive simultaneously in the same frequency band. The caveat of this scheme is that the receiver would hear the transmitted signal and become desensitized. This is termed as self-interference and is a main challenge that is hindering the complete realization of IBFD operation. The transceivers are typically required to achieve 100 dB of self-interference cancellation (SIC) [28]. This is practically accomplished via multiple isolation stages, such as antenna isolation [29], analog isolation [30, 31], and digital isolation [32].
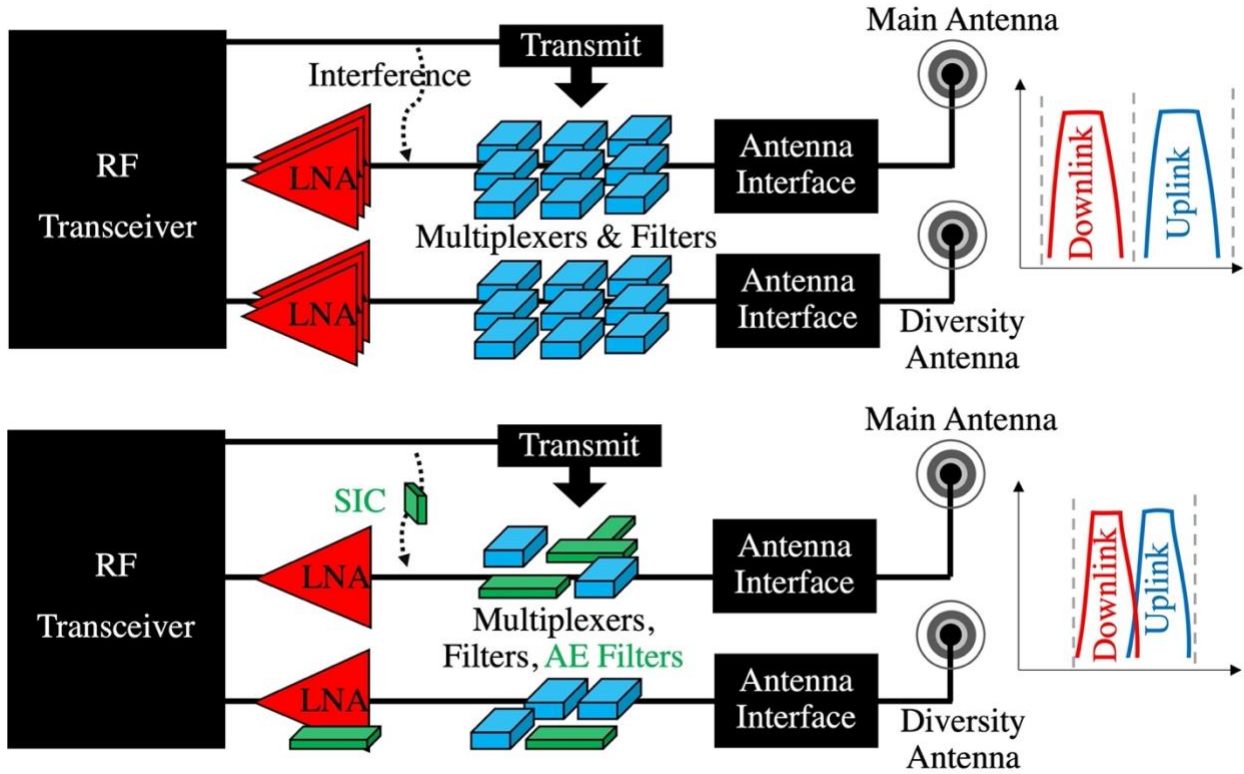
Figure 5. (Top) A simplified version of the receive chain in a typical RF frontend architecture with multiple branches of duplexers, filters, and low noise amplifiers (LNA) to support diverse communication bands. (Bottom) The potential elimination of multiple duplexers, filters, and LNAs by adopting the AE signal processing technology; AE circulators in antenna interfaces, AE filters and amplifiers in receive chains, and AE delay lines in SIC (shown as green components) could reduce the size and complexity of the frontend module despite the increased number of closely spaced channels with more stringent requirements.

With regards to SIC, circulators play a key role in providing isolation by interfacing the antenna with the frontend module and routing the signals only in the transmit to antenna and the antenna to receive directions [33]. In the analog domain, the transmitted signal could be tapped, processed with delay and attenuation, and subtracted from the signal in the receive path, so as to mimic the interference and provide SIC [34]. The circulator along with the analog domain provide about 40 to 50 dB of the total 100 dB SIC while the rest is accomplished in the digital domain.

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Since the main interference spectral power lies in the few 100 nanoseconds range [35], using micro-acoustic delay lines that provide such amount of insertion delay would be a promising solution for analog SIC. Such delays in a small form factor are only viable in the acoustic domain. By realizing non-reciprocity in same acoustic platform to build circulators, the pre-digital SIC could be ultimately realized on the same die. This is illustrated in Figure 5 where several AE components are integrated in an RF frontend module to provide amplification, filtering, circulation, and SIC.

It is worth mentioning that aside from RF communications, non-reciprocal components have niche applications for sensing, imaging, radar, and quantum processing. Non-reciprocal devices commercially available today, are based on magnetic materials, which are very bulky at low frequencies due to centimeter scale EM wavelength and lossy at higher frequencies, expensive, and most importantly incompatible with IC technology. A schematic breakdown of a typical magnetic circulator is shown in Figure 6, highlighting the complicated manufacturing process of this class of circulators. Therein, permanent magnets are incorporated to bias the ferrite material by a strong magnetic field and subsequently change the transmission direction. As a result, despite the very favorable properties that such devices could offer, for example in the wireless communications, their application has been limited to occasions where the cost and size are not priorities such as in radars and base stations, to name but two. It has been only recently that the technological advances have created an opportunity to reconsider the integration of magnet-free non-reciprocal devices into mainstream communication systems.
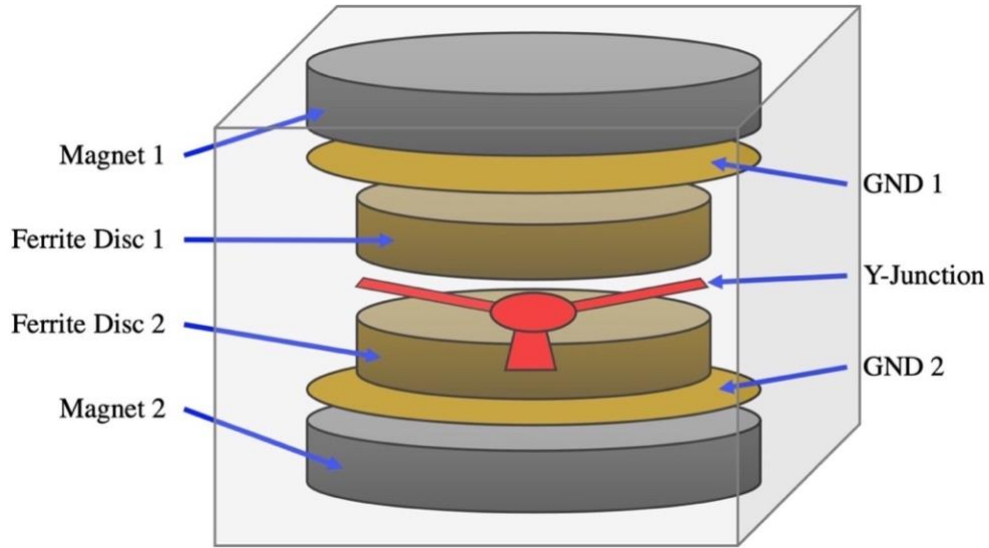
Figure 6. A breakdown of a typical magnetic-base non-reciprocal circulator highlighting the manufacturing complexity and the incompatibility of such class of devices with IC technology.

In order to achieve non-reciprocity, either linearity, time-invariance, or symmetry of the system must be violated. Some of these main approaches are briefly compared in Table 2. Several solutions based on material nonlinearities [36-38] have been proposed, however, the resulting narrow bandwidth and weak non-reciprocity largely limits the application of this class of non-reciprocal systems. With respect to time-modulation, periodic modulation of some components such as lumped element LC tanks [39, 40], micro-acoustic resonators [41, 42], or transmission lines [43, 44] have been explored. While this approach offers better performance compared to the non-linear approach, it requires a low jitter synchronizing clock for modulation, switches, or varactors which set a limit in the downscaling of size and power consumption. Aside from introducing geometric asymmetry in the system which predefines the signal transmission direction [45, 46], a fundamentally different approach is to take advantage of coupling across different domains of energy to enforce non-reciprocal behavior. For instance, non-reciprocity is achieved

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through utilization of directional momentum exchange processes between phonons and photons [47], electrons and photons [48], and phonons and electrons [49]. In the latter category, the electron-phonon interactions known as the AE effect have recently revived the interest of the research community. More details on the AE effect and its historical background are given in the following chapter.

Table 2. Summary of the main methods used to achieve non-reciprocity

	Approach			
	Ferrite	Non-Linearity	Modulation	Active
Bias	Magnetic	-	RF clock	DC
Form Factor	Large	Small	Small-Medium	Small
Bandwidth	High	Low	Medium-High	Medium-High
Non-reciprocity	Medium	Low	Medium-High	Medium-High

CHAPTER 3: THE ACOUSTOELECTRIC EFFECT

Due to the piezoelectricity, acoustic waves in a piezoelectric medium have an electric field associated with them, dividing the energy of waves into parts that produce the elastic deformation along with the accompanying electric field. In a simplifying case where the energy loss mechanism in the system is limited to interaction of acoustic phonons with charge carriers, when the piezoelectric material is an insulator – no free charge carriers present – the stress field is in phase with strain and the electric field, depending on the polarity of the piezoelectric coefficient, is either in phase or 180° out of phase and the system is lossless. This is depicted in Figure 7. In a piezoelectric semiconductor, however, as the acoustic wave propagates, it induces an accompanying space charge wave. This wave of charges, however, does not establish instantly and rather with a time constant, which is a function of geometry, distributed resistance, and capacitance [50]. Such delay results in the wave of induced charges to lag its normal position, leading to attenuation of acoustic waves which could constitute a significant energy loss mechanism. Assuming that electrons are the majority carriers in the piezoelectric semiconductor, they would bunch in the potential minima regions of the induced waves that trail behind the propagating acoustic wave. This leads to a higher electron density in regions where the electric field is directed along the wave propagation. Therefore, energy from the potential energy of the coupled electric field transfers to the kinetic energy of electrons, causing attenuation of the acoustic wave (Figure 7). By applying an electric field (E_D) in the same direction as the acoustic wave propagation, electrons in the semiconductor would drift with a velocity proportional to the applied electric field. Assuming μ is the mobility of electrons, the drift velocity will be $V_D = \mu E_D$. As long as the drift velocity of electrons is less than the acoustic velocity (V_A), the bunched electrons lag the acoustic

wave and the attenuation persists. Once V_D reaches V_A, the electrons would be synchronized with the induced wave and the attenuation vanishes. As V_D exceeds V_A, electrons (and the electric field) start leading the acoustic field and lose their momentum to it, to equalize V_D and V_A. In this scenario, the acoustic wave will be amplified as it travels through the piezoelectric semiconductor material (Figure 7). This phenomenon can be well extended to the case of a piezoelectric insulator, provided that a medium with free charge carriers is present in its vicinity so that the evanescent piezoelectrically induced electric field could penetrate such medium and interact with the charge carriers within.
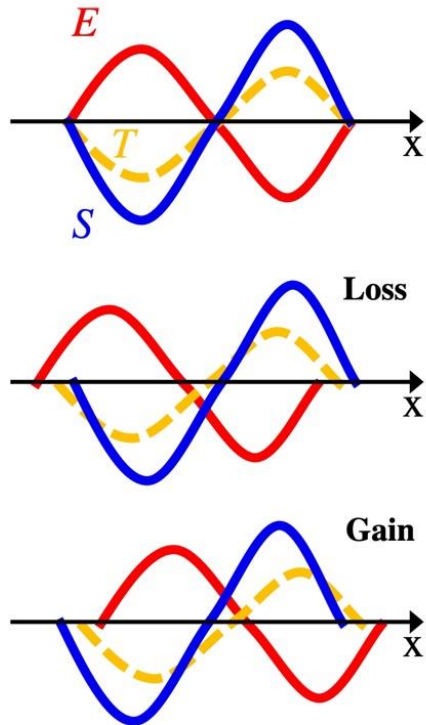
Figure 7. Strain (S), stress (T), and electric field (E) of a propagating acoustic wave in a piezoelectric insulator (top), piezoelectric semiconductor with loss (middle), and piezoelectric semiconductor with gain (bottom).

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3.1   AE Effect Through History

Research on the AE effect dates to forties when Shaposhnikov suggested that acoustic waves are affected by plasma and undergo attenuation [51]. Later, in 1953, Parmenter coined the term "Acousto-Electric Effect" by predicting the appearance of a DC current in parallel with the propagation of longitudinal acoustic waves [18]. The idea of the possibility of amplification of the acoustic waves by leveraging the momentum transfer from the DC current was discussed by Weinreich in 1956 [52] and experimentally proven by White in 1961 [49]. This was accomplished in cadmium sulfide (CdS), a piezoelectric semiconductor, through which supersonic drift of electrons led to bulk acoustic wave amplification. Nevertheless, the low electron mobility in such class of materials, being smaller than 400 cm^2/V.s, mandated application of high voltages, in kV range, ultimately resulting in low efficiency and heating problems. This bottleneck triggered the idea of providing the piezoelectricity in a medium separate from the semiconductor to allow for choice of proper materials independently. It was suggested in 1964 by Gulyaev that SAW propagating on a piezoelectric substrate along with a semiconductor layer at its vicinity would be a promising candidate [54]. The idea was that in such layered SAW device, due to the Coulomb drag or the electrostatic force between two electrically isolated media, the evanescent piezoelectrically generated electric field penetrates the adjacent semiconductor, interacts with its charge carriers, and forms a mutual coupling between the two domains. This could result in AE amplification of signal and can be considered the acoustic equivalent to an EM travelling wave tube amplifier (TWTA). In a TWTA, a beam of drifting electrons amplifies an RF signal that is guided in its proximity within a helix wire or EM resonant cavity [55]. Similarly, in a layered AE SAW amplifier, a current drifting in a semiconductor could amplify an RF signal that is

piezoelectrically transduced to a travelling SAW in its vicinity. To effectively excite SAW, a periodic pattern of electrodes matching the SAW wavelength was suggested to be used for the first time, marking the origin of IDT in 1965 [56]. This led to numerous demonstrations of SAW amplification on a piezoelectric substrate with a semiconductor layer deposited on top [19, 53, 57, 58] or held above it and along the SAW propagation path [20, 59, 60]. The original BAW AE amplifier and the subsequently proposed SAW counterparts based on the layers in contact or spaced-apart are shown in Figure 8.
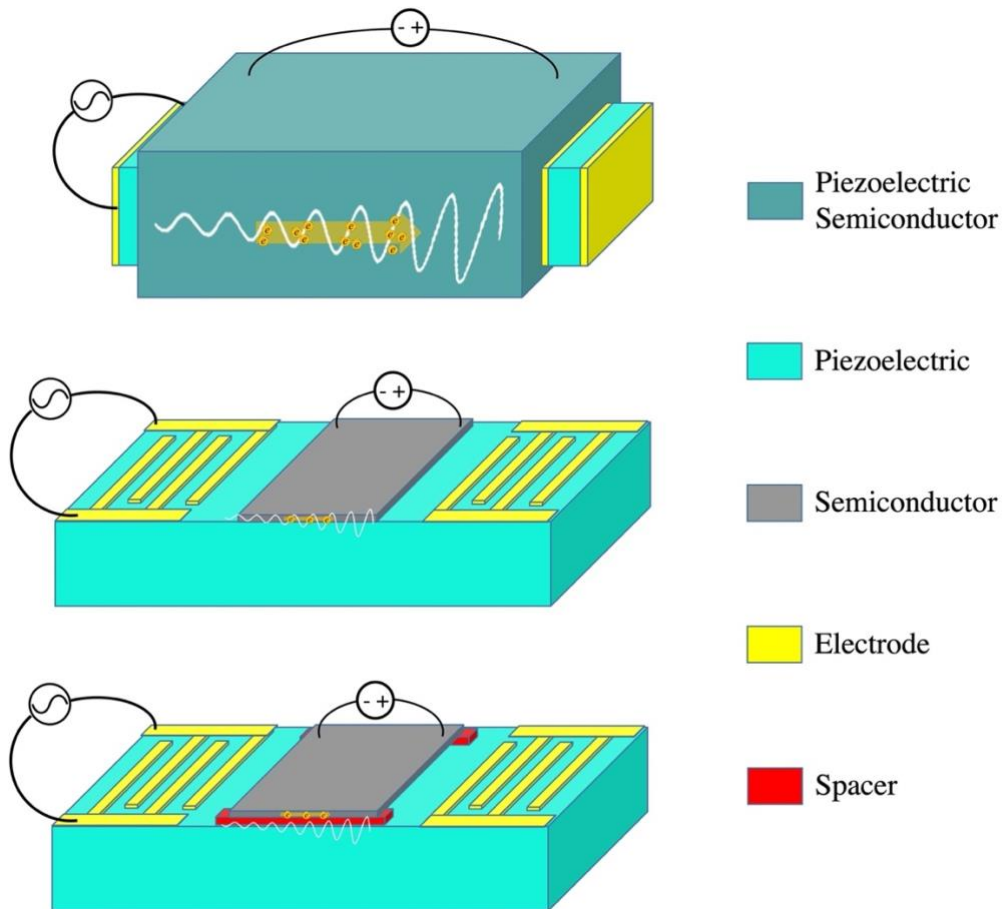
Figure 8. Conceptual schematic of AE amplifiers using a piezoelectric semiconductor slab for BAW amplification (top) and layered SAW amplifiers with the semiconductor film directly deposited on (middle) or held with a small gap above the piezoelectric substrate (bottom).

Upon introduction of IDT for SAW excitation, many active and non-reciprocal layered SAW delay lines and amplifiers were demonstrated, mostly having the monolithic piezoelectric-semiconductor configuration chosen over the devices with air-gap. The problem with the air-gap type devices was the need for an infinitesimally small air-gap to maintain a sufficient AE coupling between the semiconductor and evanescent electric fields; this made the fabrication quite challenging, especially in terms of scalability. The monolithic version, on the other hand, calls for an extremely thin deposited semiconductor layer, since otherwise SAW would not be efficiently excited at the interface of two media. A few of these SAW AE amplifiers with notable performance are summarized in Table 3. Despite achieving relatively promising results, to the extent which some researchers anticipated this technology could replace IC-based RF amplifiers, it was soon discovered that thin-film technology at the time cannot practically accommodate the implementations of such components [61, 62]. The major problem was found to be the transfer or growth of a very thin semiconductor in manner that first, does not heavily degrade the charge carrier mobility, second, does not contribute to trapped charges due to interface defects and dangling bonds, and third, does not introduce a very large SAW damping. These limitations resulted in a very high power consumption, low power efficiency, and poor noise performance as well as excitation of unwanted acoustic waves along with the targeted SAW and ultimately prevented them from coming to fruition. Another fundamentally limiting problem was stemming from the SAW itself and the fact that it travels in a depth of about one wavelength from the piezoelectric surface which becomes an extremely thin layer at high frequencies. Therefore, imperfections and damages introduced due to surface treatments makes SAW devices deficient at high frequencies, setting the practical operation frequency up to ~2 GHz. By the end of 20th

century, the interaction of SAW and two-dimensional electron gas (2DEG) received huge attention leading to the ongoing investigation of AE devices based on 2DEG [63, 64]. However, the resulting AE effect was weak as most material that readily form 2DEG suffer from poor piezoelectric properties [65-67]. It was until recently that advances in thin-film growth, transfer, and bonding enabled realization of high-performance SAW AE amplifiers based on strong piezoelectric materials such as LN [68-72]. Additionally, AE effect has been recently observed in Lamb mode TPoS micro-acoustic devices made of AlN on Si [73] and Ge [74] as well as LN on Si [75]. As mentioned, Lamb waves could offer higher electromechanical coupling, due to the localized elastic and electric fields with large overlap in thin-film, which allows the AE device to attain more gain in a wider bandwidth and be more power efficient. In addition, the larger velocity of Lamb waves which can be tailored by the thickness of thin-film allows for higher frequency devices that can cover the entire sub-6 GHz bands of the new radio.

Table 3. Notable AE SAW amplifiers in the literature

Reference	Piezoelectric	Semiconductor	Gain (dB/mm)	Power (mW)
[95]	LN (YZ)	InSb	9.2	12900
[96]	LN (41° YX)	InSb	4	14600
[20]	LN (YZ)	Si	5.5	7000

3.2   AE Effect Formulation

For an acoustic wave ψ_{in} travelling along the x axis and entering the AE interactions medium of the length Δx, the outgoing wave ψ_{out} can be expressed as

$$\psi_{out} = \psi_{in} e^{-\alpha_t \Delta x} \tag{3-1}$$

where α_t is the total attenuation coefficient and can be expanded into the sum of losses due to several processes. These loss components can be phonon-phonon losses, thermoelastic dissipation, diffraction and scattering losses, and AE loss, to name a few. Here, for simplicity, the attenuation coefficient is written as the sum of AE attenuation coefficient α_{AE} and rest of the components all together as α_r

$$\alpha_t = \alpha_{AE} + \alpha_r \tag{3-2}.$$

In its most general form, α_{AE} can be intuitively formulated by treating such phenomenon as an RC circuit since it is in essence due to charge redistribution processes [76]. In this scenario, α_{AE} can be expressed using two key parameters. First, the effective coupling between the electrons and acoustic waves (K^2) which is bounded by the effective electromechanical coupling of the system. Second, the RC time constant of the system (τ) which is a function of its effective permittivity, conductivity, and geometry. Using these two parameters, the drift velocity dependent α_{AE} which also is a function of the frequency $(\omega/2\pi)$ is expressed as

$$\alpha_{AE}/k_0 = K^2/2 \left(\gamma\omega\tau / 1 + (\gamma\omega\tau)^2 \right) \tag{3-3}$$

where k_0 is the wavenumber and γ is difference between electron drift velocity and acoustic wave phase velocity normalized to the latter, written as

$$\gamma = 1 - V_D/V_A \tag{3-4}$$

and τ is a function of the permittivity of the piezoelectric (ε_p) and semiconductor (ε_s) films and the conductivity of the semiconductor film (σ) defined as

$$\tau = \varepsilon_s + \varepsilon_p/\sigma \tag{3-5}$$

The sign of α_{AE} is determined by the sign γ; thus, for a negative γ, which occurs once V_D surpasses V_A, AE loss turns negative which accounts for the AE gain phenomenon. From (3-3) the maximum absolute value of the term in parenthesis is 0.5, therefore, the maximum coefficient of AE loss/gain possible is $K^2/4$. In (3-3), however, the diffusion, trapping and large signal effects are neglected. Once the effect of diffusion is added [49], such maximum value is lowered, which is captured by the modified denominator of the expression for α_{AE}

$$\alpha_{AE}/k_0 = K^2/2 \left(\gamma\omega\tau / (1 + k_0{}^2 L_D{}^2) + (\gamma\omega\tau)^2 \right) \tag{3-6}$$

where L_D is the Debye length and is expressed by

$$L_D = \left(\varepsilon_s k_B T / q^2 N_d \right)^{1/2} \tag{3-7}$$

with k_B being the Boltzmann's constant, T being the temperature, q being the elementary charge, and N_d being the carrier concentration of the semiconductor film. In order to attain the highest AE gain with the smallest applied electric field, both K^2 and mobility are desired to be maximized. The impact of these two parameters on AE gain ($-\alpha_{AE}$) curves is shown in Figure 9.
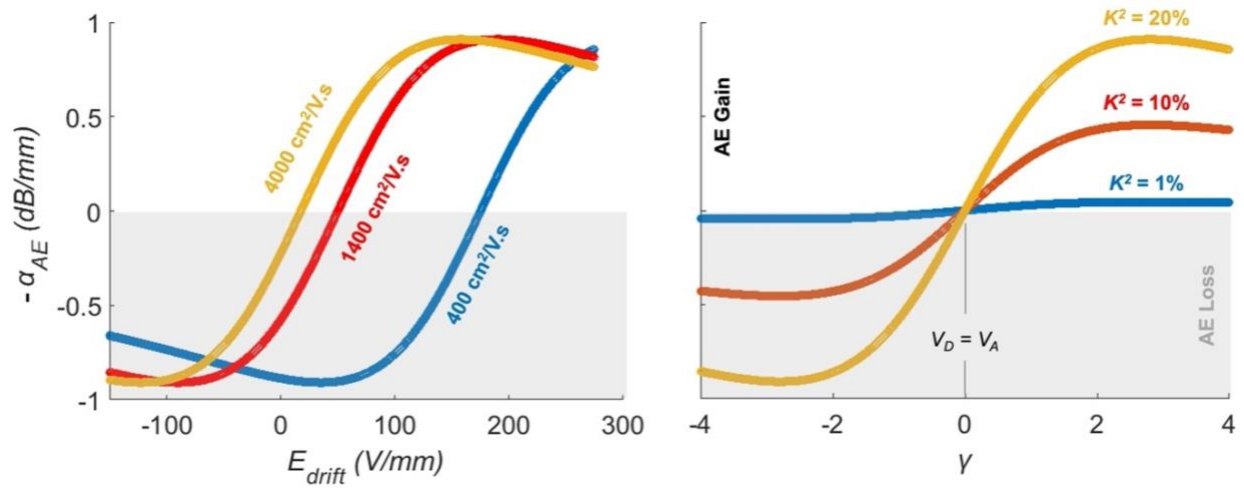
Figure 9. Typical AE gain characteristic as a function of relative electron drift to acoustic wave velocity for different effective coupling values (right) and as a function of applied drift field for different electron mobilities (left).

CHAPTER 4:
ACOUSTOELECTRIC EFFECT IN ALUMINUM NITRIDE ON SILICON RESONATORS

[1]

Today most of the BAW filters are fabricated in the AlN-Si platform as it offers complete CMOS compatibility, and a few tens of these filters are present in each cell phone. In order to explore the potential for the realization of the AE effect in this platform, in the first part of this chapter, a technique is developed to isolate the energy loss associated with the interaction of charge carriers and acoustic phonons in TPoS micro-resonators. In this method, the carrier concentration in Si at its interface with AlN is modified and the changes in Q and insertion loss (IL) of TPoS resonators are tracked. The surface carrier concentration of the Si layer is varied through application of a voltage to the metal-dielectric-Si capacitor that is intrinsically formed during the conventional fabrication of TPoS resonators. By doing so, a maximum of 3% improvement in the IL of a ~927 MHz resonance mode is recorded which is believed to stem from the reduction in AE interactions of acoustic phonons with carriers [77]. In the second part of this chapter, scandium doped AlN on Si TPoS Lamb mode resonant cavities are designed, fabricated and characterized as a proof-of-concept for AE amplification [73]. It is expected that due to the piezoelectric coupling, the evanescent EM wave be induced in the Si layer that is a part of the resonant cavity and exchange momentum with the carriers within. Therefore, by biasing the carriers to drift faster than the

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[1] Material used in this chapter is partially taken from the published papers:

- H. Mansoorzare, R. Abdolvand and H. Fatemi, "Investigation of Phonon-Carrier Interactions in Silicon-Based MEMS Resonators," 2018 IEEE International Frequency Control Symposium (IFCS), 2018.
- H. Mansoorzare and R. Abdolvand, "Acoustoelectric Amplification in Lateral-Extensional Composite Piezo-Silicon Resonant Cavities," 2019 Joint Conference of the IEEE International Frequency Control Symposium and European Frequency and Time Forum (EFTF/IFC), 2019.

acoustic waves, AE amplification could be attained. In a ~1 GHz resonant cavity, excited via LFE, concurrent improvement of Q and IL is observed upon injecting current in the Si.

4.1 Phonon-Electron Interactions in TPoS

An acoustic wave propagating in a piezoelectric-semiconductor heterostructure interacts with charge carriers within the semiconductor through two distinct mechanisms. First, the deformation potential, through which loss could occur as the electronic band structures are distorted due to the harmonic oscillation, ultimately leading to a carrier relaxation process [50]. Second, through the piezoelectrically-induced electric fields associated with the elastic waves that penetrate the semiconductor layer. Such fields, having both longitudinal and transverse components, in effect extend into the adjacent semiconductor by the amount of $1/k_0$, causing charge bunching and current excitations [54]. While both these mechanisms result in the transfer of energy and momentum between the elastic waves and charge carriers, the former is much less effective at frequencies lower than a few tens of GHz [50]. In order to observe the AE effect stemming from the piezoelectrically induced evanescent electric fields in TPoS resonators, first the penetration of such fields in Si for different configurations of the device stack is examined. Figure 10 shows the COMSOL simulated electric field component in the x (E_x) and z directions (E_z) of a Lamb mode resonator made of a stack of 1 µm AlN on 2 µm Si where in type (I) only top electrode (100 nm Mo) is present and no bottom metal is included; in type (II) the bottom electrode (100 nm Mo) is also included but it is floating; in type (III) the bottom electrode is grounded; in type (IV) a 50 nm seed AlN layer is added under the floating bottom electrode; type (V) is same as type (IV) but with a grounded bottom electrode. The results show a stronger piezoelectric

coupling once the bottom electrode is present and grounded. The grounded bottom electrode, however, shields the electric field, as illustrated for type (III), unless the AlN seed layer is included, as seen in type (V). The AlN seed layer is conventionally used in AlN-based TPoS resonators as a barrier layer underneath the bottom electrode and has shown to improve the c-axis growth of the subsequent AlN film.
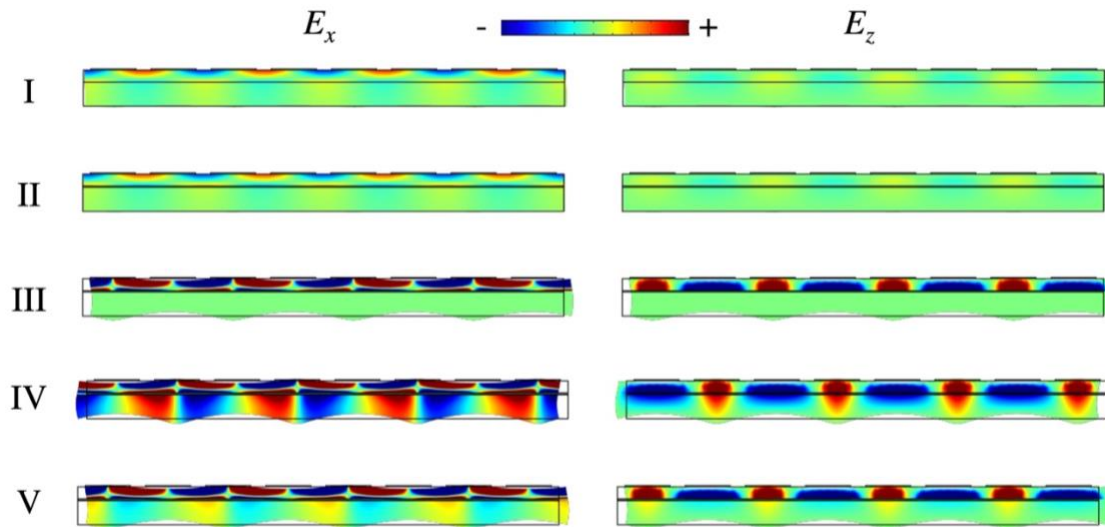
Figure 10. Electric field components in the lateral (E_x) and thickness (E_z) directions for TPoS Lamb wave resonator with (I) no bottom electrode, (II) floating bottom electrode, (III) grounded bottom electrode, (IV) floating bottom electrode with AlN seed layer, and (V) grounded bottom electrode with AlN seed layer.

As the type (V) TPoS concurrently allows for better coupling and penetration of evanescent EM waves in Si, such Lamb wave resonators are targeted. High order resonators are fabricated on a stack of 1 μm AlN sandwiched between 100 nm Mo electrodes sputtered on the ~50 nm AlN seed layer which is sputtered on a silicon-on-insulator (SOI) substrate. The AlN seed layer, moreover, forms a metal-insulator-semiconductor (MIS) capacitor in conjunction with the bottom

electrode and the Si layer. This is illustrated in Figure 11 and could be utilized to modify the surface carrier concentration in the Si, in a manner similar to the operation of field effect transistors. In order to modify the surface carrier concentration, a DC voltage is applied between the Si and the bottom Mo layer as shown in Figure 11. The behavior of AlN MIS capacitors has been characterized in [78] and used here for drawing the conclusions. The Si layer of the fabricated devices is 3 μm thick and lightly doped with boron at a doping concentration in the range of 10^{13} to 10^{14} cm^{-3}.
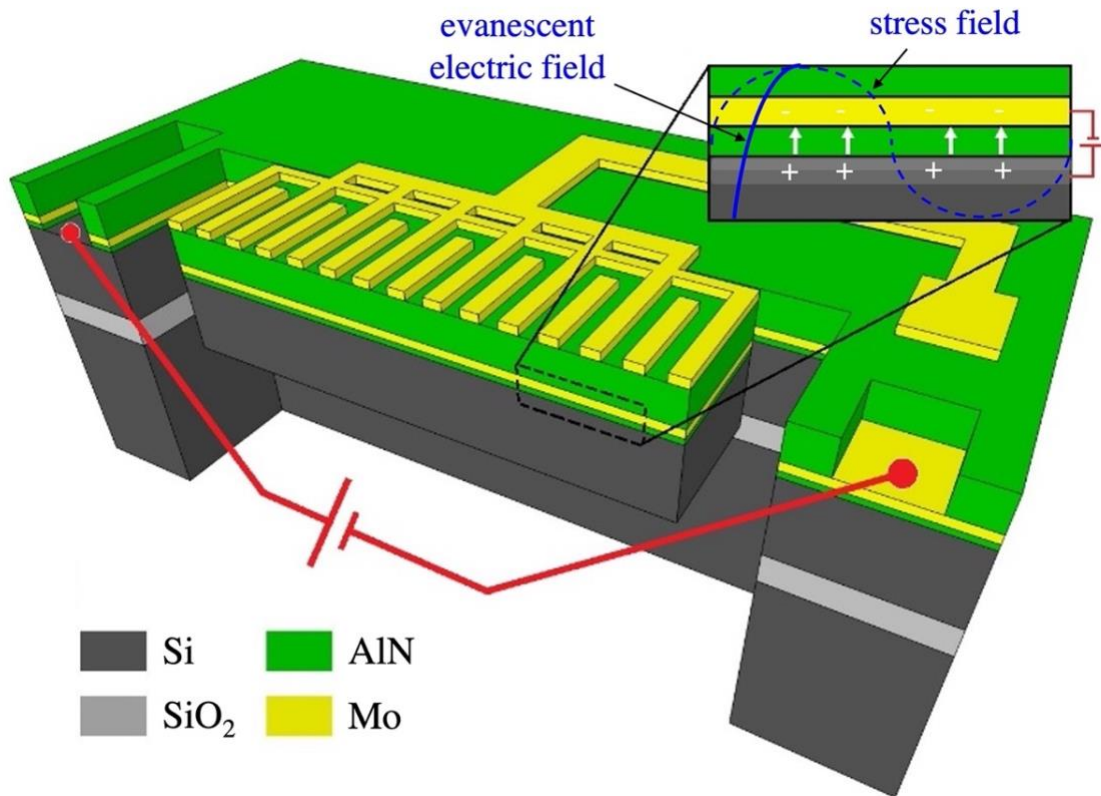
Figure 11. Cross-sectional schematic of the TPoS micro-resonator studied herein, showing that the MIS capacitor formed with the AlN seed layer could modify the surface carrier concentration in Si. The inset shows the zoomed-in stack along with the electric and stress fields.

By applying a voltage to the MIS capacitor, it is expected that the depth of the penetration of the evanescent electric field, piezoelectrically generated by the AlN layer, into the Si layer be modified. As it is limited by the smaller of the $1/k_0$ and the Debye length in Si. While the former can be regarded as constant, the latter is inversely proportional to the doping concentration as seen from (3-7). The component of loss that arises from the deformation potential is neglected here as it is considered a less significant dissipative process at lower frequencies, below ~100 GHz. In order to determine the effect of Debye length (L_D) on the intrinsic AE loss coefficient, without any carrier drift, from (3-4) γ would be equal to unity which yields the AE attenuation coefficient in the form of

$$\alpha_{AE}/k_0 = K^2/2\left(\omega\tau/(1 + k_0{}^2 L_D{}^2) + (\omega\tau)^2\right) \qquad (4\text{-}1).$$

The model predicts that a direct proportionality exists between AE loss and carrier concentrations at small values of carrier concentration and an inverse proportionality at the higher end of the spectrum. This can be intuitively attributed to insufficient electron bunching at one end and reduced evanescent wave penetration at the other end. There is a sweet spot in this range that results in highest AE interactions that would normally account for the maximum AE loss; however, this can also result in maximum AE gain upon satisfying the condition for the relative drift and acoustic velocities, i.e. $\gamma<0$. The normalized AE loss coefficient predicted from (4-1) as a function of the free carrier density in the Si layer and the frequency of interest is plotted in Figure 12.
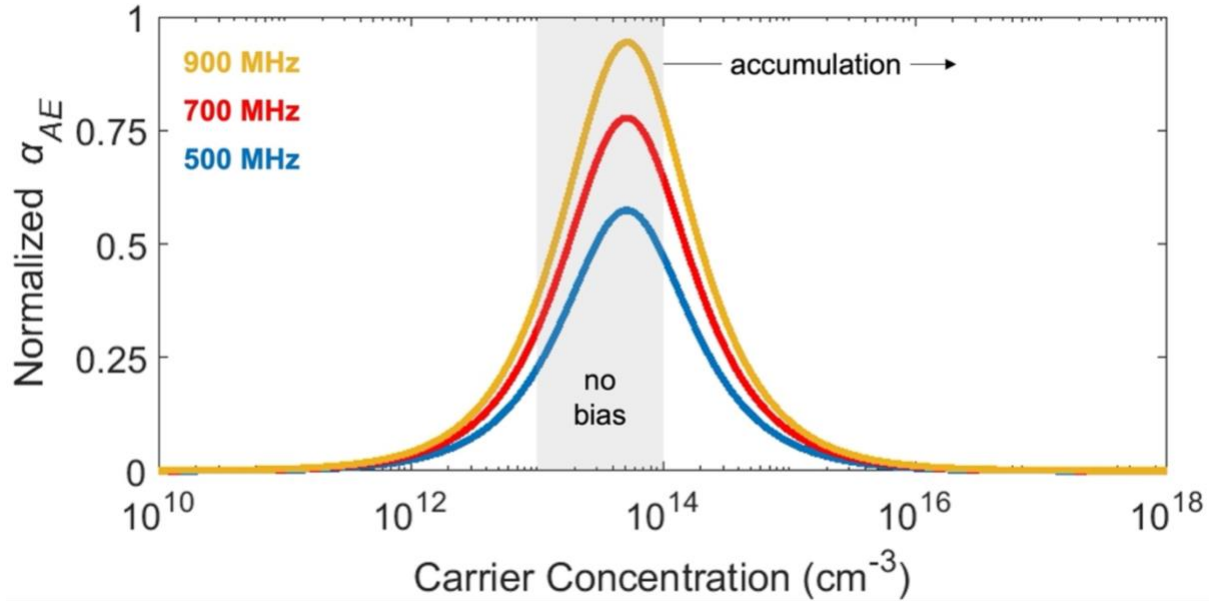
Figure 12. Normalized AE loss coefficient as a function of the concentration of holes and for different frequencies; the shaded area indicates the expected zero bias carrier density in Si.

To measure the effect of the free carrier density on AE loss, the voltage applied to the embedded MIS capacitor in a targeted 2-port TPoS resonator is varied while the transmission frequency response (i.e., S_{21}) is measured using a Rohde & Schwarz ZNB 8 network analyzer and a pair of GSG micro-probes at room temperature in atmospheric pressure. The biasing DC voltage is applied through wire-bonds in between a bottom electrode contact pad and an exposed Si contact pad while being swept at 1 V steps. The measurement is repeated few times for three resonance modes of the resonator. As expected, the loss of the main mode with the highest K^2 (at 927 MHz) shows most sensitivity to the applied voltage. The results are summarized in the Table 4.

Table 4. Change of the IL of resonance modes as a bias is applied to the MIS capacitor

	Resonance mode average IL at:		
Bias:	485 MHz	754 MHz	927 MHz
0 V	13.83	15.38	9.31
4 V	13.59	15.07	9.07
% Improvement (Absolute in μW)	1.73 (2)	2.01 (0.3)	2.57 (6)

From the measurement results, an improvement in the loss is observed upon application of a negative voltage to the metal plate with respect to the Si layer. Such improvement, however, appears to reach a saturation at voltages above 4 V. Conversely, minor changes are measured once the polarity of the voltage is reversed. The measured S_{21} of the resonator at 927 MHz is displayed in Figure 13 in wide span and around the resonance peak, showing the same trend manifested in the IL. The scanning electron micrograph (SEM) of the device is shown in same figure as well.
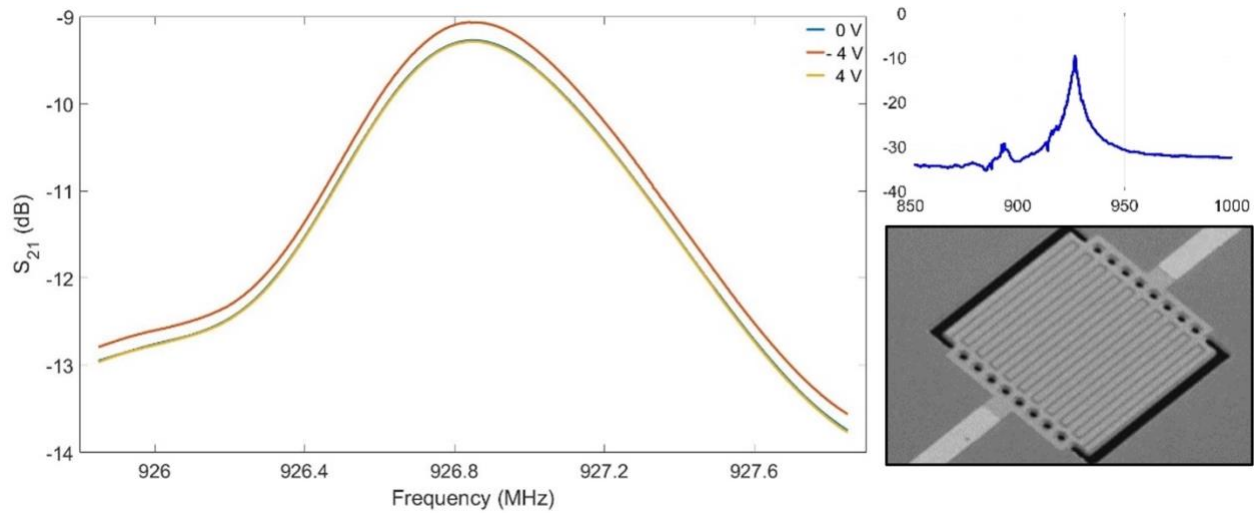
Figure 13. Measured S_{21} at different voltages applied to the metal plate showing a considerable improvement at accumulation regime while negligible changes are measured due to inability to form an inversion layer (the two curves are almost overlapping).

The measurement results are believed to be consistent with the prediction from (4-1), which is plotted in Figure 12, considering that a sharp rise in carrier (hole) concentration after application of a small negative voltage is expected at the Si surface while the concentration is almost unchanged for positive voltages. The accumulation density is estimated to be pushed beyond 10^{15} cm^{-3} by applying a -1 V or higher which corresponds to a shrinkage in the Debye length from around 1.2 μm to fewer than 100 nm. It is evident from Figure 12 that such free carrier density results in a decrease in AE attenuation coefficient compared to the original concentration. The insensitivity of carrier concentration to positive voltages is associated with the absorption of minority carriers at the interface of AlN with Si [78]. The observed trend of changes in Q as a function of the applied voltage for a resonator at 802 MHz is plotted in Figure 14, demonstrating a 3.2% improvement in accumulation regime. Again, reversing the polarity of the applied voltage

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leads to negligible changes in Q. It is worth mentioning that in order to ensure that the results do not stem from the direct application of a voltage to the network analyzer, probably due to an unwanted parasitic path, both coaxial DC block for suppressing and bias tee for direct application of the DC voltage were attached to the network analyzer and tested.
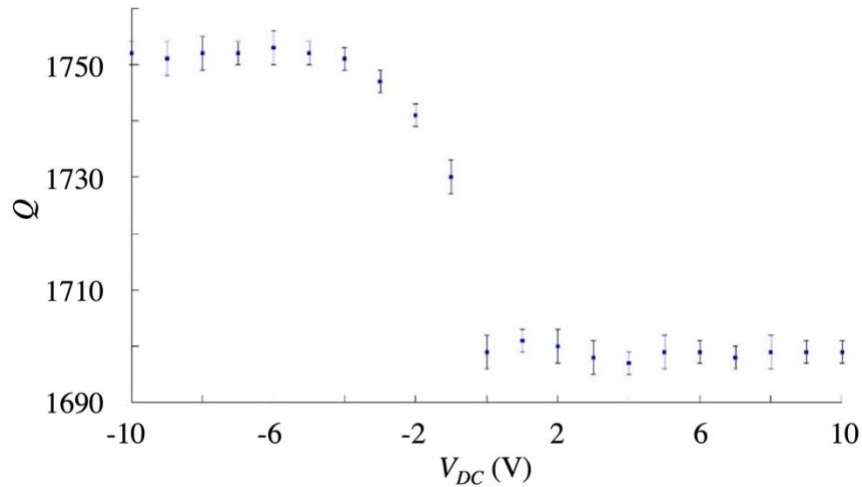
Figure 14. Average Q of the resonator with highest Q dependance on the Si surface carrier concentration as a function of the bias voltage applied to the metal plate.

4.2   Proof-of-Concept Aluminum Scandium Nitride on Silicon Devices

The loss of the AlN-Si TPoS resonators was observed to be affected by the surface carrier concentration in Si and this dependency was attributed to the AE effect. In order to further investigate such hypothesis, TPoS resonant cavities are designed and fabricated with a current injection path in the underlying Si layer and along the Lamb wave propagation direction. This is schematically shown in Figure 15. By applying a bias across the cavity so that the electron drift velocity exceeds the Lamb wave phase velocity, Lamb waves would experience an AE gain in one

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direction and AE loss in the opposite direction. The gain and loss are not symmetric with respect to wave propagation direction and the resulting quasi-standing waves could be amplified due to roundtrip gain. To increase the AE coupling, an electrically floating bottom electrode is used along with LFE. The stress profile of the excited S_0 mode at 1 GHz along with the lateral and thickness components of the electric field are shown in Figure 16. As a result of the floating bottom electrode, a strong evanescent electric field is induced in the Si layer.
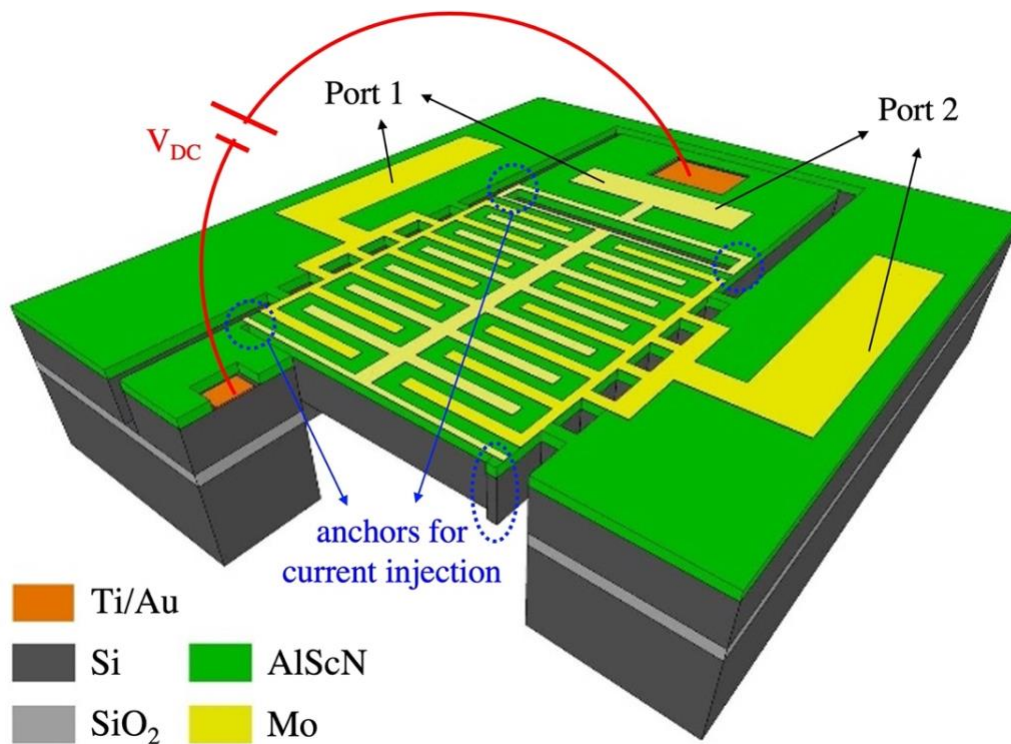
Figure 15. Schematic of a designed 2-port TPoS resonant cavity for AE amplification, showing the electrode configuration for LFE as well as the points of electrical contact to Si.
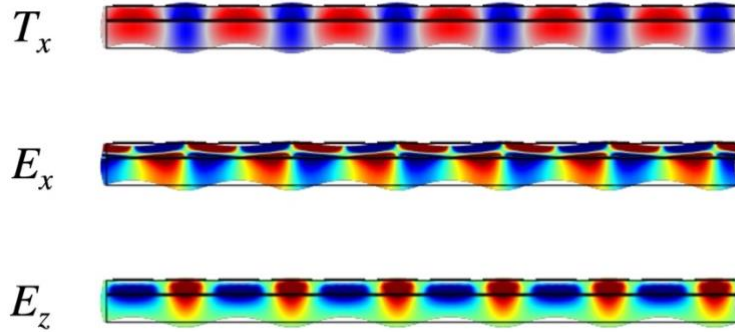
Figure 16. COMSOL simulated lateral stress (T_x) and lateral (E_x) and thickness (E_z) components of the electric field for a 1 GHz S_0 mode TPoS resonator with LFE and electrically floating bottom electrode; the evanescent electric field in the Si layer is evident.

In order to further increase the AE coupling, the K^2 of the AlN film is boosted by doping it with scandium (Sc). AlScN has shown increased K^2 compared to pure AlN as the Sc content is increased and up to five times improvement in K^2 has been reported for films at 40% doping level [79]. Here an AlScN film with 20% Sc content is sputtered on a 2 µm lightly n-type doped Si (in the order of 10^{14} cm^{-3}) as the stack for fabricating the micro-acoustic cavities. The top electrodes are designed to excite the piezoelectric film using a first set of IDT with the common ground in the middle while the second set of IDT with the common ground transduces the acoustic waves back to EM signal, enabling 2-port operation. The bottom metal is floating to enhance the penetration of evanescent electric fields in Si. Multiple tethers are placed at the displacement nodes of the S_0 mode on each of the two sides of the resonant cavity to concurrently reduce the anchor loss and suppress spurious modes [80]. In addition, two extra pairs of tethers are added in the direction of the S_0 mode propagation at the minimum displacement regions which are close to the device corners to form a current conduction path through the Si layer. To access the Si layer, two electrical contact pads are placed at the two ends of the cavity and current isolation trenches are

etched all around the device to minimize the current leakage and limit the current path to the resonant cavity. The SEM of a typical fabricated device is shown in Figure 17.
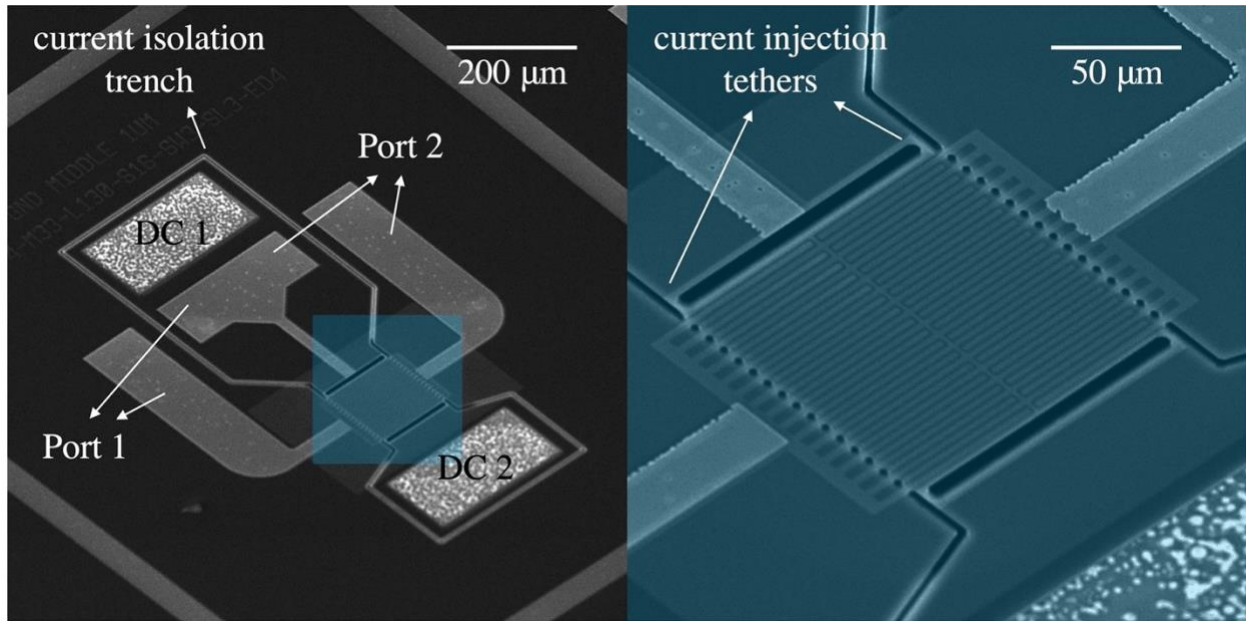
Figure 17. SEM picture of the fabricated TPoS S$_0$ mode resonant cavity used for AE amplification.

The analytical expression for the AE interactions in TPoS resonant cavities can be derived from the general expression for the AE attenuation (3-6) with slight modifications to account for the quasi-standing waves [81]. Hence, the AE loss/gain coefficient can be written as

$$\alpha_{AE}/k_0 = K^2/2 \left(\frac{(1-\eta)/\omega\tau}{(1+k_0{}^2 L_D{}^2)/(\omega\tau)^2 + (1-\eta)^2} \right.$$

$$\left. + \frac{(1+\eta)/\omega\tau}{(1+k_0{}^2 L_D{}^2)/(\omega\tau)^2 + (1+\eta)^2} \right)$$

(4-2)

where η is the ratio of the electron drift velocity to acoustic velocity ($\eta = 1 - \gamma$). Here, K^2 can be roughly extracted from the admittance response of the resonator and is measured to be 0.4%. By separating the AE attenuation coefficient from the other sources of loss, from (3-2), the IL in dB can be expressed in the form of

$$IL = 20\log \left(\frac{A_0 e^{\alpha_r + \alpha_{AE}}(\cos(\omega t + \beta z) + \cos(\omega t - \beta z))}{A_0(\cos(\omega t + \beta z) + \cos(\omega t - \beta z))} \right)$$

(4-3).

Therefore, the term due to the AE loss/gain can be separated so that the right side of the equation (4-3) is simplified to sum of IL when $\eta = 0$ – i.e., the intrinsic IL at no drift voltage – and the AE gain due to the applied drift voltage. In order to determine the intrinsic component of IL, the transmission frequency response (i.e. S_{21}) of the targeted device is measured using a Rohde & Schwarz ZNB 8 network analyzer and a pair GSG microprobes. This is done at room temperature and in atmospheric pressure. The intrinsic IL is measured to be 11.24 dB. Next, A pair of DC probes are used to apply the DC voltage across the Si electrical contacts while the injected current is measured. The average IL of the device as a function of the applied voltage is plotted in Figure 18 by solid blue. By substituting α_{AE} due to the applied voltage in (4-3), the analytically expected IL is derived and also plotted in Figure 18 by dashed red. At low injected current levels, the measured and expected values are consistent, however, the larger the injected current gets, the more the measured IL deviates from what is theoretically expected; a 0.48 dB improvement in the IL is expected upon passing 150 µA current, while only a 0.23 dB enhancement is observed. Such discrepancy is postulated to stem from the adverse effect of Joule heating in the device which

reduces the electron mobility and higher interface trapped charges that screen the evanescent field in Si layer. The frequency response of the device for the current sweep is plotted in Figure 19.
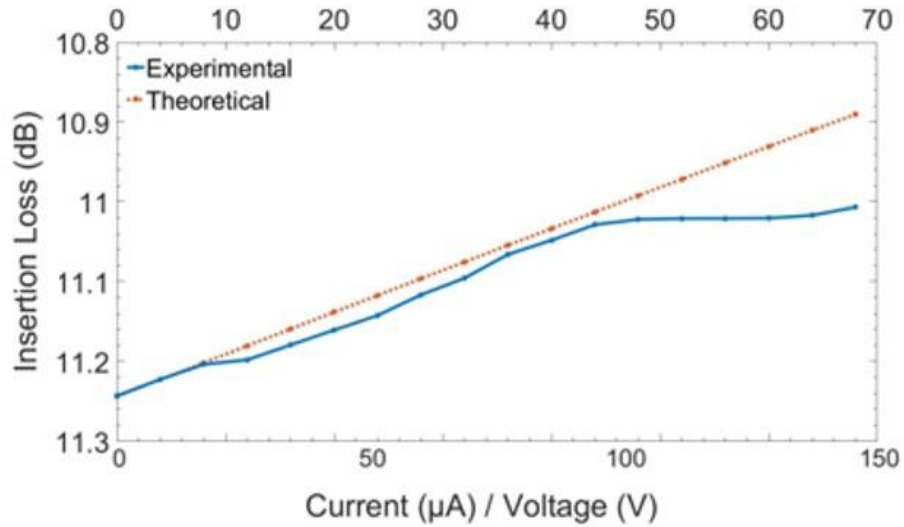
Figure 18. Measured IL of the device and the expected values as a function of the voltage applied across the Si contacts. The datapoint connecting lines serve as visual guidance.
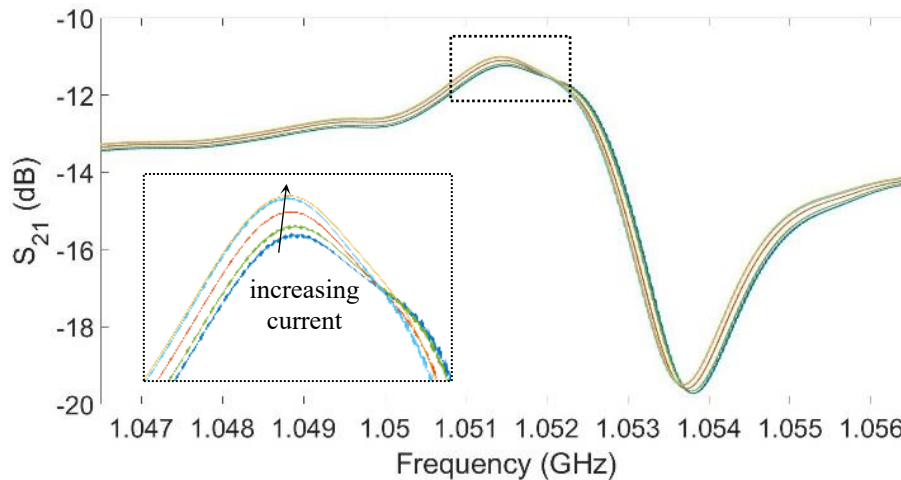
Figure 19. Transmission response of the device at different levels of injected current, from 0 μA to 150 μA, showing improvements in the IL and Q as the current increases.

CHAPTER 5:
ACOUSTOELECTRIC EFFECT IN LITHIUM NIOBATE ON SILICON PLATFORM

[2]

While the AlN on Si platform allows for CMOS compatible realization of AE effect, because of the limited piezoelectric coupling, the attainable gain and power efficiency is far from optimal. LN is a strong piezoelectric material with outstanding electro-optical properties and is emerging as a powerful driver in the integrated photonics field. On the other hand, in addition to the Si-photonics, most electronic circuits are built on Si. Therefore, a heterogeneous LN-Si platform seems like an ideal enabler of hybrid opto-electronic devices [82, 83]. Furthermore, LN has been long explored for RF signal processing due to its outstanding piezoelectric properties, making LN-Si an unrivaled platform of choice for fabricating opto-electro-mechanical components. More specifically and regarding the AE effect, as mentioned in the 3rd chapter, during the 20th century a great deal of research in this field was fueled by migrating from less efficient piezoelectric semiconductor materials to layered LN-semiconductor structures. However, limited fabrication capabilities at the time and subsequently devices with low efficiency discouraged many researchers from further investigations. Today, the advances in wafer-level bonding and thin-film transfer have enabled further exploration of the AE effect in heterogeneous LN-based devices.

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[2] Material used in this chapter is partially taken from the published papers:
- H. Mansoorzare and R. Abdolvand, "Acoustoelectric Non-Reciprocity in Lithium Niobate-on-Silicon Delay Lines," in IEEE Electron Device Letters, vol. 41, no. 9, pp. 1444-1447, Sept. 2020.
- H. Mansoorzare and R. Abdolvand, "Trapped Charge Effect on Composite Lithium Niobate-Silicon Acoustoelectric Delay Lines," 2020 Joint Conference of the IEEE International Frequency Control Symposium and International Symposium on Applications of Ferroelectrics (IFCS-ISAF), 2020.
- H. Mansoorzare and R. Abdolvand, "A Thin-Film Piezo-Silicon Acoustoelectric Isolator with More than 30 dB Non-Reciprocal Transmission," 2021 IEEE 34th International Conference on Micro Electro Mechanical Systems (MEMS), 2021.

Motivated by the outstanding properties and potentials of the LN-Si platform, in this chapter, AE effect is efficiently demonstrated in suspended LN-on-Si (LNoSi) waveguides and resonators. An electric current is passed through the Si layer in the same axis as the piezoelectrically-transduced Lamb waves which are attenuated or amplified depending on the direction of the current. Proof-of-concept Lamb mode delay lines in the 100s MHz range are demonstrated with more than 20 dB of AE gain and more than 30 dB non-reciprocal transmission with few milliwatts of DC power consumption [84]. This could offer a monolithic and dynamically tunable solution to the numerous issues that arise from the increasing congestion and interferences in the telecommunication spectrum and suggests the possibility of developing fully switchable low-IL delay lines through design/fabrication optimizations. This chapter starts with a short discussion on some of the essential properties of the LNoSi platform, namely the piezoelectric and thermal behavior. This is followed by the AE effect in resonators and delay lines, optimization of delay lines as a powerful platform for AE amplification, and a technique for widening the bandwidth of such devices.

5.1   Properties of LNoSi Platform

5.1.1   Electromechanical Behavior

In a piezoelectric RF component, the attainable intrinsic IL and bandwidth are primarily determined by the K^2 and the design of the transducer electrodes such as their phase, thickness, and mechanical properties. Moreover, the higher the K^2, the stronger the interactions between the acoustic wave and drifting electrons and subsequently the larger the AE gain and subsequent non-reciprocal behavior. Therefore, it is essential to target the maximum achievable K^2 with a tailored

electrode design. LN thin-film offers excellent confinement of acoustic and electrical field and due to its strong anisotropy offers a variety of dominant piezoelectric coefficients at different cuts and orientations of its crystal. For the case of lateral field excited Lamb waves, the highest K^2 is attained by S_0 on X-cut LN and once the wave propagation is along the ~30° off +Y axis [85, 86]. This is illustrated in Figure 20 where K^2 is shown to surpass 30%. For comparison, the highest K^2 for S_0 on Y-cut and Z-cut reaches 15% and 7%. On the other hand, the best K^2 reported for $Al_{0.6}Sc_{0.4}N$ which is the highest attained Sc-doping level is only around 8% [79].
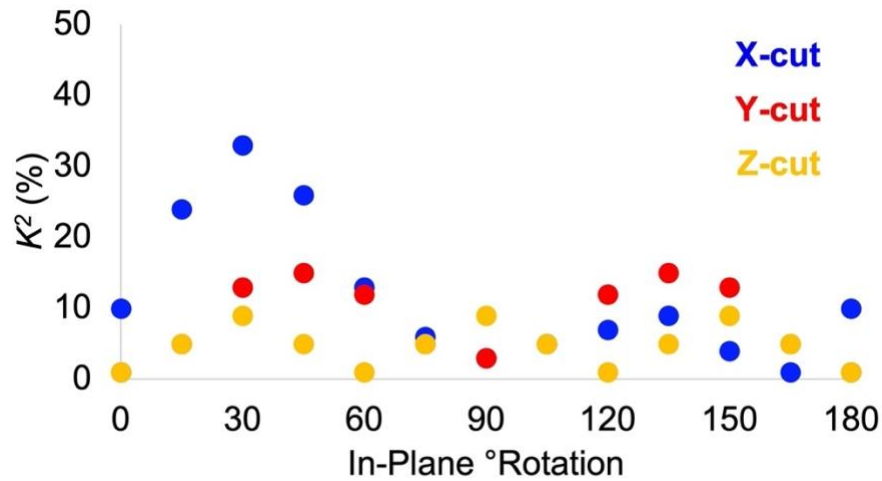
Figure 20. The values of K^2 for S_0 mode on different cuts and orientations of LN. For the X-cut the starting orientation is +Y and for the other two cuts it corresponds to +X axis.

While the addition of the Si underlayer reduces the attainable K^2, a relatively large value is still expected for the cases with thin Si layers. This can be perceived from Figure 21 where the dispersion curve of the LNoSi stack having different LN thicknesses is used to derive the Lamb wave phase velocity in two cases of electrically open (v_o) and metalized (v_m) LN on Si film and subsequently K^2 is calculated using [87]

$$K^2 = \frac{(v_o{}^2 - v_m{}^2)}{v_o{}^2} \qquad\qquad (5\text{-}1).$$

As such, COMSOL finite element analysis (FEA) is used to plot K^2 for a 0.5-1.5/0.8 μm thick stack shown in Figure 21. The FEA results suggest that the implemented 1 μm thickness with an IDT FP of 5 μm could result in a K^2 of ~16% while increasing the LN thickness to 1.5 μm increases the K^2 to ~18%. The typical effect of K^2 increase on the gain can be seen in Figure 9 and such change would increase the analytical gain by 16%.
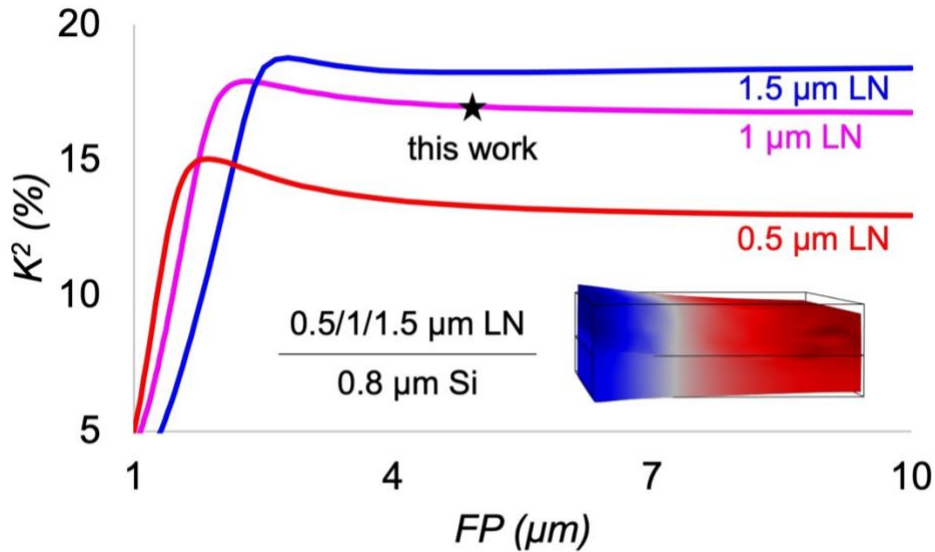
Figure 21. The electromechanical coupling of the LNoSi stack for different LN thicknesses derived from the dispersion curve of the stack.

5.1.2 Thermal Behavior

For the majority of RF applications, operation under continuous bias conditions is required, however, previously, the AE amplifiers of notable performance have been mostly reported in pulsed operation regime [69, 72]. In such cases, operation under the continuous bias results in

excessive Joule heating because of the low thermal conductivity of the utilized piezoelectric substrate to the extent of permanent damage to device. In LNoSi platform, as a result of the high thermal conductivity and power-handling of Si, continuous bias operation at room temperature and normal pressure is attainable. To better illustrate this, a COMSOL model is developed to simulate the temperature increase due to the applied bias across an AE waveguide. The stack is chosen to be 1 μm of LN on 0.5 um of semiconductor layer which is changed from Si to Ge to InGaAs. Changing the semiconductor layer in such order results in a larger electron mobility but it comes at the cost of compromised power handling, especially for the case of InGaAs. The COMSOL model consists of Joule heating due to the current flow and convective air cooling to predict the steady state maximum device temperature. The FEA results are shown in Figure 22 for a waveguide which is 200 μm wide and 800 μm long. The results confirm the superior power-handling of Si; for instance, at 40 V of applied voltage, the temperature at the center of the waveguide increases by 14° K for Si, 54° K for Ge, and 207° K for InGaAs. Having a high power-handling is especially crucial due to the high temperature coefficient of frequency of LN (TCF≈−60 ppm/K) and its low thermal conductivity (κ=5.6 W/m.K). Therefore, in contrast to a SAW AE amplifier where the thermal conduction path is mostly a low thermal conductivity piezoelectric material such as LN, in the suspended LNoSi platform, Si forms an excellent thermal conduction path that would allow for continuous wave operation of the AE amplifier.
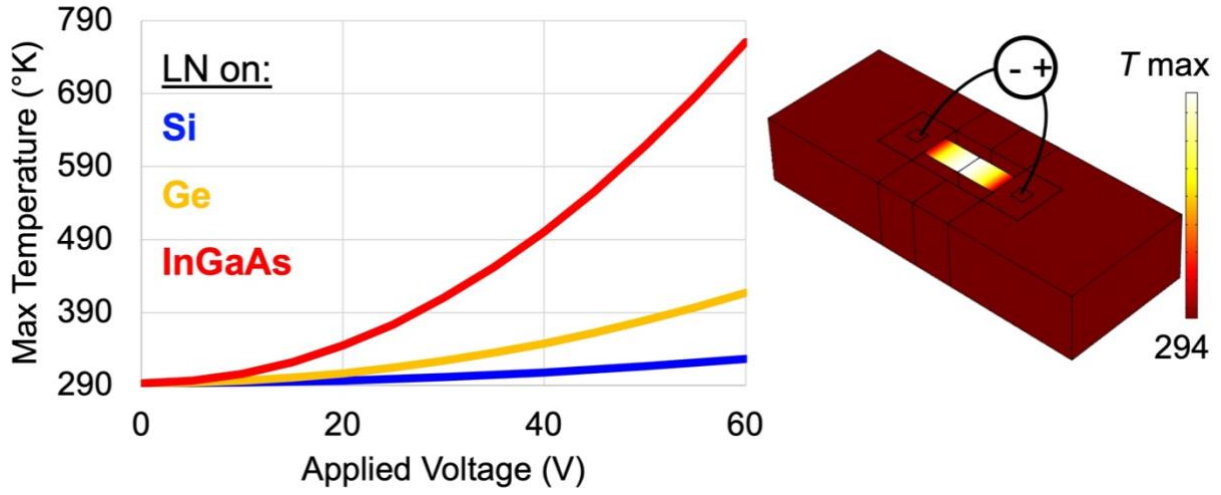
Figure 22. COMSOL simulated maximum temperature of the LN/semiconductor AE waveguide at different levels of applied voltage. The semiconductor layer (and the corresponding thermal conductivity value in W/m.K) is assumed to be Si (κ=140), Ge (κ=58), and InGaAs (κ=33).

5.2 LNoSi Resonators

Lamb wave LNoSi resonators with DC current injection path through the Si layer are designed and fabricated to demonstrate the effect of higher K^2 on the AE performance. The current injection regions into and out of the resonant body are narrow tethers that are placed at its displacement nodes for minimizing the mode distortion and anchor loss. In order to achieve a more uniform current distribution along the resonator and subsequently more efficient AE interactions, the distance between the current in and out regions is desired to be larger. This translates into wider resonators, and since the width of the resonator is set by the acoustic wavelength (i.e., nλ/2) a high harmonic order resonator is essential. The problem, however, with high order resonators with a large K^2 is the excitation of multiple spurious modes that could lower the Q. In order to suppress some of the spurious modes, placement of multiple tethers at the displacement nodes of the

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resonator has been proven effective [80] and is applied here. The resonators are fabricated on a bonded LN-SOI wafer. The SOI thickness is 3 µm and its resistivity based on the vendors availability is 5-10 ohm.cm corresponding to a carrier density in the 10^{14} cm^{-3} range. The X-cut LN wafer (provided by NGK insulators) is rotated +30° away from the +Y axis in plane and bonded to the SOI in a way that the Lamb wave propagation is along both the Y+30° axis of LN and <110> plane of Si (Figure 23). As seen earlier in this chapter in Figure 20, the d_{22} piezoelectric coupling constant of LN reaches a large maximum once the main strain tensor (i.e. the 2 axis as in d_{22}) is oriented this way. Through this piezoelectric coefficient, S_0 mode with high K^2 is targeted by means of LFE which is crucial for a strong AE effect.
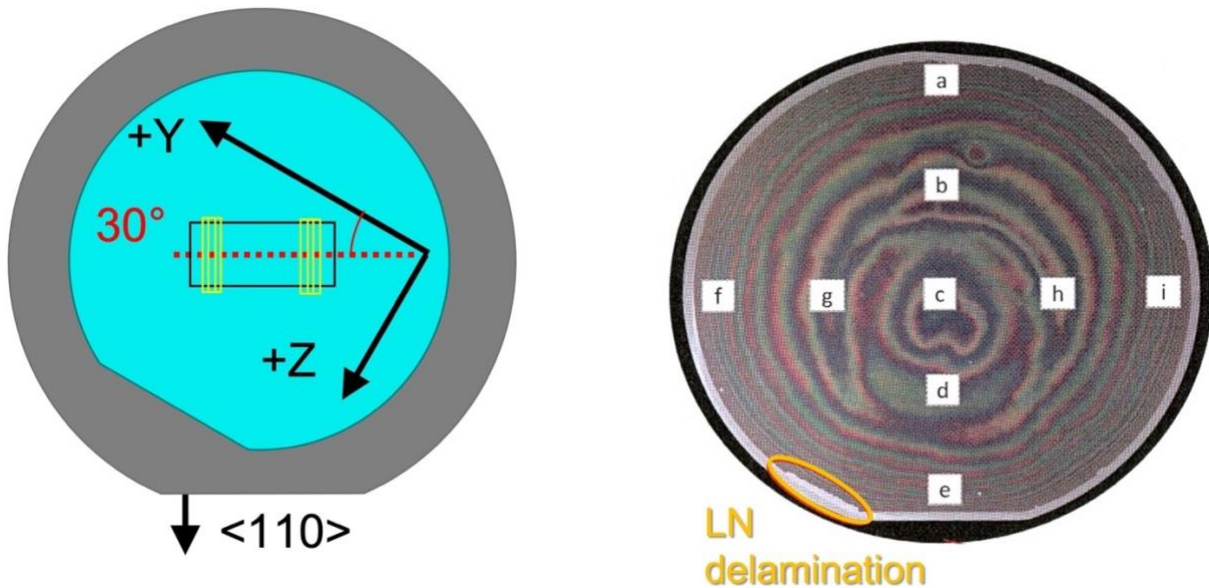
Figure 23. Relative orientation of the X-cut LN wafer and (100) SOI wafer showing the Y+30° axis of LN is aligned with 110 Si plane (left) and the image of the bonded wafer (right); slight delamination of the LN film at the bottom left is noticeable. The non-uniform pattern is due to ~500 nm variation in the films' thicknesses.
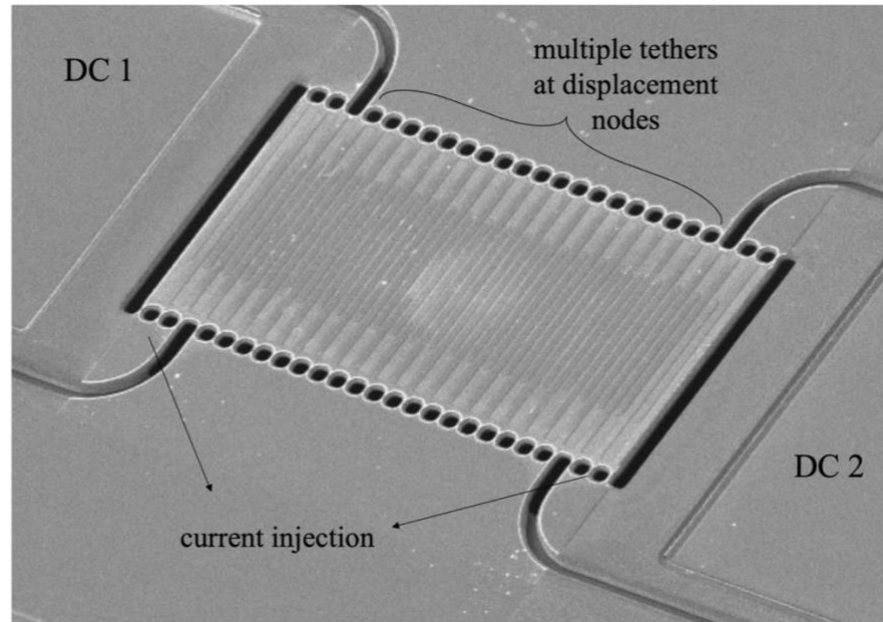
Figure 24. The SEM of a typical TPoS LNoSi resonator fabricated in this study.

The SEM of a typical fabricated LNoSi resonator is shown in Figure 24. The device IDT has a FP of 5 μm, designed for LFE of a resonance mode at ~610 MHz. The IL of the resonator is measured for different levels of V_{supply} and is plotted in Figure 25. As the supply voltage is increased from 0 to 140 V, with the measured injected DC current reaching ~40 μA, the IL is steadily improved due to the net roundtrip AE gain. The measurement results are shown for 3 levels of RF excitation power. The IL, overall, increases by ~0.5 dB for -30 and -10 dBm input powers, but this reduces to ~0.3 dB for +10 dBm input power and gain compression is observed due to large signal AE effects. The forward (S_{21}) and backward (S_{12}) transmission of this resonator is shown in Figure 26. Due to the strong quasi-standing wave formation in the resonant cavity, the device is reciprocal ($S_{21}=S_{12}$) both before and after the application of the drift field.
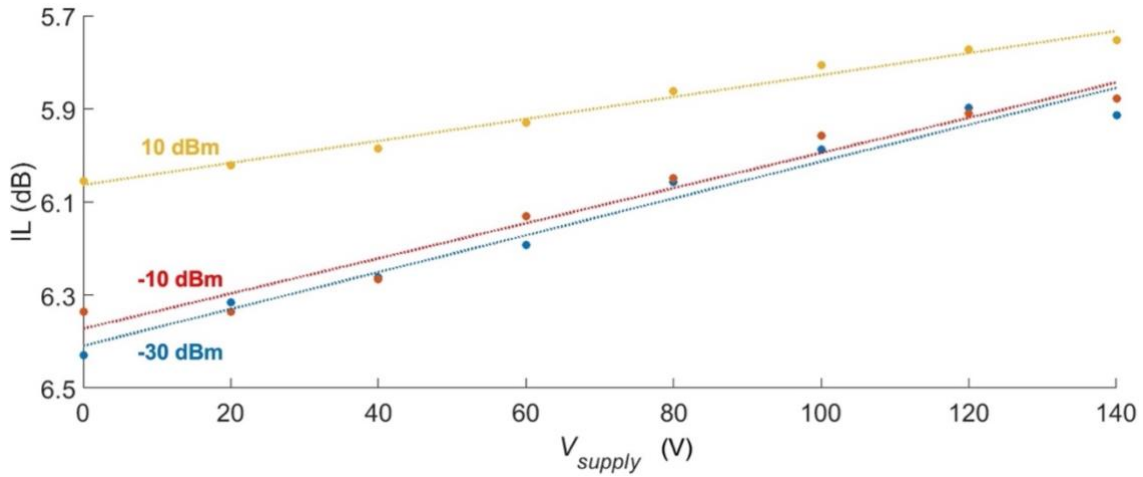
Figure 25. Measured insertion loss of a targeted LNoSi resonator as a function of applied DC voltage. The gain compression for the measurements at larger excitation power is noticeable.
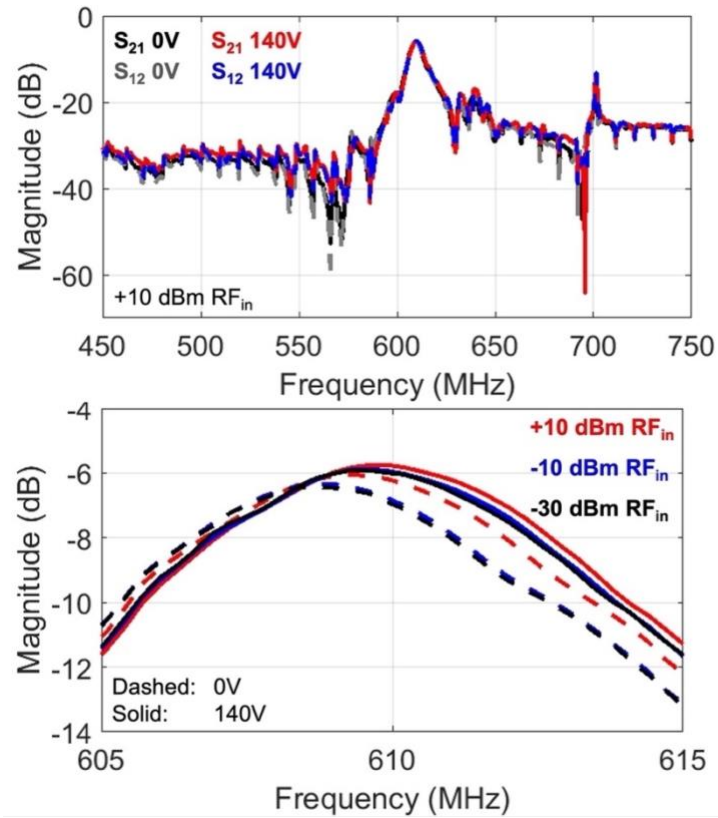
Figure 26. The measured frequency characteristic of the LNoSi resonator showing the widespan response and reciprocal behavior (top); AE gain at different excitation levels is shown by the narrow span S_{21} curves (bottom).

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5.3   LNoSi Acoustoelectric Delay Lines

5.3.1   Design of AE Delay Lines

The AE effect in TPoS resonators due to the limited interaction length and roundtrip gain was determined to be not very efficient. Moreover, their operation principle is based on standing wave formation which renders them reciprocal. Therefore, with the goal of considerably increasing the AE amplification and realizing non-reciprocal behavior, AE delay lines based on LNoSi are introduced in this section. Lamb mode delay lines are mechanically suspended acoustic waveguides with IDTs at the two ends that launch the acoustic wave from one port and sense it from the other port. The distance between the two ports would introduce a propagation delay which if implemented with low loss, is a promising solution for realization of analog signal processing elements such as delay synthesizers, transversal filters, and correlators [88]. Another major advantage of such delay lines is the design flexibility that comes with the lithographically defined passband response. This is done through the mapping between the spatial arrangement of the IDT and the frequency domain by Fourier transform. As such, a wide range of passband responses can be achieved. In the LNoSi delay line, by applying a bias to Si along the wave propagation direction, AE effect can be realized. This concept is illustrated in Figure 27 where the guided Lamb waves could be amplified by electrons drifting in the same direction and attenuated by those in the opposite direction. The magnitude of such gain or loss, for a fixed applied drift field, increases as the interaction length is increased. Therefore, in longer delay lines a larger AE gain and non-reciprocal transmission ratio could be attained. The AE gain/loss selectively applies to the passband since those are the acoustic modes with the highest K^2 excited by the IDT. This in an ideal waveguide that only supports a single targeted mode could translate into amplification

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without degrading the signal to noise ratio (SNR) [89]. Another key feature of the AE delay lines is that they can act as a tunable attenuator or switch based on the polarity and level of the applied bias, therefore, allowing for merging multiple components into one.
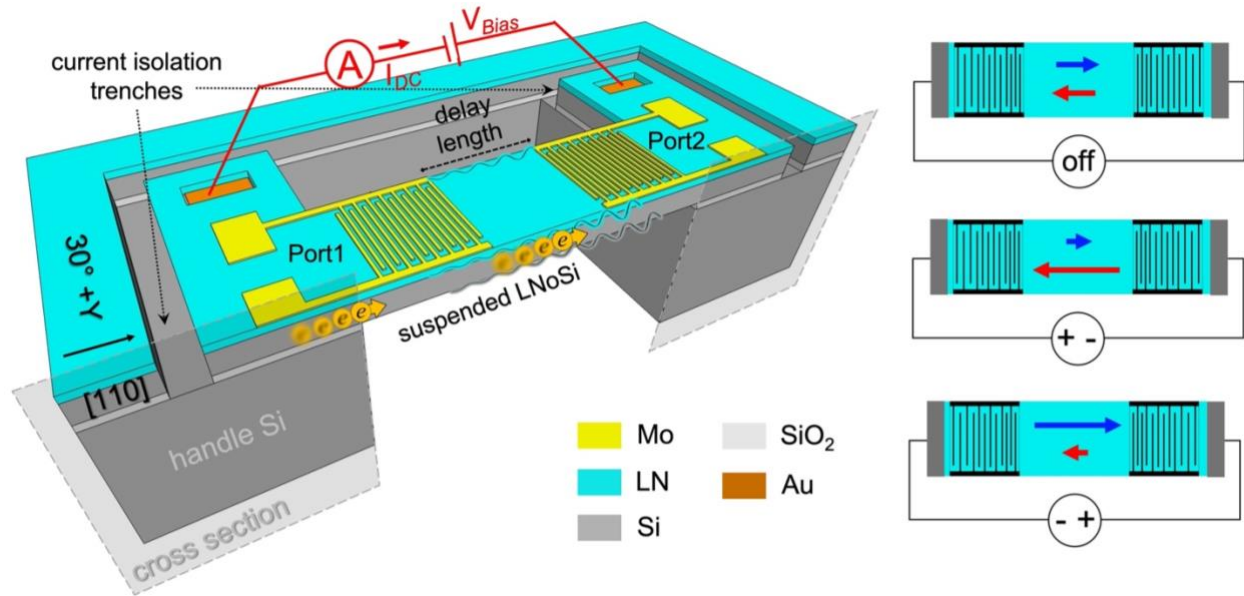
Figure 27. Conceptual schematic of AE delay line where Lamb waves launched by the IDT will be amplified or attenuated by the electrons drifting in the Si layer. This renders the delay line non-reciprocal depending on the polarity of the bias.

The proof-of-concept LNoSi AE delay lines are fabricated on a bonded LN-SOI wafer. Same as the resonators, the SOI thickness is 3 μm with a resistivity of 5-10 ohm.cm. To leverage the highest K^2 possible for S_0 in LN, X-cut LN +30° off +Y axis is targeted and aligned with <110> plane of SOI for bonding (Figure 23). By simulating the Lamb mode dispersion curve for the 1/3 μm LN/Si stack using COMSOL, the value of K^2 is approximated and plotted in Figure 28. This is done by deriving the phase velocity for the stack with free LN top surface and the reduced velocity due to the electrically shorted LN surface and then using (5-1).

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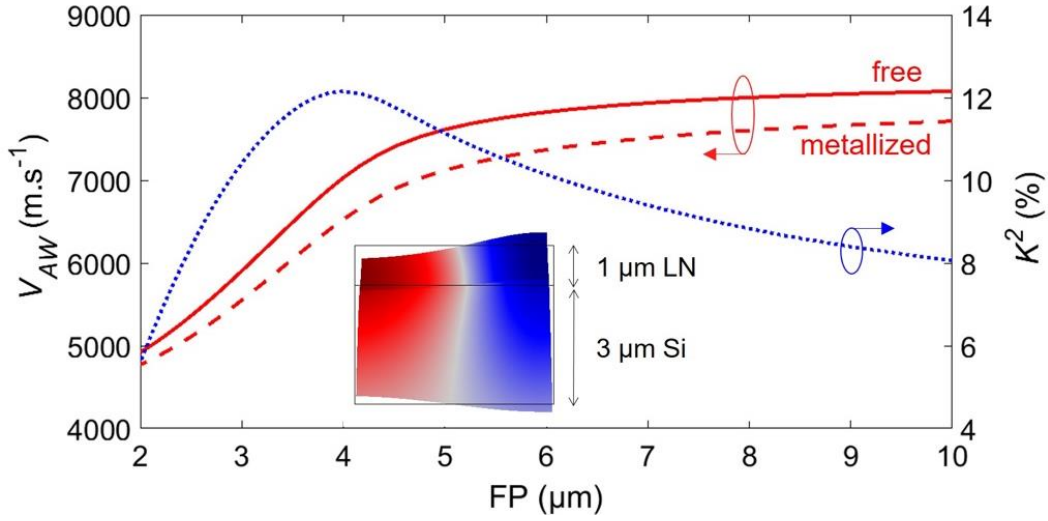
Figure 28. Dispersion characteristic of the LNoSi stack having free and metallized surface used for estimating the K^2 value for delay lines.

From (3-3) the theoretical value of α (defined as AE gain coefficient here) as a function of the applied drift field (E_d) is plotted in Figure 29 at IDT FP of 5 μm. The doping of Si is swept from 1E14 to 1E15 cm^{-3} to account for the deviation of free electrons from the initial doping (n-type at 5E14 to 9E14 cm^{-3}) as a result of trap states especially at the LN-Si boundary. The relationship between α and E_d clearly depends on the density of free electrons and a larger gain for a lower E_d is observed at the lower end of free electron density. For instance, at E_d = 60 V/mm based on the initial doping range, an AE gain of 9.7 to 17.4 dB/mm can be expected. Once α is fitted to the measurement data, an AE gain of 10.2 dB/mm and an effective carrier density of 8.5E14 cm^{-3} is projected. The waveguide's dimensions and the islands around the DC bias points for current isolation are defined by etching the LNoSi stack. By doing so, the drift current is limited to pass only through the waveguide, therefore reducing the bias power dissipation.
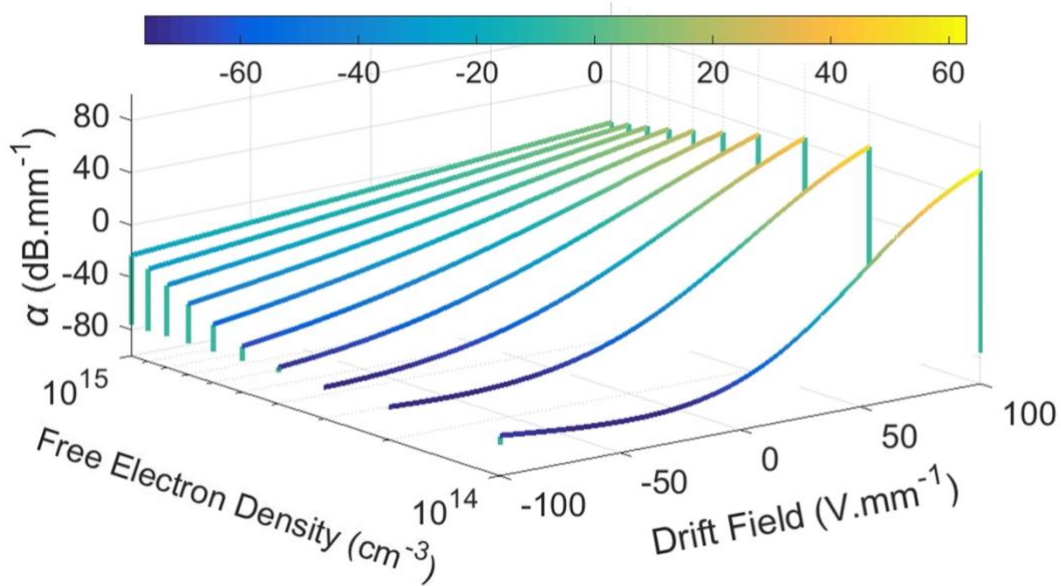
Figure 29. Theoretical value of AE gain coefficient as a function of the applied drift field for a range of free electron densities close to the doping of the Si layer.
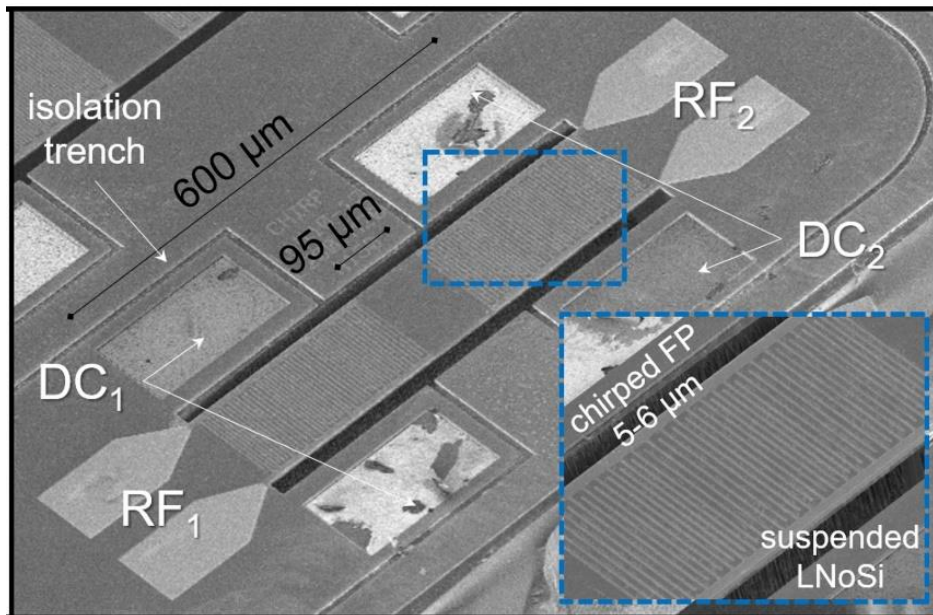
Figure 30. The SEM of a fabricated AE delay line with the inset showing its chirped IDT pattern for achieving a wider FBW.

5.3.2 AE Delay Lines Preliminary Results

The SEM of a fabricated typical delay line is displayed Figure 30. The fabricated devices are characterized at room temperature and in atmospheric pressure by a vector network analyzer (Rhode & Schwarz ZNB 8) using ground signal ground (GSG) microprobes (Cascade Microtech Inc.). In order to set the reference plane at the microprobe tips, a short-open-load-thru calibration is performed. At first, the AE effect is experimentally verified by measuring the acoustoelectrically generated DC current (I_{AE}) along the Lamb wave propagation. This is the result of the current carrying evanescent electric fields in the Si and is proportional to the intensity of Lamb wave. For measuring I_{AE}, the Si contact pads are connected to a digital multimeter (Tektronix DM2510) and I_{AE} is recorded as the frequency of the input RF signal, with the power level fixed at 10 dBm, is swept. I_{AE} is plotted in Figure 31 for a delay line with chirped IDT (FP swept from 5 to 6 μm) in both ports that are 95 μm apart. Evidently, I_{AE} peaks almost exclusively within the passband of the delay line, reaching ~0.3 μA. Figure 31 also shows the RF characteristic of the delay line with the terminations conjugately matched to the impedance of the device ports; doing so compensates the impedance mismatch loss for this device by ~3 dB and an IL of 15.2 dB is measured. Next, E_d is applied across the DC contacts by means of a pair of DC probes connected to a power supply and the current (I_{DC}) passing through the underlying Si is measured. As the passing current value is increased, the otherwise reciprocal transmission (S_{21}) and reverse isolation (S_{12}) deviate from the initial condition. In the same direction as electron drift, both S_{21} and S_{12} are concurrently improved and a gain of 2.3 dB with a nonreciprocal transmission ratio (NTR $= S_{21}/S_{12}$) of 4.9 dB is measured at a CW current of 500 μA and E_d of 80 V/mm (48 V bias).
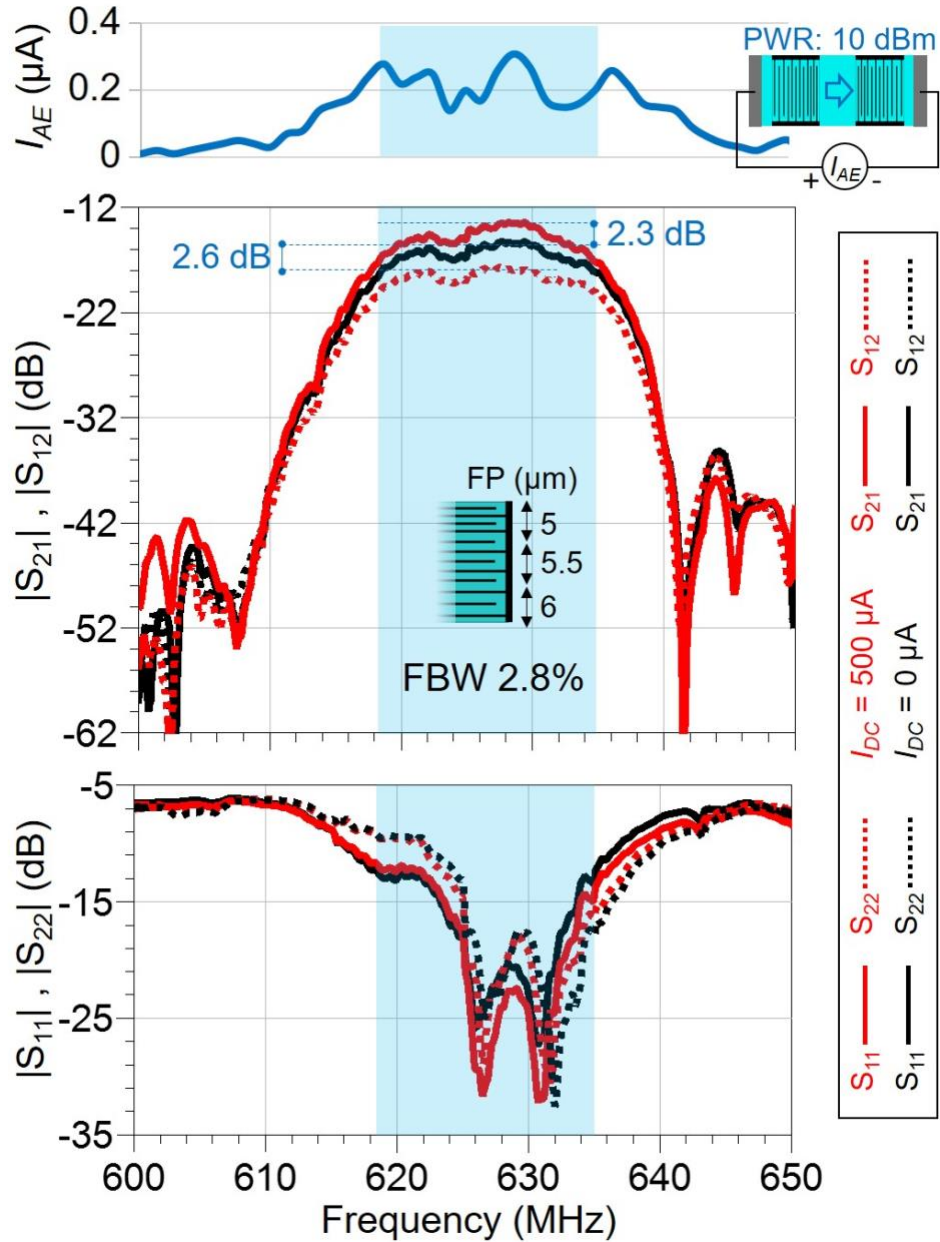
Figure 31. DC current generated as the input RF frequency is swept from 600 MHz to 650 MHz in a delay line with L = 95 μm (top). The frequency response of the device showing the reciprocal response without passing a current (black) and the acoustoelectrically induced non-reciprocity (red). A DC current of 500 μA at E_d of 80 V/mm is recorded in this case, resulting in 24 mW power consumption.

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Finally in this section, the amplitude tunability of the AE delay lines is demonstrated which can be potentially applied in SIC schemes. The LNoSi delay line IL is highly limited by the AE loss, therefore any change in the velocity of electrons via bias, would tune the IL within the range of max AE loss to max AE gain. This is shown for a ~650 MHz delay line with port IDTs 400 μm apart in Figure 32 where adjusting the I_{DC} would tune the IL. Compared to the shorter delay line in Figure 31, here as expected, a larger tuning range is realized once the current is swept from 0 to 400 μA and a 5.6 dB gain with 19.9 dB NTR is achieved at the maximum current (at 49 V bias and consuming 19.6 mW power). Furthermore, the transmission direction is reversed by reversing I_{DC}, therefore, transmission can be suppressed close to the noise floor, hence, virtually switching the device off. The measured AE gain in this case as a function of E_d is plotted in Figure 32 along with the fitted theoretical values. It is worth mentioning that the impact of the AE amplification and attenuation is much more evident in the passband of the delay line. This suggest the possibility of amplification without SNR reduction provided that coupling to spurious modes is engineered to be negligible, which is challenging but possible.
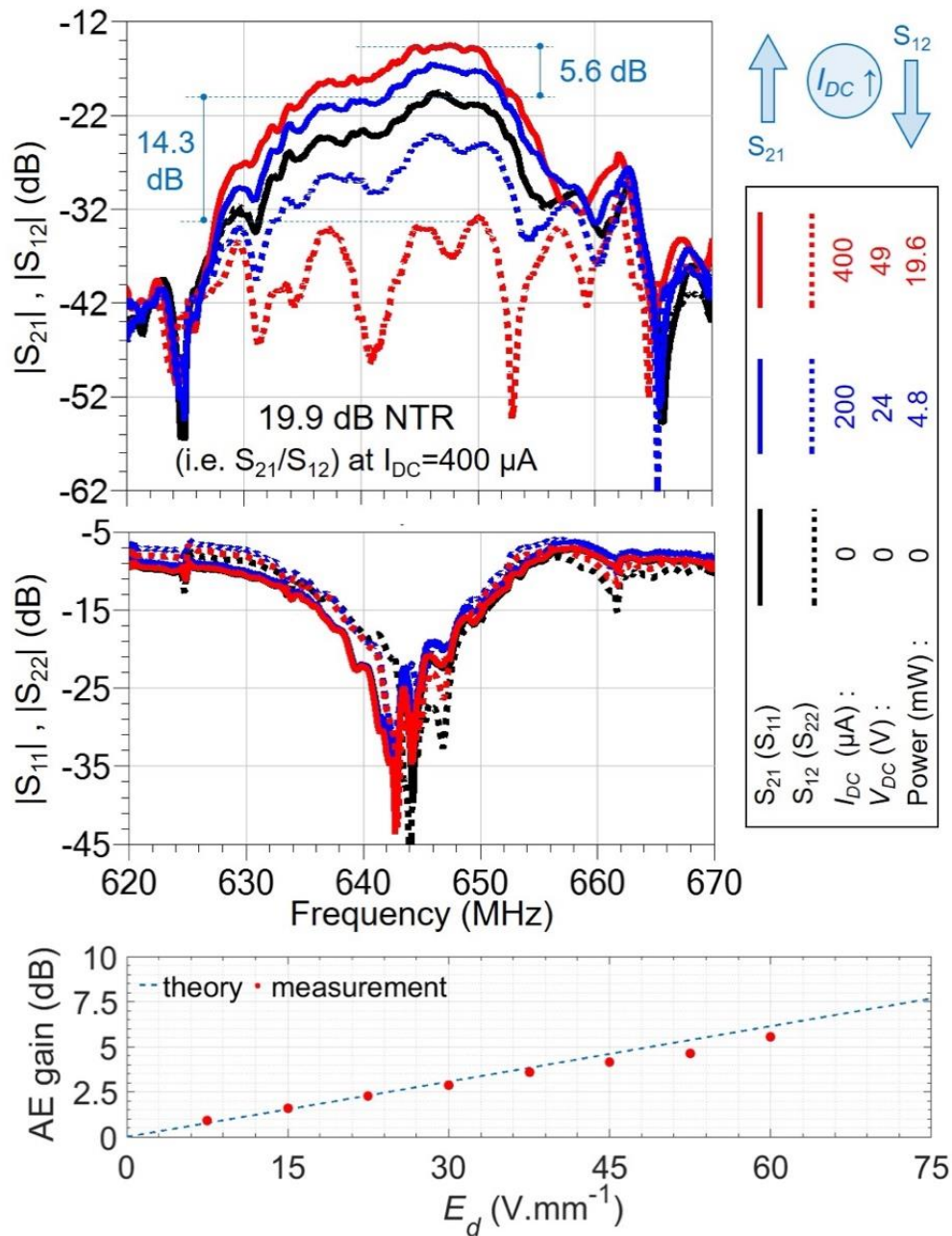
Figure 32. Measured frequency response of AE delay line with L = 400 μm for a current sweep, displaying switchable and tunable behavior. The theoretical gain curve fitted to the measurement results is shown at the bottom plot.

5.3.3   Carrier Control in AE Delay Lines

While the properties of the semiconductor layer (Si here) in the AE micro-acoustic devices can be tailored to achieve a high efficiency, the perturbation of the free carrier concentration and mobility at its interface with the piezoelectric film is inevitable. This could compromise the power efficiency and noise performance of the device. Since the depth of penetration of the evanescent electric field in Si is limited by the smaller of the L_D and $1/k_0$, surface charge control of Si at its interface with LN may provide a knob for retaining the targeted efficiency and performance. Therefore, here a technique for dynamic control of the carrier density is explored [90]. By taking advantage of the MIS capacitor inherently formed between the IDT, LN, and Si in such heterostructures (Figure 33) the carrier density in Si and subsequently the device efficiency can be modified. The preliminary results suggest that the efficiency is improved by slightly depleting the Si surface. The effect of the free carrier density and carrier mobility on the theoretical value of AE gain is plotted in Figure 33, showing a very strong dependency on the former. Therefore, the device under test (DUT) is characterized in two configurations: one with the negative terminal of V_{supply} connected to the RF signal ground (state I) and second when V_{supply} is isolated from signal (state II). The transmission response, |S$_{21}$|, of the device for the two configurations while increasing the V_{supply} from 0 V to 100 V in 25 V increments along with the measured currents in each case are presented in Figure 34. The value of V_{supply} is found to be much larger than the actual voltage across the delay line length as a result of the poor contact between the DC probe and Au-overlaid Si openings and the theoretical expectations and COMSOL simulations confirm this as well.
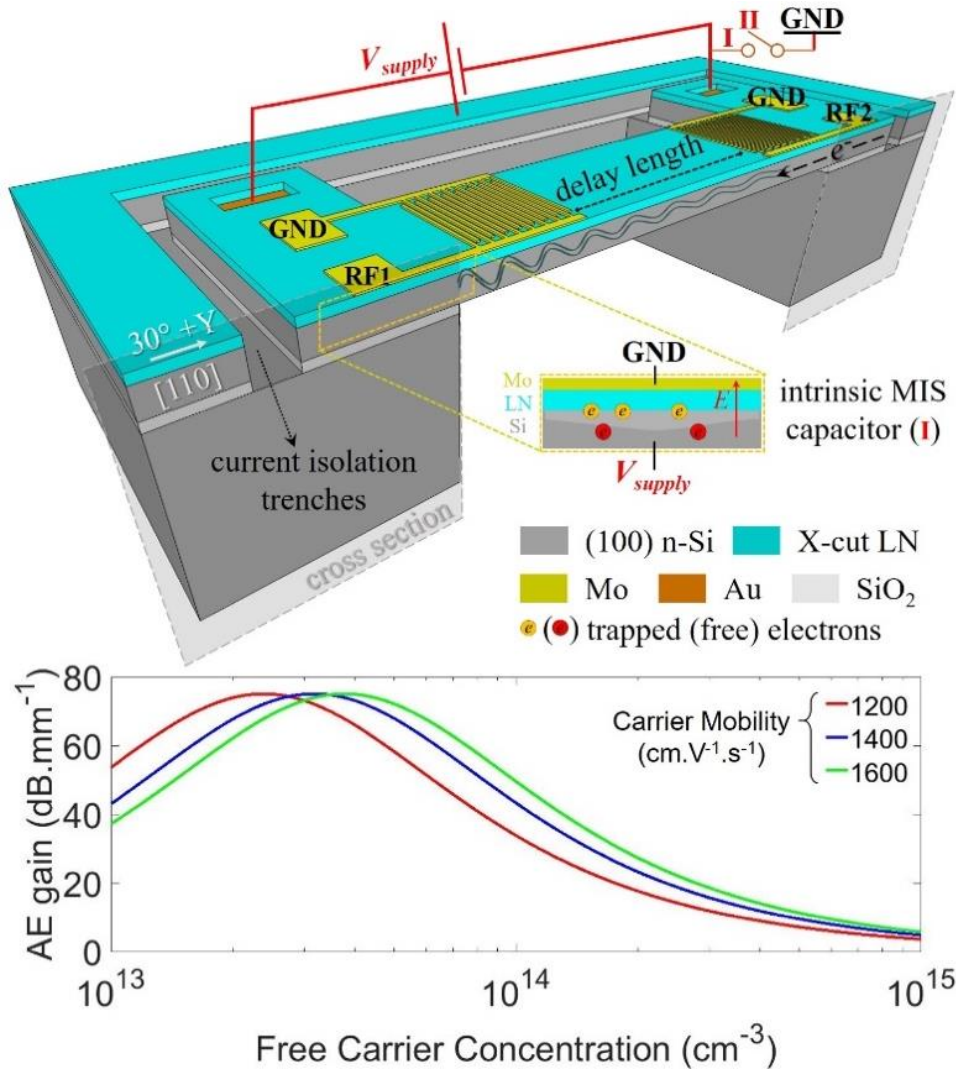
Figure 33. Device schematic showing the MIS capacitor used for adjusting the carrier density in the Si. This can be achieved by closing the switch to state (I), i.e. making the negative terminal of V_{supply} the same as ground. Theoretical AE gain as a function of free carrier density for three values of carrier mobility shown at the bottom highlights the importance of carrier density on the device efficiency.
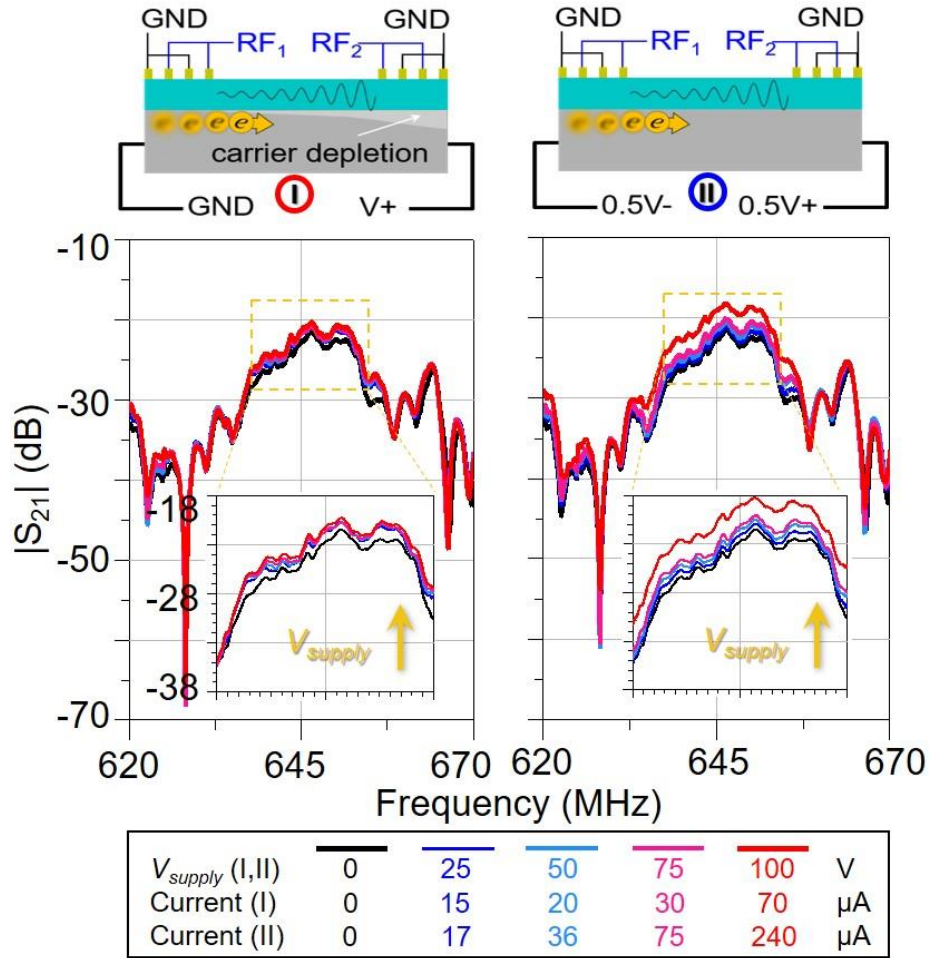
Figure 34. Transmission of DUT for the two configurations of applying V_{supply} with the corresponding measured currents. As schematically displayed at the top, in (I) the vertical electric field component results in depletion of Si.

It is evident that the measured passing currents in case (I) are lower than those of the case (II) due to the carrier depletion since a vertical electric field is induced in Si across the MIS capacitor in the first configuration. The measured AE gain and NTR as a function of V_{supply} is plotted in Figure 35; case (I) is plotted in red and case (II) in blue. It is observed that at V_{supply}=25 V the AE gain in the depleted case (I) is ~1.5 times that of case (II) while consuming slightly less

power (~60% efficiency improvement). Further depletion, however, reduces the gain relative to case (II). To further evaluate such hypothesis, a bias is applied to the top electrodes to confirm the effect of carrier depletion and accumulation. Consistent increase and decrease in the measured AE gain is observed for such cases, respectively. Figure 35 also compares the frequency characteristics of the device in the two configurations at V_{supply}=100 V, showing significant reduction of the AE gain and NTR due to deep depletion in case (I).
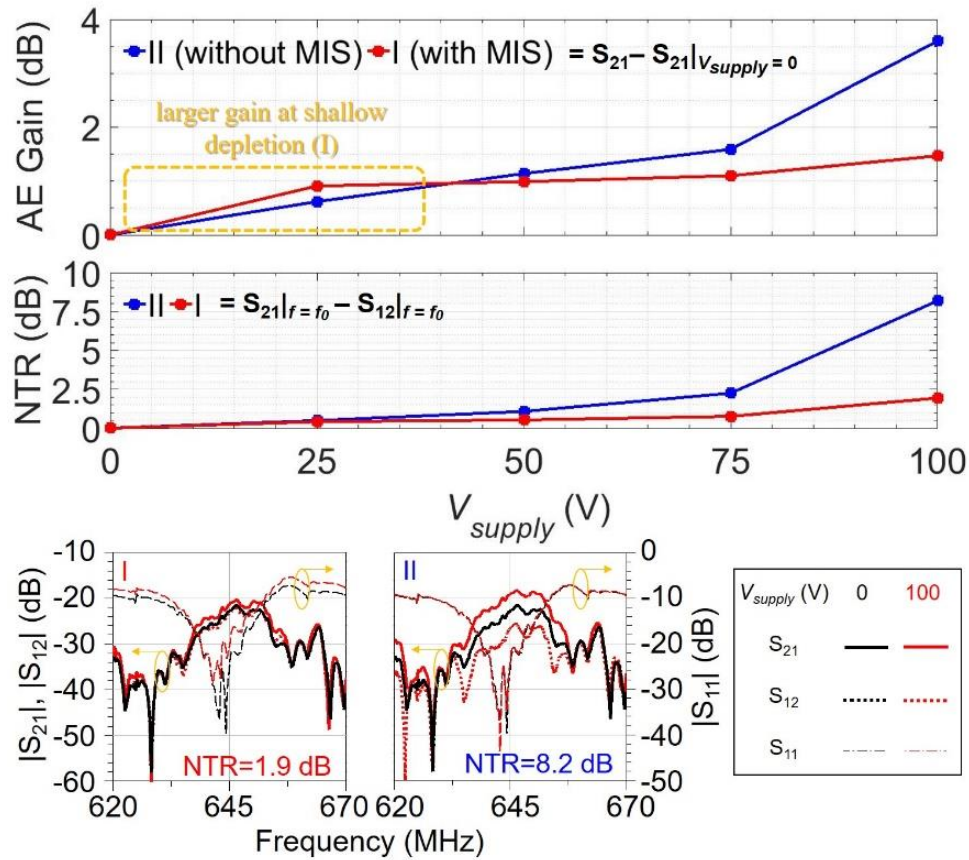
Figure 35. Measured AE gain and NTR versus V_{supply} for the two cases, red for (I) and blue for (II); a higher efficiency is observed for shallow depletion. Scattering parameters of the device at V_{supply}=100 V for the two cases is shown at the bottom.

5.3.4   Performance Optimization

The AE gain and non-reciprocal behavior obtained from delay lines having 3 μm Si layer are far from the full potential of LNoSi platform. This is contributed to the moderate K^2 of around 11% as a result of the small LN:Si thickness ratio (1/3) as well as large electron diffusion normal to the Lamb wave propagation which decreases bunching. The latter also causes the drifting electrons in Si to deviate from the homogenous current that is ideally desired. To concurrently improve the K^2 and enhance the current uniformity, a thinner Si layer must be chosen for the AE delay lines. From the AE gain equation for an acoustically thin stack, where τ is scaled by the Si thickness $\times\ k_0$ product, the effect of Si thickness on the AE gain with a simplifying assumption of constant K^2 across different Si thicknesses is shown in Figure 36. As the Si thickness decreases from the starting value of 3 μm, the slope of the curve passing through the synchronization bias ($V_A=V_D$) and 0 dB/mm gain point increases. This results in a larger gain at a smaller bias and the trend would hold until the Si thickness starts affecting the electron mobility.
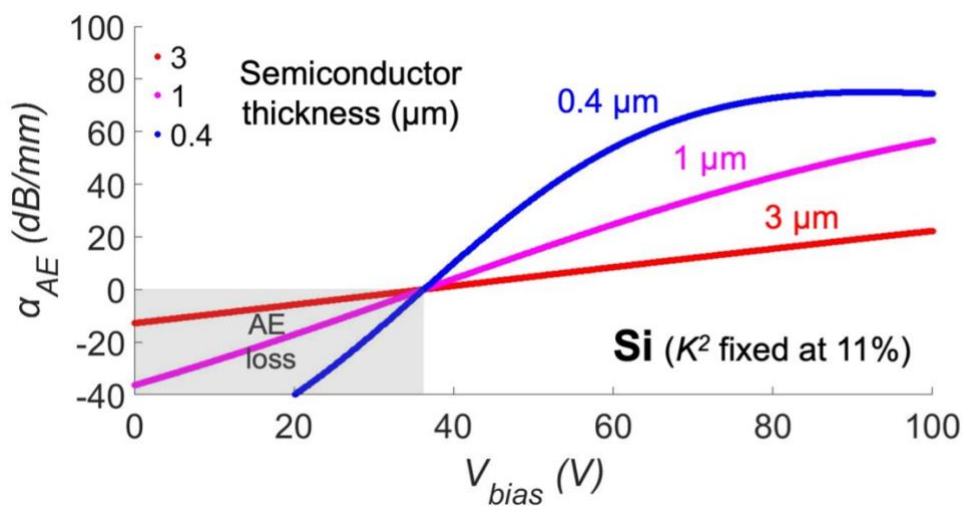
Figure 36. The effect of Si thickness on the AE gain coefficient assuming a constant K^2.

The compound effect of increased K^2 and thinner Si on the AE gain coefficient is shown in Figure 37 by comparing the AE gain curves for the LNoSi stack having 3 μm and 0.8 μm Si. The K^2 of former is assumed 11% and that of the latter is 18%. The AE gain experimentally demonstrated in the previous section is marked and the significantly improved gain expected from both increased K^2 and more drift current uniformity is clear.
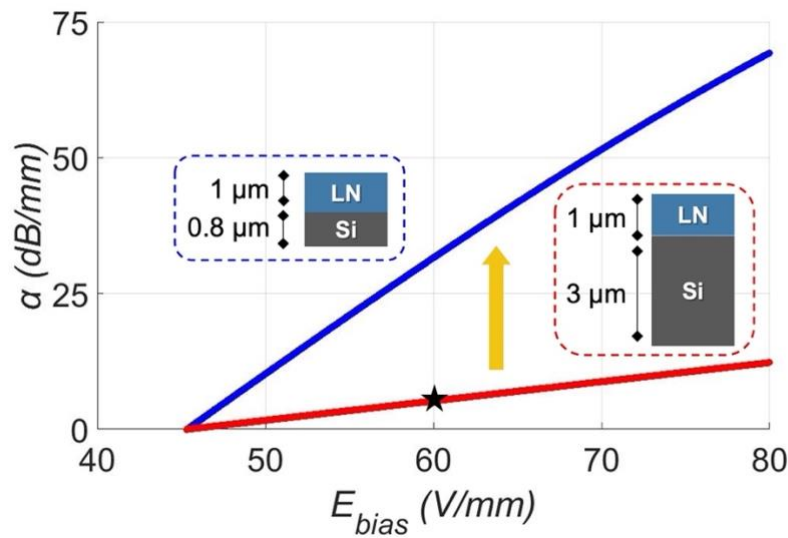
Figure 37. Modeled AE gain as a function of the applied drift field for LNoSi stacks having 3 μm and 0.8 μm Si showing improved gain for the latter case.

In order to experimentally verify the increase in AE intensity as a result of the thinner Si film, LNoSi AE delay lines are characterized after thinning the Si layer from backside in a SF_6/C_4F_8 containing plasma in ~1 μm steps. Typical frequency response of an 800 μm long delay line with a passband centered around 700 MHz is shown in Figure 38. The solid blue (after 1 etch cycle) and red curve (after 2 etch cycles) show the intrinsic IL of the device (without any bias) for a 0 dBm input RF signal. As expected from the theory, a higher IL is observed for the device with

thinner Si film since both the AE loss and gain would concurrently intensify because of the increased AE interactions. Once the bias is applied, and for a fixed voltage (plotted at 80 V here), a larger AE gain and subsequently lower IL is measured from the device with the thinner Si layer. This is shown by dashed curves in Figure 38. The etching is further performed to remove all the Si layer in order to estimate the loss imposed by the Si underlayer. This is shown in Figure 39 for a 700 μm and 800 μm long device, which respectively display a min passband IL of 10.4 dB and 11.1 dB. This translates to a Lamb wave propagation loss of 7 dB/mm in the LN waveguide which is much higher than the best reported value of 1 dB/mm [97] and implies further opportunity for film quality and fabrication optimization. The introduced loss due to Si in this case is estimated to be as high as ~32 dB which is the combined effect of AE loss, interface scattering loss, and K^2 reduction.
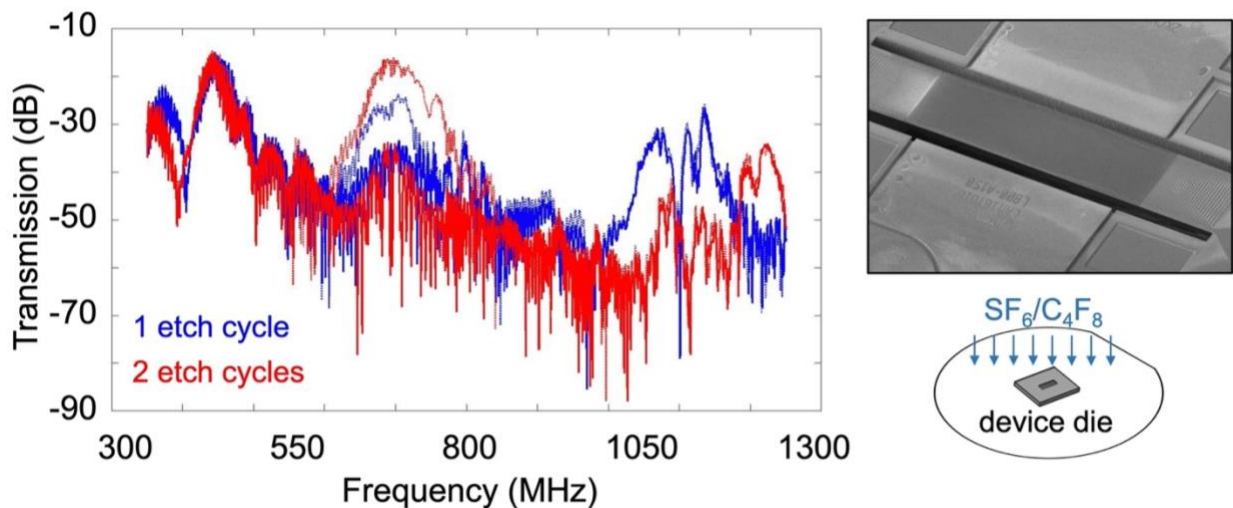
Figure 38. Measured transmission of the 800 μm long ~700 MHz AE delay line with ~2.3 μm (blue) and ~1.6 μm (red) remaining Si thickness. The device SEM and backside etching setup is shown on the right.
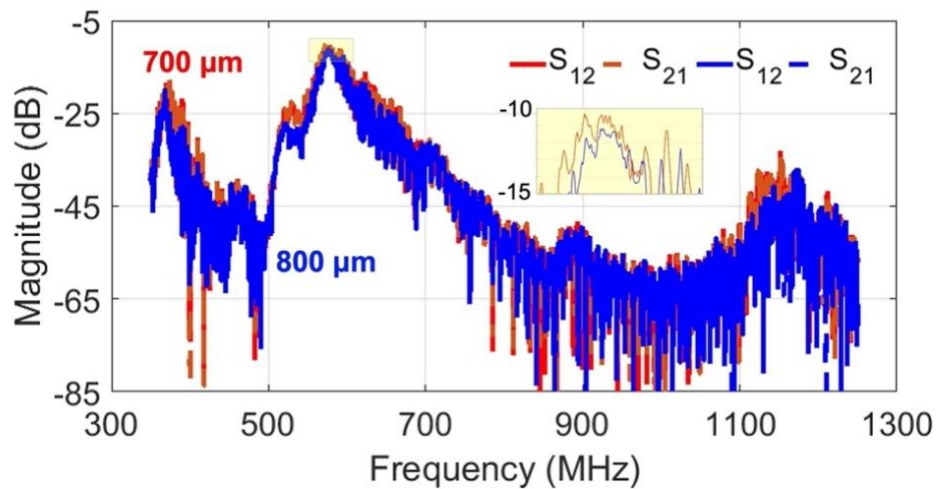
Figure 39. Measured frequency characteristic of 700 μm (red) and 800 μm (blue) delay lines after complete removal of Si underlayer. The IL is significantly improved and a propagation loss of 7 dB/mm is estimated.

The transmission (S_{21}) and reverse isolation (S_{12}) of a 400 μm long device (L400) is plotted in Figure 40 with solid and dashed black lines, respectively; without the DC pump, reciprocity is evident. Once the DC bias is applied, Lamb waves travelling along the electrons are amplified and an AE gain of up to ~22 dB (160 μW) is measured; this is plotted by red in Figure 40, leading to a minimum IL of 7.9 dB. Conversely, Lamb waves travelling opposite to the electrons are attenuated by more than 9 dB leading to a NTR of more than 31 dB; this is shown by the blue curve in Figure 40, having an IL of above 40 dB. The DUT demonstrates a spurious-free response in the span of 400 MHz with a minimum suppression of 20 dB. The 3 dB FBW of the DUT is measured to be 4.3%. The current passing through the device in this case is measured to be 85 μA which corresponds to a ~4 mW input DC pumped power; this results in a high efficiency of 4%. The reflection parameters are shown in Figure 40 as well with the DUT being matched to 50Ω ports.
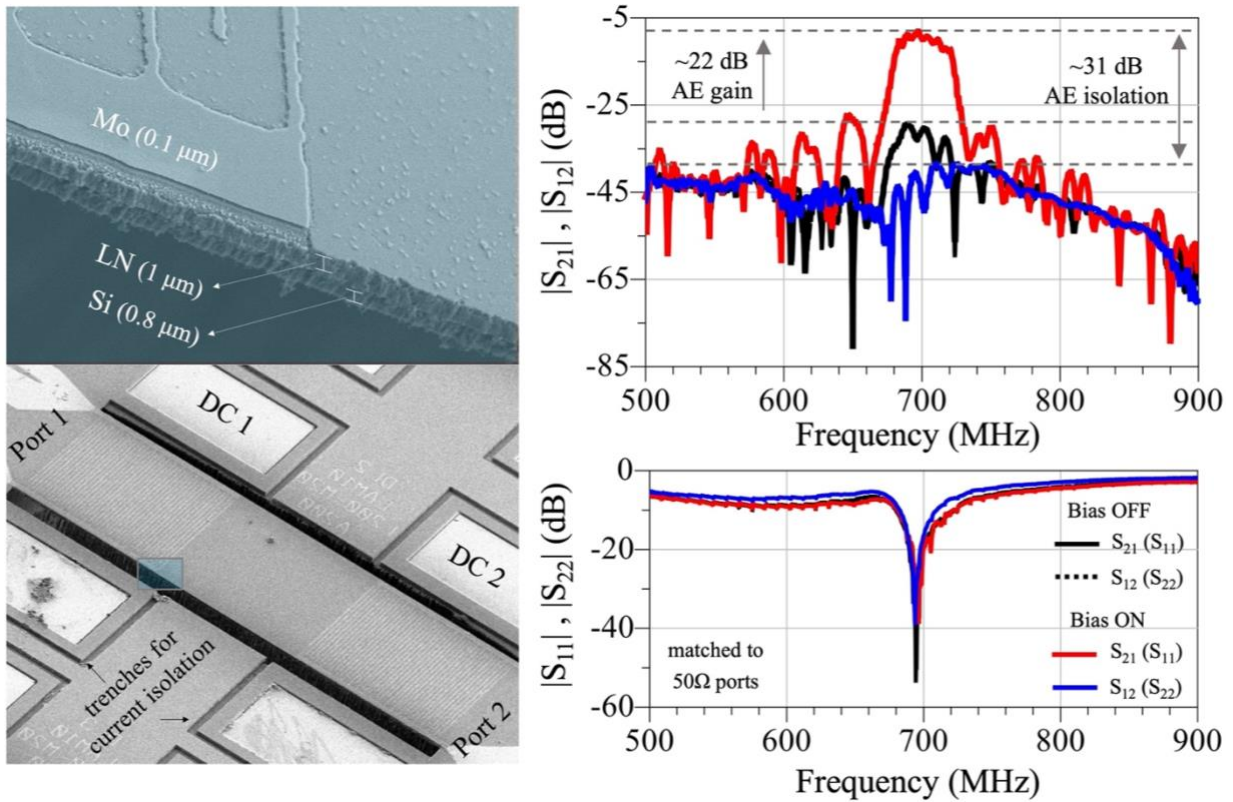
Figure 40. Measured transmission and reverse isolation of a L400 delay line once the bias is ON/OFF as well as the port reflections showing an AE gain of ~22 dB with ~31 dB isolation for a DC bias power of ~4 mW. The device SEM in shown on the left and the inset illustrates the LNoSi stack.

In order to determine the efficiency of the AE effect as a function of the input RF power level, a single tone test is performed. For this task, a 700 MHz tone at power levels of 0 to 18 dBm is generated by means of a signal generator and fed to the DUT while the output of the DUT is fed to a spectrum analyzer. The signal level before and after applying the bias is measured and from the difference of the two, the AE gain is calculated. This is shown in Figure 41 for two 200 μm long delay lines (L200) with apertures of 150 μm (A150) and 200 μm (A200). In these two cases, the bias pump power is respectively fixed at 13.5 mW (11.3 dBm) and 6.3 mW (8 dBm),

determined in the same manner as explained previously. A higher efficiency is observed for the

A200 device. Additionally, comparing the results from the L400 and L200 delay lines shows that

the longer device is much more efficient; with ~22 dB of gain at only ~4 mW for former (efficiency

= 4%) compared to ~15 dB of gain at more than 6 mW for latter (efficiency < 1%). It is worth

mentioning that the IL of all the delay lines studied in this section are in the range of 30 dB without

any bias application. This is believed to be mainly due to the AE loss, the roughness of device

boundary from etching steps, as well as the ohmic loss of the IDT.
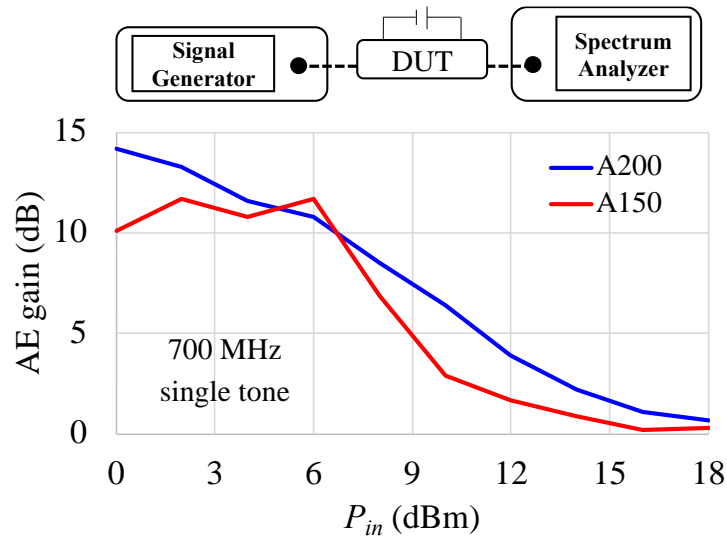
Figure 41. Measured AE gain of L200 delay lines as a function of the input RF power level. A single tone 700 MHz signal as shown in the measurement setup is used while a higher efficiency is observed for A200 device.

The excellent performance of the LNoSi delay lines in terms of the non-reciprocal

transmission makes them attractive for implementation of AE circulators [72, 91]. Thus, to

investigate the application of the AE delay lines as a building block of an AE circulator, the circuit

shown in Figure 42 is simulated using Keysight ADS; for this task, the measured data from a

biased L400 device is used while the delay lines (assumed identical) are coupled together by power

dividers.
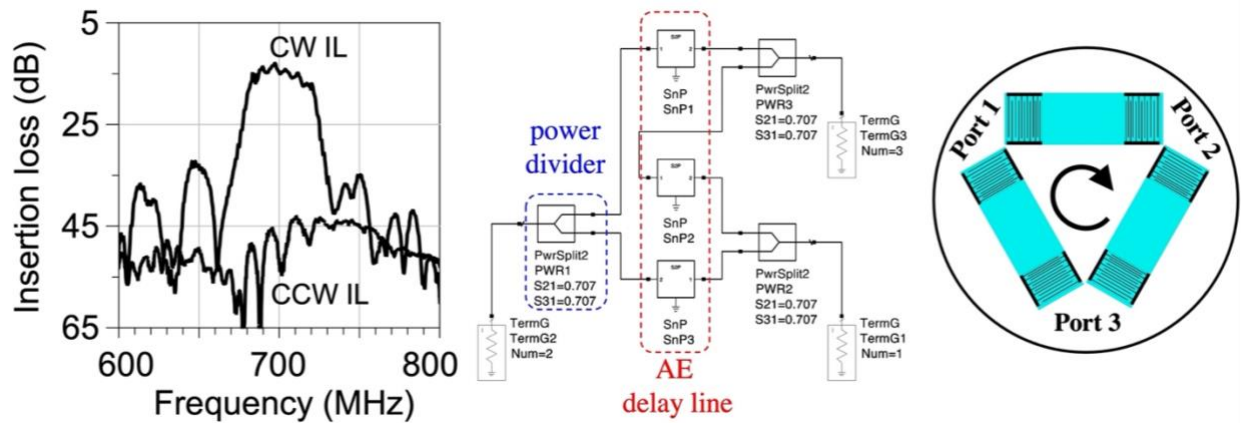
Figure 42. Simulated response of a simple AE circulator made from 3 AE delay lines electrically
connected with power dividers. The measured response of a 400 μm long device is fed into the
ADS model shown above.

As a final note, on the possibility of attaining terminal gain for realizing AE amplifiers, the

transmission response of an unmatched 600 μm long delay line is shown in Figure 43. By applying

a bias voltage of ~105 V (corresponding to 7 mW of dissipated power), the passband min IL is

improved from 42 dB to 3.6 dB, at -10 dBm input RF power. The 3.6 dB of IL is measured with

50 Ω terminations and can be improved to a -1.8 dB IL, or a 1.8 dB terminal gain by eliminating

the mismatch loss via changing the terminations to 165+j85 Ω. The resulting terminal gain,

however, does not hold for higher input RF powers as gain compression is evident in those cases.
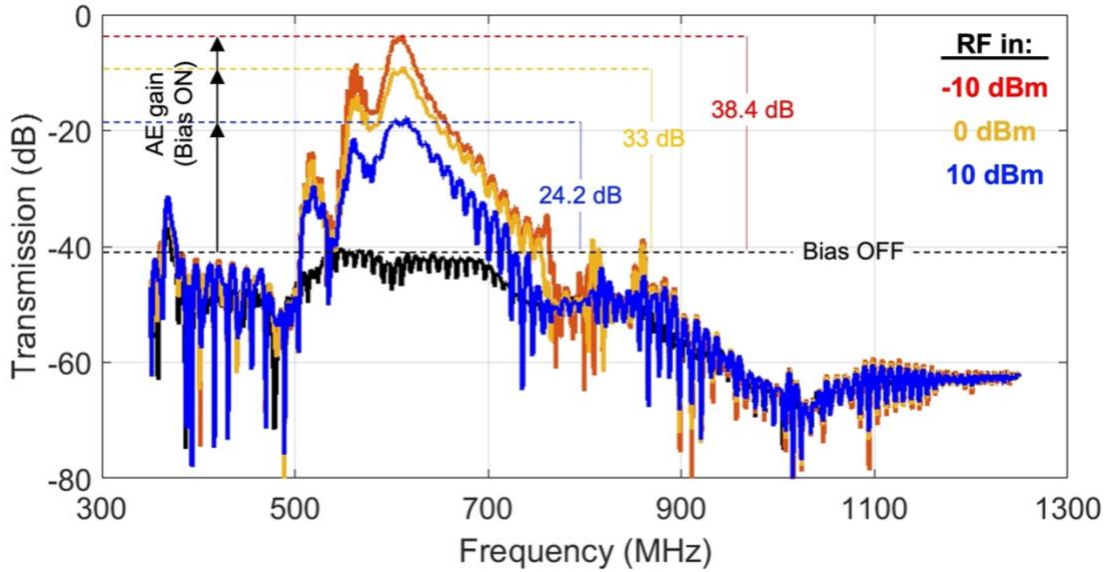
Figure 43. Measured transmission of a 600 μm long delay line once the bias is off (black curve) and at a bias voltage of 105 V for -10 dBm (red), 0 dBm (yellow), and 10 dBm (blue) input power. An AE gain of 38.4 dB is recorded leading to a min IL of 3.6 dB which is lower than the impedance mismatch loss (5.4 dB) and implies terminal gain with impedance matching.

5.3.5   Ultra-Wideband Operation Using SFIT

As previously mentioned, Lamb mode delay lines offering large delays of more than 10s of nanoseconds at very small scale, a few 100s μm in length, could be adopted in a broad range of applications given some of their performance bottlenecks such as high IL and limited FBW are addressed. A method for broadening the bandwidth of such delay lines is extending the application of slanted-finger interdigital transducers (SFIT), which has been developed for the SAW platform in the first place [92] and has been more recently entertained in suspended LN waveguides as well [93]. By doing so, a FBW of ~8% – with the convention being 6 dB below peak transmission – has been reported, however, the substantial diffraction losses associated with this type of transducers have resulted in a high IL (>26 dB) even for short delay lengths. SFIT can be perceived

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as multiple channels (sub-filters) across its aperture (Figure 44), with each channel targeting a specific wavelength via its lithographically defined FP. As a result of the relatively narrow aperture of each channel, the diffraction losses cause a significant deterioration of the device IL.
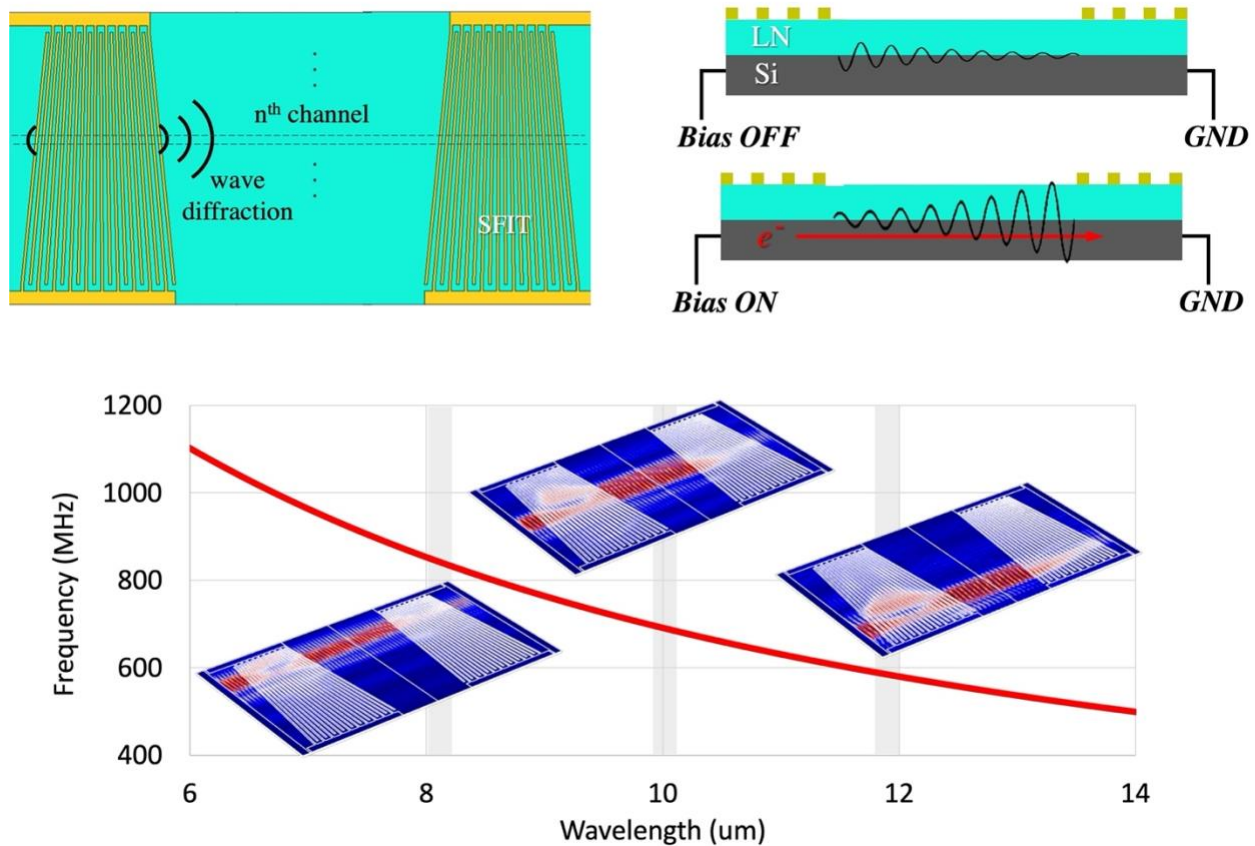
Figure 44. (Top) Device structure depicting acoustic wave diffraction in SFIT due to narrow aperture of each frequency channel. Upon bias, electrons drifting within Si could compensate such losses. (Bottom) Dispersion curve of the device stack showing >200 MHz available bandwidth for the designed SFIT with a 4-6 μm FP sweep. The delay line displacement at 3 passband frequency points is depicted using COMOSL FEA, showing diffraction effects.

To improve the high IL associated with SFIT, here such transducers are applied to LNoSi AE delay lines. By leveraging the AE amplification, therein, acoustic waves propagating along the electrons, which are drifting in the Si, will be selectively amplified, hence improving the IL [98]. This enables ultra-wideband (UWB) non-reciprocity at a low IL. From the LNoSi stack dispersion curve shown in Figure 44, more than 200 MHz bandwidth is attainable for a SFIT with its FP varying from 4 to 6 μm across the aperture. The SEM of such design is shown in Figure 45. The device has a length of 600 μm, measured from the mean distance between the two ports SFIT while the width of the delay line is 220 μm. The gold IDT coverage after fabrication is about half of the FP and the pass-band frequency is around 650 MHz.
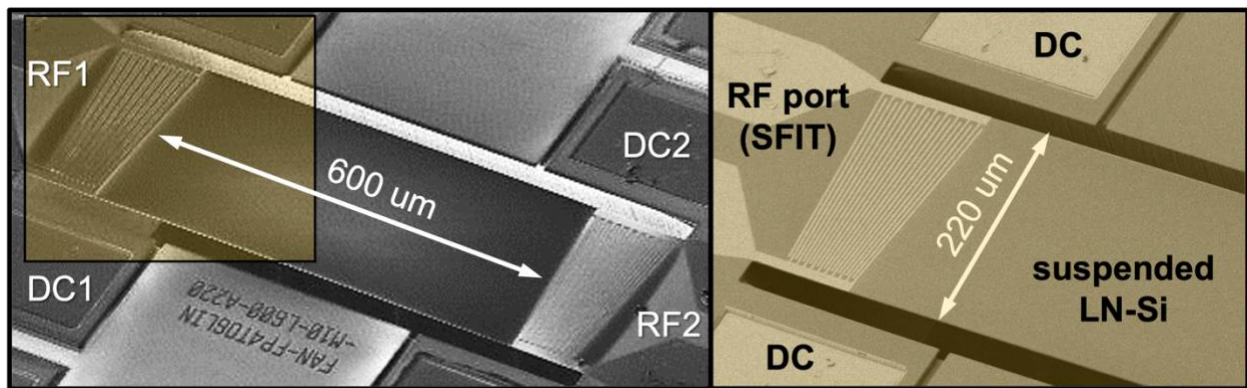
Figure 45. The SEM of a fabricated LNoSi delay line with SFIT for UWB non-reciprocity; the inset shaded by yellow shows the linearly swept FP from 4 to 6 μm across the SFIT aperture.

In Figure 46 the RF characteristic of a typical device with conjugately matched ports is shown before and after application of the DC bias. The input RF power from VNA is set at 0 dBm. Prior to the bias application, due to the large diffraction loss and AE loss, the delay line is virtually off. This is shown by the overlapping black and gray curves which respectively correspond to

transmission and reverse isolation and are roughly at -40 dB. Once the bias voltage is applied, the transmission gradually improves, reaching a maximum of -10.5 dB, as plotted by the red curve. The applied DC bias power in this case is measured to be 4.5 mW, equivalent to a 52 µA injected current. At this bias level, the measured 6 dB FBW is 33% while the minimum non-reciprocal transmission ratio is ~19 dB. From the blue curve which shows the reverse isolation, large ripples due to the formation of standing waves between the two ports SFIT are believed responsible for lowering the minimum isolation. Additionally, the observed dip in the passband is due to the destructive interference of sub-filters and could be relieved by optimizing the SFIT design, for example by adjusting the phase of sub-filters through a stepped-SFIT configuration [94]. While, so far, the reported passbands of the AE delay lines in the literature have been very narrow (generally having FBWs below 5%), the solution presented in this section that resulted in a very wide measured FBW could satisfy the need for UWB non-reciprocal transmission.
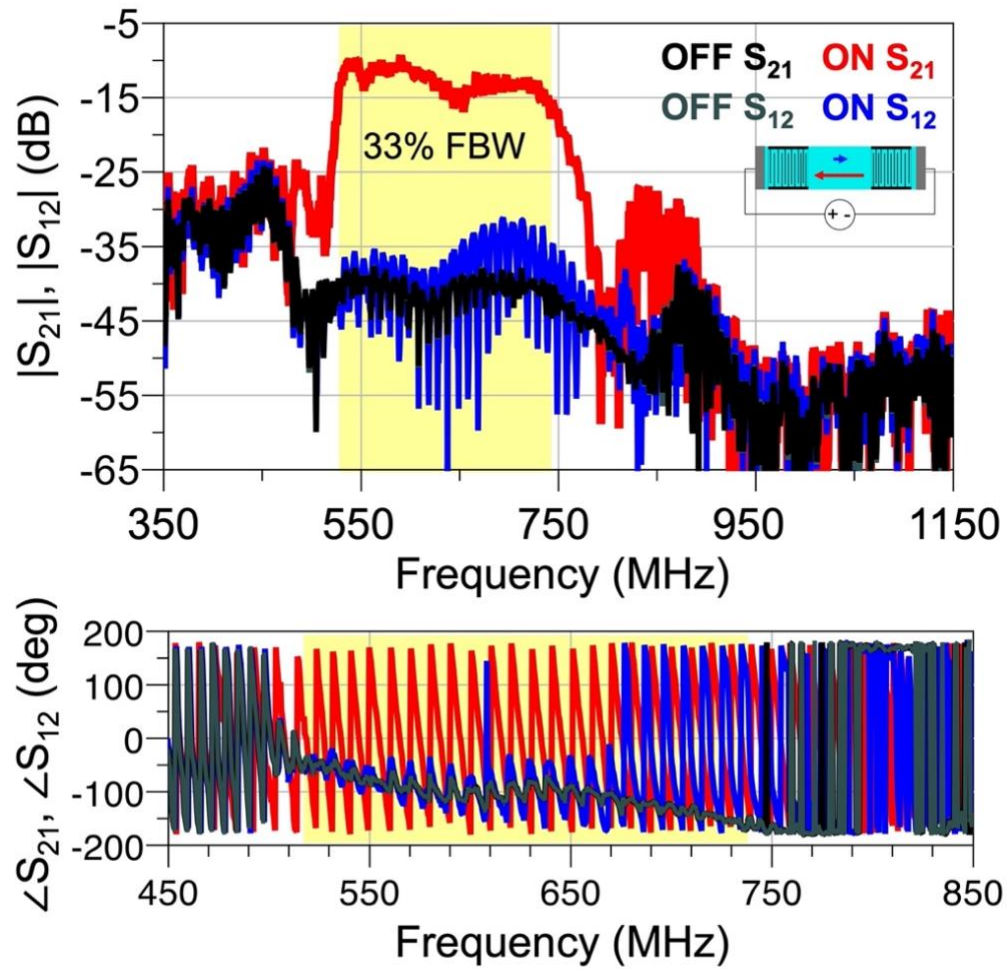
Figure 46. Measured wide-span magnitude and near-passband phase of transmission (S_{21}) and reverse isolation (S_{12}) of the 600 μm delay line with SFIT before (black & gray) and after application of bias (red & blue); The measured dissipated bias power is 4.5 mW in this case.

CHAPTER 6: FABRICATION PROCESS

In this chapter the process flow for the fabrication of the AlScN-based and LN-based micro-acoustic devices is discussed. The fabrication process in each step is explained in detail and solutions for practical problems are pointed out.

6.1   Scandium-Doped Aluminum Nitride on Silicon

AlScN-based devices are fabricated on SOI wafers in a six-mask process with all the processes being done at temperatures below 300°C. The thickness and doping of the Si device layer is chosen based on the required AE parameters discussed earlier. The fabrication of the device is summarized in Figure 47. The staring SOI wafer is sputtered with ~50 nm layer of AlN as the seed layer for promoting the c-axis growth of the subsequent AlScN film. The piezoelectric sputtering is done by Advance Modular Systems Inc. (AMSystems) and next a 100 nm layer of Mo is deposited on the seed layer and pattered to form the bottom electrode. The bottom electrodes layout is designed so that devices in three configurations of not having a bottom metal, having a floating bottom metal, and with a grounded bottom metal are fabricated. Also, it is desired to remove the bottom Mo layer in areas which could result in a parasitic capacitance like underneath the probing pads. The bottom metal is sputtered in an RF sputtering system and then dry etched in SF_6/O_2 plasma using a tabletop reactive ion etcher (RIE). The reasons for choosing Mo are manifold; as the bottom electrode material also acts as the seed layer for the sputtered AlScN film it is essential for the two to be lattice matched. Additionally, during the subsequent blanket etch and release processes, the bottom metal would also be exposed to Hydrofluoric (HF) acid, hence, it should be resistant to HF. Finally, the acoustic properties of this layer, namely, acoustic velocity

and loss are desired to be high and low, respectively. As such, Mo is chosen for the metal layer due to its small lattice and thermal expansion coefficient mismatch with AlScN, low acoustic loss, high acoustic velocity, and resistance to HF. Since the atmospheric oxidation of Mo starts at ~250°C it is essential for the process steps conducted outside a vacuum to be performed below this temperature. Next, a 1 μm $Al_{0.8}Sc_{0.2}N$ layer is sputtered on the pattered bottom Mo, by AMSystems, followed by sputtering of the top metal layer. Again, 100 nm of Mo is sputtered for this task and patterned in SF_6/O_2 based plasma to form the desired top electrode patterns. Subsequently, contacts to the underlying Si device layer and bottom electrode are formed by wet etching the piezoelectric layer. For this task, a ~400 nm thick SiO_2 is deposited on top of the wafer with plasma enhanced chemical vapor deposition (PECVD) to act as the hard mask. The SiO_2 layer is then patterned with photoresist and etched in CHF_3 plasma in RIE. It is worth mentioning that for the case of exposed Si at the backside of the wafer, it is suggested to also deposit a few 100 nm layer of SiO_2 to prevent the basic wet etch solution from rapid depletion. In order to wet etch the $Al_{0.8}Sc_{0.2}N$, an altering bath of heated tetramethylammonium hydroxide (TMAH) based solution and sulfuric acid is pursued. Once the bottom Mo and Si contacts are clear, a 25/75 nm layer of Ti/Au is electron beam evaporated on all the electrical pads and contacts and patterned via lift-off process to reduce ohmic losses and improve contact while probing. Next, the lateral boundary of the resonator is defined by etching the $Al_{0.8}Sc_{0.2}N$ and Si layer in chlorine based inductively coupled plasma (ICP) RIE and deep RIE (DRIE), respectively. For this task, a few μm thick SiO_2 layer is deposited via PECVD and patterned with photoresist and etched with CHF_3 plasma in RIE to form the etch mask. Finally, the wafer is flipped and the pattern for backside cavities are transferred onto a >10 μm thick photoresist mask on the wafer. To etch the backside, the wafer is

mounted on a handle wafer with thermal grease to allow for cooling and the backside of the substrate is etched all the way to the buried oxide (BOX) layer. The devices are finally released by etching the BOX layer in buffered oxide etchant (BOE).
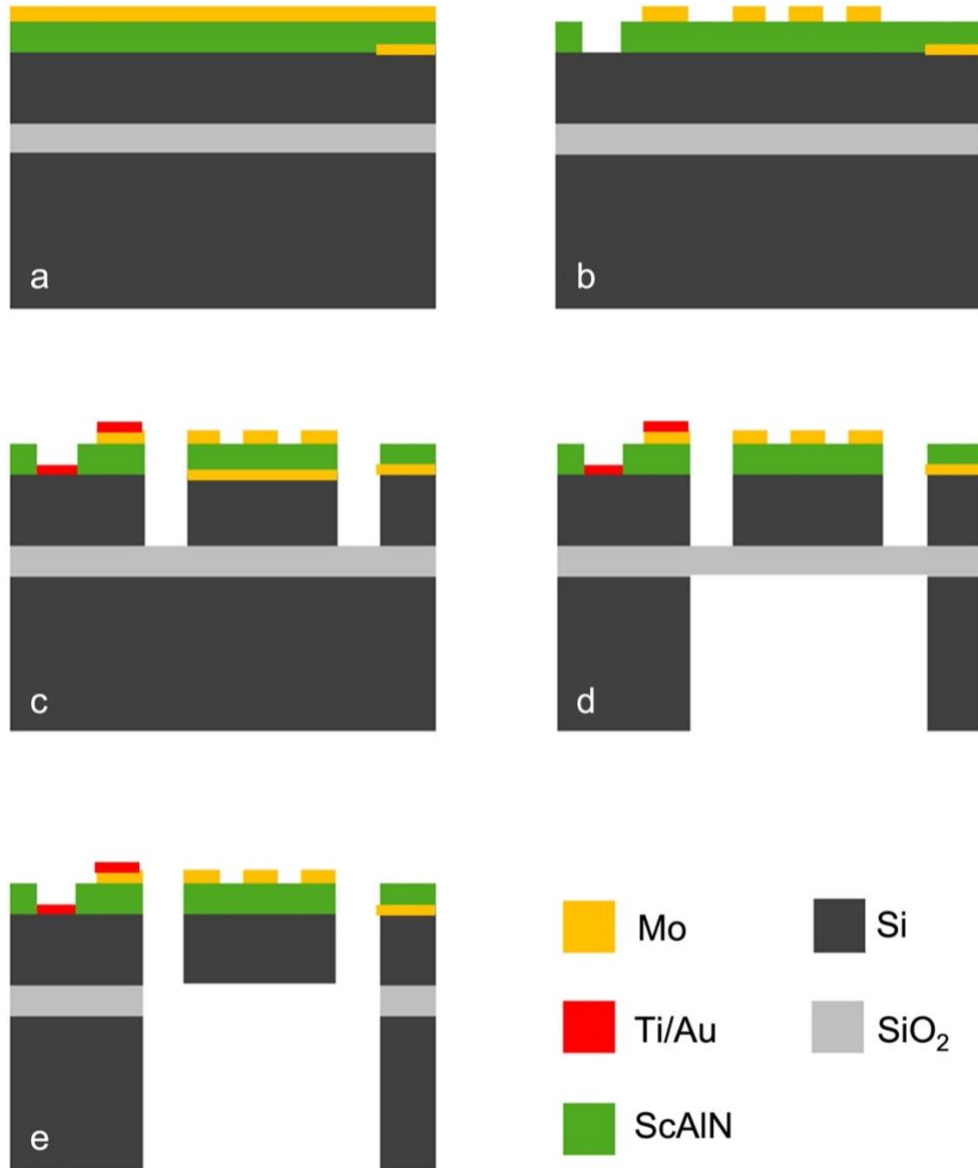
Figure 47. Fabrication process flow showing (a) the initial stack with patterned bottom electrode layer (b) patterning top electrode and etching the piezoelectric layer for contacting the Si layer (c) probing pad deposition and etching the device layer (d) etching the wafer backside and (e) releasing the device.

6.2   Lithium Niobate on Silicon

LN-based devices are fabricated in a five-mask process with all the processes being done at temperatures below 300°C. The starting substrate provided by NGK Insulators LTD is comprised of a 1 μm X-cut LN film bonded to a 3 μm (100) SOI wafer. The LN film is oriented in a way that the wave propagation axis is aligned to both the [110] Si plane and the 30° off +y-axis direction of LN, which as mentioned yields the highest electromechanical coupling for excitation of the S_0 mode acoustic waves. The Si layer is n-type doped with a 5-10 ohm.cm resistivity. For the top IDT material, two cases of Mo and Au are pursued both having a thickness of ~100 nm. For the case of Mo IDT, sputtering followed by pattering with photoresist and etching in SF_6/O_2 plasma was performed. For Au IDT, lift-off is performed with a 25/75 nm Cr/Au layer deposited via e-beam evaporation. The Mo electrodes initially outperformed the Au electrodes in terms of adhesion to the LN surface, however, during the subsequent processes and release steps they were degraded, resulting in thinner than expected IDT with increased resistivity. The Au electrodes, on the other hand, aside from some adhesion issues during the PECVD step, showed less degradation and resistive loss. Next, Au contacts to Si are made by dry etching the LN film using a combination of argon and fluorine plasma. It was determined that much lower resistive loss can be accomplished by using an Ar only recipe as the etch rate would not rapidly increase once the Si is exposed. Next, the lateral dimension of the device is defined by dry etching trenches in the LNoSi stack. The 1 μm LN film is etched using either a mixture of Ar/F or Ar only in a ICP RIE. For the former a hybrid mask of 300 nm PECVD SiO_2 and 200 nm e-beam evaporated Ni is used. The Ni is patterned with photoresist and wet etched in Ni etchant. For the latter, a ~3 μm PECVD SiO_2 is deposited and patterned using a ~4.5 μm photoresist mask. The resulting sidewall profiles after the

two different etch recipes show that a closer to 90° sidewall is achieved for the case with hybrid mask etched in Ar/F plasma, but the sidewall roughness is more pronounced due to the formation of non-volatile LiF during etch and its re-sputtering. On the other hand, the physical only etch done with thick hard mask shows less roughness but more angled sidewalls due to the nature of this type of etching (Figure 48). It is worth mentioning that RCA1 cleaning is intermittently performed during the etch to clean the re-sputtered etch byproducts. Once the LN film is etched, the underlying Si is etched with DRIE process.
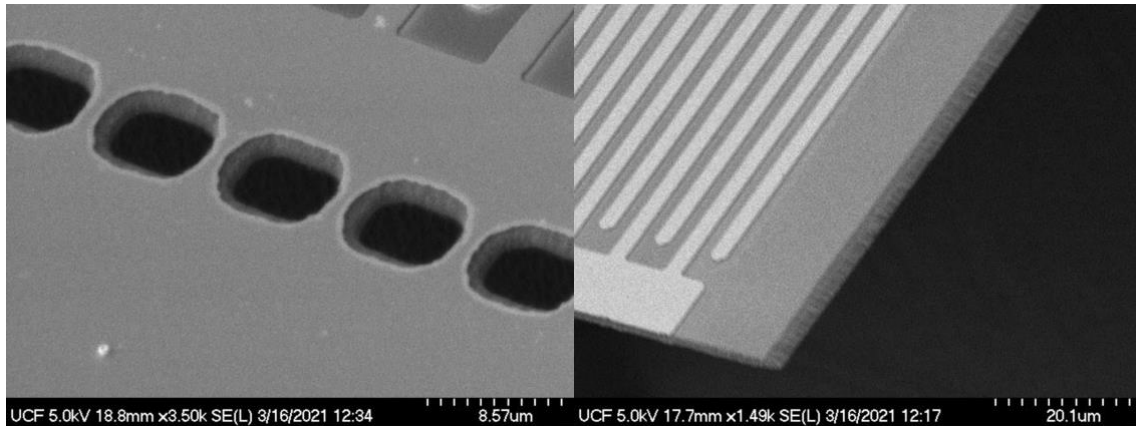
Figure 48. Device sidewalls after etching the LN film in an Ar only plasma showing the sloped etch profile.

The wafers are subsequently flipped, and the backside is patterned with a ~12 μm photoresist. To etch the backside, the wafer is mounted on a handle wafer with thermal grease to allow for cooling and the backside of the substrate is etched all the way to the BOX layer. This is followed by placing the devices in BOE so that they become released. The wet release is properly timed to avoid excess undercut of BOX layer that can form short electrical paths between the

device and handle Si layers due to stiction or upon large bias application. The bonded wafer is shown in Figure 23 and the fabrication steps are summarized in Figure 49.
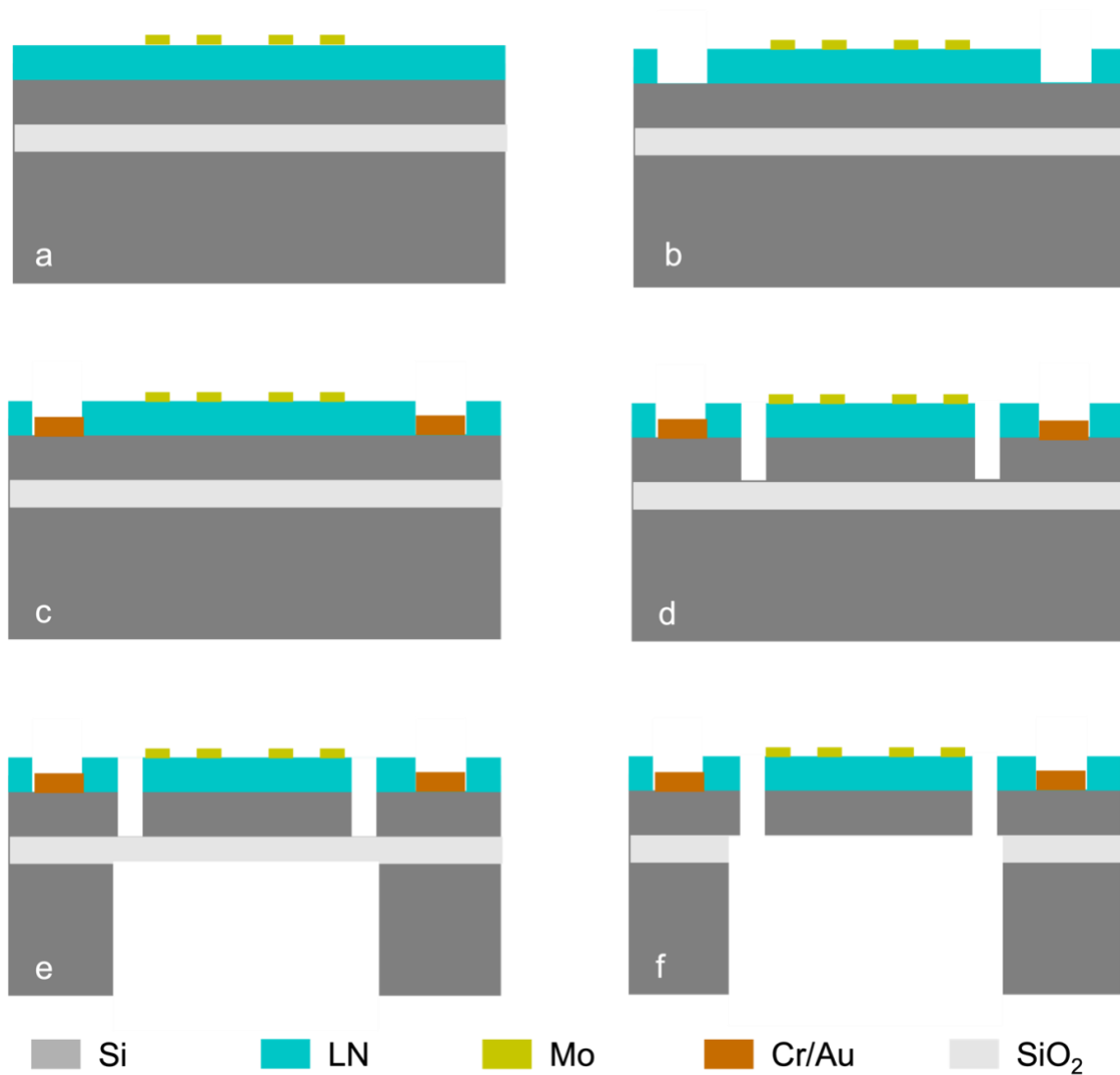
Figure 49. The LNoSi fabrication process flow showing (a) the bonded LN-Si with patterned top electrodes (b) etching LN to open Si contact windows (c) forming electrical contact to Si layer (d) etching the lateral device boundaries (e) etching the backside of the wafer (f) releasing the device.

CHAPTER 7: CONCLUSIONS

In this dissertation, it was demonstrated that micro-machined Lamb mode waveguides made of piezoelectric-semiconductor thin films provide an excellent platform for analog signal processing by taking advantage of the acoustoelectric effect. This platform could potentially enable a single-chip and frequency-disperse solution for attaining the superior performance of piezoelectric acoustic wave devices augmented with amplification and nonreciprocal functionalities. Single-chip fabrication of acoustic filters, delay lines, switches, amplifiers, isolators, and circulators could significantly reduce the size and packaging complexities. The heterostructured design allows for independent choice of a strong piezoelectric along with a high mobility and high power-handling semiconductor to attain unprecedented power efficiency in a sub-millimeter footprint. In Table 5 the performance of LNoSi Lamb wave devices introduced in this work is compared against that of the SAW counterparts with the highest reported performance.

Table 5. AE performance metrics of SAW platforms and the Lamb wave platform (this work)

Reference	Platform	Frequency (MHz)	Gain (dB/mm)	Non-Reciprocity (dB)	Power (mW)	Continuous Bias
[20]	Si-LN	107	5.5	-	7000	✔
[70]	Si-LN	470	-	10	-	✔
[71]	Graphene-LN	170	9	16	137	✔
[72]	InGaAs-LN	276	80.6	46	15	✘
This work	**LNoSi**	**700**	**>40**	**>40**	**<10**	✔

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