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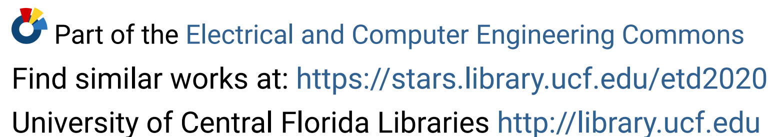
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STUDY OF MoS_2/HIGH-*k* INTERFACE & IMPLEMENTATION OF MoS_2 BASED MEMRISTOR FOR NEUROMORPHIC COMPUTING APPLICATIONS

by

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A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
in the Department of Electrical and Computer Engineering
in the College of Engineering & Computer Science
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ABSTRACT

The scientific world is witnessing an unprecedented triumph of artificial neural network (ANN)- a computing system inspired by the biological neural network. With the enthralling quest for Internet of Everything (IoE), it is expected to have an unparalleled dominance of ANN in our day-to-day life. In recent times, memristor has come as an emerging candidate to realize ANN through emulating biological synapse and neuron behavior. Molybdenum disulfide (MoS_2), one well-known two-dimensional (2D) transition metal dichalcogenides (TMDCs), has drawn interest for high speed, flexible, low power electronic devices since it has a tunable bandgap, reasonable carrier mobility, high Young's modulus, and large surface to volume ratio. Hence, in this work, 2D MoS_2 based field effect transistor (FET) and memristor devices have been developed to evaluate the performance for advanced logic and neuromorphic computing applications. We probe the superior quality of 2D/high-κ dielectric interfaces by fabricating MoS_2 based FET transistors with different gate dielectrics. This low interface trap density of $\sim 7\times10^{10}$ states/cm^2-eV at the MoS_2/Al_2O_3 interface establishes the case for van der Waals systems where the superior quality of 2D/high-κ dielectric interfaces can produce high performance electronic and optoelectronic devices. This work also demonstrates Au/MoS_2/Ag threshold switching memristor (TSM) device with low threshold voltage, sharp switching, high ON-OFF ratio and endurance. A leaky integration-and-firing (LIF) neuron is implemented with this TSM. It successfully emulates the key characteristics of a biological neuron. The LIF neuron is monolithically integrated with the MoS_2 based synapse device to realize a single layer perceptron operation and Boolean logic gates. The Au/MoS_2/Ag TSM device also imitates a nociceptor, the single device exhibits all the key features of nociceptors including threshold, relaxation, "no adaptation" and sensitization

phenomena of allodynia and hyperalgesia. This work indicates applicability of this device in artificial intelligence systems-based neuromorphic hardware applications and artificial sensory alarm system.

To my family

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LIST OF ACRONYMS (or) ABBREVIATIONS

2D	Two-Dimensional
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
ANN	Artificial Neural Network
CMOS	complementary Metal–Oxide–Semiconductor
CVD	Chemical Vapor Deposition
D_{it}	Interface Trap Density
E-beam	Electron-beam
EDS	Energy-Dispersive X-Ray Spectroscopy
EOT	Equivalent Oxide Thickness
FET	Field Effect Transistor
h-BN	Hexagonal Boron Nitride
HCS	High Conductance State
HH	Hodgkin–Huxley
HRS	High Resistance State
HRTEM	High Resolution TEM
IF	Integrate-and-Fire
IoT	Integrate of Things
IQHE	Integer Quantum Hall Effect
IR	Inhibition Ratio
ITD	Interaural Time Difference

LCS	Low Conductance State
LIF	Leaky Integrate-and-Fire
LRS	Low Resistance State
LTD	Long Term Depression
LTP	Long Term Potentiation
MOS-C	Metal Oxide Semiconductor Capacitor
MOSFET	Metal Oxide Semiconductor FET
PCM	Phase Change Materials
RT	Room Temperature
SNN	Spiking Neural Network
SS	Subthreshold Swing
STDP	Spike Timing Dependent Plasticity
STEM	scanning Transmission Electron Microscopy
STP	Short Term Potentiation
TCR	Temperature Coefficient of Resistance
TEM	Transmission Electron Microscopy
TEMAZ	Tetrakis(ethylmethylamino)zirconium
TMA	Trimethylaluminium
TMDC	Transition Metal Dichalcogenides
TSM	Threshold Switching Memristor
WGFMU	Waveform Generator/Fast Measurement Unit

CHAPTER 1 INTRODUCTION

The semiconductor industry has experienced an unprecedented growth for the last five decades. The continuous shrinking of the geometrical dimensions along with the rapid evolution of the performances, the silicon-based field effect transistor (FET) has played the central role for this enormous expansion of the semiconductor field. The tremendous evolution like the shifting from the planner FET to FinFET, scaling down from the μm gate length to few nm gate lengths, introduction of high-κ gate dielectric etc. has kept the FET technology in line with the Moore's law and enabled to keep pace with the ever-increasing demand of super-fast and low power electronic and optoelectronic devices. [1-4] The technology has been reached to a critical point where the challenges like gate leakage current, high static power dissipation, mobility degradation are getting prominent with the scaling down process. [3, 5, 6] To sustain the Moore's law, implementation of new device geometry and utilization of the new material is getting inevitable.[7, 8] Along with the miniaturization of the electronic devices, there is increasing trend of shifting from rigid substrate to the flexible and wearable platform for electronic devices.[9, 10] With the tremendous technological development, we are getting more dependent on the electronic devices in our day-to-day life. Most of these devices travel with us and are connected to the network for communicating, providing service, and transferring information. Flexible or wearable platform for these devices is in high demand as it provides better durability, space efficiency and comfort compare to the rigid substrate. The coexistence of the bendability, flexibility and stretchability with the preservation of electronic properties even at maximum deformation are the unique requirement for the flexible and wearable electronics.[11] These exceptional properties are not readily available with the traditional electronic materials, hence, there is also ongoing quest for

new materials for future flexible and wearable electronic devices. The isolation of the graphene in 2004 and subsequent rediscovery of other two-dimensional (2D) materials like transition metal dichalcogenides (TMDCs), Bi_2Se_3, Bi_2Te_3, hexagonal boron nitride (h-BN), black phosphorus has set a new direction for the expedition of next generation electronic materials.[12-15] The layered structure and high carrier mobility along with other exceptional thermal, chemical, mechanical, and electrical properties initiates the opportunity of getting ultimate "thin" devices with the faster speed and low leakage current. The exceptional tensile strength with high Young's modulus and spring constant of the 2D materials also made it a very promising candidate for the next generation flexible and wearable electronics.

1.1 Two Dimensional (2D) Materials

2D materials are solid crystalline having single or few layers of atoms with very large lateral dimension as compared to their thickness.[16] The high aspect ratio enables the 2D materials to attain complete unique properties compare to its bulk counterpart. Recent report showed, in nature there are around 1800 layered structures that can be thinned down to 1 layer or multilayer (<10 nm) and termed as 2D material.[17] This large family encompasses materials with all different kind of conduction mechanisms (metal, semimetal, semiconductor, insulator, superconductor) as shown in **Figure 1**.[18] Out of this large number of materials, graphene is the most popular and most studied 2D material. Graphene is the single layer of sp^2 hybridized carbon atoms with 2D hexagonal (honeycomb) lattice structure. [12] Graphene shows ambipolar characteristics with exceptionally high carrier mobility (10^5 $cm^2/V.s$) due to the ballistic transport.[19] The exceptional behavior of Dirac fermions in presence of the magnetic field

enables graphene to show integer quantum hall effect (IQHE) at room temperature.[20] Graphene also has astounding material properties like very high Young's modulus (~0.5–1 TPa), spring constant of ~1-5 N/m and tensile strength of ~130 GPa. [21-24]This noble material also covers the wide range of optical absorption spectrum (300-1400 nm) and shows transparency of 97% at the visible wavelength. Along with the high thermal and chemical stability, it offers other materials large specific surface area for conformal adhesion.[19] Due to all these extraordinary material, electrical, thermal and chemical properties graphene has been extensively explored for wide range of electronic-optoelectronic applications. Despite of having a significant number of tunable properties the zero bandgap of graphene limits its operation for logic devices.

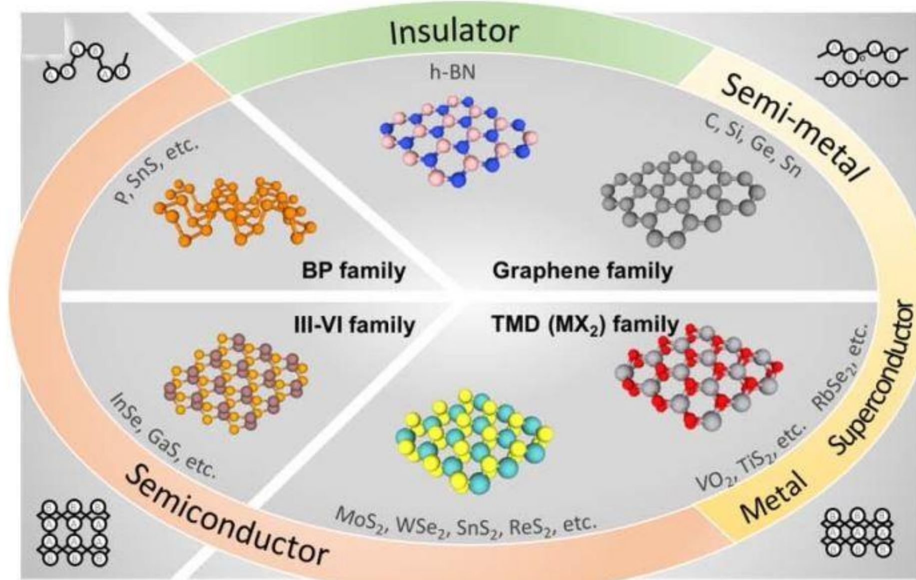


Figure 1: The 2D material family. Adopted with permission from the reference [18]©2018 *IEEE*

1.1.1 Transition Metal Dichalcogenides (TMDCs)

The wide range of tunable bandgap with the inherent noble properties of 2D materials TMDCs have garnered huge interests in the recent times. TMDCs consist of two types of atoms

M and X where M represents transition metals like Mo, W, Pt, Pd and X stands for chalcogens such as S, O, Se, Te etc. The M and X atoms are arranged in 2D honeycomb array where M atoms are stacked between X atoms to form X-M-X sandwiched layer, hence the general chemical formula of TMDCs is MX_2. The periodic table shown in the **Figure 2** demonstrates the possible combination of transition metal and chalcogen to form the TMDCs.

Figure 2: The highlighted transition metals and chalcogens in the periodic table predominantly crystallize to form the 2D layered structure. Adopted with permission from the reference [25]

The spatial confinement along the thickness direction during the bulk to monolayer scaling down causes indirect to direct bandgap transition of the TMDCs. **Figure 3a** shows the bandgap alignment for different TMDCs and compared with black phosphorus, III-V materials, and Si. The wide range of the tunability of the bandgap enables to design optimal strain free and atomically sharp heterostructures for electronic devices like diodes, transistors and tunneling devices.[26] For the multilayer TMDCs, different properties like bandgap, phonon vibration and magnetism can be altered by adopting different interlayer stacking strategy like 2H and 3R configurations [27]. The ultra-thin structure, absence of dangling bonds, tunable bandgap, strong spin-orbit coupling with other tunable electrical and material properties, TMDCs has become an exceptional choice in the research field of emerging technologies like sensors for internet of things (IoT) devices,

neuromorphic computing, biomimetic devices, optoelectronics, spintronics and energy harvesting devices. [28-37]

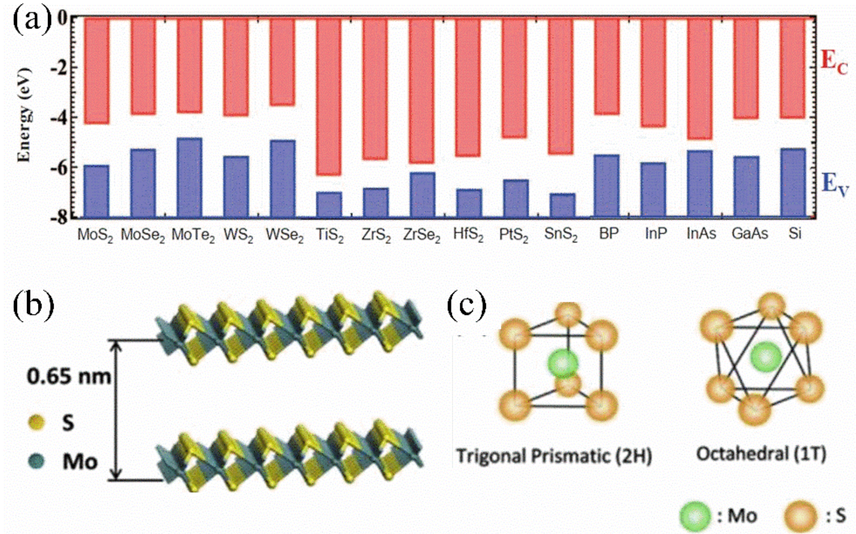


Figure 3: (a) Band alignment of monolayer 2D TMDCs compared with the Si and III-V materials. Adopted with permission from the reference [26] ©2015, *IEEE* (b) Chemical structure of 2 layer MoS2; thickness of monolayer MoS2 is 0.65 nm, (c) Polytypes of monolayer MoS_2; trigonal prismatic (2H) and Octahedral (1T). Adopted with permission from reference [38]

1.1.2 MoS_2 for post Si electronics

Among all the 2D materials, MoS_2 is considered as the most promising candidate for the post silicon electronics, mainly because of its indirect bandgap of ~1.2 eV to direct bandgap of ~1.8 eV transition, high ON-OFF current ratio of 10^8 at room temperature and carrier mobility of 200 cm^2/V.s. [39] These features are super critical for future transistor and other electronic devices Another fundamental reason for considering the MoS_2 as the future replacement of the Si is the abundance and innoxious nature of its constituent elements. Like other TMDCs, in MoS_2, transition metal Molybdenum (Mo) sandwiched between the chalcogen Sulfur (S) to form the single layer of 0.65 nm thickness as shown in **Figure 3b**. The atoms are bonded by strong covalent bond within the layer and weak vdW exists between the layers.[38] **Figure 3c** demonstrates the

monolayer with trigonal prismatic poly type crystal (2H) configuration which depicts semiconducting nature. The octahedra crystal symmetry (1T) shows the metallic behavior.[40] The high Young's modulus of ~0.33 ± 0.07 TPa makes MoS_2 an exceptional choice for flexible and wearable electronics.

1.2 Motivation

In electronics, the primary reason for the success of silicon among all the semiconductors lies in the superior quality of the interface between silicon and silicon dioxide. Typical production quality SiO_2 gate dielectrics have a mid-gap interface trap density of only ~10^{10} states/cm^2-eV. At a silicon/high-κ dielectric interface, the trap densities range from 10^{11}–10^{12} states/cm^2-eV.[41] The clear goal of any potential semiconductor system is to possess an interface as close to that of Si/SiO_2, since a high-quality interface is critical for all imaginable electronic and optoelectronic devices. Two-dimensional materials, by virtue of their layered structure, do not have out-of-plane bonds.[42] Thus, they have been predicted to bear pristine interfaces and surfaces, backed by experimental support. For the efficient and successful implementation of MoS_2 as channel material for transistors it is very critical to investigate the interface quality of MoS_2 with different gate dielectric material. Hence, this dissertation is aiming to study the interface quality of 2D MoS_2 with different high-κ gate dielectric to predict the viability of the MoS_2 material system for future electronic devices.

The phenomenal evolution of information and communication has driven us to envision the future technologies that demand faster, highly parallel, low power, and self-learning information processing system like human brain. The limitation of the current state of the art like

von Neumann architectures to meet these criteria has paved the way for artificial neural network (ANN). Specially, for solving the probabilistic and unstructured complex computation tasks like face and speech recognition, medical diagnostics, autonomous driving and high-speed data analysis; ANN showed superiority over the digital computer.[43-46]. Spiking neural network (SNN), an advanced technology of ANN is expected to minimize the gap between the machine learning and the neuroscience by emulating the cognitive process of human brain more efficiently. Artificial neuron and artificial synapse are the building blocks of SNN. Revival of memristor devices has opened the opportunity of realizing artificial neuron and synapse with single memristor device. Demonstration of artificial neuron and artificial synapses based on two dimensional (2D) TMDC single memristor device enables the realization of highly scalable, stackable, energy efficient, flexible, wearable and reliable neuromorphic hardware. Moreover, the implementation of both artificial neuron and synapse with the same material system would not make the process limited to the thermal budget and substrate incompatibility due to heterogeneous integration. Therefore, the dissertation also aims to the development and monolithic integration of the MoS_2 based neuromorphic computing devices for future computing technology.

1.3 Objectives

The main objectives of this dissertation are as follows:

1. To fabricate the MoS_2 based FET for different high-κ gate dielectric.
2. To study the MoS_2/high-κ interface quality by adopting the subthreshold swing and conductance method of interface trap density (D_{it}) extraction.

3. To develop a MoS_2 based reliable threshold switching memristor (TSM) device with the low threshold voltage, high ON-OFF ratio, sharp switching, and high endurance.
4. To study the switching mechanism of the TSM device.
5. To develop the artificial leaky integrate-and-fire (LIF) neuron circuit and implement the MoS_2 based TSM device for the LIF neuron circuit.
6. To study the different feature and performance of the developed LIF neuron
7. To do the monolithic integration of the MoS_2 based artificial neuron and synapse device for realizing single layer perceptron and different Boolean logic gates.
8. To implement the MoS_2 based TSM for realizing a robust artificial nociceptor which can efficiently emulates the key features of the biological nociceptor.

1.4 Dissertation Overview

Chapter 2 gives an overview of the different interface trap density (D_{it}) extraction techniques. The mathematical models, advantages, and disadvantages for different *Dit* extraction techniques are discussed in this chapter. This chapter also gives a brief introduction about the High-κ materials and the nucleation layer. The sources of interface traps for MoS_2/High-κ are also discussed in this chapter. The chapter explores the relevant literatures on the D_{it} of the MoS_2/dielectric interface.

Chapter 3 presents the experimental methodology and results for the D_{it} extraction of the different MoS_2/High-κ interface. The MoS_2 FET fabrication steps and electrical characterization techniques are discussed in detail in this chapter. In the result and discussion section, the experimental transfer characteristics of the MoS_2 FET, capacitance-voltage, conductance-voltage,

and conductance-frequency curves shown and explained. The chapter includes the comparative study of the D_{it} values extracted from the different interface.

Chapter 4 covers the brief introduction about the neuromorphic computing system and spiking neural network (SNN). The necessity of realizing a single device artificial neuron is highlighted in this chapter. This chapter explores the different neuron models also. The chapter includes a literature survey on the 2D materials based artificial neuron.

Chapter 5 presents the fabrication steps for the MoS_2 based TSM device and its implementation as a LIF neuron. The chapter also reveals the switching mechanism of the TSM device. The chapter demonstrates the ability of the LIF neuron to emulates the key features of the biological neuron.

Chapter 6 explores the monolithic integration of the MoS_2 based artificial neuron and synapse devices. The chapter demonstrates the experimental results obtained from the monolithically integrated single layer perceptron. The chapter also presents the successful implementation of AND, OR and NOT logic gates with the single layer perceptron.

Chapter 7 demonstrates the successful implementation of the MOS_2 based TSM device as artificial nociceptor. The chapter delineates the ability of the artificial nociceptor to emulate the complex functionality of the biological nociceptor .

Chapter 8 draws the conclusion of the dissertation and discusses the future directions and challenges to realize neuromorphic computing hardware on complete 2D platform.

CHAPTER 2 INTERFACE TRAP DENSITY (D_{it}) EXTRACTION TECHNIQUES

2.1 Introduction

The performance of the semiconductor based electronic devices is greatly influenced by the presence of the interface trap states. Therefore, it is very crucial to precisely quantify the parameters like interface trap density, capture cross-sections, trap time constant for any potential material system prior to the implementation. The comprehensive knowledge about the trap states at any interface facilitates to design and develop high performance devices. Over the years, a good number of interface trap density extraction techniques have been proposed. In this chapter, we will define the interface trap states and explore the mathematical models, advantages, and disadvantages of the different D_{it} extraction techniques. The chapter also gives a brief introduction on the high-κ dielectrics and the possible sources of the interface traps for MoS_2/high- κ interface.

2.2 Interface Trap States

At the oxide-semiconductor interface, the abrupt termination of the periodic nature of the semiconductor initiates electronic energy states within the forbidden bandgap. These energy states are termed as the interface trap states. Interface trap states are very crucial for the device performance because charge can flow between the semiconductor and the interface trap states. The net charge in the interface trap states is dominated by the position of the Fermi level of the semiconductor. The interface trap is considered as acceptor while it is neutral but can accept electron to get negatively charged. At neutral condition it remains above the Fermi level but at negatively charged condition it stays below the Fermi level as shown in the **Figure 4a**. On the

contrary, the donor type interface trap stays below the Fermi level at neutral condition and goes above the Fermi level while it becomes positively charged by donating the electron.[47] Hence for the metal oxide semiconductor FET (MOSFET) or MOS capacitor (MOS-C), the charge in the interface trap states is dependent on the applied gate voltage. The presence of interface traps adversely affects the MOSFET by shifting the threshold voltage, lowering the subthreshold swing, reducing the channel mobility and conductivity.

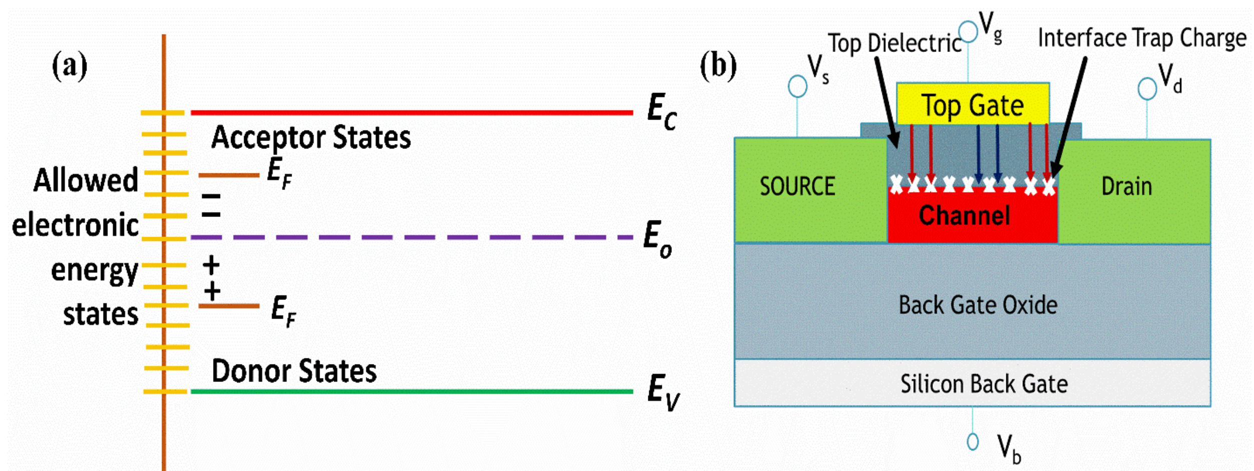


Figure 4: (a)The position of the interface trap states in the bandgap of the semiconductor. (b) physical location of the interface trap states in the MOSFET device.

2.3 Interface Trap Density (D_{it}) Extraction Techniques

2.3.1 Low Frequency (Quasi-static) Methods

Low frequency method also known as Quasi-static method is the most common technique of interface trap density (D_{it}) measurement. The method only can quantify the D_{it} but does not provide any information regarding their capture cross-sections.[47] During the low frequency *C-V* measurements, the interface traps respond to the lower probe frequency. In this condition, the *C-V* curve gets distorted as interface traps capacitance C_{it} adds up with the oxide capacitance. At

higher frequency, interface traps cannot follow the probe frequency and do not contribute to the overall capacitance. Hence, the *C-V* curves come out like an ideal *C-V* curve. This feature is utilized in the low frequency method. The low frequency *C-V* curve is compared with the high frequency *C-V* curve to extract the D_{it}. The low frequency capacitance (C_{lf}) is given by

$$C_{lf} = \left(\frac{1}{C_{0x}} + \frac{1}{C_S + C_{it}}\right)^{-1} \quad (1)$$

Here C_{ox} is the oxide capacitance, C_s denotes semiconductor capacitance. The D_{it} can be extracted using following equations

$$D_{it} = \frac{C_{it}}{q^2} \quad (2)$$

$$D_{it} = \frac{1}{q^2}\left(\frac{C_{ox}C_{lf}}{C_{0x} - C_{lf}} - C_S\right) \quad (3)$$

The low-frequency method can extract interface density over the entire bandgap. The perfect estimation of the ideal *C-V* curve or high frequency *C-V* curve is always challenging for this measurement. This measurement is also found difficult for the very thin oxide layer due to the comparatively higher leakage current.[48]

2.3.2 Terman Method

Terman method is a high frequency capacitance method of D_{it} extraction. The method relies on the *C-V* measurement at a sufficiently high frequency where the interface traps are unresponsive to the probe frequency. [47] Though the interface traps do not respond to the high probe frequency, the net interface charges change with the slowly varying gate voltage. This variation of interface charge causes the stretching of the *C-V* curve along the gate voltage axis. For the calculation of the D_{it} with this method, first semiconductor work function (Φ_s) for a given high frequency

capacitance C_{hf} is determined from the ideal MOS-C *C-V* curve. Next, the V_G is extracted from the experimental *C-V* curve for the same C*hf*. This step is repeated to obtain a satisfactory Φ_s vs VG curve. The D_{it} can be extracted from this curve using following equation.

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{dV_G}{d\Phi_s} - 1\right) - \frac{C_s}{q^2} = \frac{C_{ox}}{q^2}\frac{\Delta V_G}{d\Phi_s} \tag{4}$$

Where ΔV_G=V_G-V_G (ideal), the gate voltage shift from the ideal condition. This method is applicable for the D_{it} equal or above10^{10} $cm^{-2}eV^{-1}$. The method is not well-accepted due to the inaccurate capacitance measurement. Moreover, with the thinner oxide or increasing capacitance the voltage shift become insignificant and the D_{it} extraction become difficult.[47]

2.3.3 Subthreshold Swing Method

Subthreshold swing (SS) method is one of the simplest and direct methods of D_{it} extraction. The D_{it} can be calculated analytically using the experimentally extracted SS from I_D-V_G graph of the MOSFET. [49, 50] The following analytical expression is used to extract D_{it},

$$SS = \frac{2.3KT}{q}\left(1 + \frac{C_{it}}{C_{tg}} + \frac{C_S}{C_{tg}} - \frac{\frac{C_S^2}{C_{tg}C_{sio_2}}}{1+\frac{C_{it}}{C_{SiO_2}}+\frac{C_S}{C_{SiO_2}}}\right) \tag{5}$$

Here, C_{tg} is the capacitance of the top gate dielectric, given by $C_{tg} = \epsilon_{tg}/t_{tg}$, where $\epsilon_{tg}$is the dielectric constant and t_{tg} is the thickness of the top gate dielectric. This method is mostly dependent on the theoretical estimation of the capacitance value, which make it difficult to accurate estimation of the interface traps. Moreover, this method does not give the information about the capture cross section and the defect location. Despite of these limitations, SS method is frequently adopted to get a rough estimation of the interface traps for the MOSFET devices.

2.3.4 Conductance Method

The conductance method developed by Nicollian and Goetzberger is considered as one of the most complete and sensitive methods of D_{it} extraction.[47, 48, 51] Also, the capture cross sections of the traps and the interface trap time constant τ_{it} can be extracted using this method.[47] For a conventional metal oxide semiconductor FET (MOSFET), this method yields D_{it} in both depletion and weak inversion regions. The technique utilizes the equivalent parallel conductance G_P *vs* gate voltage (V_G) *and* Gp *vs* frequency (f) measurement of a MOS-C or MOSFET for the accurate estimation of the interface trap density. The conductance incorporates the loss mechanism due to the interface trap capture and emission of carriers and thus infer the interface trap density. **Figure 5** shows the equivalent circuit model of a MOS-C for the explanation of the conductance method. The basic circuit model at **Figure 5a** includes the C_{ox}, C_S and C_{it}. The loss due to capture-emission of carriers is represented by the R_{it} in the circuit. The circuit is further simplified at **Figure 5b** by replacing circuit element with parallel capacitance C_P and parallel conductance G_P. The C_P and G_P are defined as following

$$C_p = C_S + \frac{C_{it}}{1+\left(\omega_{\tau_{it}}\right)^2} \tag{6}$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+\left(\omega_{\tau_{it}}\right)^2} \tag{7}$$

Here $C_{it}=q^2D_{it}$, $\omega=2\pi f$ (f=*measurement* frequency), the interface trap time constant $\tau_{it}=R_{it}C_{it}$. It is clear from the Equation 6 and 7 that, the conductance method is simplified compare to the traditional capacitance method because it does not require C_S for the D_{it} interpretation. Equation 6 and 7 consider the interface traps with a single energy level within the bandgap. Practically, the interface traps are continuously distributed in energy over the entire bandgap of

the semiconductor. The interface traps located within the few $\pm\frac{KT}{q}$ of the Fermi level are primarily contributes to the capture and emission of the carriers and causes the time constant dispersion. To incorporates this phenomenon the following normalized conductance is considered for the model.

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega_{it}} \quad (8)$$

Experimentally, the conductance G_P measured as a function of frequency and GP/ω is plotted against ω. The peak position of G_P/ω at $\omega = 1/\tau_{it}$ is determined which gives the maximum $D_{it}=2G_P/q\omega$. Experimentally obtained G_P/ω vs ω curve is generally broader compared to the predicted curve considering Equation 8. The anomaly is attributed to the surface potential fluctuations originates from the oxide charge, interface traps non-uniformity and doping density. The equation for D_{it} is rectified as following equation considering the effect of surface potential fluctuations.

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_p}{\omega_{max}}\right) \quad (9)$$

The capacitance measuring unit (CMU) generally considers the parallel C_m-G_m combination of the device under test (DUT) as shown in the **Figure 5c**. The following equation is used to calculate the G_P/ω from the measured parallel capacitance and conductance.

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2+\omega^2(C_{ox}-C_m)^2} \quad (10)$$

The equation neglects the series resistance of the device, but **Figure 5d** is the modified circuit which incorporates the series resistance r_s and the tunneling conductance G_t. The following equation gives the G_p/ω value considering the effect of series resistance.

$$\frac{G_p}{\omega} = \frac{\omega (G_c-G_t) C_{ox}^2}{G_c^2+\omega^2(C_{ox}-C_c)^2} \quad (11)$$

Where G_c and C_c is the corrected conductance and capacitance respectively for the series resistance. Equations are developed to measure G_c and C_c from the measured conductance and capacitance.

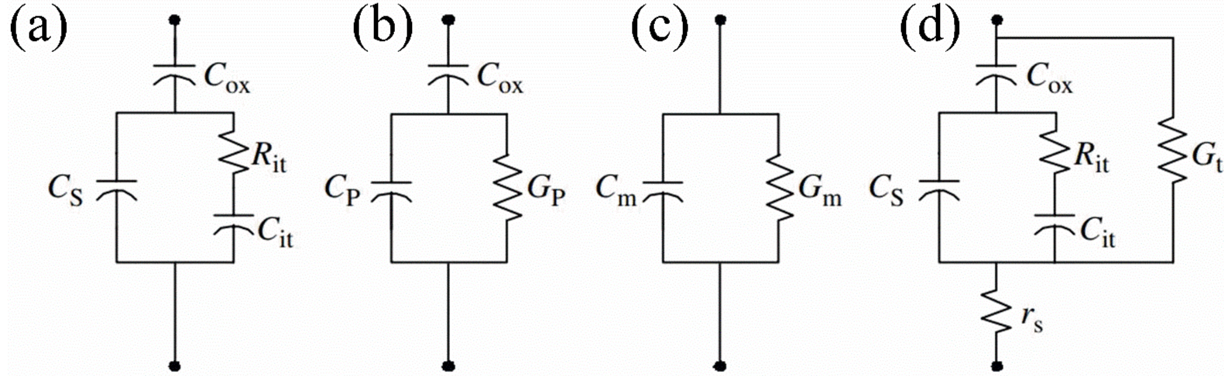


Figure 5: Equivalent circuits for conductance method (a) MOS-C with interface trap time constant $R_{it}C_{it}$. (b) simplified circuit of (a), (c) measured circuit (d) considering series resistance and tunneling conductance G_t, adopted with permission from the reference [47]

For this measurement the frequency should be precisely determined, and it is suggested to conduct the measurement for the wide range of frequency. The ac signal amplitude should be kept in the range of 50 mV to avoid the spurious conductance arise from the signal harmonics. [47]

The conductance method is recognized as complete method because it yields D_{it}, capture cross section for the majority carriers, and surface potential fluctuations in the depletion to weak inversion region of the bandgap. The method is viable for the high gate leakage current unlike the capacitance method and can measure D_{it} even lower than10^9 $cm^{-2}eV^{-1}$. Capacitance based D_{it} extraction techniques demand the accurate measurement of oxide capacitance, semiconductor capacitance and the interface trap capacitance which increases the complexity and results erroneous estimation. On the other hand, for the conductance method, the measured conductance is directly convertible to the response of interface traps as a function of gate voltage and frequency.[52] In this method all the mathematical calculations are based on the experimentally

obtained value, no assumptions are made for the quantification. Moreover, this method is readily applicable to the MOSFET structure which reduce the complexity of fabricating separate MOS-C devices.

2.4 MoS_2/High κ Interface

2.4.1 High-κ Gate Dielectric

The dielectric insulator is one of the main components of the electronic logic devices. The enhancement of the metal-semiconductor capacitive coupling and suppressing the leakage current is the main function of the dielectric insulator in the electronic devices. In the past decades, SiO_2 was the only choice as dielectric insulator for the microelectronic devices mainly due its defect free uniform growth. With the scaling down process, the SiO_2 was also thinned down proportionally. The industry faced the major challenge while SiO_2 needed to scale down below 1 nm. At this thickness, the leakage current due to the quantum tunneling became inevitable and also the uniform growth of SiO_2 all over 12-inch wafer also became challenging. At this scenario, scientists gave a breakthrough by replacing SiO_2 by the high-κ dielectric materials.

The high-κ materials are defined as the dielectric materials with the higher dielectric constant (κ) compare to the SiO_2. HfO_2, Al_2O_3, ZrO_2, $ZrSiO_4$, $HfSiO_4$ are some of the common high-κ dielectric materials.

The capacitance of the parallel plate capacitor is given by

$$C = \frac{\kappa \varepsilon_{0A}}{t} \quad (12)$$

Where, κ represents dielectric constant, ε_0 is the permittivity of the free space, *A* denotes the capacitor area and *t* represent the thickness of the capacitor insulator. Equation 12 clearly

indicates that, the dielectric materials with higher κ value offers larger capacitance for the same thickness of the material with lower κ. Therefore, high dielectric constant of the high-κ dielectric material allows to use a gate with higher physical thickness while achieving the same capacitance obtained for much thinner SiO_2. The equivalent oxide thickness (EOT) is the required thickness of the SiO_2 to achieve the same capacitance value for the high κ dielectric. EOT is defined by the following equation

$$EOT = t_{high-\kappa}\left(\frac{\kappa_{SiO_2}}{k_{high-\kappa}}\right) \tag{13}$$

Here, $t_{high\text{-}\kappa}$ is the thickness of the high-κ dielectric material. So, the high κ dielectric facilitates the implementation of the thicker gate dielectric to reduce the leakage current while maintaining the required capacitance for the efficient device performance.

2.4.2 Sources of interface traps at MoS_2/high κ interface

2.4.2.1 Defects in MoS_2

Though it is expected to have very low interface trap density for MoS_2 and other 2D materials because of absence of the out of plane dangling bonds, the experimental studies showed significant trap density at MoS_2/oxide interface. The intrinsic defects in the geological MoS_2 are the main reason for the performance degradation of the MoS_2 based devices. The variation in the stoichiometry within the same layer as sulfur rich and sulfur deficient region, presence of impurities, structural defects etc. play key role for the high interface trap density at MoS_2/oxide interface. The polycrystalline MoS_2 layer obtained by CVD, thermal evaporation, hydrothermal

synthesis, electrochemical lithiation etc. process generally contains more defect compare to the exfoliated MOS_2.

2.4.2.2 Nucleation layer

The atomic layer deposition (ALD) of the high κ gate dielectric requires initial precursor at the growth surface to initiate the self-limiting chemical reaction. The chemically inert basal plane of MoS_2 does not provide that precursor, hence for the thin layer growth of the high κ gate dielectric, the growth takes place only at the defect site or. only the physical adsorption happens. To obtain the high quality growth of the high κ gate dielectric, the functionalization of the surface of the 2D material or deposition of additional buffer layer is required.[53] The functionalization process includes O_2 plasma or Ozone treatment. Both processes improve the ALD nucleation but the O_2 plasma treatment causes an interfacial layer of MoO_3 while Ozone treatment requires thicker deposition of dielectric material for leakage free gate. Another approach is to initiate a buffer layer in between the 2D material and the high κ gate dielectric. Titanyl phthalocyanine and metal oxides are generally used as the buffer layer. Thermal or E-beam evaporation of very thin layer of the buffer layer offer favorable surface for the uniform growth for the high κ gate dielectric. At the same time this buffer or nucleation layer initiate trap states and carrier scattering effects. Hence, the nucleation layer is another major source of the interface traps of Oxide-MoS_2 interface.

2.5 Literature on MOS_2 Interface Trap Density

Different D_{it} extraction techniques are adopted to quantify the interface traps for MOS_2 based FET with different gate dielectrics. Since surface roughness scattering at high electric fields

is absent in an all-two-dimensional MoS_2 transistor with h-BN top gate, it can be argued that there are few interface traps due to the absence of dangling bonds.[54] However, contrary to these speculations, a trap density between mid-10^{11} and 10^{14} states/cm^2-eV was reported for monolayer MoS_2 grown by chemical vapor deposition, with a top gate of AlO_x (2 nm)/HfO_2 (30 nm).[55] Exfoliated monolayer and tri-layer MoS_2 on a local bottom gate with h-BN as the dielectric exhibits an interface trap density (D_{it}) of ~10^{12} states/cm^2-eV.[56] A peak D_{it} of 10^{13} states/cm^2-eV was reported at 0.35–0.4 eV from midgap in MoS_2 regardless of the gate dielectrics.[57] A constant D_{it} of 10^{12} states/cm^2-eV at a MoS_2/dielectric interface is revealed using the Terman method, when sulfur vacancies are absent in MoS_2.[57] Due to the absence of dangling bonds in 2D materials, it is difficult to deposit high quality dielectrics on them using atomic layer deposition (ALD). By functionalizing the surface of MoS_2 using UV-ozone, researchers have been able to deposit high quality HfO_2 by ALD on MoS_2.[58] However, the interface trap density between few-layer MoS_2 channel and 8-13 nm HfO_2 thus deposited is 10^{12}–10^{13} states/cm^2-eV.[59] Other researchers advocate the use of a nucleation layer for facilitating the ALD of dielectrics.[60-62] The introduction of a nucleation layer by physical vapor deposition or by functionalization of the 2D surface increases the interface traps. There are very few conclusive reports on trap density lower than 10^{11} states/cm^2-eV at a 2D semiconductor/gate dielectric interface. D_{it} extracted for MoS_2-based field effect transistors (FETs) with various dielectrics are tabulated in Table 1.

Table 1: D_{it} values for MoS_2-based devices reported in literature

Device Structure	Thickness	Type of MoS_2	Method of Dit Extraction	Dit Value (cm^2/eV)
MoS_2/ HfO_2[59]	7 layer MoS_2 13 nm HfO_2 4 layer MoS_2 8 nm HfO_2	CVD grown	High low frequency method and multi-frequency	1.2×10^{13} $2\times10^{11} - 2 \times 10^{13}$
MoS_2/ HfTiO[63]	50 layers (32.5 nm) MoS_2 39.65nm HfTiO	Transferred by scotch tape	From SS	5.58×10^{12}
MoS_2/ Al_2O_3[64]	1 layer (0.85 nm) MoS_2 1nm Al_2O_3 seeding layer 15 nm Al_2O_3 dielectric	CVD		1.6×10^{13}
MoS_2/h-BN[65]	Single or bilayer MoS_2	Exfoliated by scotch tape	observed noise magnitude	6×10^{10} -1×10^{12}
MoS_2/h-BN[66]	Trilayer MoS_2	Exfoliated	High low frequency method and multi-frequency	~10^{12}
MoS_2/ZrO_2[67]	Few layers MoS_2 5.8nm ZrO_2	Transferred	From SS	1.7×10^{12}
MoS_2/ HfO_2[68]	Monolayer to trilayer (0.7nm to 2.1nm) MoS_2 10nm HfO_2	Exfoliated	From SS	5×10^{12}
MoS_2/ Al2O_3[69]	30nm MoS_2 50nm Al_2O_3	Exfoliated	From SS	2.6×10^{11}
MoS_2/SiN_x[70]	140 layers MoS_2 250nm SiN_x	Exfoliated	From SS	1.14×10^{13}
MoS_2/SiO_x/SiN_x[70]	125 layers MoS_2 50nm SiO_x 200nm SiN_x	Exfoliated	From SS	2.13×10^{12}
MoS_2/thermal SiO_2[70]	154 layers MoS_2 100 nm SiO_2	Exfoliated	From SS	3.32×10^{12}
MoS_2/Al_2O_3[71]	7 – 8 nm MoS_2 10 nm Al_2O_3	Exfoliated	Terman	1×10^{12}
MoS_2/HfO_2[71]	7 – 8 nm MoS_2 10 nm HfO_2	Exfoliated	Terman	2×10^{12}
MoS_2/HfO_2[55]	Monolayer MoS_2 30 nm HfO_2	CVD	Conduction	3.3×10^{14}
MoS_2/HfO_2[72]	Monolayer MoS_2 5 nm HfO_2	CVD	High-low frequency method	7.03×10^{11}
MoS_2/Al_2O_3[73]	11.3 nm MoS_2 30 nm Al_2O_3	Exfoliated	Low Frequency Noise characterization using CNF Model	1.8×10^{12}
MoS_2/Al_2O_3[74]	15nm MoS_2 16nm Al_2O_3		Exfoliated	2.4×10^{12}

2.6 Conclusion

The exploration for the high quality MoS_2/high κ gate dielectric interface is crucial prior to its implementation for the next generation electronics. Owing to the importance of nucleation layer for the uniform growth of the high κ gate dielectric, it is also vital to find out the best combination of the nucleation layer and the gate dielectric. Conduction method of D_{it} extraction is considered as the most accurate and comprehensive method for the D_{it} extraction. Hence, in this work, the conductance method is adopted to determine the best possible interface of MoS_2 among the different combinations of the nucleation layer-high κ gate dielectric layers.

CHAPTER 3 MoS_2/HIGH-κ DIELECTRIC INTERFACE EXTRACTION

The contents of this chapter have been published in: Dev, D., Krishnaprasad, A., Kalita, H., Das, S., Rodriguez, V., Calderon Flores, J., Zhai, L. and Roy, T., 2018. High quality gate dielectric/MoS_2 interfaces probed by the conductance method. Applied Physics Letters, 112(23), p.232101.

3.1 Introduction

In this chapter, we are going to investigate the interface quality of the MoS_2/high κ interfaces by developing MoS_2 based field effect transistors (FET) having high-κ top gate dielectrics (Al_2O_3 and ZrO_2). Two different nucleation layers SiO_x and AlO_x are used for this study. Primarily, the D_{it} is calculated using simple SS method based on I_D-V_G measurement. Next, the most sensitive method named conductance method is adopted for the precise extraction of the D_{it} and its location in the bandgap. The extracted results are compared to determine the best possible MoS_2/nucleation layer/high κ gate dielectric interface for the advanced electronic devices.

3.2 Device Fabrication and Characterization Techniques

3.2.1 MoS_2 FET Device Fabrication

Figure 6a and **6b** shows the device schematic and optical image respectively of a top-gated MoS_2 transistor. The first step of the fabrication is the mechanical exfoliation of the MoS_2. In this step, Scotch-tape method is used to cleave the few layers of the MoS_2 from the bulk MoS_2 source

and then transferred on the patterned p+ Si substrate with 260 nm of thermally grown SiO_2. The thickness of the exfoliated MoS_2 flakes can be confirmed from the optical contrast of the micrograph. For this work, four-layer MoS_2 flakes are used as the channel material of the FET devices. The precise locations of the flakes on the patterned substrate are determined and NPGS DesginCAD layout editor is used to design the mask according to the location of the flakes. NPGS e-beam lithography system integrated with Zeiss ULTRA-55 FEG SEM is used for the patterning the source/drain contact. E-beam evaporator is used to deposit 60 nm of Ni. Finally, the lift-off process results the patterned source/drain contact. To obtain different combination of nucleation layer and top gate dielectric, four different kinds of devices are fabricated.as shown in the **Figure 6c**.

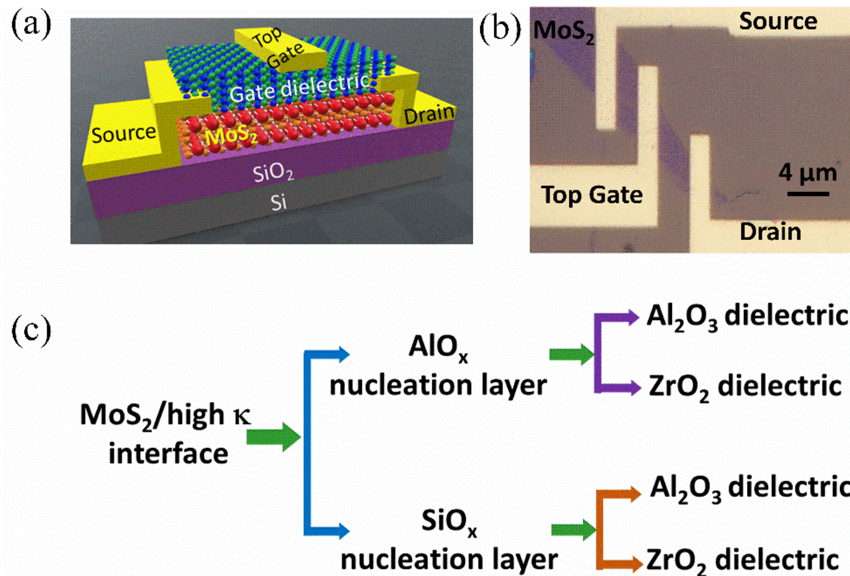


Figure 6: (a) Device schematic – the channel is underlapped by the gate. (b) Optical microscope image; scale bar: 4 µm.(c) The MoS_2/High κ interface combinations for two different (AlO_x and SiO_x) nucleation layers with two different high κ gate dielectrics (Al_2O_3 and ZrO_2).

The nucleation layers used are AlO_x and SiO_x. For AlO_x nucleation layer, 1.5 nm of Al was e-beam operated and kept in ambient condition to transform Al to AlO_x. The SiO_x seed layer was obtained by directly depositing 1.5 nm of SiO_x using E-beam evaporator. The top gate

dielectric consisting of 9.5 nm of Al_2O_3 was deposited by atomic layer deposition (ALD) at 250 ^{0}C using Trimethylaluminium (TMA) and H_2O precursors. ZrO_2 top gate dielectric was also deposited by ALD at 150 ^{0}C, while the precursor tetrakis(ethylmethylamino)zirconium (TEMAZ) and H2O was kept at 110 ^{0}C. The top gate contact was patterned using e-beam lithography, and 60 nm Ni was deposited and lifted off to form the electrode. The top gate contact was designed such that there are underlapped regions near the source and drain, as shown in **Figure 6b**. The devices were annealed in forming gas (120 ^{o}C for 0.5 h on Al_2O_3 device). A lower annealing temperature and duration was chosen for the devices since they showed increased gate leakage for higher annealing temperatures and durations.

3.2.2 Electrical Characterization

Electrical measurements are performed on the devices. The transfer characteristics are measured, followed by capacitance vs. voltage and capacitance *vs.* frequency measurements, using a Keysight B1500A Semiconductor Device Analyzer and Room temperature (RT) probe-station.

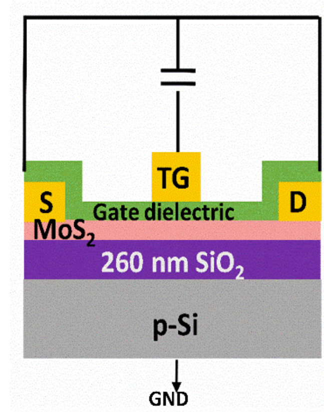


Figure 7: Circuit diagram for capacitance and conductance measurement

During the measurements, we shorted the source and drain and connected them to one terminal of the capacitance measurement unit. We modified the bias on the other terminal of the capacitance measurement unit that was connected to the top gate electrode as shown in **Figure 7**. The back gate (V_{BG}) was grounded at 0 V, since in our depletion mode MoS_2 FET, the channel is quite populated with electrons at V_{BG} = 0 V, keeping the underlapped channel regions conductive.

3.3 Results & Discussions

3.3.1 Transfer Characteristics of MoS_2 FET

Figure 8 shows the transfer characteristics of MoS_2 based FET for different high-κ dielectric material as top gate dielectric. **Figure 8a** depicts the I_D-V_G curve of MOS_2 FET for AlO_x nucleation layer**.** The subthreshold swing (*SS*) of the device with ZrO_2 gate dielectric is 120 mV/decade (**Figure 8a(i)**), while it is 180 mV/decade for Al_2O_3 gate (**Figure 8a(ii)**). I_D-V_G curve for MOS_2 FET with SiO_x nucleation layer shown in **Figure 8b** indicates the better *SS* compare to the AlO_x nucleation layer. With SiO_x nucleation layer, *SS* of 110 mV/decade (**Figure 8b(i)**) and 95 mV/decade (**Figure 8b(i)**) obtained for ZrO_2 and Al_2O_3 gate dielectric respectively.

3.3.2 Subthreshold Swing Method for D_{it} Extraction

The D_{it} at the interface of MoS_2 channel and different high-κ gate dielectric can be calculated analytically using the Equation 5. *SS* values obtained from the transfer characteristics are used to calculate the $D_{it.}$ For the calculation, $C_{SiO_2} = \epsilon_{SiO_2}/t_{SiO_2}$=0.013 μF/cm^2, given ϵ_{SiO_2}= 3.9, and 260 nm thickness of SiO_2, $C_S = C_{MoS_2} = \epsilon_{MoS_2}/t_{MoS_2}$= 1.26 μF/cm^2, using $\epsilon_{MoS_2} = 4$,[16]

and 2.8 nm thickness of 4-layer MoS_2 flake are considered. With the AlO_x nucleation layer, for ZrO_2, C_{tg} = 1.56 μF/cm^2, considering the gate dielectric stack thickness t_{zrO_2} = 9.5 nm and a nucleation layer t_{AlO_x} = 1.5 nm, with ϵ_{ZrO_2} = 25 and assuming $\epsilon_{Al_2O_3}$ = 5 (experimental), For AlO_x/Al_2O_3 combination, C_{tg} = 0.402 μF/cm^2, considering the gate dielectric stack thickness $t_{Al_2O_3}$ = 9.5 nm With the SiO_x nucleation layer, for ZrO_2, C_{tg} = 1.15 μF/cm^2 considering a nucleation layer t_{SiO_x} = 1.5 nm, with assuming ϵ_{SiO_x} =3.9 The SiO_x/Al_2O_3 combination results C_{tg} = 0.387 μF/cm^2.

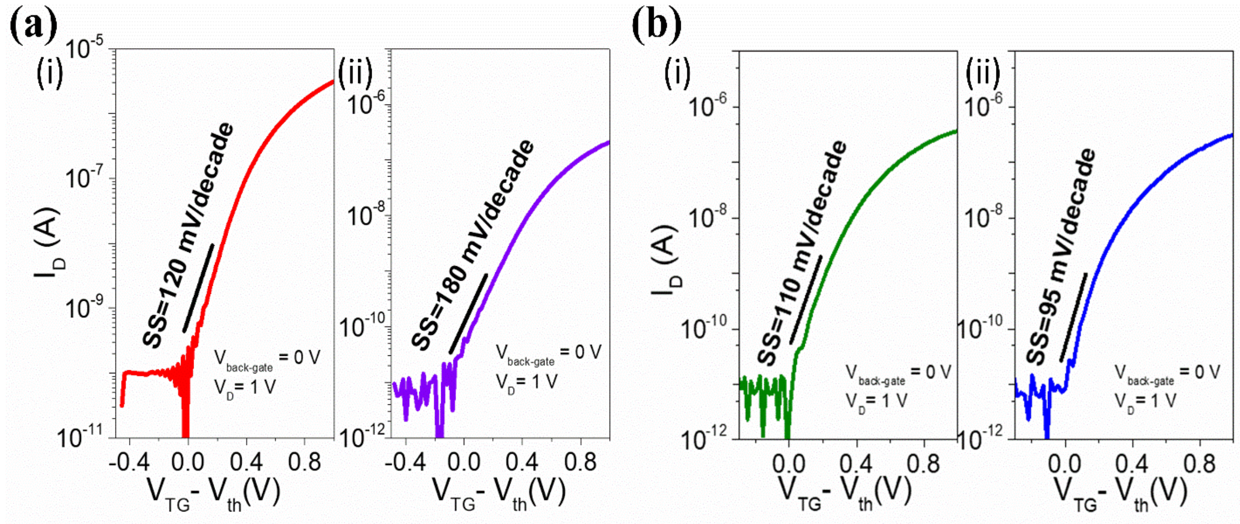


Figure 8: Transfer characteristics of the MoS_2 based FET (a) AlO_x nucleation layer i) ZrO_2 gated MoS_2 FET i) Al_2O_3 gated MoS_2 FET (b) SiO_x nucleation layer i) ZrO_2 gated MoS_2 FET i) Al_2O_3 gated MoS2 FET

Obtained SS value and calculated capacitance are utilized to extract the D_{it} for different combinations of nucleation layer and gate dielectric, the resultant D_{it} values are tabulated in the Table 2. The interface trap density obtained for MoS_2/Al_2O_3 interface is impressive and can be compared with the highest reported quality of Si/high-κ dielectric interfaces. [75-77]

Table 2: Interface trap density (D_{it}) of MoS_2 FET for different high gate dielectric extracted using subthreshold swing (*SS*) method.

Nucleation Layer	Top Gate Dielectric	D_{it} (states/cm^2-ev)
AlO_x	ZrO_2	5.2×10^{12}
	Al_2O_3	3.0×10^{12}
SiO_x	ZrO_2	3.7×10^{12}
	Al_2O_3	6.0×10^{11}

3.3.3 Capacitance and Conductance Measurement

The conductance method demands the capacitance and conductance measurement of the FET device. All the capacitance and resistance sources contribute to the measured capacitance and conductance are shown in the equivalent circuit model at **Figure 9**.

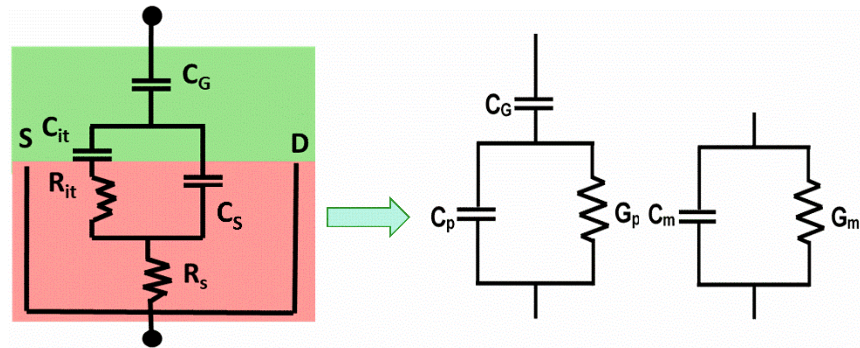


Figure 9: Equivalent circuit model for MoS_2 FET on Si/SiO_2 substrate with top gate.

Figure 10 shows the capacitance-voltage characteristics as a function of frequency for MoS_2 for the different gate dielectrics. **Figure 10a** shows *C-V* curves of the MoS_2 FET with the ZrO_2 gate dielectric and AlO_x nucleation layer. The *C-V* curve contains significant frequency dispersion at the depletion region. Similar trend is observed for the Al_2O_3 gate dielectric with AlO_x nucleation layer as shown in **Figure 10b**. The dispersion in the depletion region is a clear signature of the presence of interface traps. The different response of the traps at the different frequency

causes the dispersion in the depletion region of the *C-V* curve.[51, 78] On the other hand**,** with SiO_x nucleation layer devices show little hump for ZrO_2 top gate dielectric and no dispersion for Al_2O_3 gate dielectric. The presence of little hump in the **Figure 10c** for ZrO_2 gate dielectric is also indicative of trap states. [78] In the **Figure. 10d**, the *C-V* curves do not show any significant frequency dependence in the depletion region from 1 kHz to 500 kHz, indicating the presence of few interface traps. Similar observations of dispersion-less *C-V* characteristics were made by Chen et al., in an MoS_2 metal-insulator-semiconductor capacitor with h-BN bottom gate.[56] The high capacitance in the accumulation region is attributed to parasitic capacitances due to the ungated regions adjacent to the source and drain. The frequency dispersion in the accumulation region for all the devices is attributed to border traps.[72, 79]

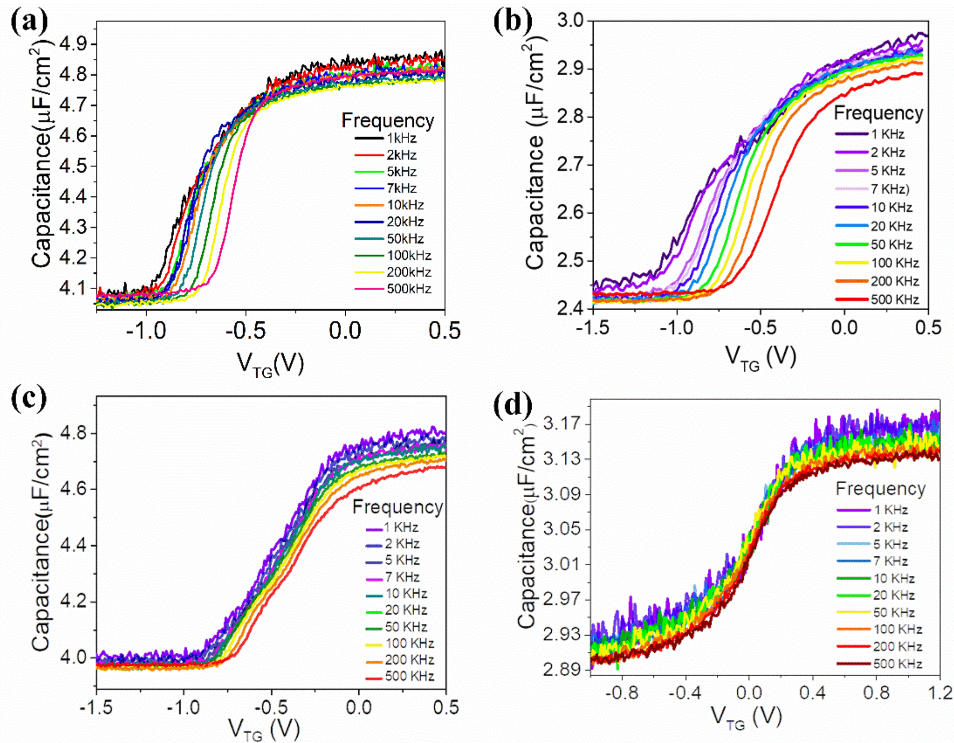


Figure 10: Frequency dependence of capacitance-voltage curve of the MoS_2 FET with (a) AlO_x/ZrO_2 gate dielectric (b) AlO_x/Al_2O_3 gate dielectric (c) SiO_x/ZrO_2 gate dielectric (d) SiO_x/Al_2O_3 gate dielectric.

Figure 11 delineates the parallel conductance *vs.* top gate voltages of the MoS_2 FET for different gate dielectrics. Parallel conductance curve with the sharp peak is another indication of the interface traps. [80, 81]The parallel conductance curves shown in the **Figure 11a** and **11b** for AlO_x/ZrO_2 and AlO_x/Al_2O_3 gate dielectric respectively have prominent peaks and support our results obtained from the SS method and findings from the capacitance-voltage measurement. The absence of sharp peaks for both gate dielectric material with SiO_x nucleation layer (**Figure 11c and 11d**) denote the better-quality interface for the SiO_x nucleation layer compare to the AlO_x nucleation layer.

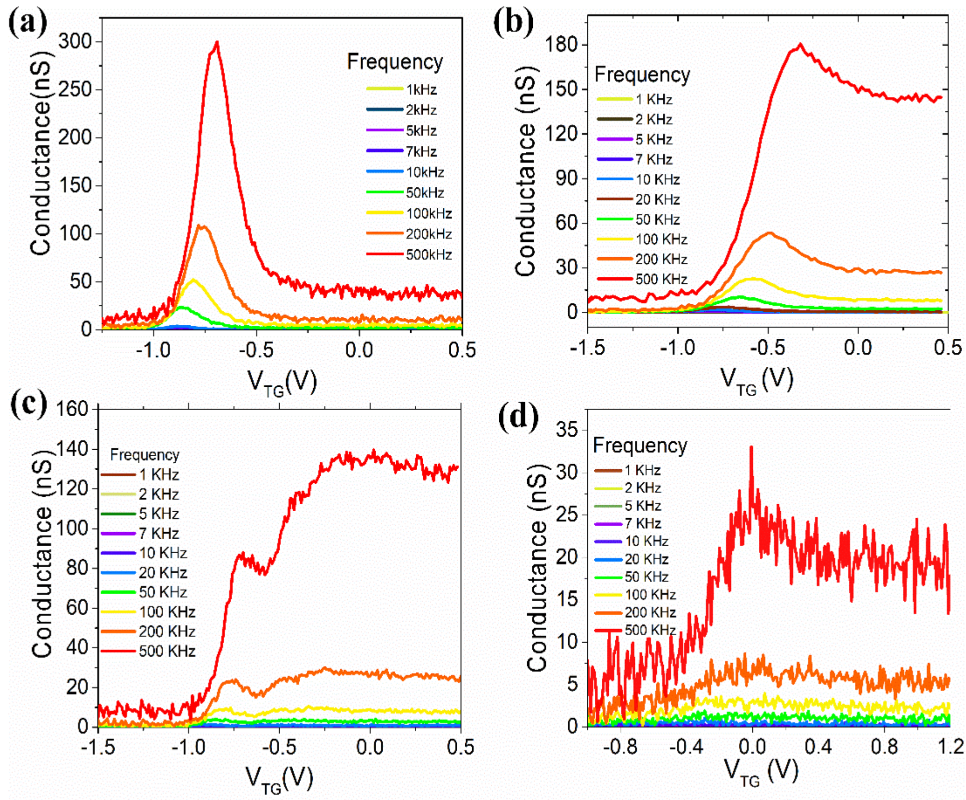


Figure 11: Conductance-voltage curve of the MoS_2 FET with (a) AlO_x/ZrO_2 gate dielectric (b) AlO_x/Al_2O_3 gate dielectric (c) SiO_x/ZrO_2 gate dielectric (d) SiO_x/Al_2O_3 gate dielectric

3.3.4 Conductance Method for D_{it} Extraction

The interface trap densities are now extracted more rigorously, using the conductance method. In the case of an MoS_2 FET, the channel is populated with electrons when gate voltage is 0 V, and as the gate voltage is swept to negative, the channel is depleted of electrons. Thus, the interface trap profile at depletion and deep depletion can be obtained in these devices. The technique for the conductance method relies on measuring the equivalent parallel capacitance of a MOS-Capacitor as a function of bias voltage and frequency. The conductance gives an idea of the interface trap density as it fluctuates with the capture and emission of carriers by the traps at the interface between the channel and the dielectric.

The conductance method was implemented at room temperature, in air. Since the device possesses series resistances from the ungated regions and from the contacts, the corrected capacitance C_c and conductance G_c need to be extracted first from the measured capacitance and conductance. First, the series resistance R_s is obtained by biasing the device in accumulation, and then the following expression is applied

$$R_S = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \quad (14)$$

where G_{ma} and C_{ma} are the measured conductance and capacitance, respectively, in the accumulation region, and $\omega = 2\pi \times$ frequency. Now, the series resistance factor is calculated as $a = G_m - (G_m^2 + \omega^2 C_m^2)R_S$, where G_m and C_m are the measured conductance and capacitance, respectively. The corrected G_c and C_c can be then calculated as:

$$G_C = \frac{(G_m^2 + \omega^2 C_m^2)a}{a^2 + \omega^2 C_m^2} \quad (15)$$

$$C_C = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{a^2 + \omega^2 C_m^2} \quad (16).$$

Now G_p/ω is calculated as:

$$\frac{G_p}{\omega} = \frac{\omega G_C C_G^2}{G_C^2 + \omega^2 (C_G - C_C)^2} \tag{17}$$

Here, G_p is the equivalent parallel capacitance, C_G is the gate capacitance, which not only involves the gate dielectric capacitance, but also the quantum capacitance of MoS_2. We take C_G as the capacitance in the accumulation region of the *C-V* curves. Finally, D_{it} is calculated as: $D_{it} = \frac{2.5}{q}\frac{G_p}{\omega}$ at the maximum value of G_p/ω for the corresponding top gate voltage.

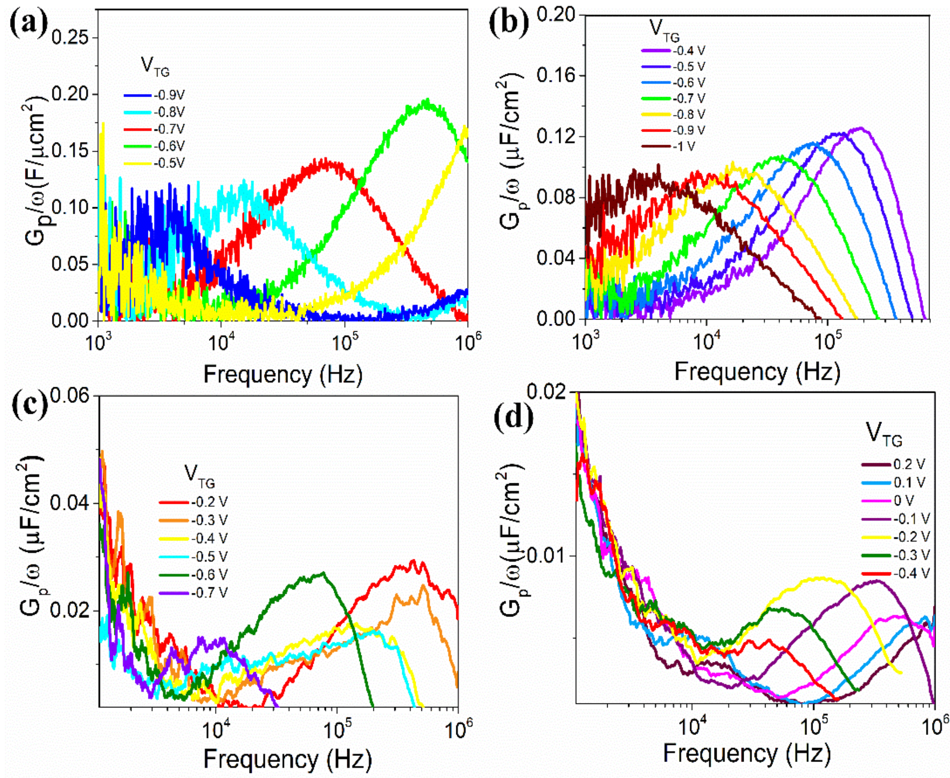


Figure 12: G_p/ω vs. frequency curve of the MoS_2 FET with (a) AlO_x/ZrO_2 gate dielectric (b) AlO_x/Al_2O_3 gate dielectric (c) SiO_x/ZrO_2 gate dielectric (d) SiO_x/Al_2O_3 gate dielectric

Figures 12 shows the G_p/ω–f curves for gate voltages varied from depletion to accumulation in an MoS_2 FET with ZrO_2 and Al_2O_3 gate dielectric for two different nucleation layers. The G_p/ω peak positions for all the devices are voltage dependent, which clearly indicates

that the Fermi level is unpinned. This confirms that the conductance method can be used to determine the interface trap density.[78] In certain cases of III-V/high-κ interfaces, the Fermi level is pinned and the conductance peak does not change with the gate voltage applied, causing the conductance method to be inapplicable there.[78] In case of the device with AlO_x nucleation layer, the G_p/ω peak gets reduced from flat band to depletion as shown in the **Figure 12a** and **12b**. **Figure 12c** shows the same trend for SiO_x/ZrO_2 device with one exception near the midgap where the peak is as high as the peak of the flat band position. For the device with SiO_x/Al_2O_3 gate dielectric (**Figure 12d**), the G_p/ω peak increases as the gate voltage is swept from flat band to depletion, indicating the increase in D_{it} as the Fermi level shifts further into the band gap from the conduction band edge. An opposite trend is observed below the mid-gap.

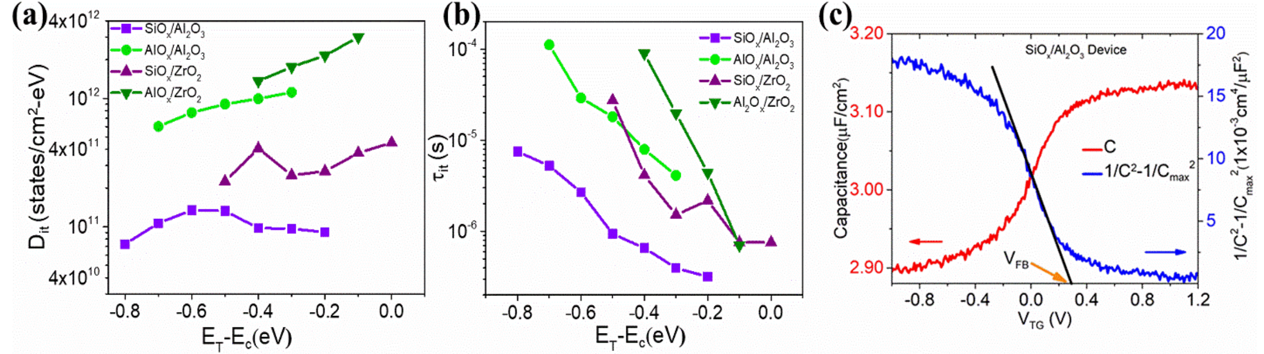


Figure 13: (a)D_{it} and (b) interface trap time constant τ_{it} of MoS_2 device with different nucleation layer and gate dielectric combinations.(c) extraction of flat band voltage from *C-V* characteristics

Figure 13a and **13b** shows the extracted D_{it} values and interface trap time constants respectively as a function of the trap position (E_T–E_c) for the devices with different nucleation layer and gate dielectric combinations. The position of the interface trap in the band gap of MoS_2, E_T-E_c, is obtained from the gate voltage applied during the capacitance and conductance measurements by subtracting the flatband voltage (obtained from *C-V* curves) from V_G. The flat band voltage is extracted from the x-intercept of ($\frac{1}{C^2} - \frac{1}{C_{max}{}^2}$) vs. V_{TG} curve as shown for a

representative device in **Figure 13c**. At flat band, the Fermi level is close to MoS_2 conduction band edge, since MoS_2 FET is a depletion-mode device. Any voltage applied below the flat band voltage directly translates to how much the Fermi level moves into the bandgap of MoS_2. Thus, V_{TG} applied below flat band voltage moves the Fermi level (equivalent to the interface trap energy level) from the E_c toward E_v of MoS_2. **Figure 13a** clearly reports that irrespective of the nucleation layer, the interface between MoS_2/Al_2O_3 exhibits lower trap densities compared to the MoS_2/ZrO_2 interfaces. It is also evident from the **Figure 13a** that SiO_x nucleation layer offers lower interface trap density while compared to the AlO_x nucleation layer. Therefore, the lowest D_{it} is obtained for $MoS_2/SiO_x/AlO_x$ interface. At the mid gap, the D_{it} extracted for SiO_x/Al_2O_3 gate dielectric is ~1.3×10^{11} states/cm^2-eV, while the D_{it} is 9×10^{10} states/cm^2-eV near the conduction band edge, and the D_{it} is 7×10^{10} states/cm^2-eV near the valence band edge. It is well-known that the inclusion of a nucleation layer increases the interface traps. However, our experiments show that the interface quality of a 2D/high-κ system where SiO_x is used as the nucleation layer for ALD of Al_2O_3 exhibits D_{it} values close to the 2D/2D dangling-bond-free interface enabled by h-BN on MoS_2.[82] The observation of low D_{it} values using SiO_x nucleation layer could be due to its ability to facilitate faster reactions between surface hydroxyl groups and ALD precursors.[83] The D_{it} values we obtained from the SS analysis are in the ballpark of the D_{it} values extracted using the conductance method. The low D_{it} clearly establishes the superior quality of 2D/high-κ interfaces for realizing high performance and reliable (opto)electronic devices. The interface trap time constants can be obtained from the relation: $\tau_{it} = 2/\omega$, where ω is the radial frequency corresponding to the peak of the G_p/ω *vs.* f curve. The interface trap time constants shown in the **Figure 13b** are similar for all three different interfaces except the $MoS_2/SiO_x/Al_2O_3$ interface, signifying that different defects

contribute to the interface traps of $MoS_2/SiO_x/Al_2O_3$ compare to other three interface. The identity of defects in MoS_2 causing interface trap formation is debatable.[84] Several reports indicate that the interface traps in MoS_2 based FETs is attributed to the sulfur vacancies in MoS_2 and the presence of nucleation layer .[53, 84]

3.4 Conclusion

In summary, we have successfully fabricated MoS_2 FET using different high-κ gate dielectric materials. The detailed electrical characterizations of the fabricated device are carried on to determine the interface trap density by adopting SS and conductance method. The D_{it} values obtained by the SS method is validated by the results obtained for conductance method. we report high-quality interfaces in a semiconductor system, enabled by 2D/high-κ-dielectric systems. Using the conductance method, a mid-gap interface trap density of as low as 7×10^{10} states/cm^2-eV can be obtained by MoS_2/Al_2O_3 interface if SiO_x is used as the nucleation layer. The D_{it} values are at par with the state-of-the-art Si/high-κ interface. Our results reinforce the promise of van der Waals systems for high performance and reliable electronics and optoelectronics.

CHAPTER 4 NEUROMORPHIC COMPUTING DEVICES

4.1 Introduction

The digital computer technology is based on complementary metal–oxide–semiconductor (CMOS) transistors and von Neumann architecture. With the rapid growth of the Internet of Things (IoT) and demand for faster and energy efficient processing of huge amount of datacentric tasks, it seems current computing technology has reached to the limits in terms of scaling down and data processing speed. As mentioned earlier, CMOS technology is facing major challenge of leakage current while trying further shrinking of the transistors. Moreover, the separate memory and processing unit of von Neumann architecture proved inefficient in terms of speed and energy while needs to handle huge amount of data. This is known as "von Neumann bottleneck". These limitations have motivated the researchers to explore beyond von Neumann paradigm. Neuromorphic computing system based artificial neural network (ANN) architecture is one of the emerging computing technologies inspired by the human brain's cognitive processing system. The computing capability of human brain is not limited by the separation of memory and processing unit which enable it to process the data in exaflop speed compare to teraflop speed of the supercomputer. A human brain comprises 10^{11} neurons which are responsible for all the signal processing job while ~10^{15} synapses do the signal transmission and store information. As the name suggests, just like the human brain, artificial neuron and synapse are the building blocks of ANN. The efficient and successful implementation of the neuromorphic computing system is greatly dependent on the ability of precise emulation of the biological neuronal characteristics by the artificial neuron and synapse.

This chapter briefly discuss about the spiking neural network (SNN)- an advanced architecture of the ANN and highlights the importance of realizing artificial neuron and artificial synapse based on single memristor device. The chapter also shades light on the leaky integrate-and-fire (LIF) biological neuron model and presents the way of adaptation of this model for realizing artificial neuron. At the end of the chapter, recent reports on the 2D materials based artificial neuron is discussed.

4.2 Spiking Neural Network (SNN)

Spiking neural network, a third-generation technology of ANN mimics the human brain most faithfully among all the neural networks and are projected to be more energy-efficient in processing speech, videos and other temporal data. While for the other architectures of ANN, results are obtained only after processing all the layers, SNN can generate output result even after producing the first spike. This enables SNN to reduce latency and computational complexity.[85] Initially, event driven SNNs were simulated in software and implemented on a machine that works based on von Neumann architecture.[86] This approach holds back the whole process in terms of speed and power consumption due to physical separation of memory and processing unit of von Neumann architecture. The more realistic approach to mimic the enormous parallel processing with extreme low power consumption capability of human brain would be realization of SNN with hardware system that has building blocks like biological neuron and synapse. The expedition of realizing hardware based artificial neuron and synapse started with complex CMOS circuitry, where single neuron and synapses are realized with multiple transistors.[87] Due to areal and energy limitation, this technology is not suitable for large scale implementation of SNN. This

influences the exploration for single device that can emulate the biological neuron or synapse efficiently. The revival of memristor in 2008 was a huge breakthrough to implement this idea.[88] Oxide,[89] phase change material (PCM),[90, 91] 2D material based simple two terminal non-linear memristor devices with dynamic memory switching effect and tunable conductance have been utilized to emulate bio-synaptic learning rules and key characteristics of biological synapse like long term potentiation and depression (LTP/LTD), pair-pulse facilitation/depression.[28] In spite of equal importance of artificial neuron, to date, memristor based neurons are not well-explored. Because, emulation of the transient switching with rich dynamics and processing data at temporal or frequency domain like the biological neuron is quite complex and challenging.[92]

4.3 Artificial Neuron for SNN

In the biological neuron, the lipid bi-layer membrane of a neuron has leaky ion channels, and it modulates the ion (Na^+, K^+) movements between the extracellular and intracellular fluid. With the incoming signals through synapses, the membrane potential changes due to the variation of the ion concentration between the extracellular and intracellular fluid. Once the membrane potential reaches a threshold value, the ions flow through the leaky ion channels to transmit the signals and bring down the membrane potential to the equilibrium state. The schematic of the biological neuron shown in the **Figure 14** explains the process of generating action potential for incoming signal.

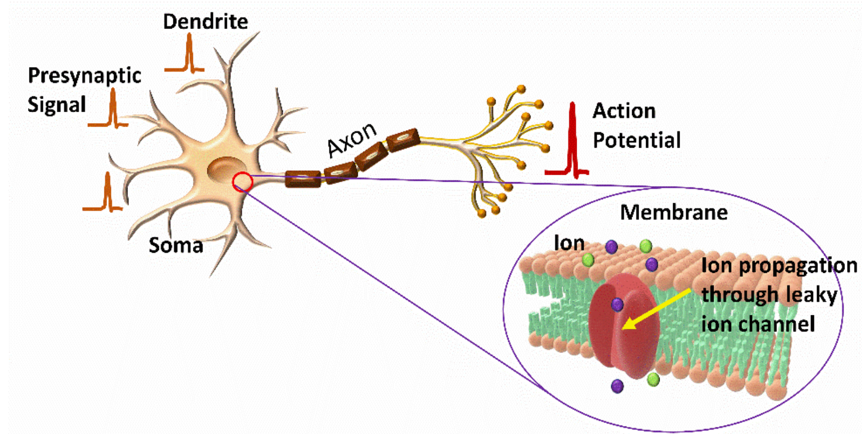


Figure 14: Schematic of the biological neuron. The presynaptic signal changes the membrane potential and causes the ion propagation through the leaky ion channel. The process the generates the action potential and transmit the signal to the next neuron.

These neuronal characteristics are explained with different models like integrate-and-fire (IF), leaky integrate-and-fire (LIF) Hodgkin–Huxley (HH) model. Out of them IF and LIF model describes bio plausible neuronal activity with a superficial explanation of biophysical reason of electrical activity. On the other hand, biophysical HH model describes precisely the ion dynamics at ion channels during the spiking. [93] While biophysical HH neuron has some advantages over IF and LIF neuron like precise control over the rate of spiking, it demands complex circuits. For the energy and areal efficient implementation of neuromorphic hardware system, LIF model is found more suitable compare to the HH neuron model.

4.3.1 Leaky Integrate-and-Fire Model

The IF model is the simplest model for the biological neuron. The IF model is based on the following equation to explain the spiking of the neuron

$$I(t) = Cm\frac{dV_m}{d_t} \tag{16}$$

Where I is the input current, V_m and C_m denotes the membrane potential and capacitance respectively. With the input current, the membrane potential increases with time, once it reaches to a constant threshold value, the spike generates at the output and V_m reset to 0. The firing frequency of the neuron proportionally changes with the input current. [94]

To match the biological neuronal activities more closely, the LIF model added a "leaky" term with the IF model. This addition emulates the diffusion of ion through the leaky ion channel of the membrane of the biological neuron. The LIF model is explained by following equation

$$I(t) - \frac{V_m}{R_m} = Cm\frac{dV_m}{d_t} \tag{17}$$

R_m is the membrane resistance, inclusion of the R_m initiates time dependency for the spike. While IF model consider the membrane as perfect insulator i.e. R_m is infinity, LIF model says that eventually the potential across the membrane would decay to zero, if the neuron does not receive continuous input. [95]The firing frequency of the LIF neuron is defined by the following equations

$$f(I) = \begin{Bmatrix} 0, & I < I_{th} \\ \left[t_{ref} - R_m C_m log\left(1 - \frac{V_{th}}{IR_m}\right)\right]^{-1}, & I > I_{th} \end{Bmatrix} \tag{18}$$

The LIF model is applicable to both excitatory and inhibitory neuron. [96] **Figure 15** demonstrates the SNN algorithm using a LIF neuron. The presynaptic input voltage spikes are converted to time varying current signal, synaptic weights control the overall current value. The current through different synapse summed up and fed to the LIF neuron. Depending on the threshold value the LIF neuron generates the output spike.[97]

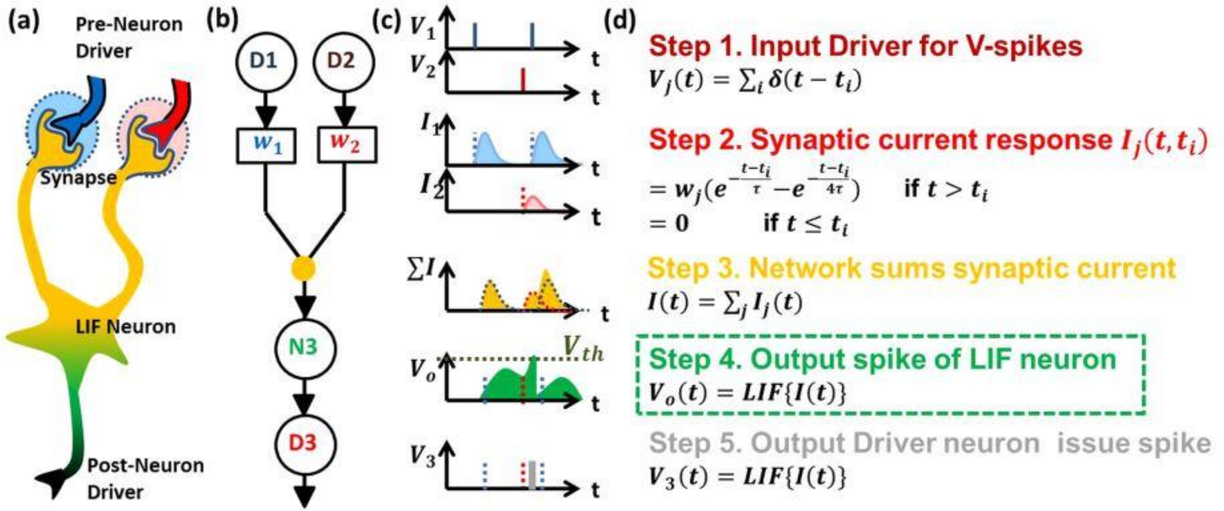


Figure 15: (a) Biological neuron network represented with (b) algorithmic SNN analog (c) the signal timing at each step of input presynaptic signal to output action potential generation process. (d) the evolution of the signal at each step. Adopted with permission from the reference [97]

This algorithm can be implemented with a simple electronic circuit which requires the elements to emulate the synaptic weight and integration and a device that has leaky and threshold characteristics as shown in the **Figure 16**. Recently, threshold switching memristor (TSM) devices [98], non-volatile memristors [99], phase change materials (PCM) [100] and ferromagnetic materials-based field effect transistors (FET) [101, 102] and floating body transistors [97] have been utilized to demonstrate leaky integrate-and-fire (LIF) neuron for SNNs. Memristive properties in 2D materials provides opportunities of realizing artificial neurons with these atomically thin systems, which will allow the vertical scaling of neural network hardware [28, 29, 103]. Some reports demonstrated the artificial neuron with the 2D materials-based threshold switching memristor (TSM) [29, 92, 104, 105] while others used the 2D materials-based field effect transistor (FET)[30, 106-108].

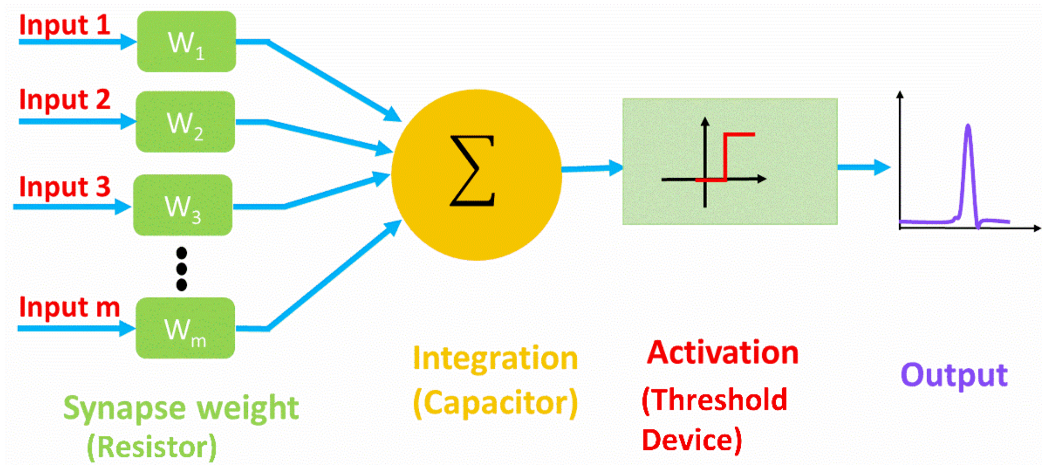


Figure 16:The schematic of circuit components for LIF neuron realization.

4.4 Literature Review on 2D Materials Based Artificial Neuron

H. Kalita *et al.* first realized the artificial neuron based on 2D materials based TSM. [29, 109] In this work, van der Waals heterojunction based TSM device is fabricated with the chemical vapor deposition (CVD) grown multilayer MoS_2 and graphene. The memristor device having threshold voltage (V_{th}) ~2.8-4.2 V shows consistent volatile switching characteristics up to 1μA. Authors postulated the threshold switching of the TSM device is attributed to grain boundaries of polycrystalline MoS_2. The TSM device is integrated with a RC circuit to demonstrate an artificial neuron. The artificial neuron emulates all or nothing spiking, refractory period and strength modulated frequency response of biological neuron. Though the MoS_2/graphene TSM device demonstrates basic properties of an artificial neuron, it suffers from high threshold voltage, low ON-OFF ratio, low ON current characteristics which would make it challenging to integrate with a synaptic circuit and unsuitable for energy-efficient operation. S. Hao *et al.* optimized the channel length of monolayer MoS_2 (500 nm) of the lateral TSM device to acquire the volatile behavior.[92, 109] The device depicts threshold voltage of ~1.2 V and ON-OFF ratio of ~10^4. With 1 μA

compliance current device shows consistent volatile behavior and for higher compliance current device has tendency of losing volatile properties. However, this work demonstrated artificial neuron without an external circuit. The device connected with the voltage pulsing source initially does not respond to the pulse train having voltage amplitude lower than V_{th}. After certain time period similar to the integration period of biological neuron, the device turns ON which resembles the firing of biological neuron. The integration period is tunable with the amplitude of the incoming pulse train. The device recovers from the firing state with appropriate time interval (50 ms) between set of pulse trains which is analogous to the leaky behavior of the biological neuron. Authors fabricated a memristive artificial neural network by incorporating MoS_2 based neuron and Cu/GeTe based synapse to demonstrate the computing ability of the neuron.

Y. Chen *et al.* also demonstrated LIF neuron based on 2D Mxene (Ti_3C_2) TSM without external circuit.[105] The Cu/MXene/Cu memristor device shows bidirectional volatile switching with the threshold voltage of 0.68 V. The OFF-state current is high (~10 μA) and it loses the volatile characteristics only after 3 consecutive cycles. The conductance of the device at HRS is explained by space-charge limited conduction while the resistive switching is due to the formation of Cu filament through the MXene. The positive pulse train with constant amplitude causes a gradual increase of the device current and after certain number of pulses the current increases sharply. This behavior is compared with integration and fire characteristics of biological neuron. The number of pulses required for the sharp increase of current is higher for pulse train with the higher pulse interval which indicates the leaky nature of the artificial neuron. The recovery time is around 0.6 s after the neuron fires.

Along with memristor devices FET configuration is also explored to realize an artificial neuron. [30, 106-108] Recent reports demonstrate the viability of FET based neurons for

applications like sound localization[30], logic gate implementation along with single neuron implementations.

M. E. Beck *et al.* demonstrated a spiking neuron that follows the Hodgkin-Huxley model utilizing a Gaussian heterojunction transistor (GHeT).[106, 109] The CVD grown monolayer MoS_2 and carbon nanotube (CNT) are used to form the p-n junction for dual gated GHeT. The drain current shows an anti-ambipolar response under the dual gate control. The height, peak position and full-width-half-maximum (FWHM) of the antiambipolar response can be tuned by varying the offset between the top and bottom gate voltage. The tunable antiambipolar response of the GHeT is utilized to demonstrate the spiking neuron. The circuit incorporates GHeT, n-type FET, resistors and capacitors to emulate the Na+ ion channel of the biological neuron, while the K+ ion channel is mimicked by delayed turn ON of a n- type FET. Depending on the input synaptic current (I_{syn}), OFF current (I_{OFF}) and peak current (I_{peak}) of GHeT, the GHeT and delay transistor turn ON and turn OFF sequentially and generates the continuous spikes at output terminal. The simulations show, the spiking neuron consume energy ~250 nJ per spike. Simulation using the experimental circuit depicts that, the circuit can generate constant spiking, class-I spiking, phasic spiking, phasic bursting, tonic bursting by varying the biasing at top and bottom gate.

S. Das *et al.* utilized exfoliated MoS_2 based split gate transistor to demonstrate the coincidence neuron for the audiomorphic computing application.[30, 109] To localize the source of sound accurately by processing the interaural time difference (ITD) is a complex computational task for any animal. The Jeffress model- a model that closely resembles the brainstem of barn owl, explains how the nerve cells process the acoustic timing difference to determine the source of a sound. The three main neural components of Jeffress model are the time delay neuron, the coincidence detector neuron and the spatial computational map. The concurrent arrival of spikes

at corresponding delay neuron only turn on the coincidence neuron. The distance of the delay neuron from right and left cochlear is maintained in such a way that, one coincidence neuron only fire at a time, so that the source of sound can be precisely localized. S. Das et al. fabricated a MoS_2 based multiple split gate transistor which turns on only when a pair of split gates receive the input voltage pulse simultaneously. Electrical measurements show that, the ON-OFF ratio which is termed as inhibition ratio (IR) is highest while voltages are applied to vertically aligned split gates. This behavior mimics the coincidence neuron. The delay neuron is realized with a fully top gated MoS_2 FET, where the delay or time constant is controlled by the top gate voltage. To build complete biomimetic audiomorphic architecture, the drain terminal of delay neurons is connected to each split gate of the coincidence neuron. By varying the channel width and length the resistance of the delay neuron is varied in such a way that, for top gate it increases monotonically right to left and for bottom gate it increases left to right. With this arrangement, for positive, negative and zero ITD, three different vertically aligned split pair gate of coincidence neuron receives the coincident signal. The ability of tuning the current of the coincidence neurons with back gate, added the feature of neuroplasticity to the audiomorphic device.

L. Bao demonstrated a dual gate neuristor using the exfoliated MoS_2 based FET. [107, 109]PEO:$LiClO_4$ l is used as the top gate dielectric which control the ionic migration and the back gate dielectric SiO_2 controls the electronic migration. Utilizing the ionic migration of Li^+ from top gate, the synaptic characteristics like STP, LTP and PPF are demonstrated. To emulate the propagation of action potential through axon of biological neuron with the neuristor, both back gate and top gate of the are utilized. The sampling clock applied at back gate is incapable to populate the MoS_2 channel with n-type carriers, hence no current flow from drain to source. In this condition, the drain terminal voltage remain high compare to source terminal. Once the top gate is

fed with input voltage pulses at same frequency of sampling clock at back gate, the device turns ON and the potential at source terminal increases to drain potential like the action potential propagation at axon. The variation of output spikes is dependent on the amplitude of input voltage pulse at top gate and follows the sigmoid function. The simulation using the shifted and scaled sigmoid function obtained from the neuristor results faulty output at neural network for written digit recognition. However, the performance can be improved by the parameter optimization of the algorithm.

S.G. Hu *et al.* reported an exfoliated MoS_2 based coplanar neuron transistor with one floating gate and two control gates.[108, 109] The ability of controlling the transistor with both control gate simultaneously is implemented to emulate the summation function of biological neuron. To demonstrate neuromorphic application, abacus like counting scheme, AND logic and OR logic are demonstrated using this transistor. For logic gate application two control gates are fed with square waves at different frequency and the drain current level is labeled as high and low state.

4.5 Conclusion

In summary, the inclusion of the time dependent function in the SNN, enhances its ability to emulate the neuronal dynamics more accurately. The efficient hardware implementation of the SNN demands reliable low power individual artificial neuron and synapse device. In the recent years, the artificial synapse has been well explored with different materials and device system. The research field of artificial neuron is still immature compare to the artificial synapse. There is dire need of realizing scalable, robust, and low power artificial neuron with the capability of reliable

emulation of the functions of the biological neuron. The realization of the artificial neuron with 2D material will advance the field in terms of scalability, energy efficiency and pave the way for realizing neuromorphic hardware on flexible and wearable platform.

CHAPTER 5 ARTIFICIAL NEURON

The contents of this chapter have been published in: Dev, D., Krishnaprasad, A., Shawkat, M.S., He, Z., Das, S., Fan, D., Chung, H.S., Jung, Y. and Roy, T., 2020. 2D MoS_2-Based Threshold Switching Memristor for Artificial Neuron. IEEE Electron Device Letters, 41(6), pp.936-939.

5.1 Introduction

In this chapter, we demonstrate an artificial neuron using chemical vapor deposited (CVD) 2D MoS_2-based TSM. The volatile switching characteristics of the TSM is enabled by a top silver (Ag) electrode. The Au/MoS_2/Ag TSM exhibits volatile switching characteristics with a low threshold voltage, high ON-OFF ratio and high endurance. Area and temperature-dependent measurements establish that the volatile switching originates from complex Ag ion dynamics. The TSM device is integrated with a simple RC circuit to emulate a LIF neuron, which exhibits all-or-nothing spiking, threshold-driven firing and stimulus strength-based frequency response like biological neurons and shows controllable variation of temporal response with varying input and circuit parameters.

5.2 Device Fabrication and Characterization Techniques

5.2.1 Au/MoS_2/Ag Memristor Device Fabrication

The device schematic and optical image of the Au/MoS_2/Ag device is shown in the **Figure 17**. The device fabrication starts with the standard cleaning and patterning of the Si/SiO_2 substrate for the bottom electrode and the alignment marks. The patterning is done with the standard

photolithography process using SUSS MicroTec MJB4 mask aligner. E-beam evaporator is used to deposit Ti/Au (5/100 nm) as bottom electrodes. Mo (10 nm) is patterned and deposited by e-beam evaporation on the bottom electrode. The samples are then placed in a quartz tube chemical vapor deposition (CVD) furnace pre-loaded with sulfur powder in alumina boat. The base pressure of the CVD furnace is brought down to ~ 1 mTorr with a mechanical pump. To remove any residual gases, the quartz tube is purged with Argon (Ar) gas. The furnace temperature is raised to ~ 780 ^{o}C in 50 mins and held there for an additional 50 mins. Continuous supply of Argon (Ar) gas flow is provided during the reaction between sulfur and Mo. The furnace is finally allowed to cool down to room temperature naturally. The sulfurization process converts Mo to 2D MoS_2. To enable diffusion dynamics for threshold switching of neuron, the top electrode is patterned and Ti/Ag/Au (2/15/40 nm) is deposited by electron beam evaporation. Ti is deposited as adhesion layer and Au is deposited to prevent oxidation of Ag electrode.

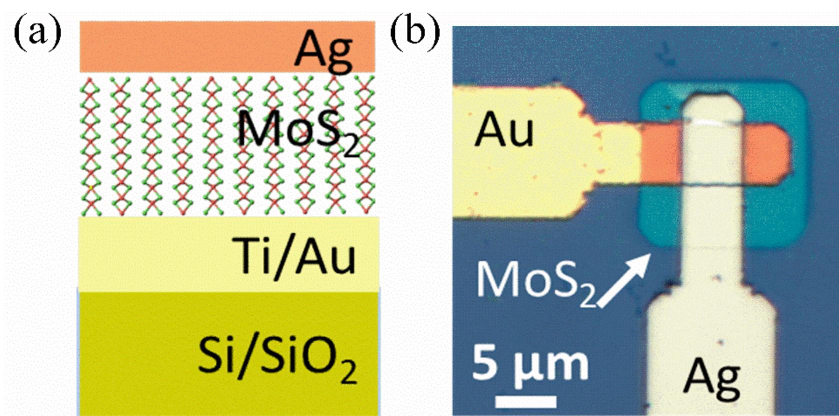


Figure 17:Au/MoS2/Ag threshold switching memristor (a) Device schematic, (b) optical image of the fabricated device.

5.2.2 Material Characterization

Confocal Raman system WITEC Alpha 300RA at room temperature was used for Raman characterization. 532 nm laser excitation source was focused by a Zeiss 50x objective with 0.7 numerical aperture. For carrying out the AFM Anasys Nano IR2 system was used in tapping mode. The TEM imaging was performed using JEOL ARM-200F at an operating voltage of 200 kV and a spatial resolution down to ~ 1 Å.

5.2.3 Electrical Characterization

We perform electrical measurements to characterize the LIF neuron and the artificial nociceptor using a B1500A Semiconductor Device Parameter Analyzer, Tektronix AFG3022C function generator and an DPO 2024B Oscilloscope, on a Janis cryogenic probe-station. Lakeshore 336 cryogenic temperature controller is used to control the temperature during temperature dependent *I-V* measurement. B1530A Waveform generator/ fast measurement unit (WGFMU)- 1 is used to apply the input voltage pulse to the artificial neuron circuit and WGFMU-2 is used to read the output current spikes. For the artificial neuron measurement, the resistor and the capacitor of the RC circuit are externally connected.

5.3 Results and Discussion

5.3.1 Material Characterization

Figure 18a shows the Raman characterization of chemical vapor deposition (CVD) grown MoS_2. The presence of prominent in-plane (E^1_{2g}) peak at 382 cm^{-1} and out-of-plane (A_{1g}) peak at

407 cm^{-1} in the Raman spectrum indicates the growth of high-quality multilayer MoS_2. [110] Atomic force microscopy (AFM) confirms the thickness of MoS_2 as 23 nm, as shown in **Figure 18b**. **Figure 18c** shows the vertical stack of the fabricated device in a cross-sectional view via transmission electron microscopy (TEM) characterization. The left and mid images in **Figure 18c** are dark-field scanning TEM (STEM) and bright-field high-resolution TEM (HRTEM) characterization, respectively. 2D MoS_2 layers are confirmed to grow vertically in direct contact with both the Ag and Au electrodes with a thickness of ~ 23 nm, consistent with the AFM height profile. The right image in **Figure 18c** shows the corresponding energy-dispersive x-ray spectroscopy (EDS) elemental map distribution of constituting elements within the device.

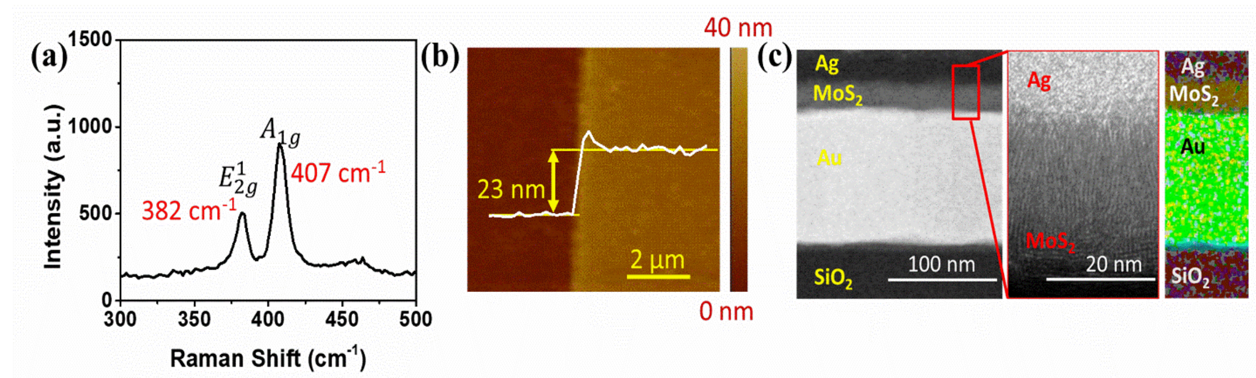


Figure 18: Material properties (a) Raman spectrum of CVD-grown multilayer MoS_2. (d) AFM height profile of MoS_2 shows thickness of MoS_2 ~23 nm. (e) STEM, HRTEM and EDS image of cross-section of the vertical stack of MoS_2/Ag shows the vertically oriented grains of polycrystalline MoS_2.

5.3.2 Electrical Characterization and Switching Mechanism

First, we analyze the DC behavior of the Au/MoS_2/Ag vertical device. In **Figure 19a,** with the application of a positive bias on the top electrode, the device switches sharply from a high resistance state (HRS) to a low resistance state (LRS) at a threshold voltage (V_{th}) of ~ 0.2 V. The transition of the device from a low OFF state current (~ 100 pA) to an ON-state current of 100 µA

dictated by setting the current compliance, accounts for an ultra-high ON-OFF ratio of 10^6. The device maintains the LRS for positive bias beyond threshold voltage. When the voltage is reduced to a value lower than V_{th}, say ~ 0.1 V in this case, the device returns to its HRS and hence loses the programing information. This clearly demonstrates the volatile nature of the device, making it a threshold switch.

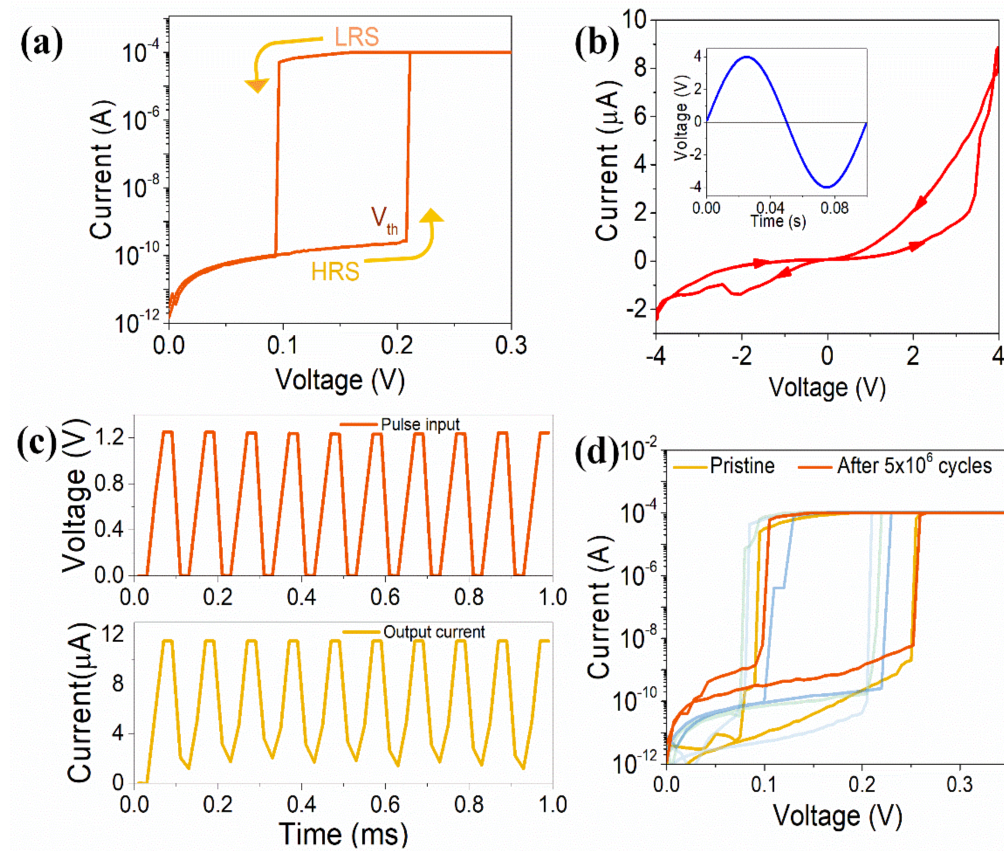


Figure 19: Electrical measurement of Au/MoS_2/Ag TSM device (a) *I-V* characteristics of the device exhibits threshold switching behavior. (b) Pinched hysteresis response of Au/MoS_2/Ag TSM device in response to sinusoidal input (shown at inset). (b) Output current response of TSM device in response to continuous pulses. TSM device is turned ON and Off by applying pulse of 1.2 V amplitude and 50 μs pulse width for 5×10^6 cycles. (b) *I-V* characteristics of the TSM device at pristine condition and after pulsing for 5×10^6 cycles. The faded *I-V* characteristics are measured after intermediate (between pristine and 5×10^6 cycles) pulsing cycles. Identical threshold voltage and volatile characteristics before and after pulsing implies excellent endurance of device.

Pinched hysteresis obtained for 10 Hz sinusoidal input voltage, shown in **Figure 19b**, confirms that the Au/MoS_2/Ag threshold switch is memristive.[111] The volatility, the low threshold voltage of 0.2 V, the sharp switching, the high ON state current and the high ON-OFF ratio observed from the DC *I-V* curves makes Au/MoS_2/Ag TSM a propitious contender for artificial neuron applications on the 2D platform. To investigate the reliability of the fabricated TSM device, continuous pulses of 1.2 V (pulse width 50 μs and 50% duty cycle) are applied on the device. The device switches to the LRS with every pulse applied and reverts to the HRS during the OFF time, as shown in **Figure 19c**. The *I-V* characteristics of the device in pristine condition and after the application of the 5×10^6 pulsed cycles are shown in **Figure 19d**. The device endures its threshold switching behavior with sharp switching characteristics, establishing the high endurance and robustness of the device.

TSM devices with active cation electrode like Ag or Cu are often termed as "diffusive memrisors".[112] In these devices, *I-V* nonlinearity and temporal conductance evolution is attributed to conductive filament formation by diffusion of active metal. It is found that, with appropriate electric field, Ag diffuses from the top electrode through the active channel material and forms a conductive path between the top and bottom electrodes. Upon removal of the electric field, the Ag filament spontaneously turns into a sphere for minimizing the interfacial energy.[112] This behavior facilitates the relaxation of the device by rupturing the conductive filament, and enables the volatile behavior. We attribute the threshold switching nature of the Au/MoS_2/Ag TSM to the formation of Ag conductive filaments through 2D MoS_2 and the self-rupturing of those filaments. The switching of the Au/MoS_2/Ag TSM device from HRS to LRS with the filament formation and transition from LRS to HRS with the filament rupturing is depicted in the **Figure 20.**

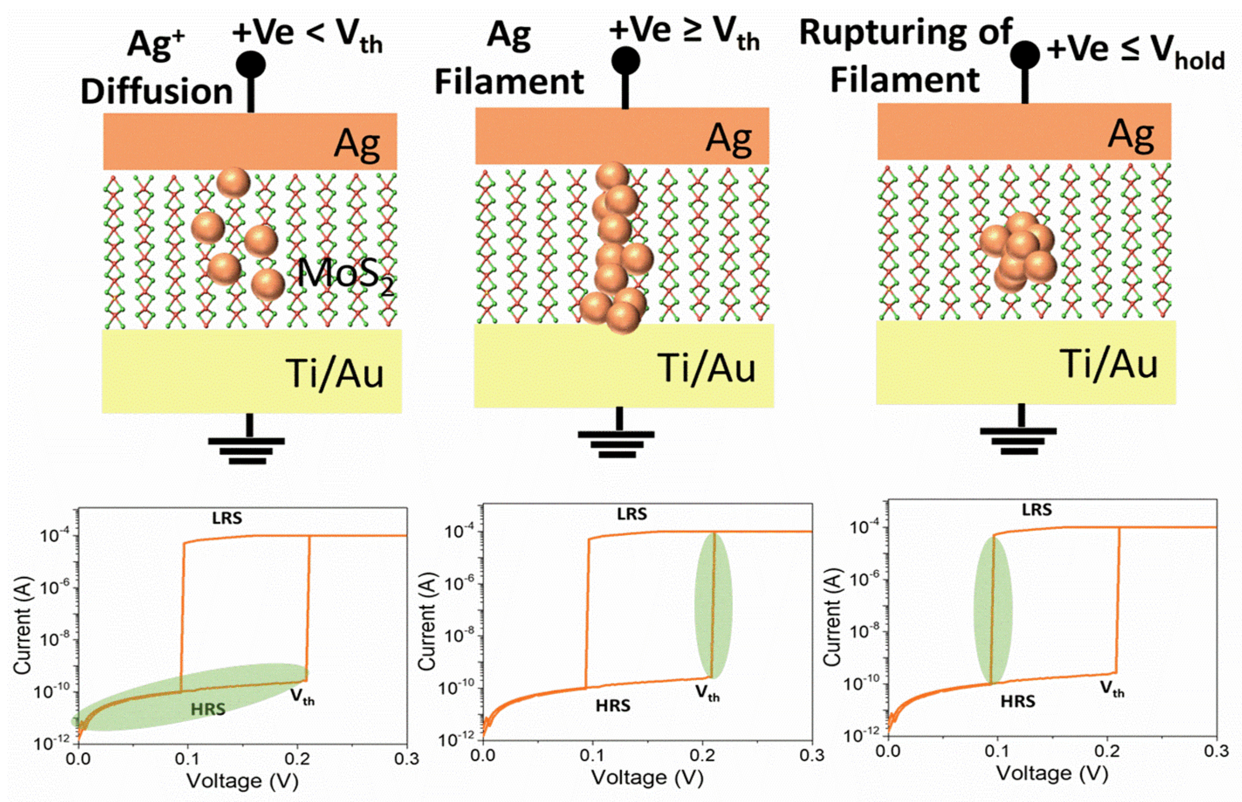


Figure 20: With the positive bias at top electrode Ag diffuses through MoS_2; at threshold voltage (V_{th}) the conductive filament of Ag forms between top and bottom electrodes and causes the transition of current from HRS to LRS; Once the positive bias gets reduced at the top electrode self-rupturing of filament reverts current LRS to HRS.

To support the claim, several electrical measurements are reported in **Figures 21a – 21f**. In **Figure 21a**, the resistance of the TSM device as a function of device area is shown. The almost invariant LRS with respect to area supports the theory of conduction through single or localized filament.[113] The inverse relation between area and HRS is ascribed to the uniform conduction, such as variable range hopping, through polycrystalline MoS_2.[114] The presence of localized grain boundaries, that limit conduction by scattering, causes the invariant HRS at larger area.[113] The filamentary switching process of the TSM is further confirmed by subjecting the device to voltage pulses with increasing amplitude. **Figure 21b** shows the *I-V* characteristics of the device in pristine condition and after the application of voltage pulses with amplitudes varying from 2-5

V with a pulse duration of 1 ms. The increase of the OFF state current after voltage pulsing indicates the ionic migration or the formation of a partial conductive path between the top and bottom electrodes.[115] As the voltage pulse amplitude is increased, the conductive filament becomes stronger and the relaxation time increases [112]. Therefore, after applying the pulse of 5 V amplitude, the device remains at LRS and this condition of the device is termed as “fully formed”. These characteristics also support the Ag diffusion-based switching process.[116, 117]

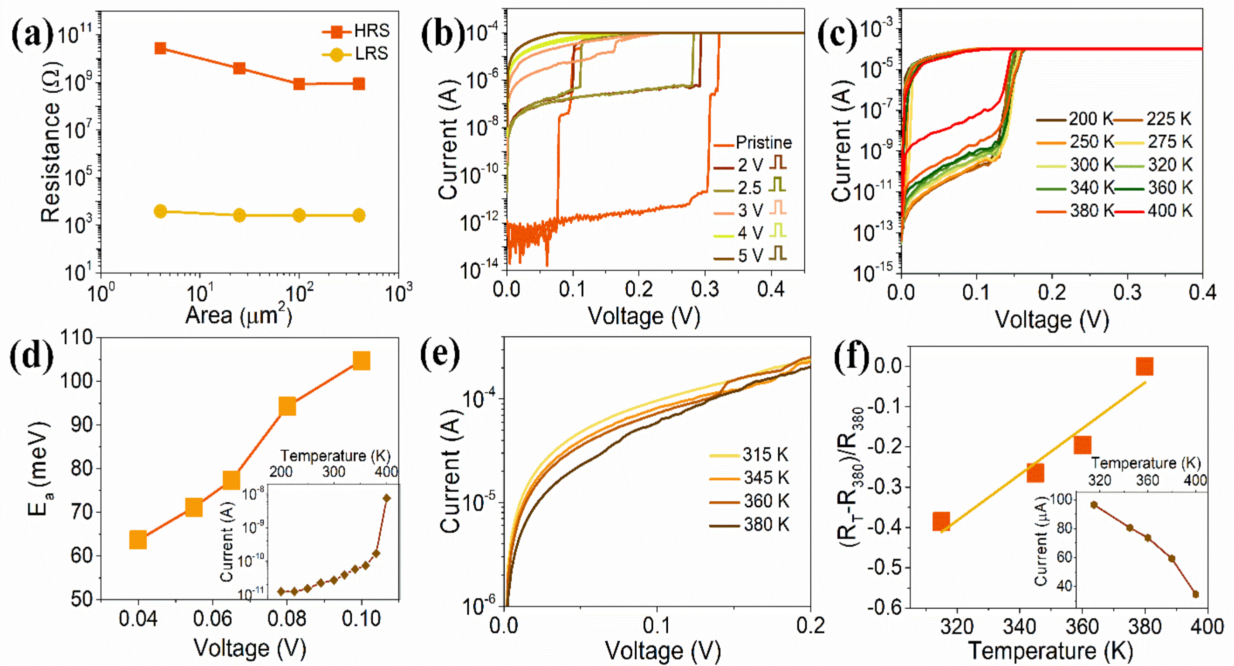


Figure 21: (a) Area dependence of LRS and HRS of Au/MoS_2/Ag TSM device. (b) *I-V* characteristics of the device in pristine condition and after subjecting the device with pulses of varying voltage amplitudes of 2 V, 2.5 V, 3 V, 4 V and 5 V for 1 ms. OFF current of the device increases compared to pristine condition after pulsing the device. At 5 V device is fully formed and device remains in ON state. (c) Temperature dependent *I-V* characteristics of the pristine TSM device. (d) The activation energy at different voltages extracted from OFF-state of temperature dependent *I-V* curves. Inset shows increasing trend of OFF-state current with increasing temperature. (e) Temperature dependent *I-V* characteristics of the TSM device at fully formed condition. (f) $(R_T - R_{380})/R_{380}$ *vs.* T graph extracted from temperature dependent *I-V* characteristics of fully formed TSM device. At fully formed condition, current decreases with increasing temperature (inset).

Temperature dependent *I-V* measurements are performed on a pristine device and a fully electroformed device to study the conduction mechanism of the Au/MoS_2/Ag structure at HRS and LRS. **Figure 21c** shows the temperature dependent *I-V* sweep of the pristine device. For the temperature range of 200 K– 400 K, the TSM device demonstrates threshold switching behavior without any significant change in threshold voltage. With increasing temperature, an increasing trend of HRS current, as shown in the inset of **Figure 21d**, is observed for the pristine device, which is similar to the temperature-dependent conductivity of intrinsic semiconducting MoS_2.[114] The low activation energy of 62 to 104 meV extracted from temperature-dependent *I-V* characteristics of the pristine device, shown in **Figure 21d**, implies variable range hopping conduction in polycrystalline MoS_2.[118] When the device is fully formed, the OFF state current decreases with increasing temperature similar to the electrical characteristics of a metallic conductor, as shown in the **Figure 21e** and inset of the **Figure 21f**, clearly indicative of the formation of a metallic path between the two electrodes. This electrochemical formation of the conductive filament can be explained by the excellent ionic mobility of Ag within MoS_2.[119] Temperature coefficient of resistance (TCR) obtained from $(R_T - R_{380})/R_{380}$ *vs. T* plot shown in **Figure 21f** is 5×10^{-3} K^{-1}, which is the closest match to the TCR of Ag nanowire (3.32×10^{-3} K^{-1}).[120] Here R_T denotes the resistance at temperature T.

5.3.3 Realization of Artificial Neuron

The Au/MoS_2/Ag TSM device can be efficiently utilized to emulate the LIF model by simply integrating it with a RC circuit as shown in **Figure 22a**. The RC circuit mimics the integration process of the membrane potential while the ion movement of a biological neuron is

emulated by the Ag ion dynamics of a TSM device. The volatile characteristics of the TSM device reflects the leaky nature of ion channels.[121]

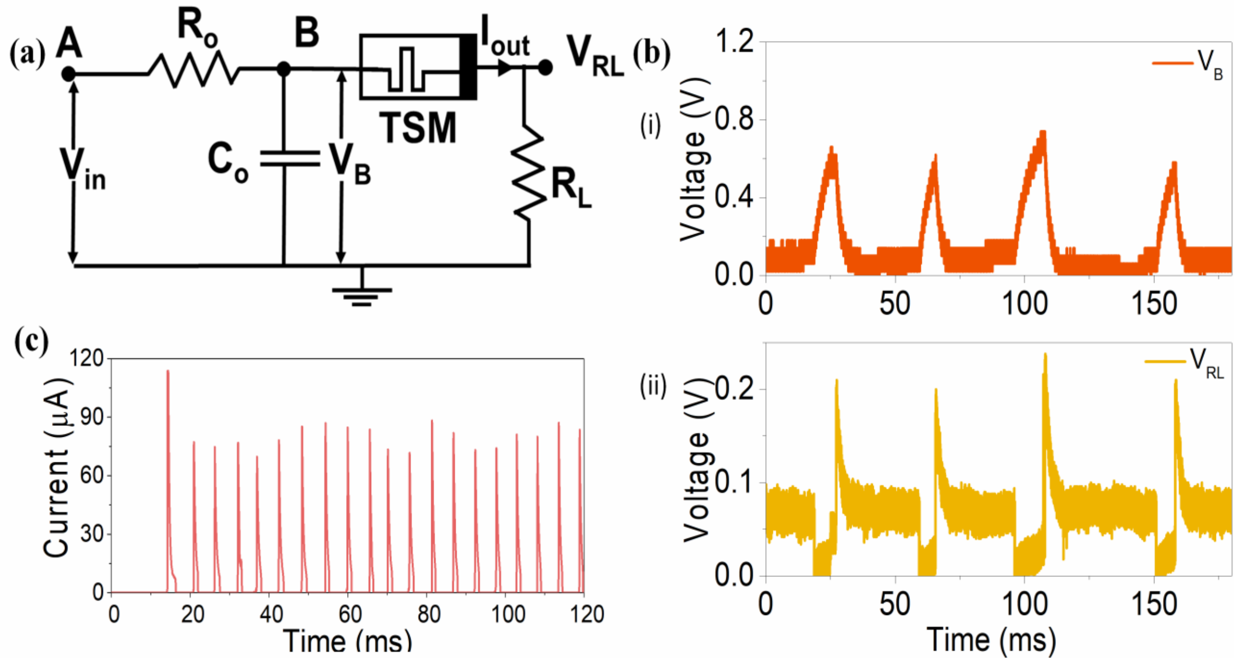


Figure 22: Realization of artificial neuron with Au/MoS_2/Ag TSM device. (a) Circuit diagram for realization of artificial neuron with Au/MoS_2/Ag neuron. (b) i) Voltage at node *B* (V_B). With incoming pulses, capacitor accumulate charges at node B till it reaches the threshold voltage of connected TSM device. ii) Voltage across load resistor R_L (V_{RL}). As soon as potential at node B reaches the threshold value, TSM switches from HRS to LRS and capacitor discharges through TSM device and R_L to produce the output spikes. (c) Continuous output current spikes for input voltage pulse train with 100 µs pulse width and 1 V pulse amplitude.

Initially the TSM device remains at the HRS and allows a negligible leakage current to flow through load resistor R_L. Therefore, in response to continuous pulses, the capacitor accumulates charge and the potential at node *B* (V_B) increases, which mimics the integration properties of a biological neuron, as shown in **Figure 22b(i)**. The time required for the potential at node *B* to reach the threshold voltage V_{th} of the TSM is known as the integration period. As soon as, V_B reaches the threshold value, the TSM switches to LRS and the capacitor discharges

through the load resistor, resulting in an output spike, as shown in **Figure 22b(ii),** and the whole process emulates the threshold driven firing behavior of a biological neuron. No response below the threshold voltage and output generated upon surpassing the threshold voltage demonstrate the all or nothing spiking of a biological neuron. The discharging of the capacitor causes V_B to decrease below V_{th} and the TSM reverts to its HRS. Figure **22c** shows the multiple current spikes generated by the artificial neuron circuit for a continuous stream of input voltage pulses with 100 µs pulse width and 1 V pulse amplitude.

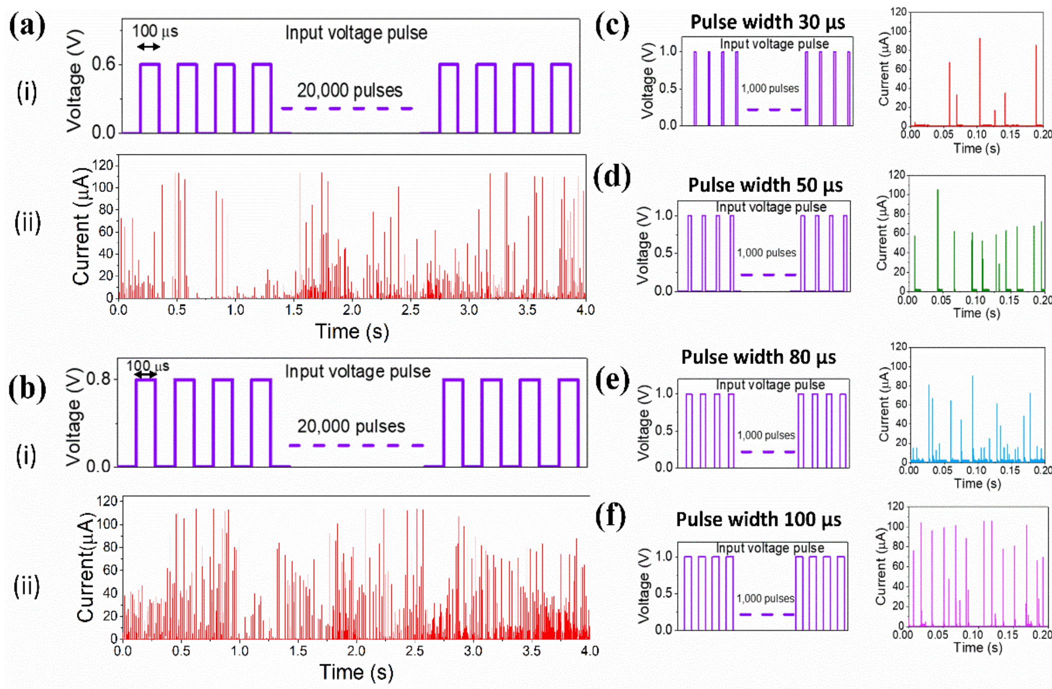


Figure 23: Stimulus strength-based frequency response of artificial neuron for pulse amplitude variation (a) i) Schematic of input voltage pulse train of 0.6 V. ii) Output current spikes for 0.6 V input pulse train. (b) i) Schematic of input voltage pulse train of 0.8 V. ii) Output current spikes for 0.8 V input pulse train. Stimulus strength-based frequency response of artificial neuron for pulse width variation. Input pulse scheme and output current spikes for (c) 30 µs pulse width. (d) 50 µs pulse width. (e) 80 µs pulse width. (f) 100 µs pulse width.

Along with the threshold driven firing and all or nothing spiking, another key feature of biological neuron is stimulus strength-based frequency. With the intensified incoming signals, the biological neuron responds with the increasing frequency of the action potential instead of

increasing the amplitude of the action potential. To emulate this characteristic, we have applied input pulses with different pulse amplitude and different pulse width to the artificial neuron circuit. The variation of input pulse parameters replicates the incoming signal of different strength to the biological neuron. **Figure 23a** and **Figure 23b** clearly indicates that, for 100 μs pulse width, spiking frequency is much higher for 0.8 V input pulses compare to 0.6 V pulse input. Similarly, the increasing pulse width with constant amplitude generates output current spikes of higher frequency as shown in **Figure 23c-23f**. This behavior clearly imitates the stimulus strength-based frequency response of biological neuron.

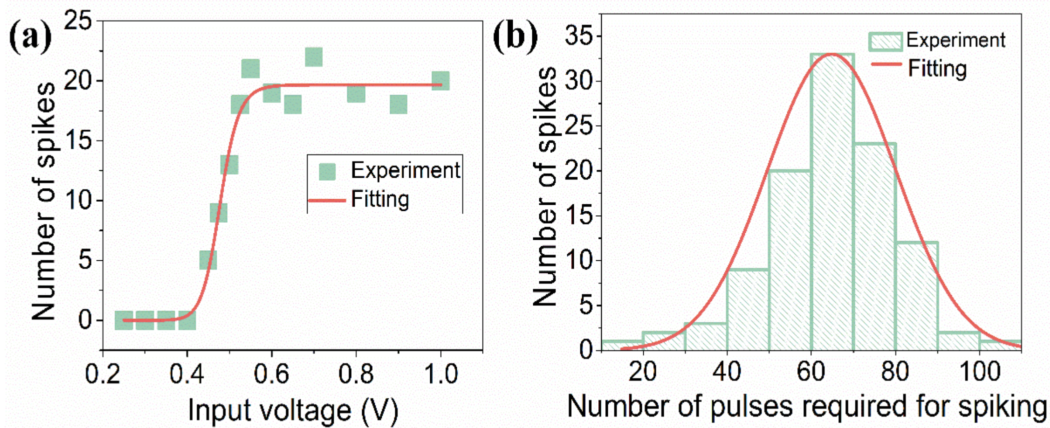


Figure 24: Activation function and stochastic nature of Au/MoS_2/Ag artificial neuron (a) The variation of number of output spikes for a given time period with increasing input pulse amplitude replicates a sigmoid activation function. (b) The variation in the number of pulses required for generating an output spike. The variation follows a normal distribution.

In a neural network, the activation function determines whether the neuron would be activated or not depending on the weighted synaptic input. **Figure 24a** demonstrates the variation in the number of output spikes as the input voltage pulse amplitude is varied. The number of spikes increases with increasing voltage amplitude. The variation of output spikes with increasing voltage amplitude follows the sigmoid function, which has been a common choice for activation functions in SNNs. It is reported that a certain degree of stochastic, noisy or probabilistic behavior is

advantageous for enhanced capability and stability of many neuromorphic systems.[100, 122] It is known that in any artificial neuron application, inherent stochasticity can play a vital role for signal encoding and transmitting in extremely noisy environments. In intricate computational tasks, such as in Bayesian inference, stochastic neuronal dynamics shows superiority over deterministic neuronal dynamics.[100] We perform a statistical analysis of the distribution of output current spikes over a time period of 4 s, consisting of 106 output spikes for 20,000 input voltage pulses. **Figure 24b** shows the distribution of the number of input voltage pulses required to generate an output spike. The variation of number of pulses to generate the spiking output follows a normal distribution due to the stochastic nature of the device.

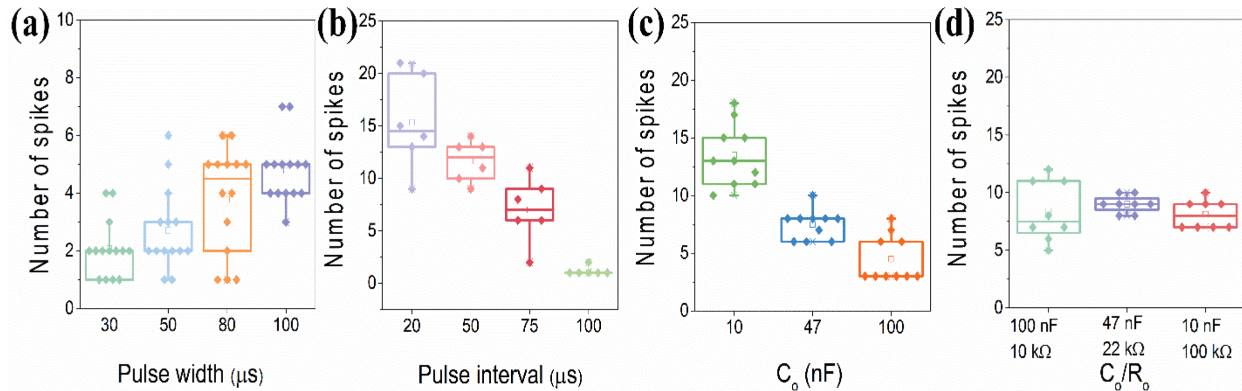


Figure 25: Controllable neuron firing for varying input pulse and circuit parameters. (a) Increasing pulse width with constant pulse interval and pulse amplitude leads increasing spiking frequency. (b) Increasing pulse interval with constant pulse amplitude and width results in decreasing spiking frequency. (c) Lower capacitance (C_o) increases the spiking frequency. (d) Variation of both R_o and C_o by keeping RC time constant unchanged does not affect the spiking frequency.

Controllable temporal response of the artificial neuron is another critical requirement for SNN application. **Figure 25a-25d** depicts the variation of the number of output spikes with the modulation of the input pulse parameters and circuit parameters. **Figure 25a** shows that increasing pulse width facilitates faster charging of input capacitor C_o, hence an increasing number of spikes is observed with increasing pulse width. The firing output is also controllable with pulse interval;

increasing the pulse interval results in decreasing number of output spikes, as shown in **Figure 25b** Reduction of the value of the input capacitance C_o brings down the integration period, which in turn results in an increase in spiking frequency, shown in **Figure 25c**. **Figure 25d** demonstrates that changing the input resistance while keeping the *RC* time constant at a fixed value does not affect the output spiking frequency. The ability of tailoring these input pulse and circuit parameters for controlling the firing rates makes the Au/MoS_2/Ag artificial neuron viable for use in neuromorphic applications.

For validating the performance of the artificial neuron from a system perspective, we apply the experimentally obtained parameters of the Au/MoS_2/Ag TSM-based artificial neuron to an SNN simulation[123] for unsupervised image classification task using an MNIST dataset. The network architecture consists of two layers as shown in **Figure 26a**. The first layer is the input layer containing 28×28 neurons (one neuron per image pixel) and the second layer is the processing layer containing 20×20 output neurons. Output neurons only fire when the input image matches with the learned pattern. The simulation shows 88% classification accuracy on 10,000 test images, with the results shown in **Figure 26b**.

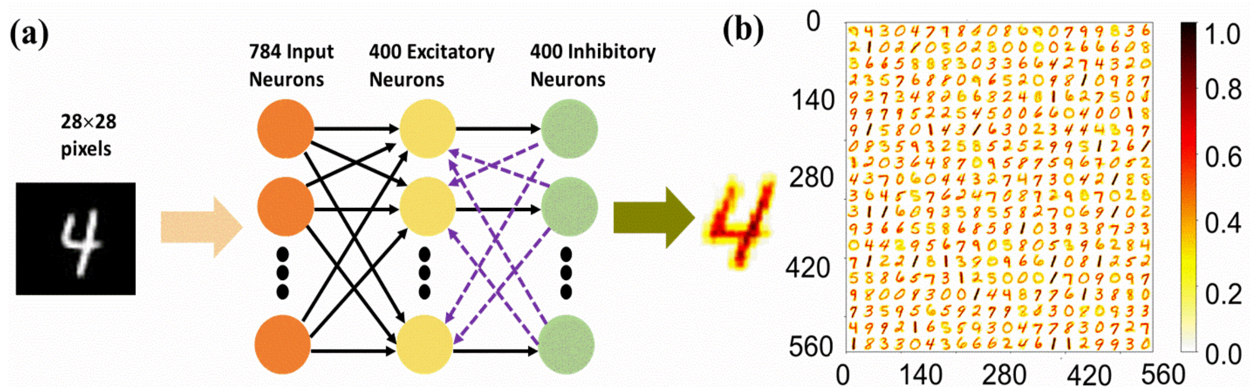


Figure 26: (a) Block diagram of network architecture adopted to classify MNIST dataset with unsupervised learning technique. (b) The trained weight connections between 28×28 input and 20×20 output-neuron, for MNIST pattern recognition.

5.4 Conclusion

In conclusion, Au/MoS_2/Ag memristor devices are fabricated with large area CVD-grown MoS_2, exhibiting threshold switching characteristics at a high ON state current, high ON-OFF ratios and excellent endurance. Electrical measurements confirm that the threshold switching originates from conductive filament formation by Ag diffusion through 2D MoS_2. A LIF neuron with controllable spiking characteristics is realized using the TSM device. The demonstration of the artificial neurons with 2D MoS_2 exhibits the viability of this device for future neuromorphic applications and edge computing on a complete 2D platform.

CHAPTER 6 MONOLITHIC INTEGRATION OF ARTIFICIAL NEURON & SYNAPSE

6.1 Introduction

The demonstration of the artificial neuron with 2D MoS_2 exhibits the viability of this device for neuromorphic computing hardware. Especially low threshold voltage, consistent volatile characteristics along with the high endurance and wide tunability made this device a potential contender for low power reliable applications. Along with the 2D MoS_2 artificial neuron device, we also developed two different MoS_2 based artificial synapse. Both the Graphene/MoS_2 and Au/MoS_2/Ti/Au synapse device demonstrates all the critical synaptic characteristics like long-term potentiation (LTP) long-term depression (LTD), short-term potentiation (STP), spike timing dependent plasticity (STDP) which are critical for neuromorphic applications. The unique linear and symmetric weight update exhibited by Graphene/MoS_2 synapse device prove its viability for unsupervised learning. The low device to device and run to run variation exhibited by the Au/MoS_2/Ti/Au synapse device make it reliable for large scale implementation. This chapter starts with the brief description about the two different synapses used for the integration.

Next, we present the monolithic integration of MoS_2 based artificial neuron and artificial synapse for realizing single layer perceptron and Boolean logic gates. For the single layer perceptron realization, Gr/MoS_2 artificial synapse is integrated with the Au/MoS_2/Ag TSM based artificial neuron. The realization of the single layer perceptron proves the ability of our devices for large scale integration. From the recent report, it is evident that, biological neuron of human brain is capable of Boolean functions.[124, 125] To enable the logical operation through the neural network it is critical to demonstrate the Boolean logic gates utilizing artificial neuron and synapse.

The chapter also demonstrates the Au/MoS_2/Ti/Au artificial synapse and Au/MoS_2/Ag TSM based artificial neuron integration process to realize the AND, OR and NOT logic gates.

6.2 Artificial Synapse Device

6.2.1 MoS_2/graphene Synapse Device

To study the DC and pulsed characteristics of the monolithically integrated single layer perceptron we have incorporated MoS_2/graphene memristor device as artificial synapse. **Figure 27a** shows the schematic for the MoS_2/graphene cross-point memristor device, the graphene performs as bottom electrode while 60 nm Ni on top of SiO_2/MoS_2 acts as top electrode [28]. The CVD grown MoS_2 has around 9 nm of thickness. **Figure 27b** depicts the scanning electron microscopy (SEM) image of the fabricated device. **Figure 27c** shows the non-volatile switching characteristics of the MoS_2/graphene device. With the positive bias at the graphene bottom electrode the device shows forming-free resistive switching up to 10 µA. The device can be SET to certain conductance state by varying the compliance current from 100 nA to 10 µA. The presence of distinct 5 states with the continuous SET process indicates its ability to undergo DC potentiation. The device can be depressed from the high conductance state to the lower conductance state by applying negative bias to the bottom electrode, the process is termed as RESET. Seven distinct conductance states are observed during the RESET process as shown in **Figure 27c**. The DC potentiation and depression enable us to set the device at certain conductance state. For the electrical synapse application, this is very important as with this process we can control the synaptic weight of the device. The common synaptic characteristics like STP, LTP,

retention, spike timing dependent plasticity (STDP) are demonstrated with this device.[28] The low programing current of this device makes it promising for extreme low power applications.

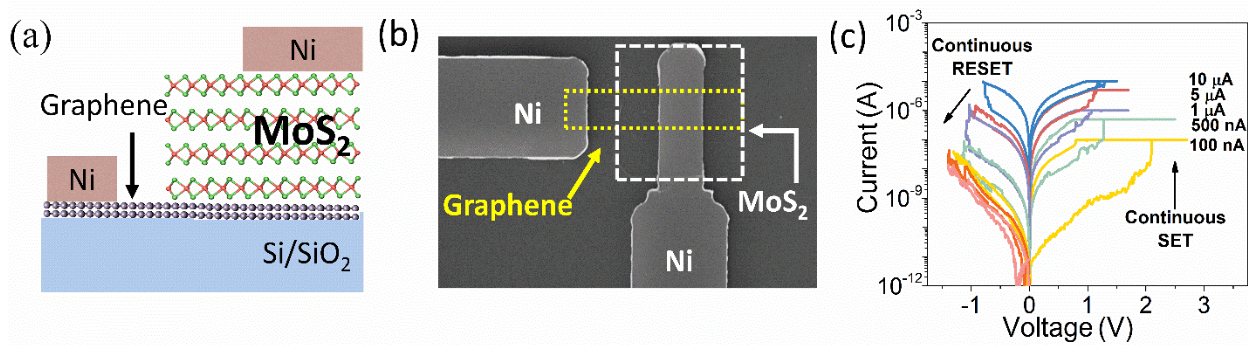


Figure 27: (a) Device schematic of the graphene/MoS2 memristor device (b) SEM image of the fabricated graphene/MoS_2 memristor device (c) DC *I-V* characteristics of the graphene/MoS_2 memristor device; SET- RESET process shows distinct conductance state of the device.

6.2.2 Au/MoS_2/Ti/Au Synapse Device

To realize the logic gates, the Au/MoS_2/Ag artificial neuron monolithically integrated with the Au/MoS_2/Ti/Au artificial synapse. **Figure 28a** shows the device schematic for the Au/MoS_2/Ti/Au memristor device. In this vertical device, the CVD grown ~9 nm MoS_2 layer stacked between top and bottom electrode of Au and performs as the active layer. This device shows distinct multiple conductance state during SET and RESET process like graphene/MoS_2 synapse device as shown in **Figure 28b**. Though this device has high OFF-state current, but it shows very low run to run and device to device variability. This exceptional characteristic makes the device superior for reliable and long-lasting applications.

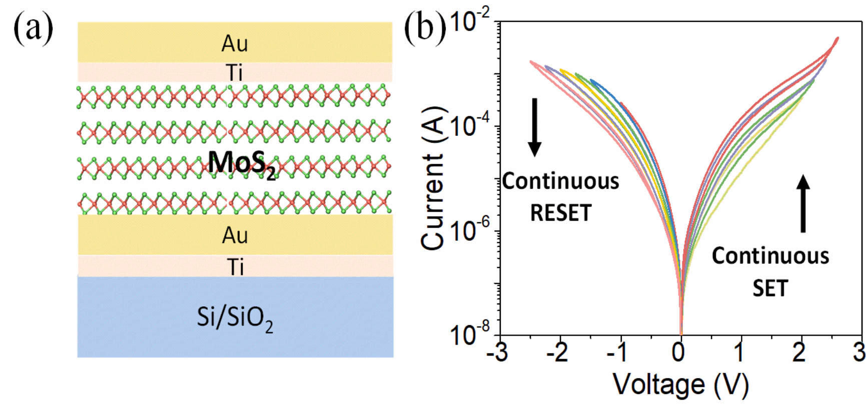


Figure 28: (a) Device schematic of the Au/MoS_2/Ti/Au memristor device (b) DC *I-V* characteristics of the Au/MoS_2/Ti/Au memristor device; continuous SET-RESET process shows multiple conductance state of the device.

6.3 Electrical Characterization Techniques

For the logic gate realizations, B1500A Semiconductor Device Parameter Analyzer, Tektronix AFG3022C function generator and Janis cryogenic probe-station is used. Like the artificial neuron measurement, the resistor and capacitor are connected to the external circuit. For the NOT gate realization, the input voltage pulse is fed to the circuit using the function generator while the bias input from the Waveform Generation/Measurement Unit (WGFMU)- 1 is connected to the bias resistor. On the other hand, for the AND & OR gate realization WGFMU-1 is used to feed the input voltage pulses and function generator is used for the bias input. The '0' input to the circuit realized by providing a negligible voltage pulse (10 mV) to the circuit from the function generator.

6.4 Results and Discussion

6.4.1 Single Layer Perceptron Realization

The viability of monolithic integration of the developed artificial neuron and synapse devices confirmed by the DC measurement of series connected Au/MoS_2/Ag and graphene/MoS_2 device. **Figure 29a** demonstrates two steps switching of the series connected devices while the positive bias is applied to the Au/MoS_2/Ag device terminal. The two steps switching is attributed to the different switching voltage of the neuron and synapse device. For the first cycle with 10 μA compliance, the switching observed at lower voltage is attributed to memristive switching of the neuron device while the synapse device switches around at 3.5 V. The subsequent cycles for different compliance current also follow the two steps switching. For all the three cycles, the first step switching at lower voltage start from the same OFF state current indicates the volatile characteristics of the Au/MoS_2/Ag neuron device. It is also clear from the **Figure 29a** that, synapse device preserves its non-volatility while connected with the neuron device. This measurement confirms that both artificial neuron and synapse device retain their intrinsic characteristics even after the integration.

The artificial neuron is realized by incorporating Au/MoS_2/Ag device with the *RC* circuit. The resistor in the *RC* circuit plays the role of synaptic weights of the neural network. For the monolithic integration, we replace the resistor with a graphene/MoS_2 synapse device as shown in the **Figure 29b**. While the resistor has a fixed value, for the synapse device we have the liberty to set the device at certain conductance state. For this measurement, the conductance of the synapse device set to 11.6 μS. To study the performance of the artificial neuron circuit, stream of pulses of a duration of 60 μs and an amplitude of 5 V applied to the input terminal and **Figure 29c** shows

the output current spike from the circuit. The tunability of the circuit verified by varying the pulse amplitude and pulse width of the input pulses. For different pulse amplitude and pulse width, **Figure 29d (i) & (ii)** shows the same trend of spiking frequency variation that we observed for artificial neuron realization. The synaptic weight of the connected synapse device is modulated, and the output spikes are observed for two different conductance state of the synapse device. **Figure 29d (iii)** delineates that, with increasing conductance state of the synapse device, the overall *RC* time constant of the circuit reduces, hence the circuit generates higher number output spikes.

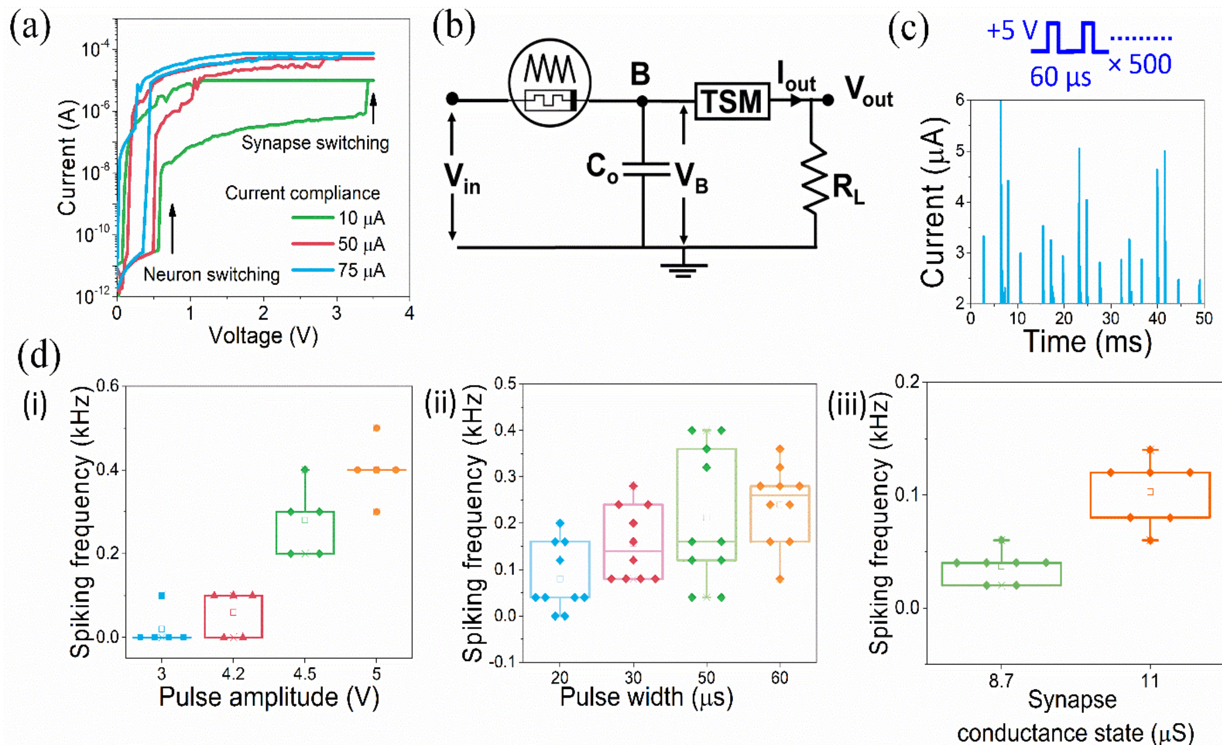


Figure 29: Monolithic integration of graphene/MoS_2 synapse and Au/MoS_2/Ag neuron device (a) DC *I-V* characteristics of the series connected Au/MoS_2/Ag and graphene/MoS_2 memristor device (b) Circuit diagram of the monolithically integrated artificial neuron circuit (c) Output current spikes from monolithically artificial neuron circuit for 5V input pulse train with 60 µs pulse width (d) Variation of the spiking frequency for (i) different pulse amplitude (ii) different pulse width (iii) different conductance state of the synapse.

The successful demonstration of the single layer perceptron with single synapse neuron leads us to the integration of three synapse devices with a single neuron device. **Figure 30a** depicts the schematic of the connection diagram for the integration. **Figure 30b** shows the optical image of the fabricated array of synapse devices connected with the single neuron device. The frequency of output current spiks are studied for the different combination of the conductance state of the synapse devices. The state of the synapse devices with conductance state < 10 µS is termed as low conductance state (LCS) and conductance state ≥ 10 µS is defined as high conductance state (HCS). State A, B, C and D corresponds to different set of conductance state of the connected three synapse devices. State A indicates the LCS for all three-synapse device, while state B corresponds to HCS for one device and LCS for others. For State C, two synapses are in HCS while one other is in LCS. All three synapses are in HCS for the State D.

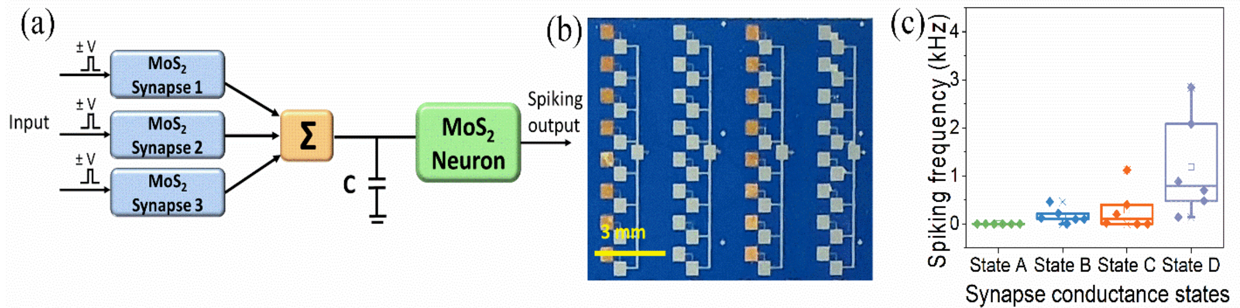


Figure 30: Integration of 3 MoS_2/graphene synapses with one Au/MoS_2/Ag neuron. (h): Optical image of chip showing multiple arrays of synapses connected to an neuron (c) Spiking frequency varies as input states of synapses changes.

The stream of voltage pulses with 3V and 50 µs pulse width applied to the circuit for State A, B, C D and the output current spikes are observed. **Figure 30C** shows the variation of output spiking frequency for four different states. It is clearly visible that, the state with more HCS synapse device generates more output current spikes as the combination offers less *RC* time constant. These results validate that the monolithic integration of the MoS_2/graphene synapses and

Au/MoS_2/Ag neuron is viable without the incorporation of any external circuitry for the current matching. Moreover, the tunability of the conductance and output current spikes enable its application in neural network for cognitive tasks.

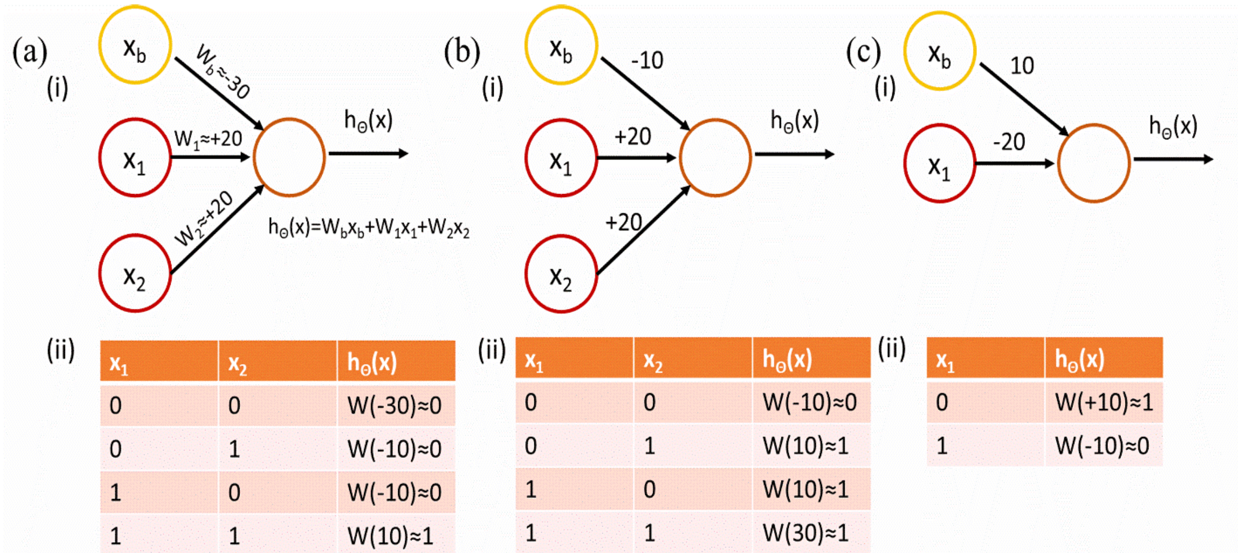
6.4.2 Logic Gate Realizations

In this monolithically integrated single layer perceptron, the synapse devices along with a bias resistor are connected to the single neuron device. The capacitor with the appropriate value is connected externally with the bias resistor to incorporate the RC circuit. The value of the bias resistor and the weight of the synapse is systematically modulated to obtain both the AND & OR gate with the same set of artificial synapses The NOT gate demands a single synapse and its weight also modulated to obtain the desire output. The schematic of single layer perceptron shown in **Figure 31** demonstrates the required combination of the wights to obtain the different gates. **Figure 31a (i)** indicates that for AND gate, the main input should have positive weighted connection while the bias input should have negatively weighted connection to the output neuron. The truth table shown in **Figure 31a (ii)** explains the resultant weight with different binary input to the single layer perceptron considering the output

$$h_{\Theta}(x) = W_b x_b + W_1 x_1 + W_2 x_2 \quad (19)$$

Where, W is the weight of the synapse and x is the input value either '1' or '0', x_1 and x_1 denotes main input and x_b is the bias input. The bias input x_b remains '1' for all the logic operation. Because of the higher negative weight for the bias input compare to the individual weight of the main input connections, the resultant weight becomes positive only when the perceptron receives '1' input for both the synapse. In this arrangement, the neuron should response or generate output

spikes only when it has positive weighted connections with the input and thus it will emulate a AND logic gate.



x_1	x_2	$h_\Theta(x)$
0	0	W(-30)≈0
0	1	W(-10)≈0
1	0	W(-10)≈0
1	1	W(10)≈1

x_1	x_2	$h_\Theta(x)$
0	0	W(-10)≈0
0	1	W(10)≈1
1	0	W(10)≈1
1	1	W(30)≈1

x_1	$h_\Theta(x)$
0	W(+10)≈1
1	W(-10)≈0

Figure 31: Logic gate realization (a) i) Schematic of single layer perceptron for AND gate realization; the weights (*w*)between input and output neuron are carefully chosen to obtain desired logical operations. ii) Truth table for AND gate (b) i) Schematic of single layer perceptron for OR gate realization ii) Truth table for OR gate (c) i) Schematic of single layer perceptron for NOT gate realization ii) Truth table for NOT gate

Figure 31b demonstrates the combination of weights in between the input and the output neuron connections for OR gate. Though the OR gate also requires positive weights for the main input connections and the negative weights for the bias input like AND gate, here the negative weight of the bias input is lower compare to the individual main input connections. Hence, the output neuron experiences positive weighted connections for all the combination of inputs except the “00” condition The positive weight activates the output neuron and causes the perceptron to behave like a OR gate.

The NOT gate has one main input and one bias input. **Figure 31c** shows, for the NOT gate the bias input has positive weighted connection to the output neuron. The larger negative weighted

connection of the main input to the output neuron causes the output neuron to activate only when it gets ‘0’ input.

Figure 32a shows the circuit diagram to realize the AND gate. Two synapses and one bias resistor are connected in series with the. output neuron. The synapses and bias resistor receive the input in the form of voltage pulses. The resistance value of the synapse and the bias resistor emulates the weight of the connection between the input and output neuron. Before the integration, the synapse devices are set to desired state. The lower the resistance of the synapse or bias resistor, the higher the weight of the respective connections. For AND gate realization, a resistor with 100 KΩ resistance is chosen as bias resistor. As mentioned earlier, the weight of the individual synapse should be lower than the bias resistor for realizing AND gate. Hence both the synapses are set to the higher resistance state of ~ 125-140 KΩ. **Figure 32b** shows the resistance state of the synapse devices for AND gate operation. To achieve the negative weight for the bias input, the negative voltage pulses of 0.7 V with 1 ms pulse width applied to bias resistor for all the operations. The bias resistor can be termed as differential resistor as negative current through this resistor initiates the differential operation in the circuit. To emulate ‘1’ input, voltage pulses of 0.7 V amplitude and 1ms pulse width fed to the synapse. The 10 mV voltage pulses with 1 ms pulse width applied to the synapse for ‘0’ input. When all the three input terminals receive voltage pulses the resultant current at node B is

$$I_B = I_1 + I_2 - I_b \tag{20}$$

The positive current at node *B* causes the accumulation of charges across the capacitor and build up the potential V_B. Like the LIF neuron operation, the output neuron turns ON once the V_B reaches the threshold value of the neuron device and generates the output spike. The spike from the output neuron indicates the output ‘1’ for AND gate and no spike is considered as ‘0’ output

Figure 32c demonstrates the output spikes from the neuron for different combinations of the input to the perceptron. For (00), (01) and (10) condition, the negative current plays dominant role because of higher weight of the bias resistor and causes no spike at the output which is shown in **Figure 32c (i) - (iii)**. For (11) input the combined weight of both the synapse cause positive current to node *B* and results output spikes as shown in **Figure 32c (iv)**. These operations are verified with multiple runs which is statistically depicted in the **Figure 32d**.

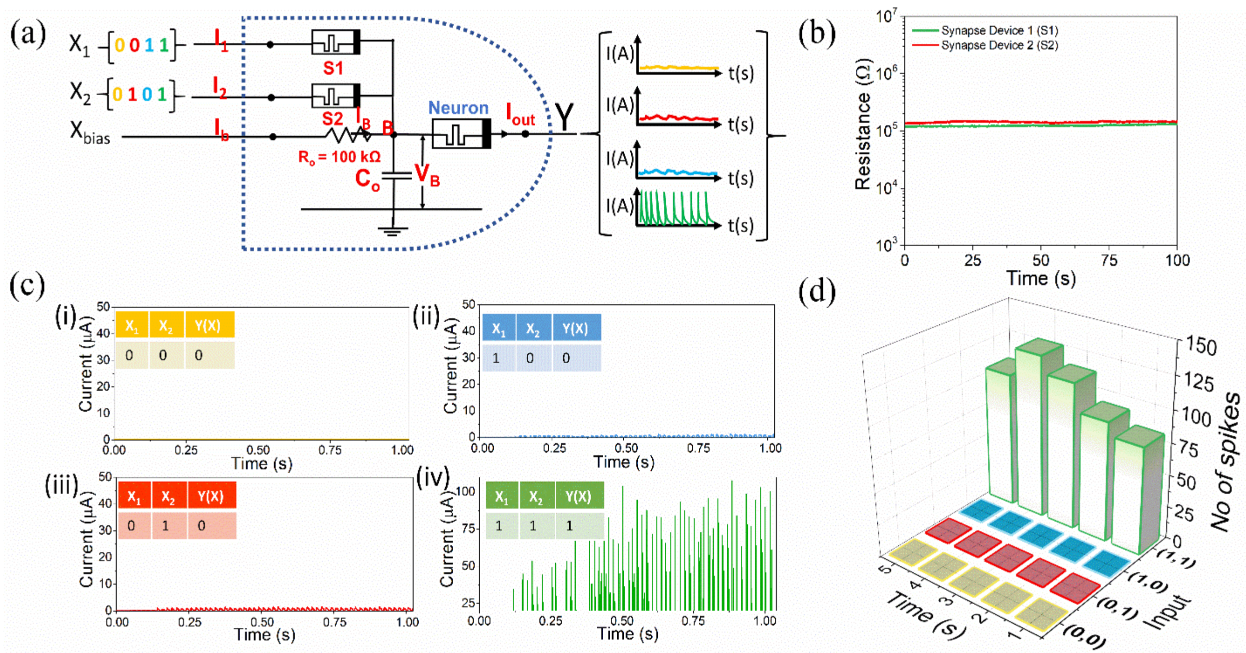


Figure 32: (a) Circuit diagram for AND gate realization (b) resistance state of the synapse device 1 and 2 for AND gate realization (c) output current spikes obtained for (i) 00 (ii) 10 (iii) 01 and (iv) 11 input to the AND gate (d) Output current spikes obtained for AND gate as a function of input and time.

Single layer perceptron with the same synapse and neuron devices is utilized to realize the OR gate. The circuit diagram for OR gate realization shown in **Figure 33a** is almost same as the AND gate. Only difference is the bias resistor with increased resistance of 470 KΩ. The increased value of the bias resistor emulates the lower weight require for OR gate realization. The resistance state of the synapse devices is kept low (~80-90 KΩ) to emulate the higher conductance state

compare to the bias connection as shown in **Figure 33b**. The bias input receives 0.7 V negative voltage pulses with 1ms pulse width for all the operations. With this arrangement, the node *B* only receives negative current while input to the synapses is (00); the neuron does not generate any spike at the output and satisfy the (0,0) condition of the OR gate (**Figure 33c(i)**). For all other combinations i.e. (01), (10) and (11) the node B gets positive current, and the circuit performs the normal LIF operations. Hence, the neuron generates the output currents spikes as shown in **Figure 33c(ii-iv)**. The statistical results shown in **Figure 33d** clearly indicates higher frequency of spikes for (11) condition compare to (01) and (10). (11) condition offers less equivalent resistance to the circuit because of parallel connection between the two synapses, hence reduce the *RC* time constant and results higher frequency of output spikes.

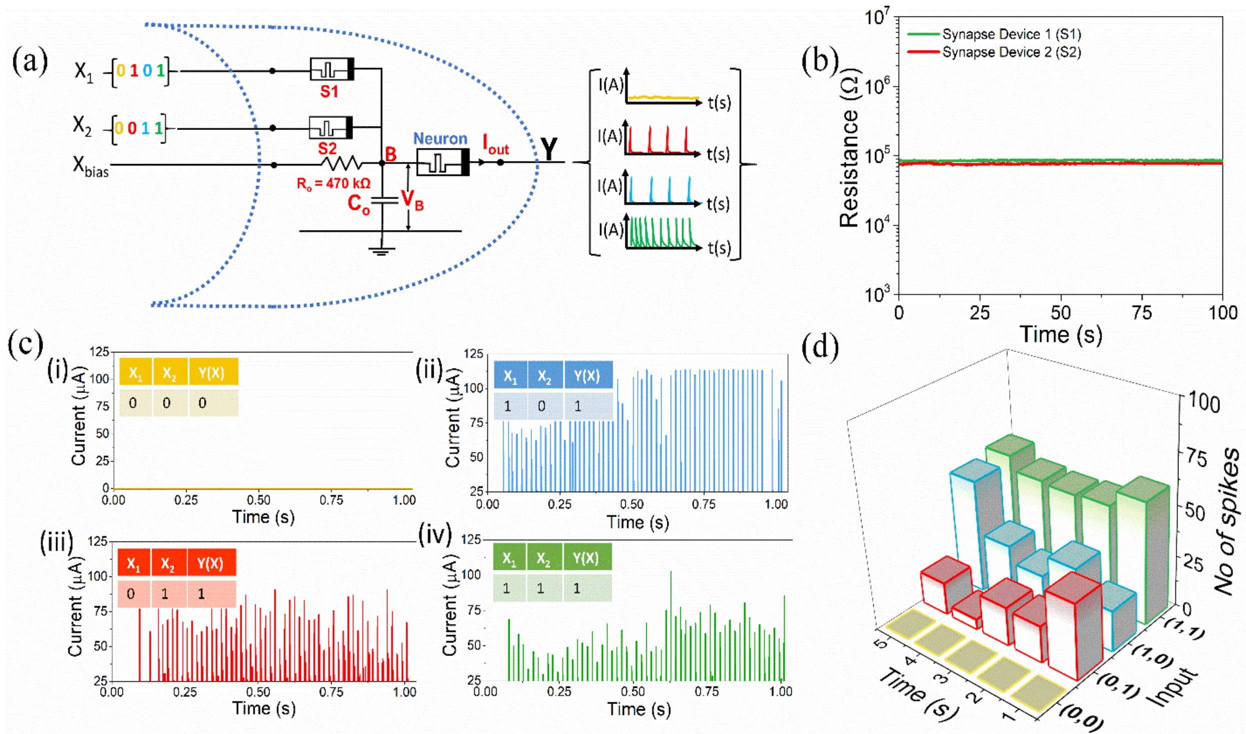


Figure 33: (a) Circuit diagram for OR gate realization (b) resistance state of the synapse device 1 and 2 for OR gate realization (c) output current spikes obtained for (i) 00 (ii) 10 (iii) 01 and (iv) 11 input to the OR gate (d) Output current spikes obtained for OR gate as a function of input and time.

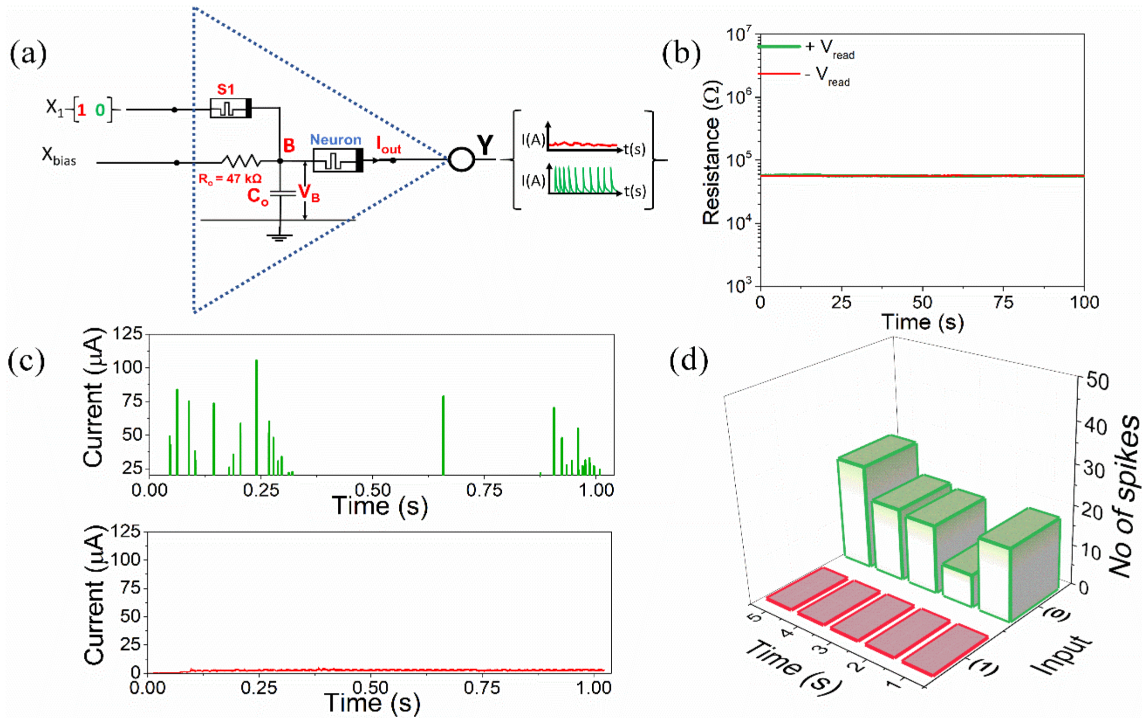


Figure 34: (a) Circuit diagram for NOT gate realization (b) resistance state of the synapse device for NOT gate realization at +0.7V and -0.7V(c) output current spikes obtained for (i) 0 and (ii) 1 input to the NOT gate (d) Output current spikes obtained for NOT gate as a function of input and time.

Figure34a demonstrates the circuit diagram for NOT gate realization. The circuit requires one synapse unlike AND & OR gate. Here the synapse instead of the bias resistor performs the differential function. **Figure 34b** shows the resistance state of the synapse device for both the positive and negative 0.7 V. For '0' condition the synapse receives 10 mV pulses with 1ms pulse width and for '1' condition the negative voltage pulse of 0.7 V with 1ms pulse is fed to the synapse. For both '0' and '1' condition, the bias resistor with 47 kΩ resistance receives positive train of pulses with 0.7 V amplitude and 1ms pulse width. Therefore with '0' input the current through the bias resistor plays dominant role and activates the output neuron to generate the current spikes. But during '1' operation the negative current through the synapse nullifies the current through bias resistor and inhibits the neuron from generating output spike. The output current spikes with the

‘0’ condition and no spikes for ‘1’ condition are demonstrated in the **Figure 34c(i) and (ii)**. The same results are shown for 5 s operation in the **Figure 34d**.

6.5 Conclusion

In conclusion, the MoS_2 based LIF neuron is successfully integrated with the two different synapse devices. The individual devices preserve their inherent electrical characteristic and demonstrates the ability of emulating the function of the neural network. The unprecedented demonstration of logic gates utilizing monolithically integrated MoS_2 synapses and neurons establishes the viability of these devices for future neuromorphic applications and edge computing.

CHAPTER 7 ARTIFICIAL NOCICEPTOR

The contents of this chapter have been published in: Dev, D., Shawkat, M.S., Krishnaprasad, A., Jung, Y. and Roy, T., 2020. Artificial nociceptor using 2D MoS_2 threshold switching memristor. IEEE Electron Device Letters, 41(9), pp.1440-1443.

7.1 Introduction

Nociceptor is a key receptor of human sensory system. **Fig. 35a** illustrates the function of a biological nociceptor. The peripheral terminal of the nociceptor receives noxious stimuli and generates a biochemical signal depending on the intensity, duration and recurrence of the stimuli to alert the central nervous system about potential danger. [126, 127] Unlike any other sensory receptor, the nociceptor shows “no adaptation” to noxious stimuli by not reducing its sensitivity to frequently experienced noxious stimuli. To protect an injured area, the nociceptor enhances its sensitivity by reducing its threshold for generating signals (allodynia) and by intensifying its signals (hyperalgesia). [128, 129]

With the rapid progress of artificial neural network (ANN) along with the improved artificial intelligence algorithm and outstanding locomotion system, humanoid robot is now more efficient than ever before. The application of humanoid robot is expanding from just research and entertainment platforms to more sophisticated jobs in industry, battlefield, disaster relief, space mission and so on. To perform reliably in forbidding environment, humanoid robots need to have highly sensitive sensory system. A reliable artificial nociceptor would enable humanoid robot to be responsive to any undesirable pressure, external forces, mechanical stress, temperature and toxic gas to function efficiently and increase the lifetime. Mimicking all the critical features of the

biological nociceptor system with the traditional CMOS based sensors would require elaborate circuitry and be power- extensive. [130, 131] The threshold switching characteristics of the TSM devices facilitates the realization of the artificial nociceptor as shown in the **Figure 35b.**

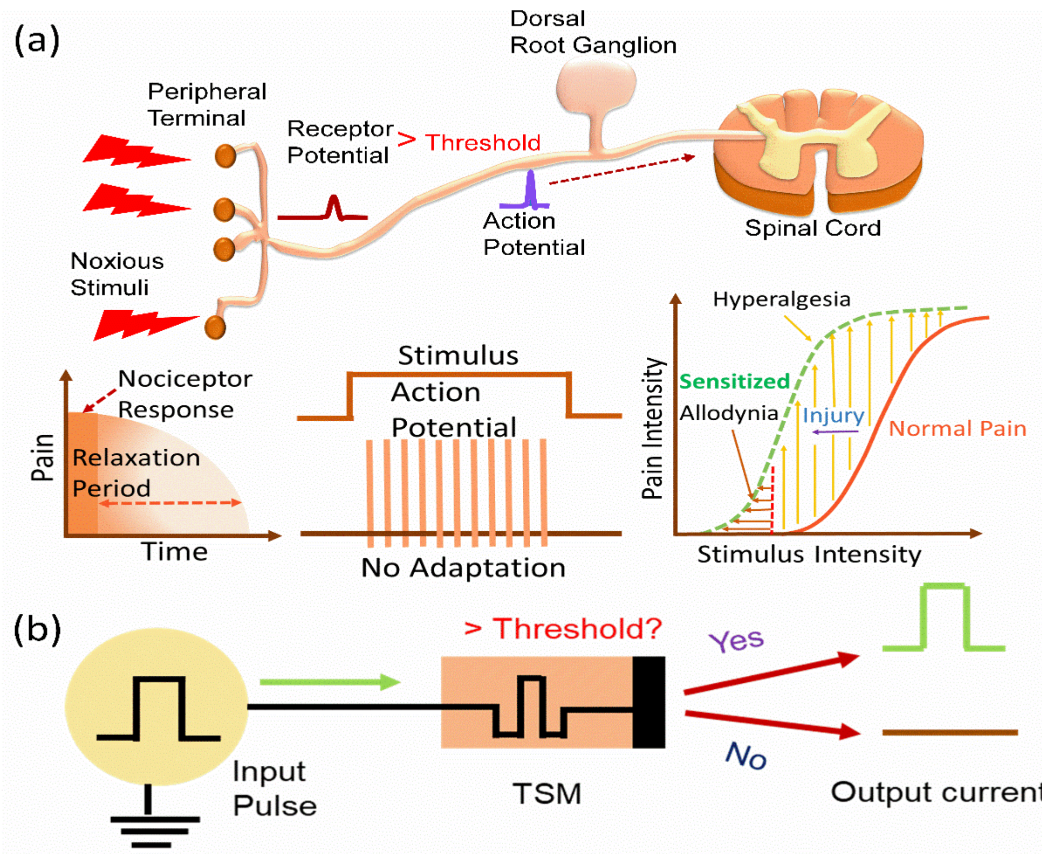


Figure 35: a) Schematic of biological nociceptor and its key features of threshold, relaxation, “no adaptation” and sensitization. (b) Block diagram of artificial nociceptor circuit realized with TSM device.

Recently, oxide-based memristors have been used to emulate the biological function of nociceptor. [115, 126, 132] Most of these reports show devices with a high threshold voltage and low ON-OFF ratio and require stimulus voltage pulses with extremely high amplitude and width to emulate the nociceptor actions, which is not suitable for energy efficient applications. [126, 132] The reliable and robust operation of the nociceptor in a forbidding environment demands a highly stable and energy efficient device. The 2D materials-based memristor devices holds promise for

such applications since they can withstand higher temperatures compared to the conventional oxide-based memristors. [27]

In this chapter, the recent works on memristor based artificial nociceptor are briefly discussed. Next, we report an artificial nociceptor realized with the same Au/MoS2/Ag TSM device that we used for artificial neuron realization. The Au/MoS_2/Ag TSM device does not require any external circuitry to realize an artificial nociceptor. The device exhibits threshold driven output response when subjected to voltage pulse trains of varying amplitude and width. In response to continuous voltage pulses, the TSM device demonstrates “no adaptation” characteristics of the biological nociceptor. When the device is stressed with voltage pulses much higher than its threshold value, the device successfully emulates the sensitization characteristics of the nociceptor and its output resembles the allodynia and hyperalgesia characteristics of the biological nociceptor.

7.1.1 Literature Review on Memristor Based Artificial Nociceptor

Y. Kim demonstrated nociceptive memristor using Pt/HfO_2/TiN device.[126] The charge trapping/detrapping to/from the traps in HfO_2 causes the memristive switching of the device. The memristive characteristics is utilized to demonstrate the threshold, relaxation, allodynia and hyperalgesia characteristics of the nociceptor. For the realization of the threshold characteristics of the nociceptor, the required pulse amplitude is as high as 6 V and pulse width 6.5 ms. The pulse ON-OFF ratio of the memristor device is ~10^4.

J. H. Yoon reported the artificial nociceptor based on diffusive memristor.[115] The memristor device has stacked structure of 30 nm Pt/10 nm SiO_x:Ag(11 at. %)/1 nm Ag/15 nm Pt.

The main characteristics of nociceptor like threshold, no adaptation, relaxation, sensitization are realized in this work.

M. Xiao utilized TiO_2 nanobelt device for the artificial nociceptor realization. [132] The voltage dependent volatile switching characteristics arise from dynamic electron trapping is exploited to demonstrate the artificial neuron. Though the single metal-oxide nanobelt device demonstrates the basic feature of the artificial nociceptor, the device requires high voltage (~7-10 V) and pulse width (50 ms) for the operation.

7.2 Results & Discussion

7.2.1 Artificial Nociceptor Realization

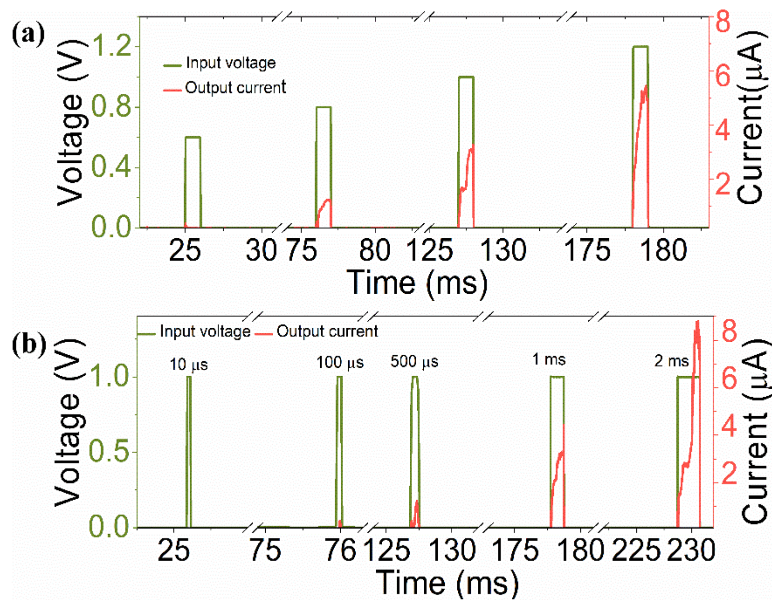


Figure 36: Threshold characteristics of Au/MoS_2/Ag artificial nociceptor (a)Output current of TSM based artificial nociceptor for input pulse amplitude varying from 0.6 to 1.2 V; pulse width is 1 ms for all pulses. The output current is observable only when pulse amplitude ≥ 0.8 V (b) Output current of artificial nociceptor with varying input pulse width of 10 μs, 100 μs, 500 μs, 1ms and 2 ms; pulse amplitude is held constant at 1 V for all pulses. Device responds to pulses of width ≥ 100 μs.

The threshold characteristics of the nociceptor is dependent on strength, duration and repetition of the incoming stimuli. To emulate these characteristics, the Au/MoS_2/Ag TSM device is fed with pulses of increasing amplitude (0.6 V to 1.2 V) with fixed pulse width of 1 ms. Due to the threshold-driven characteristics, the TSM device turns ON only when the pulse amplitude reaches 0.8 V, as depicted in **Figure 36a**. Once the device turns ON, the output current increases for any further increase of pulse amplitude, which implies the increasing responsivity of the nociceptor with intensified noxious stimuli. Pulses with varying pulse width (10 µs to 2 ms) and constant pulse amplitude of 1 V are also applied to the device to demonstrate the threshold-driven characteristics of the TSM device. From **Figure 36b**, it is clear that the device turns ON only after the pulse width reaches 100 µs, and the output current increases for further increase in pulse width. For both varying pulse width and varying pulse amplitude measurements, the interval between the pulses is carefully chosen to be 50 ms, so that device can get relaxed and return to its HRS.

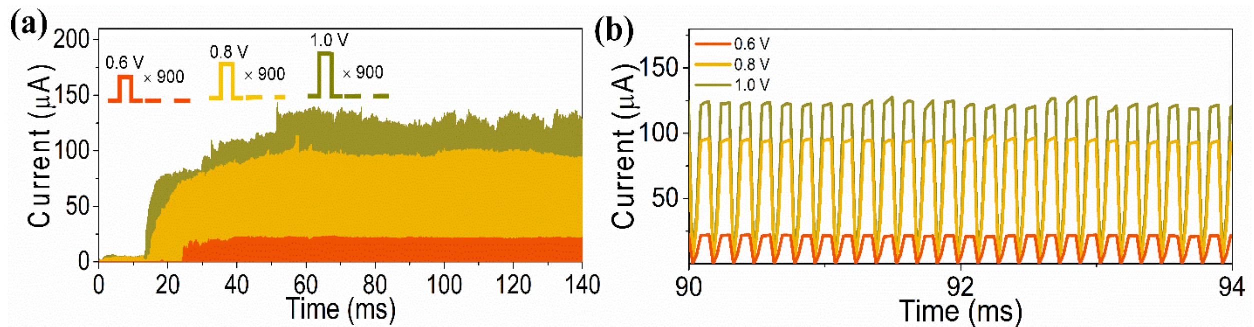


Figure 37: "No adaptation" property of Au/MoS_2/Ag artificial nociceptor (a) Output current response for pulse trains of varying pulse amplitudes of 0.6 V, 0.8 V and 1.0 V; device turns on within a shorter time period for higher voltage amplitudes (24 ms for 0.6 V, 14.5 ms for 0.8 V and 13.3 ms for 1.0 V). Once the device turns on, it maintains the same current level for additional incoming pulses. These characteristics mimic the "no adaptation" property of a biological nociceptor. (b) Zoomed in image of **Figure 5a**. Output current response of artificial nociceptor for pulse train with different amplitude.

To investigate the device's response to continuous pulses, a pulse train of varying voltage amplitudes with 100 µs pulse width and 50 µs pulse interval are applied to the device. **Figure 37a**

shows that the number of pulses required to turn the device ON depends on the voltage amplitude of the pulse. The higher the pulse amplitude, the lower the pulse number required to turn the device ON, which implies that the nociceptor will respond faster to stronger stimuli. **Figure 37a** also demonstrates that once the TSM device turns ON, it maintains the current level for additional pulses without any degradation (zoomed in current output is shown in **Figure 37b**). This behavior is a clear indication of the "no adaptation" characteristics of a biological nociceptor followed by our device.

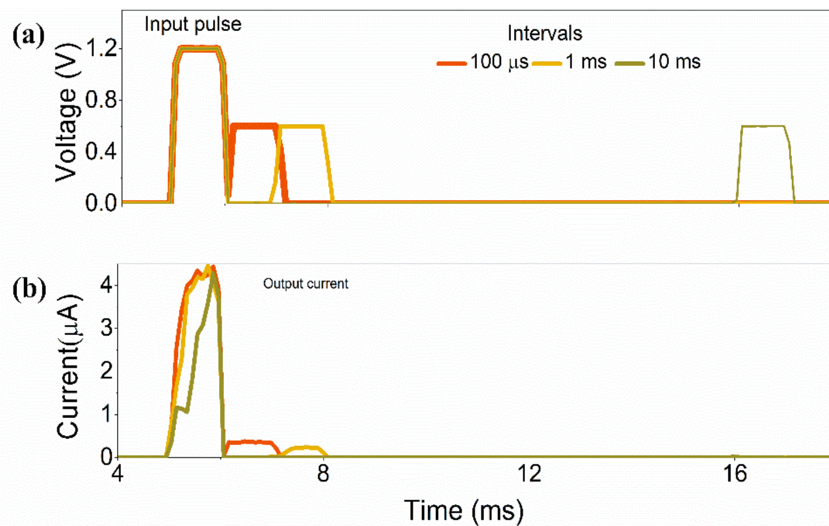


Figure 38: Demonstration of relaxation process of artificial nociceptor: (a) Input voltage pulse of 1.2 V is followed by a 0.6 V pulse with varying interval of 100 μs, 1 ms and 2 ms. (b) Output currents are recorded for both input pulses. The device responds to 0.6 V for shorter intervals of 100 μs and 1 ms between two input pulses. At higher interval of 10 ms, device gets relaxed and does not respond to 0.6 V pulse.

After experiencing a noxious stimulus, the biological nociceptor remains more sensitive for a certain period known as the relaxation period. Within this period, the nociceptor responds to noxious stimuli even if they are lower than the threshold value and alerts the central nervous system. To emulate this sensitivity, two pulses of 1.2 V and 0.6 V with 1 ms pulse width are applied at different intervals as shown in **Figure 38a**. It is observed from **Figure 38b,** for the lower pulse

interval, the TSM device responds to the 0.6 V pulse even though it is below the threshold value. As the interval is extended to 10 ms, the device does not respond to pulses of 0.6 V amplitude any more, which implies that the device is completely relaxed.

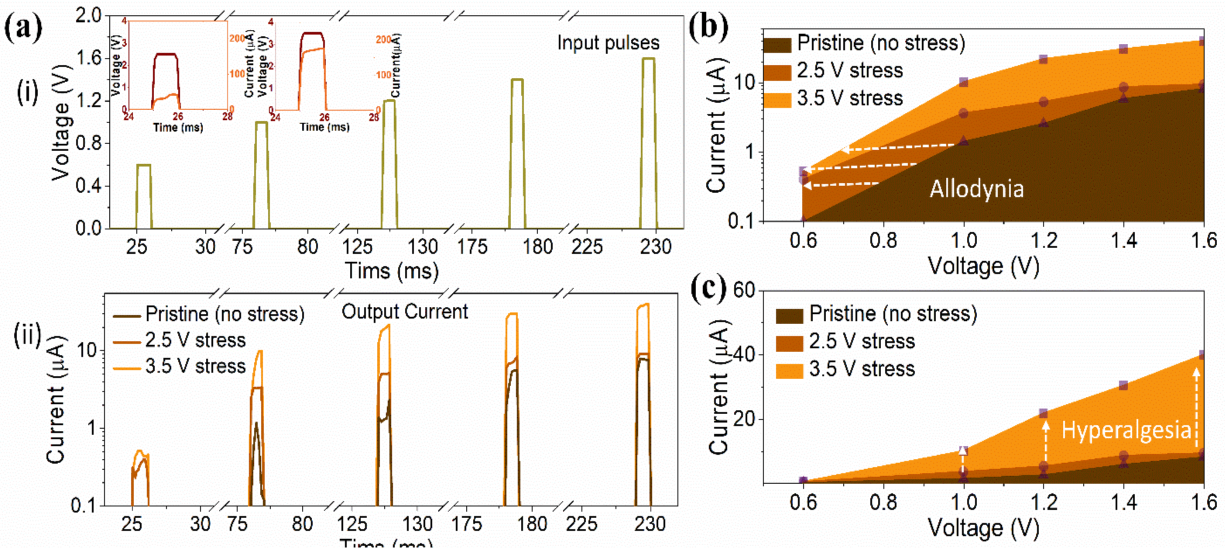


Figure 39: Sensitization properties of artificial nociceptor (a) i) a train of pulses with increasing pulse amplitude of 0.6 V, 1V, 1.2 V and 1.6 V, and 1 ms pulse width is applied to device at pristine condition and stressed condition. Device is stressed by applying a single pulse of 2.5 V and 3.5 V with pulse width 1 ms (input and output shown in inset). ii) Output current in response to pulse train at pristine and injured conditions of 2.5 V stress and 3.5 V stress. (b) Output currents obtained for pulse train at pristine and injured condition are plotted in log scale. The shift of threshold voltage towards lower values implies allodynia characteristics of nociceptor. (c) Output currents obtained for pulse train at pristine and injured condition are plotted in linear scale. The increase of current at injured condition implies hyperalgesia characteristics of nociceptor.

Sensitization is another important characteristic of the biological nociceptor. For an injured tissue, the nociceptor responds with lower threshold and higher intensity. For replicating the injury condition, a pristine TSM device is stressed with pulses of much higher amplitude (first at 2.5 V, then at 3.5 V) than normal threshold value. The inset of **Figure 39a(i)** shows the output current response of the TSM device in response to single stress pulses of amplitude 2.5 V and 3.5 V. A pulse train of increasing amplitude is applied to the pristine device (no stress) and then after stressing the device at 2.5 V and 3.5 V, as shown in **Figure 39a(i)**. **Figure 39a(ii)** indicates that,

while the pristine device shows a threshold at 0.8 V, the threshold reduces to 0.6 V for the stressed conditions. For subsequent voltage pulses of amplitudes 1 V, 1.2 V, 1.4 V and 1.6 V, the stressed devices exhibit higher currents compared to the pristine device. **Figure 39b** shows the output currents at pristine and stressed condition in log scale. The shift of the threshold towards lower voltage after stress implies the allodynia characteristics of the nociceptor. The increasing current output for stressed devices shown in **Figure 39c** emulates the hyperalgesia nature of the nociceptor.

7.3 Conclusion

In conclusion, we have used the threshold switching characteristics of a large area CVD-grown 2D MoS_2 based Au/MoS_2/Ag memristor device to emulate the key features of threshold, "no adaptation", relaxation and sensitization of a biological nociceptor. The device successfully emulates the allodynia and hyperalgesia characteristics of the biological nociceptor when stressed. This work shows the application of lightweight 2D materials in improving the sensory functionalities of a humanoid robot.

CHAPTER 8 SUMMARY AND FUTURE PERSPECTIVES

8.1 Summary

In summary, this dissertation has explored the potentiality of the 2D MoS_2 for the next generation logic and neuromorphic computing devices. In this work a comprehensive study has been carried out to determine the high quality 2D/high-κ interface. For the study, MoS_2 FET is fabricated using two different high-κ gate dielectric Al_2O_3 and ZrO_2. The challenges of uniform growth of the gate dielectric over the MoS_2 is overcome by evaporating the nucleation layer prior to the deposition of the high κ gate dielectric by ALD. Two different interface trap density extraction methods are adopted to quantify the interface trap density Both the SS and conductance method confirm the superior quality of the MoS_2/Al_2O_3 interface while AlO_x is used as the nucleation layer. The high quality 2D/high-κ interface extending the promise of 2D materials for future high-performance electronics and optoelectronics devices.

In this work, the CVD grown MoS_2 is implemented to develop a reliable TSM device with Ag top electrode and Au bottom electrode. The device demonstrates low threshold voltage, high ON-OFF ratio, sharp switching and high endurance. The mechanism study through electrical characterization proves that, the threshold switching is attributed to the Ag diffusion through the MoS_2. The reliable performance of the MoS2 based TSM motivated us to implement it for realizing the artificial LIF neuron. The TSM device is integrated with the *RC* circuit to demonstrate all the critical functions of the artificial neuron.

The successful implementation of the artificial neuron motivated us to integrate the artificial neuron with our own graphene/MoS_2 and Au/MoS_2/Ti/Au synapse device. The single layer perceptron realized by integrating the Au/MoS_2/Ag LIF neuron and graphene/MoS_2 synapse

demonstrates the viability of our developed neuron for neural network. In this single layer perceptron, the artificial neuron responds according to the synaptic weight of the connected synapses and generates the output spike. Boolean logic gates AND, OR and NOT gates are realized through the monolithic integration of the Au/MoS_2/Ag LIF neuron and Au/MoS_2/Ti/Au synapse. The efficient implementation of the logic gates with a single neuron for the multiple synaptic inputs indicates the potentiality of energy efficient logic operations for the future computing technology.

In this work, the application of the Au/MoS_2/Ag extended further by realizing an artificial nociceptor. The single TSM device emulates the threshold, "no adaptation" relaxation and sensitization characteristics of the biological nociceptor. This demonstration bolsters the confidence on Au/MoS_2/Ag TSM device for utilizing as a sensing module for the sensory system of the humanoid robot.

8.2 Future Perspectives

This dissertation successfully developed reliable and robust 2D MoS_2 based artificial neuron and implemented for the integration with the MoS_2 based synapse. Our demonstration of monolithic integration establishes the viability of our developed device for the large-scale neural network. To advance this field, the monolithic integration should be realized with crossbar structure for pattern or image recognition. The approach would reveal more challenges on the way of developing a 2D MoS_2 based large neural network. At this point, the successful implementation of the crossbar architecture of 2D MoS_2 based neuromorphic devices is mainly dependent on the reliable characteristics of the individual devices. In the crossbar structure IR drop and sneak path

are two important performance deteriorating factor. Increasing the thickness of interconnect metal would improve the IR drop and proper biasing would help to get rid of the sneak path.

The realization of artificial nociceptor with 2D MoS_2-based single TSM device will further the field of 2D neuromorphic devices by allowing compact, scalable, ultra-light and energy-efficient sensory system, perfect for the large-scale deployment of humanoid robots. The implementation of artificial nociceptor with neuromorphic hardware would enable modeling human body experience in humanoid robots more faithfully.

To keep pace with the rapid transition towards the flexible and wearable platform, the Au/MoS_2/Ag TSM device should be realized over flexible substrate. The choice of the compatible flexible substrate, performance analysis of the TSM device at maximum deformation, evaluation of scalability for neural network implementation are the key steps towards realizing the 2D TSM device on flexible platform.

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