

1 AMIGA at the Pierre Auger Observatory: The
2 interface and control electronics of the first prototype
3 muon counters

4 M. Videla^a, M. Platino^a, B. García^{b,c}, A. Almela^a, G. de la Vega^b, A.
5 Lucero^a, F. Suarez^a, O. Wainberg^a, F. Sanchez^a, D. Yelos^b

6 ^a*Instituto de Tecnologías en Detección de Astropartículas (CNEA, CONICET, UNSAM)*
7 *Centro Atómico Constituyentes, Avda. Gral. Paz 1499 (1650) San Martín, Pcia. de*
8 *Buenos Aires, Argentina*

9 ^b*Instituto de Tecnologías en Detección y Astropartículas, (CNEA, CONICET, UNSAM)*
10 *Regional Cuyo, Azopardo 313 (5501) Godoy Cruz, Pcia. de Mendoza, Argentina*

11 ^c*Universidad Tecnológica Nacional. Facultad Regional Mendoza*
12 *Rodríguez 273, Ciudad Mendoza, CP (M5502AJE), Argentina*

13 **Abstract**

AMIGA is an enhancement of the Pierre Auger Observatory. The main goals of AMIGA are to extend the full efficiency range to lower energies of the Observatory and to measure the muon content of extensive air showers. Currently, it consists of 61 detector pairs, each one composed of a surface water-Cherenkov detector and a buried muon counter. Prototypes of the muon counter - buried at a depth of 2.25 m - were installed at each vertex of a hexagon and at its center with 750 m spacing. Each prototype has a detection area of 10 m² segmented in 64 scintillation strips and coupled to a multi-anode PMT through optical fibers. The electronic systems of these prototypes are accessible via a service tube. An electronics interface and control board were designed to extract the data from the counter and to provide a remote control of the system. This article presents the design of the interface and control board and the results and performance during the first AMIGA acquisition period in 2012.

14 *Keywords:* Underground Detector, Segmented Scintillators, Data handling,
15 Detector control systems, Data acquisition concepts

Email addresses: mariela.videla@iteda.cnea.gov.ar (M. Videla),
manuel.platino@iteda.cnea.gov.ar (M. Platino)

16 1. Introduction

17 The Pierre Auger Observatory, optimized for the highest energies of the
18 cosmic ray spectrum, has already studied two cosmic ray spectral features: the
19 ankle and the GZK-cutoff [1][2][3]. However, the cosmic ray energy spectrum has
20 two other observed features at lower energies where the spectral index changes:
21 the knee ($\approx 8 \times 10^{15}$ eV) and a second knee ($\approx 8 \times 10^{16}$ eV)[4]. The transition
22 from galactic to extragalactic sources is supposed to occur according to models
23 is either in the region near the second knee or along the ankle [5][6][7]. A
24 way to identify this transition would be to measure a change in the cosmic
25 ray composition from dominant heavy primaries to either a mixed or a light-
26 dominated composition. Although galactic magnetic fields deflect the particle
27 trajectories, making it impossible to identify the sources in the range of the knee
28 and second knee, composition studies should help to discriminate whether the
29 sources are galactic or extragalactic, and where the transition occurs.

30 The Pierre Auger Observatory has two kinds of detectors, water-Cherenkov
31 detectors and fluorescence telescopes. Enhancements to the Observatory lower
32 the full efficiency range down to the second knee. The fluorescence telescope
33 enhancement is called the High Elevation Auger Telescopes (HEAT)[8]. Addi-
34 tionally the surface detector enhancements consist of an infilled area of standard
35 water-Cherenkov detectors deployed in a triangular grid of 750 m spacing, each
36 with an associated muon counter. This latter enhancement is called Auger Muon
37 Infill for the Ground Array (AMIGA).

38 Prototypes of the muon counter were developed and installed in an area
39 designated as the Pre-Unitary Cell (Figure 1). These prototypes consist of a
40 10 m^2 scintillation detector segmented in 64 strips. Each strip is 400 cm long,
41 4.1 cm wide and 1 cm thick and made out of extruded polystyrene doped with
42 fluorine and co-extruded with a TiO_2 reflective coating. Strips are placed in
43 two groups of 32 at each side of a central dome where the photomultiplier
44 and electronics are located. Saint-Gobain 1.2 mm diameter optical wavelength-
45 shifting fibers are attached with optical cement to the strips in a groove along the

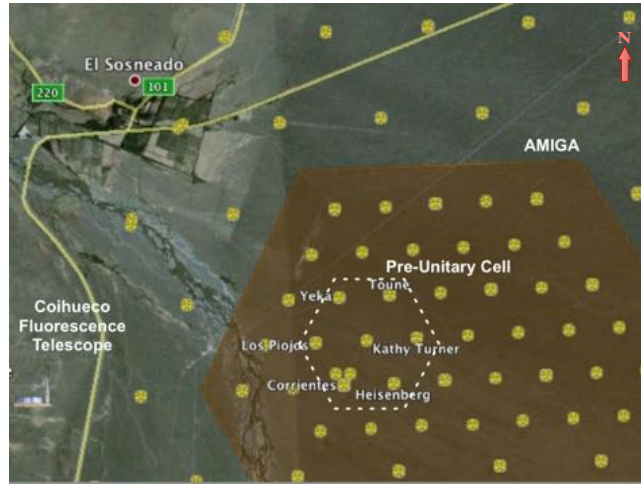


Figure 1: Map of the area for deployment of AMIGA muon counters (brown color). The dotted line encloses the hexagonal array where pairs of water-cherenkov and muon counters have been installed for first prototype tests. The Coihueco fluorescence telescopes and the HEAT extension are located about 5 km to the west.



Figure 2: Two muon counters in the laboratory without their top PVC cover. In the middle of the counters are the ends of the 64 optical fibers and the connector to couple the fiber ends to the PMT.

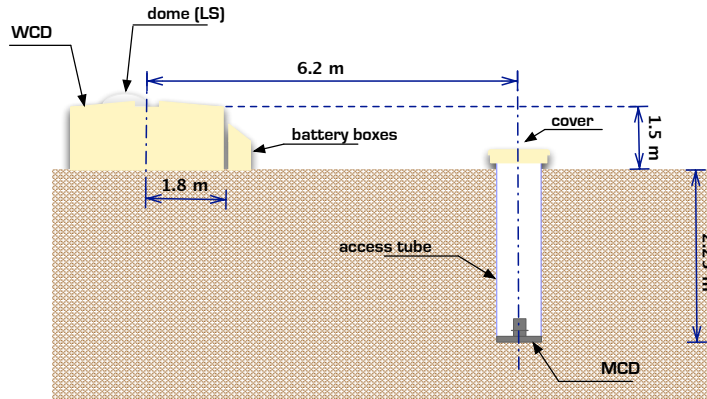


Figure 3: Cross-section of the water-Cherenkov detector (WCD) and the muon counter (MCD) on site.

46 strips. The fibers end at an optical connector, which is attached and aligned to
 47 a 64 channel multi-anode photomultiplier tube (PMT) H8804 with $2\text{ mm} \times 2\text{ mm}$
 48 pixels (Figure 2).

49 To avoid contamination from the electromagnetic component of the shower,
 50 the modules are buried underground at a depth of 2.25 m (equivalent to $540\text{ g}/$
 51 cm^2 of mass overburden of the site soil).

52 The shielding of the soil imposes a threshold of around 920 MeV [9] for vertical
 53 muons and assures negligible electronic contamination because it contains more
 54 than $20X_0$ (where X_0 is the radiation length).

55 As a consequence of the installation of the counters underground, the elec-
 56 tronics is split into two components: the underground electronics, which is
 57 integrated into the buried muon counter modules and accessible through a ser-
 58 vice tube, and the surface electronics placed next to the electronics of the water
 59 Cherenkov Detector (WCD) (see Figure 3).

60 The underground electronics includes a 64-pixel PMT, an analog front-end,
 61 an FPGA, the interface and control board and a power distribution board (Fig-
 62 ure 4). The front-end includes a high voltage power supply, a PMT socket and
 63 two low drop-out linear regulators to power the amplifiers for the 64 analog
 64 channels of the front end. The power distribution board has separate switching

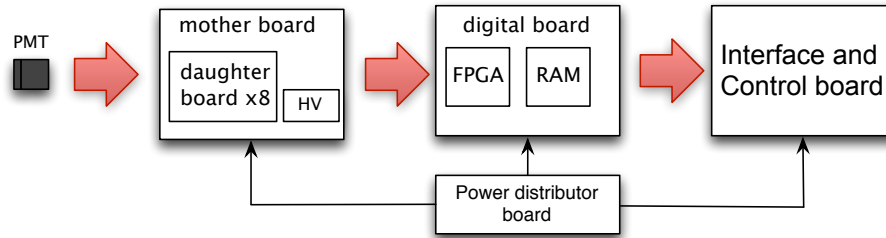


Figure 4: The set of boards implemented in the muon counter that are accessible via the service tube. The prototype version of the electronics is split into a motherboard (plus daughter cards), a digital board, an interface and control board and a power distribution board. The final design will integrate the electronics into only two boards: a front-end and a digital acquisition board.

65 power supplies to feed the complete set of boards. The electrical ground of both
 66 the buried and the surface electronics is decoupled by floating power supplies
 67 to avoid ground loops and noise.

68 The output currents of the PMT are converted into voltage pulses and com-
 69 pared with a threshold level. The threshold level can be set individually for each
 70 channel by a 12 bit digital-to-analog converter (DAC). Below threshold level,
 71 the digital output signal is set to one, while above threshold, the signal is set
 72 to zero (inverted logic). The DAC can be programmed by a serial peripheral
 73 interface (SPI).

74 At each trigger, 256 words (64 bits length) from a circular buffer are cap-
 75 tured and stored together with additional 512 words from a linear buffer into
 76 an external RAM memory. Each time data are requested, the external RAM
 77 memory content is transferred to the interface microcontroller (μ C) by a parallel
 78 bus.

79 The mean power consumption of the underground electronics including the
 80 interface and control board is 5.28 W with a peak around 5.52 W.

81 The surface electronics of the muon counter is located inside the dome of the
 82 water-Cherenkov detector. It has two main components: a wireless communi-
 83 cation system (TS7260 Single Board Computer from Technologic Systems) and

84 synchronization hardware connected to the electronics of the water-Cherenkov
85 detector. Additionally, a TSCAN1 board from Technologic System was added
86 to implement a CAN bus in the counter to handle the data stream between
87 underground and surface electronics.

88 **2. Trigger and acquisition modes**

89 The muon counter can use either an external trigger signal provided by
90 the water-Cherenkov detector or a stand-alone trigger (a coincidence trigger
91 generated with the coincidence of one or more channels). In external trigger
92 mode, the underground electronics receives a trigger pulse (T1[10]) and a local
93 timestamp from the electronics of the water-Cherenkov detector (Local Station
94 or LS). Meanwhile the surface electronics receives a GPS timestamp with the
95 local timestamp from the Local Station. The GPS timestamps and the local
96 timestamps are transmitted from the LS to the Single Board Computer (SBC).
97 Thus, each event recorded by the muon counter is synchronized with the water-
98 Cherenkov detector event at T1 level. The latency between the local timestamp
99 and the trigger of the underground electronics is a fixed number given by the
100 delay of the T1 pulse through the cable between the LS and the underground
101 electronics (about a few 10 ns). For the muon counter there is no latency between
102 the GPS timestamp and the local timestamp since they are transmitted at the
103 same time from the LS to the SBC.

104 The memory size of the underground electronics is designed to store 2048
105 events. At an average T1 trigger rate of 100 Hz this corresponds to a storage
106 time of about 20 seconds.

107 The counter can be programmed with three acquisition modes implemented
108 in the interface and control board: stand-alone trigger, an external trigger and
109 a calibration trigger. In stand-alone trigger mode, the trigger condition is the
110 presence of a signal in specific channels. The aim of this acquisition mode is to
111 record the trigger rate of a channel or group of channels given a known threshold
112 level and PMT voltage.

113 The external trigger mode is used to store the signal traces when a T1 signal
114 is received by the counter. In the first counter prototypes, the traces have $9.6\ \mu\text{s}$
115 length with a trigger point at $3\ \mu\text{s}$. Each event is a collection of 768 words of 64
116 bits corresponding to the 64 detector channels stored at 80 MHz.

117 All the T1 events are stored locally in the underground electronics until
118 a T3[10] is received from the Central Data Acquisition (CDAS) of the Pierre
119 Auger Observatory.

120 In calibration mode, the counter operates in stand-alone trigger mode but
121 the threshold level is swept over a range to record the threshold dependent
122 trigger rate per channel. In this case the recorded data are rates and traces.
123 The main goal of this trigger mode is to record the threshold level at a given
124 rate. The data readout in calibration mode is done by programming a fixed
125 acquisition time. The counter records data for the selected time period and
126 then transfers the data to the SBC. The main difference between the external
127 trigger and the other two modes is that with the external trigger the counter
128 has to work in real time. Therefore, in external trigger mode the event data
129 transfer from the underground to the surface electronics has to be faster than
130 the T3 rate in order to avoid data losses.

131 **3. Interface and control board design**

132 The acquisition modes described above define the main interface and control
133 board design requirements. These requirements are described below.

- 134 • Physical line: A 20 m cable length (Figure 3) is needed because the mini-
135 mum distance between the water-Cherenkov detector and the underground
136 electronics is about 12 m and we added an extra 8 m to have enough flex-
137 ibility during cabling or land preparation. The transceiver in the under-
138 ground electronics must work with 3.3 V and the transceiver in the surface
139 electronics must work with 5 V due to compatibility reasons between the
140 underground and surface electronics. There are 6 physical lines: two lines
141 for data, two lines for triggering and two lines for power.

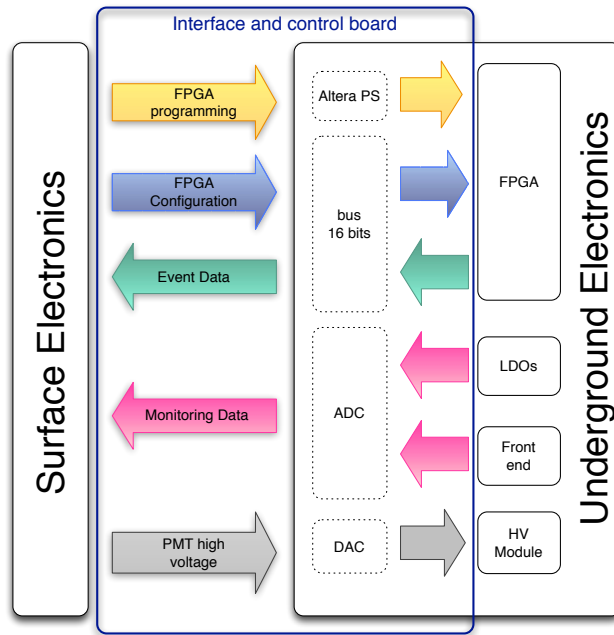


Figure 5: Functional blocks and data flow of the interface and control board. The design of the interface and control board met the acquisition requirements.

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- Event transfer rate: The raw event size is 6 kB. The T3 event rate was measured to be 150 events per day (peak value) during a test period of six months. However, the maximum payload occurs while working in calibration mode. This is not real time. The payload in calibration mode depends on threshold levels and acquisition period (i.e. if the threshold level is set below the noise level and the acquisition period is too large, the event rate will be too high). The external memories of the FPGA can only store 2048 events. In this case 1 MB has to be transferred, but there is no time constraint since the counter is working off line.
 - FPGA programming: This task has to be done each time the system is powered up or in case a new upgrade of the FPGA code is ready to be downloaded. The programming has to be done through a serial connection using the passive serial protocol from Altera.

- 155 • FPGA configuration and data handling: FPGA configuration and data
156 request handshake is defined by a 16 bit parallel bus and an 8 bit address
157 bus (with three control signals). A parallel bus was selected to map the
158 FPGA registers in the μC memory. In this way any access from the μC to
159 the FPGA is done using standard read and write transactions. The final
160 design will have a 16 bit address bus.
- 161 • Slow control: The board has to include a DAC to set the PMT with a
162 gain of 7.7×10^6 (which corresponds to 950 V) and it has to be monitored.
- 163 • Monitoring: The regulator outputs from the motherboard and the digital
164 board have to be monitored to detect any failure during acquisition. Also
165 the PMT and interface temperatures have to be acquired for the same
166 reason. Additionally, the lines coming from the motherboard have to be
167 isolated from the interface and control board ground.

168 The functionality of the interface and control board is not integrated in the
169 digital board at the prototype stage to allow for parallel development. In the
170 final version, however, all the analog boards will be integrated in a single front-
171 end. Also, all the digital boards will be integrated into a single acquisition
172 board.

173 The interface and control board design provides a solution to the require-
174 ments: the communication between the underground and the surface electronics,
175 the monitoring and the control of the underground electronics and as an inter-
176 face for the automatic processes implemented in the SBC at the surface (Figure
177 5).

178 One of the main design criteria was to include the minimum amount of
179 hardware and to use standard communication protocols. The core of this board
180 is a 32 bit ARM (TMS470) μC from Texas Instruments running at 20 MHz.
181 An ARM architecture microprocessor was selected because of its low current
182 consumption (110 mA@24MHZ). The schematic in Figure 6 shows the modules
183 programmed in the μC . The communication between the underground and the

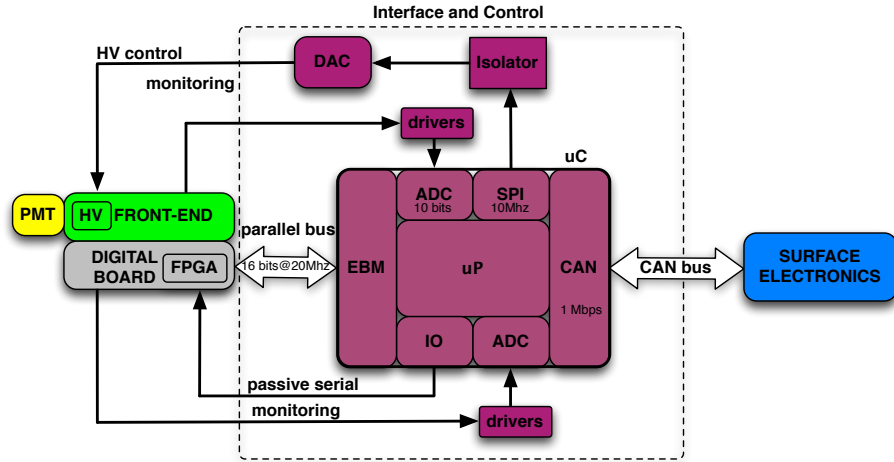


Figure 6: The microcontroller (μC) is in charge of multiplexing data to its corresponding modules. A CAN link between the underground and surface electronics is accomplished by an built-in CAN module.

184 surface electronics is accomplished by a built-in CAN module because of its low
 185 power consumption and its standard protocol. The data received through the
 186 CAN bus are multiplexed to the corresponding modules.

187 3.1. Physical line: CAN bus

188 Two constraints related to the maximum length of the physical line were
 189 analyzed for the design of the CAN bus: the round-trip delay and the amplitude
 190 bit drop, which is the amplitude drop of the analog signals corresponding to
 191 one bit. The round-trip delay (RTD) is a critical parameter of the CAN bus
 192 concept because the CAN protocol uses a bit-wise arbitration to select which
 193 node should continue signalling. Thus the bus length is limited by RTD to avoid
 194 bit corruption due to delayed bits being sensed by other nodes. The round-trip
 195 delay was calculated for the selected design (Figure 7). As conservative estimate
 196 we assume a delay of 215 ns.

197 Using the equation

$$t_{RTD} = \frac{1}{baudrate} \quad (1)$$

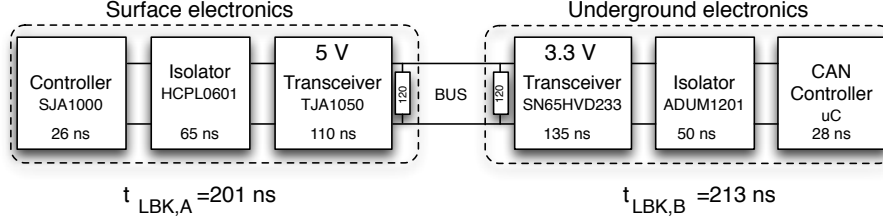


Figure 7: Signal path from surface to underground electronics used in the design.

198 and after substituting with $t_{RTD} = bus_{prop} \times L_{max}$ [11] it is found that the
 199 maximum bus length (L_{max}) at the maximum baudrate of 1 Mbps would be
 200 57 m (using UTP cable CAT5e with $bus_{prop}=5$ ns/m):

$$L_{max} = \frac{baudrate^{-1} - 2 \times t_{loop}}{2 \times bus_{prop}} = 57 \text{ m} \quad (2)$$

Nevertheless, the maximum achievable bus line length in a CAN bus network is also determined by the amplitude due to the series resistance of the bus cable and the input resistance of the bus nodes. This relationship is expressed in the following equations:

$$L_{max} = \frac{1}{2 \times \rho} \times \left(\frac{V_{diff.out.min}}{V_{th.max} + \Gamma_2} - 1 \right) \times \frac{R_{T.min} \times R_{diff.min}}{R_{diff.min} + R_{T.min}} \quad (3)$$

where

$$\Gamma_2 = k_{sm} \times (V_{diff.out.min} - V_{th.max}) \quad (4)$$

201 and ρ = is the specific resistance per length unit.

202 Here k_{sm} is the safety margin expressed as the fraction of the difference be-
 203 tween the output level at the transmitting node and the receiver input threshold
 204 for detection of a dominant bit [11]. Thus, the maximum cable length is esti-
 205 mated to be 25 m when taking a safety margin of 75% and the worst transceiver
 206 type (see Figure 8).

207 Eye patterns provide a good representation of how the data have been af-
 208 fected by a transmission line. Positive and negative pulses are superimposed on
 209 each other. Overlaying many bits produces an "eye" diagram, so called because
 210 the resulting image looks like the opening of an eye.

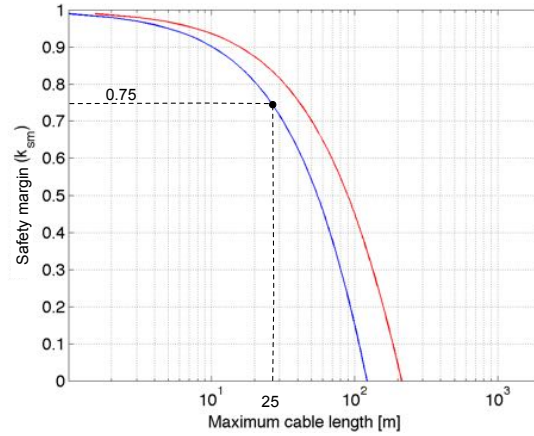


Figure 8: Bus length dependence on the given safety margin. The red and blue lines represent the maximum lengths using underground and surface transceiver parameters, respectively.

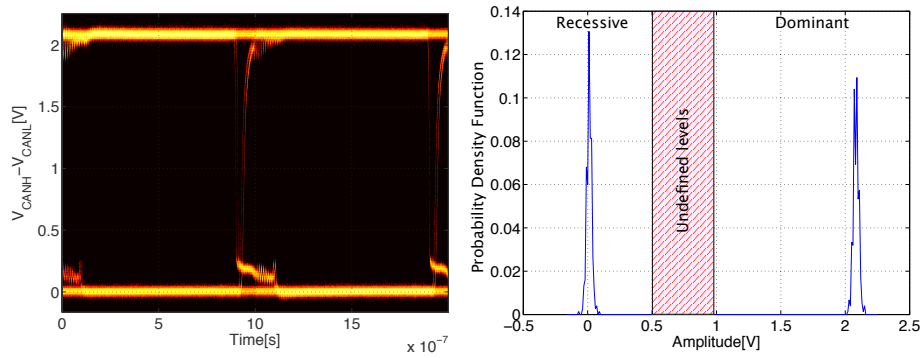


Figure 9: Eye pattern and vertical histogram at sample point ($t=1.8 \mu s$, Number of traces= 1×10^6). Recessive and dominant levels appear well defined at 0V and 2.1V. The forbidden area is colored red. In this area, bus levels are undefined for the transceivers.

211 In the setup, random patterns were generated at the surface electronics and
212 sent by CAN bus to the underground electronics. The patterns were received
213 by the μC and then echoed to the surface. Since CAN uses a differential bus,
214 the signals were measured in the CANH (high level port of CAN) and CANL
215 (low level port of CAN) ports with an oscilloscope. The measurements were
216 done using the surface transceiver because the transceiver selected for the un-
217 derground (SN65HVD233) is powered with 3.3 V. Thus, the most demanding
218 configuration is when the TJA1050 transceiver (5 V) receives signals from the
219 underground transceiver (3.3 V). The results of the tests are shown in Figure
220 9 where one can see the eye pattern and the vertical histogram at the sample
221 point ($t=1.8 \mu\text{s}$). The distribution of both levels (dominant and recessive) are
222 well defined with peaks at 0 and 2.1 V. None of the 10^6 pulses recorded fell in
223 the forbidden area where the bus levels are undefined for the transceivers thus
224 ensuring a proper transmission.

225 3.2. *Passive serial bus*

226 **Passive Serial** (PS) is a programming method that can be performed on the
227 Cyclone III device family with an external intelligent host, such as a micropro-
228 cessor [12]. In the PS scheme, a μC controls the configuration of the FPGA. In
229 this mode the configuration data are clocked into the Cyclone III device using
230 the DATA0 pin at each rising edge of the DCLK (clock). A simple routine
231 was programmed into the μC to receive the configuration file from the surface
232 electronics via the CAN bus and then transfer it by PS to the Cyclone using
233 five I/O general purpose ports: nCONFIG, nSTATUS, CONFDONE, DLCK
234 and DATA0. During configuration, the Cyclone III (FPGA) decompresses the
235 bitstream in real time and programs SRAM cells. This decompression feature
236 is supported in PS mode. As mentioned in the Cyclone III handbook [12],
237 compression reduces the configuration bitstream size by 35-55%; thus the data
238 transfer during configuration in the CAN bus is packed with a certain compres-
239 sion factor reducing its size and the transfer time.

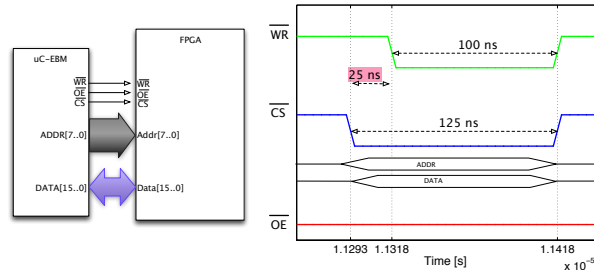


Figure 10: Left: Interconnection between μC and FPGA using the EBM. Right: EBM signal timing for write cycle: Data were taken with a logic analyzer and then plotted.

240 3.3. Parallel bus

241 In the underground electronics, the core of the acquisition system is imple-
 242 mented in a Cyclone III (FPGA) and a memory bank for event data storage.

243 The interconnection between the μC and the FPGA to configure its registers
 244 is implemented by a data bus of 16 bits, an address bus of 8 bits and three
 245 signals (see Figure 10). In the μC , these ports are supported by the Expansion
 246 Bus Module (EBM) designed to connect external memories. In this way, the
 247 FPGA is directly mapped to the μC and the FPGA registers can be accessed
 248 by the μC as an external memory. Each μC transaction requires a minimum
 249 of one clock cycle. Nevertheless, five wait states were added because the EBM
 250 is clocked by a 40 MHz internal Phase-Locked Loop (PLL) and the μC internal
 251 PLL is not synchronized with the FPGA clock. This provides the stability
 252 required for the desired performance. Using this configuration each access cycle
 253 to the FPGA takes 125 ns (Figure 10).

254 The tests were done by performing 10000 write/read cycles into the FPGA
 255 registers to detect any perturbation in the synchronization between the FPGA
 256 and the μC (not synchronized with the same clock) during the access to the bus
 257 using five wait states. In order to achieve that, random data were generated by
 258 the SBC and sent to the underground electronics. The μC wrote each pattern,
 259 read it and sent it back to the SBC where patterns were compared. No data
 260 loss was detected using five wait states.

261 *3.4. High voltage control*

262 The PMT high voltage (HV) is provided by a module from Hamamatsu
263 (C4900-1). As the HV will never change during normal operation, the control
264 of this parameter is just for compensating the gain due to PMT aging. However
265 it is known that if voltage is applied abruptly to a tube connected in negative
266 polarity, the amplitude of the initial dark-current transient may be high enough
267 to damage the sensitive measuring apparatus. Therefore the μC can apply the
268 voltage gradually to reduce the transient. The controlling voltage input of the
269 C4900-1 varies from 0 V to 5.3 V [13]. The control of the HV module input is
270 performed by the μC using an external 10 bit DAC that is connected to the
271 μC via SPI (Serial Peripheral Interface). In this way the μC can set any value
272 between -3 V and -1000 V with a minimum step of 1.2 V.

273 The SPI application is configured at a rate of 10 MHz with a word length
274 of 16 bits. The DAC (TLV5617A from Texas Instruments) is used with an
275 external reference of 2.5 V. The resistor string output voltage of the TLV5617A
276 is buffered by a $\times 2$ gain rail-to-rail output buffer. The buffer features a Class-
277 AB output stage in order to improve stability and to reduce settling time, and
278 provides an output voltage at full scale given by

$$V_{out} = \frac{2 \times REF \times CODE}{2^n} [V]. \quad (5)$$

279

280 Here REF is the reference voltage of 2.5 V, CODE is the digital input value
281 within the range of 0 to 2^n-1 and $n = 10$ (bits).

282 As the DAC is powered with a 5 V regulator, its internal amplifier is used
283 to get a full range (0-5V) and to improve its output linearity. The 3.3 V output
284 from the motherboard is used to power a 5 V regulator isolating the digital
285 section of the interface board. Furthermore an isolator (ADuM1400ARW) was
286 added between the μC SPI and the DAC ports. This configuration allows the
287 μC to transfer the control voltage codes from the surface electronics directly to
288 the SPI module.

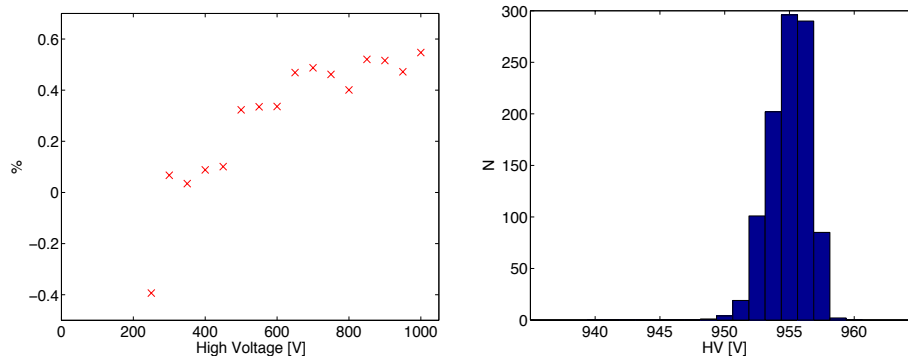


Figure 11: Left: HV was programmed in 50 V steps and measured; the y axis was calculated with $(\frac{V_{measure}-V_{fit}}{V_{measure}})\times 100$. Right: PMT HV was set at 954 V; 1000 measurements were taken with the monitoring circuit. The standard deviation observed was ± 1.50 V

289 A test to check the DAC offset and gain errors was done by programming
 290 high voltage values and plotting them versus the measured high voltage values.
 291 To determine deviations from a linear behaviour the points were fitted with a
 292 linear function $a_1 + a_2 \times HV$ resulting in an offset error $a_1=-2.25$ and an gain
 293 $a_2=1$. The plot of the residuals in Figure 11 confirms a deviation from linearity
 294 below 0.6 %. over the full range.

295 3.5. Monitoring

296 The interface and control board provide twelve 10 bit ADC channels to mea-
 297 sure parameters of the underground electronics. The channels are used to moni-
 298 tor the PMT high voltage, the supply voltage of 12 V, 3.3 V, -3.3 V from the
 299 front-end regulators, and the 3.3 V, 1.2 V and 2.5 V of the FPGA power supply.
 300 In addition, the μC and PMT temperatures are monitored by sensors from Ana-
 301 log Devices (AD22103). The sensors provide a voltage level that is digitized by
 302 the ADC. The input amplifiers for the ADC channels are included in the inter-
 303 face and control board. Two schemes are implemented taking into account that
 304 the ground reference of the ADC is not the same as the motherboard ground.

305 As an example, one of the circuits implemented to monitor a voltage level
 306 from the motherboard is shown in Figure 12. The PMT high voltage module

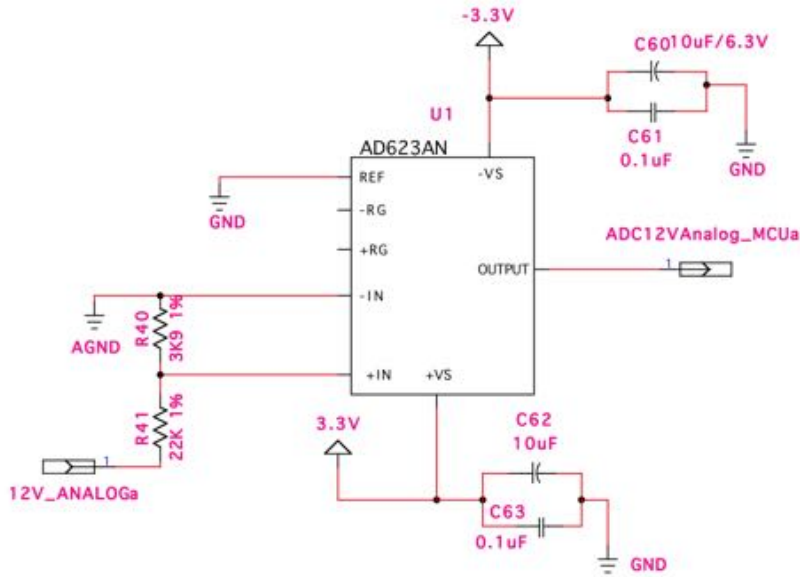


Figure 12: Monitoring circuit implemented for 12 V signal. The signal comes from a regulator to power the high voltage module in the motherboard.

307 uses a 12 V regulator and it is monitored by the interface board using a resistive
 308 divider together with a differential amplifier **at unity gain**. The HV module
 309 reference terminal defines the zero output voltage. This is useful if the load does
 310 not share a common ground with the rest of the system as in this application.
 311 Because the AD623 output voltage is set with respect to the potential on the
 312 reference terminal, the grounding problem is solved by connecting the REF pin
 313 to the local ground (GND in Figure 12). Because the motherboard includes a
 314 HV monitoring circuit with a scale factor of 1:1000 the same configuration shown
 315 before **is used** to measure the PMT high voltage level. Similar configurations
 316 **are implemented with** ± 3.3 V regulators.

317 Additionally, the digital board regulators, which do share the ground level
 318 with the ADC, **are interfaced** as shown in Figure 13, where the signals **are** only
 319 buffered and adapted to the ADC input ranges.

320 A gain around 7.7×10^6 is expected with 954 V and this gain value was se-
 321 lected in the laboratory to get a good SPE resolution. The standard deviation

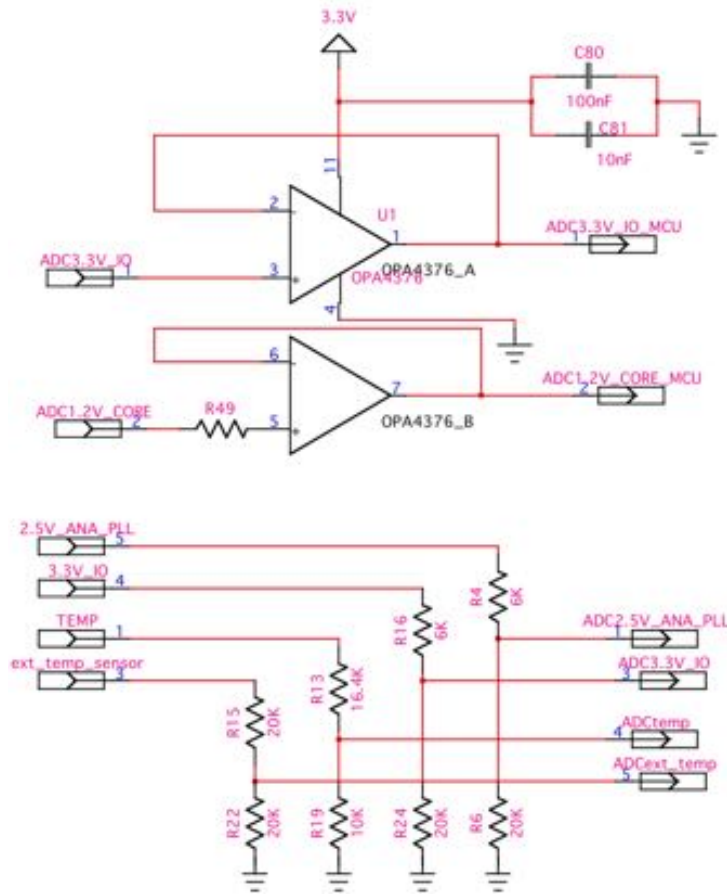


Figure 13: The signals 2.5V_ ANA_ PLL and 3.3V_ IO come from regulators used to power the FPGA. TEMP and ext_ temp_ sensor come from the interface board.

322 obtained is ± 1.50 V which represents a low dispersion.

323 Also, monitoring measurements were taken in the laboratory with the inter-
 324 face board to check the components stability as a function of temperature in the
 325 range of interest. The PMT high voltage was set to 954 V (anode to cathode).
 326 The PMT temperature was increased using a heat resistor, since some prelimi-
 327 nary tests of the mechanical design of the module showed a daily thermal and
 328 a seasonal excursion inside the underground electronics dome[14]. One of the
 329 temperature sensors from the interface and control board was attached to the

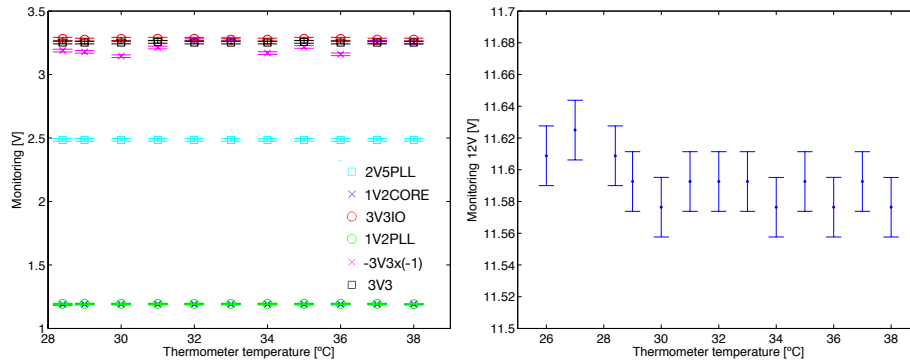


Figure 14: Left: Monitoring of regulator output levels implemented in the underground electronics. Output levels seem to be stable in the whole temperature range. The negative power supply (-3.3 V) shows fluctuations that could be related to bad filtering. Right: Monitoring of the 12 V regulator used to power the high voltage module. Error bars show the accuracy of the measurements. The deviation from the nominal value of 12 V was detected at room temperature. It shows that the regulator was working outside the component specification (output voltage accuracy of 1 %).

330 PMT socket. Meanwhile, a second sensor was added to the interface and control
 331 board. Both these sensors provided the voltages to the ADC. A reference
 332 thermometer (with a type K thermocouple) was located inside the electronics
 333 enclosure next to the sensor located in the interface and control board. Since
 334 both sensors were located next each other, a difference was not expected in the
 335 measurements of the distance to the source of heat. The monitoring system
 336 acquired the temperature measurements and all the monitoring values.

337 The results of temperature stability in the acquisition chain of the monitoring
 338 signals are plotted on the left side of Figure 15. As can be seen from the figure,
 339 there is only a negligible dependence on temperature. The comparison of the
 340 reference temperature and the integrated temperature sensor is shown on the
 341 right side of Figure 15. The measurements are in agreement, but the integrated
 342 sensor shows a bias of about 2°C, which is within the specified absolute accuracy
 343 and which can be corrected by a temperature calibration. The error bars on
 344 the right side of Figure 15 are the errors provided by the manufacturer of the
 345 reference thermometer and the errors due to the circuits implemented in the

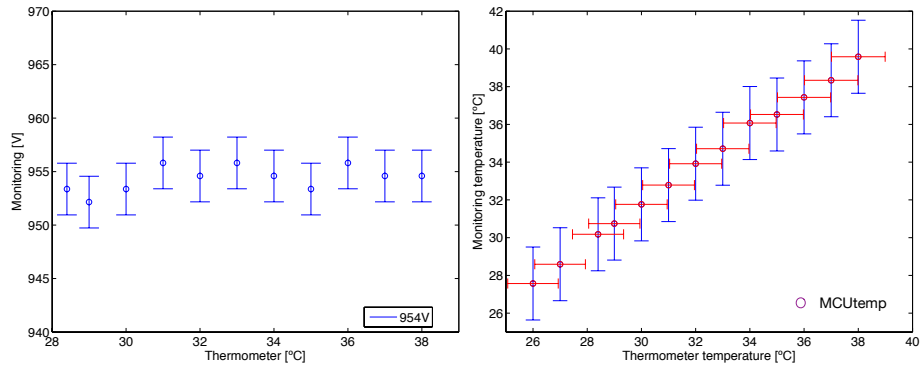


Figure 15: Left: Monitoring of the high voltage set to the PMT. The DAC was programmed to set 954 V in the HV module. The selected HV value corresponds to the selected gain for the PMT. Right: Temperature comparison between thermometer measurements and interface sensor. A systematic error is found and could be improved with a temperature calibration.

346 interface and control board.

347 Monitoring data are transmitted to the central data acquisition by request.
 348 The idea of the monitoring is to check the voltages around a nominal value.
 349 If voltages are outside the manufacturer specification range, corrective actions
 350 have to be taken by a monitoring control. Implementation of a monitoring
 351 central is foreseen with alarms management.

352 4. Acquisition and compression algorithm

353 The Pre-unitary Cell was the first array of counter prototypes deployed in
 354 AMIGA and data were recorded during one year (2012). The footprint of a
 355 shower with the core falling within the prototype hexagon is shown in Figure 16
 356 along side the digital trace patterns recorded by the muon counters participating
 357 in this event.

358 Basically, data in the buried counters are active samples **within a region**
 359 around the trigger bin 256 (length of the circular buffer). The spread around
 360 the trigger bin of the active samples provides a rough estimate of the time width
 361 of the shower front. **An active sample represents one sample of the input signal**
 362 **having an amplitude above the threshold level.** The result of a three-month

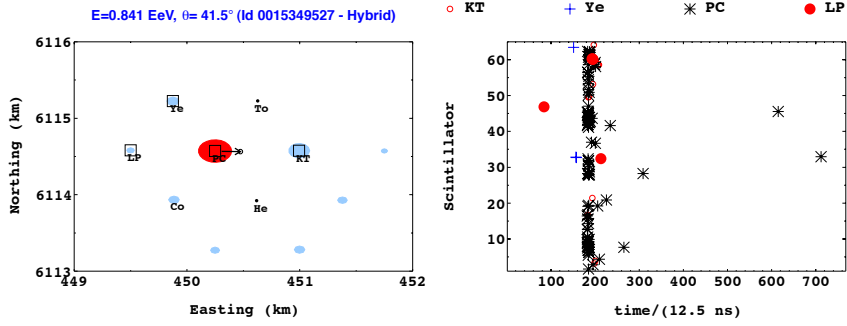


Figure 16: Example of a T3 shower event. LP, Ye, To, KT, He, Co and PC are detector pairs. Left: Pair positions, the red point represents the shower impact, sky-blue points mark Auger detectors triggered in the event. Square points are the muon counters which recorded data. Right: Scintillator strip positions are represented in y axis. Samples in time are represented in x axis. PC was the Auger detector with the highest signal. LP, Ye and KT were also triggered.

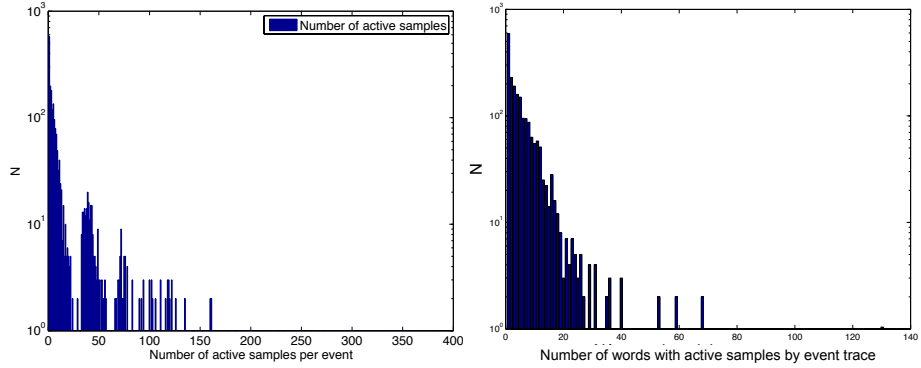


Figure 17: Left: Distribution of the number of active samples for T3 events in 3 months of data from the Pre-Unitary Cell. The distribution is not continuous, and there are some groups. The analysis was made only to explain data compression. Groups could be related to trace shapes. Right: Number of words with active samples. Events collected with the Pre-Unitary Cell with a threshold level of 200 mV.

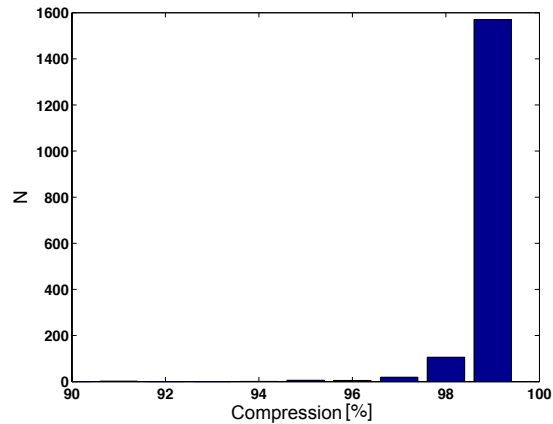


Figure 18: Compression applied to data shown in the right side of Figure 17. The compression of data traces is bigger than 90%.

363 period of data analysis from the Pre-Unitary Cell is that the maximum number
 364 of active samples in a T3 event is 381 and most of the active samples cease at
 365 approximately 160 as shown in Figure 17. The maximum number of samples
 366 (381) represents only 0.77% of the maximum possible value of 49152 ($768 \times$
 367 64), where all the samples of an event are in an active state. Later, a simple
 368 compression algorithm was implemented in the μC of the interface and control
 369 board to improve the data transfer up to the surface electronics. Only time bins
 370 of event traces from channels with active samples are transferred along with its
 371 corresponding bin position.

372 The results of the compression algorithm can be seen in Figure 17. The
 373 minimum compression achieved is 90% while the average compression is 98.8%.

374 5. Results and discussion

375 Studies and measurements of the interface and control board functions (data
 376 transfer, FPGA programming, monitoring and slow control) and CAN bus char-
 377 acteristics were performed and analyzed. It was found that the CAN protocol is
 378 a suitable solution for a single AMIGA module or more than one interconnected
 379 module through a CAN bus (backbone topology) having a cable length of 25 m

380 (considering a safety margin of 75%). This system has been successfully imple-
381 mented in the Pre-Unitary Cell construction phase of the AMIGA project and
382 particle shower events were successfully acquired and transmitted through the
383 interface and control board. Data recorded with the Pre-Unitary Cell were used
384 to implement a compression algorithm in the μC of the interface and control
385 board **to reduced** the amount of data transfers. The minimum and maximum
386 compression factor was found to be 90% and 99% respectively. The acquisition
387 mode flexibility of the interface and control board allowed performing several
388 tests with the counters and it was used for engineering re-design purposes.

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