Two-Layered Microstrip Diplexer Based on High-Selectivity Wideband Bandpass Filters

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***Abstract*—This paper presents a microstrip diplexer based on two high-selectivity wideband bandpass filters (BPFs) in a two-layered structure. Both the lower and upper channels are designed with third-order microstrip-to-microstrip vertical transitions using open-circuit-ended slotline stepped-impedance resonators (SIRs). Specifically, open-circuit-ended microstrip lines on the top and bottom layers for the lower channel are employed, whereas the upper channel is equipped with short-circuit-ended ones. Thus, owing to the slotline SIRs, two close-to-passband transmission zeros (TZs) leading to sharp-rejection capabilities for both BPF channels are attained. The theoretical foundations and RF operating principles of the devised diplexer are discussed in detail. For practical-validation purposes, a two-layered microstrip wideband diplexer prototype is designed, simulated, and tested. It features two three-pole high-selectivity filtering responses for the measured lower and upper channels that are centered at 1.52 GHz and 2.76 GHz, and exhibit 3-dB fractional bandwidths of 60% and 24.93%, respectively.**

Keywords—Bandpass filter (BPF), diplexer, high selectivity, microstrip filter, multilayered circuit, vertical transition, wideband filter.

I. Introduction

As key microwave components to connect the transmitter and receiver sides in full-duplex RF front-ends, RF diplexers with low insertion losses, sharp-rejection passbands, and high isolation levels are always required. Recently, microstrip wideband diplexers developed with different methods and structures have been reported [1]–[5]. In [1], a high-performance diplexer aimed at direct-sequence ultra-wideband communication systems was designed based on hairpin-line-type microstrip resonators. Similarly, through half-wavelength open-loop resonators, a microstrip wideband diplexer with narrow guard band was realized in [2]. In [3], in order to increase the passband-widths of the two building bandpass filters (BPFs), a wideband diplexer using broadside-coupled microstrip and slotline stepped-impedance resonators (SIRs) was presented. In [4], a microstrip diplexer exploiting signal-interference stepped-impedance microstrip lines was conceived. In addition, based on bandstop-mode half-wavelength microstrip lines, a resonator-based wideband diplexer with improved cut-off slopes was suggested in [5]. On the other hand, although microstrip diplexers with controllable transmission zeros (TZs) were discussed in [6], only narrow bandwidths for their two bandpass channels are attained. Consequently, one or several of the following drawbacks can still be found for all the aforementioned devices of planar diplexers: a) narrow or moderate bandwidth for the lower and/or upper channel, b) poor filtering selectivity, and/or c) degraded inter-channel power-isolation levels.

In this paper, a multilayered microstrip wideband diplexer based on two third-order high-selectivity BPFs is proposed. Its lower bandpass channel is built by means of a three-pole wideband microstrip-to-microstrip vertical transition using an open-circuit-ended slotline SIR as detailed in [7]. Besides, by replacing the open-circuit-ended microstrip lines by short-circuit-ended ones in the employed vertical transition, a wideband sharp-rejection passband located at a higher frequency region is attained to configure the upper bandpass channel. The RF operational foundations of the engineered diplexer approach are detailed. Moreover, for experimental-validation purposes, a microstrip prototype of the designed two-layered wideband diplexer is developed and measured.

II. Theoretical Analysis and Design

Fig. 1 depicts the transmission-line equivalent circuit of the proposed wideband diplexer, where its two constituent BPF channels are built with third-order wideband microstrip-to-microstrip vertical transitions. Here, the lower-passband channel centered at f_L is actually designed with a wideband high-selectivity vertical transition using open-circuit-ended microstrip resonators and a slotline SIR as suggested in [7]. As shown, the impedance variables of the cascaded open-circuit-ended stubs for the open-circuit-ended microstrip resonators, and the shunt transmission-line sections and open-circuit-ended stubs for the slotline SIR are Z_{m_1}, Z_{s1_1}, and Z_{s2_1}, respectively. By substituting the open-circuit-ended stubs of the lower-channel network by short-circuit-ended ones, a sharpened passband shaping the upper channel that is centered at f_U is obtained. The impedance-type parameters of its employed stubs and sections are Z_{m_2}, Z_{s1_2}, and Z_{s2_2}, respectively. All the stubs and sections of the engineered diplexer are set with the same electrical length θ = 90°, but at different design frequencies—quarter-wavelength long at f_L for the lower channel and at $f_U/2$ for the upper channel. In addition, to account for the impedance variations of the coupled microstrip resonator and slotline SIR of each channel appearing in the practical design, two sets of three transformers with different turns ratios of N_{m_1}, N_{s1_1} and N_{s2_1}, and N_{m_2}, N_{s1_2} and N_{s2_2}, respectively, are utilized [8].

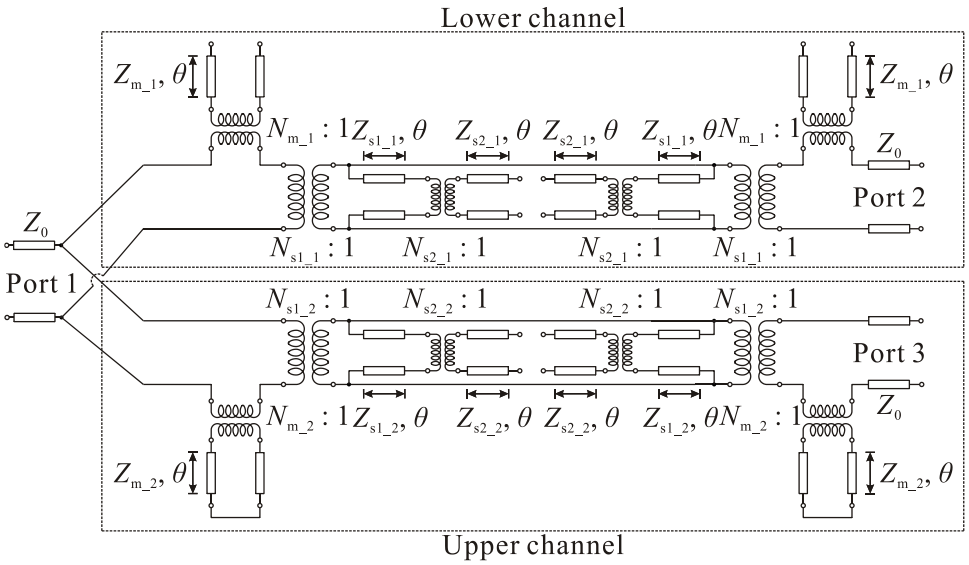

Fig. 1. Transmission-line equivalent circuit of the proposed multilayered wideband microstrip diplexer shaped by two high-selectivity third-order microstrip-to-microstrip vertical transitions using open-/short-circuit-ended microstrip resonators and slotline SIR.

Next, based on the equivalent circuit of the proposed three-port diplexer network in Fig. 1, the RF operational principles of the two constituent wideband BPF channels are detailed. Here, the whole circuit network is assumed to be lossless with the turns ratios of the used transformers being $N_{m\_1} = N_{s1\_1} = N_{s2\_1} = N_{m\_2} = N_{s1\_2} = N_{s2\_2} = 1$. With the cascaded *ABCD* sub-matrices of the two-port vertical-transition-based lower- and upper-channel networks, their characteristic functions F_L and F_U can be determined as below

$$F_L = j\left(\frac{z_{m\_1}^2}{z'_{s\_1}}\cot^2\theta - z_{m\_1}\cot\theta + \frac{1}{z'_{s\_1}}\right) \tag{1}$$

$$F_U = j\left(\frac{z_{m\_2}^2}{z'_{s\_2}}\tan^2\theta + z_{m\_2}\tan\theta + \frac{1}{z'_{s\_2}}\right) \tag{2}$$

where

$$z'_{s\_i} = \frac{z_{s1\_i}^2\tan^2\theta - z_{s1\_i}z_{s2\_i}}{(z_{s1\_i} + z_{s2\_i})\tan\theta} \quad with\ i = 1\ and\ 2 \tag{3}$$

and z_{m_1}, z_{s1_1}, z_{s2_1}, z_{m_2}, z_{s1_2}, and z_{s2_2} are the corresponding normalized impedances. With (1)–(3), the spectral locations of the TZs of these two BPF channels at which their relevant power transmission coefficients are zero are derived. For the lower-channel network, its periodical TZs caused by the open-circuit-ended stubs are located at $2nf_L$ (n = 0, 1, …, N), whilst the additional close-to-passband TZs (i.e., f_{L_TZ1} and f_{L_TZ2}) that are related to the slotline SIR are formulated as

$$f_{L\_TZ1} = \frac{2f_L\tan^{-1}\sqrt{\dfrac{z_{s2\_1}}{z_{s1\_1}}}}{\pi} + 2nf_L \tag{4a}$$

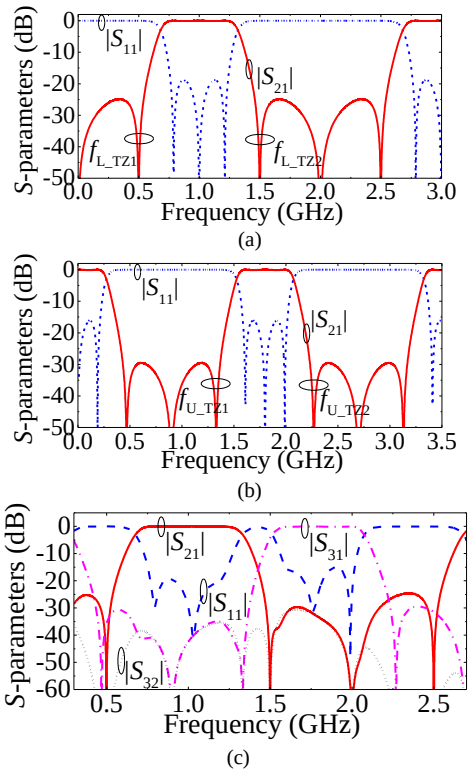

Fig. 2. Theoretical *S*-parameter responses of the proposed multilayered wideband diplexer with Z_{m_1} = 101.9 Ω, $Z_{s1\_1} = Z_{s2\_1}$ = 83.1 Ω, and Z_{m_2} = 122 Ω, Z_{s1_2} = 72.9 Ω, Z_{s2_2} = 83.1 Ω. (a) Power transmission ($|S_{21}|$) and reflection ($|S_{11}|$) responses of the two-port lower-passband channel centered at f_L = 1 GHz. (b) Power transmission ($|S_{21}|$) and reflection ($|S_{11}|$) responses of the two-port upper-passband channel centered at f_U = 1.8 GHz. (c) Power transmission ($|S_{21}|$ and $|S_{31}|$), reflection ($|S_{11}|$), and isolation ($|S_{32}|$) responses of the three-port wideband diplexer with f_L = 1 GHz and f_U = 1.8 GHz.

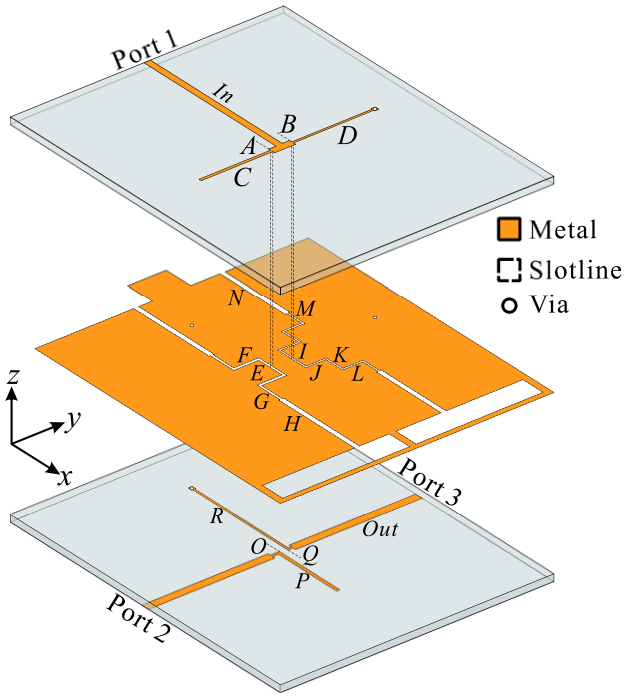

Fig. 3. Layout of the designed microstrip wideband diplexer circuit in a two-layered substrate with the following dimensions: L_{in} = 76.09, L_{out} = 45.3, L_A = L_B =3, L_C = 30.67, L_D = 34.875, L_E = 9.2, L_F = 12.4, L_G = 12, L_H = 45, L_I = 9.76, L_J = 8.59, L_K = 5.12, L_L = 8.59, L_M = 9.96, L_N = 37.04, L_O = 2.5, L_P = 29.57, L_Q = 1.5, L_R = 34.875, W_{in} = W_{out} = W_A = W_B = 1.82, W_C = W_E = W_F = W_G = W_H = W_N = W_O = W_P = 0.4, W_D = W_Q = W_R = 0.22, and W_I = W_J = W_K = W_L = W_M = 0.12 (unit: mm).

$$f_{\mathrm{L\_TZ2}} = 2(n+1) f_{\mathrm{L}} - f_{\mathrm{L\_TZ1}}. \tag{4b}$$

On the other hand, the intrinsic TZs that are attributed to the short-circuit-ended stubs for the upper channel are produced at $(n+1/2)\,f_{\mathrm{U}}$, while its close-to-passband TZs (i.e., $f_{\mathrm{U\_TZ1}}$ and $f_{\mathrm{U\_TZ2}}$) generated by the slotline SIR are derived as

$$f_{\mathrm{U\_TZ1}} = (n+1) f_{\mathrm{U}} - \frac{f_{\mathrm{U}} \tan^{-1}\sqrt{\frac{z_{s2\_2}}{z_{s1\_2}}}}{\pi} \tag{5a}$$

$$f_{\mathrm{U\_TZ2}} = (n+1) f_{\mathrm{U}} + \frac{f_{\mathrm{U}} \tan^{-1}\sqrt{\frac{z_{s2\_2}}{z_{s1\_2}}}}{\pi}. \tag{5b}$$

To verify the above discussions, the proposed wideband diplexer is designed with its lower and upper channels centered at f_{L} =1 GHz and f_{U} = 1.8 GHz. Firstly, the frequency responses of the constituent two-port three-pole lower- and upper-BPF channels are illustrated in Fig. 2(a) and 2(b), respectively. As can be seen, due to the above discussed TZs, these two channels are featured with the expected quasi-elliptic-type third-order wideband BPF filtering responses. Whilst, Fig. 2(c) depicts the theoretical frequency responses of the whole diplexer network. As observed, whereas the high-selectivity wideband responses

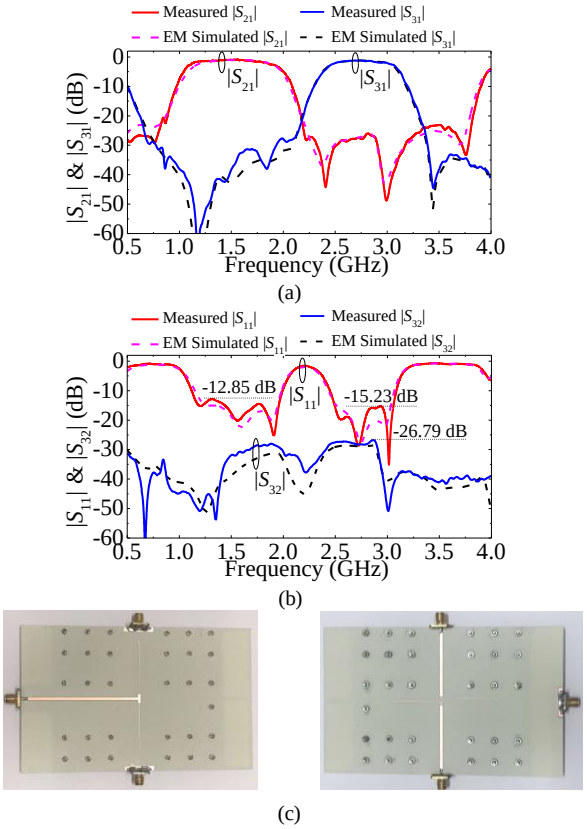

Fig. 4. Manufactured two-layered microstrip wideband diplexer prototype. (a) Simulated and measured power transmission ($|S_{21}|$ and $|S_{31}|$) responses. (b) Simulated and measured power reflection ($|S_{11}|$) and isolation ($|S_{32}|$) responses. (c) Photographs (top/bottom view) of the assembled diplexer prototype.

of these two BPF channels remain nearly unchanged with regard to the ones in Fig. 2(a) and 2(b) for the isolated BPF channels, their in-band power-matching levels are slightly degraded. Meanwhile, power-isolation levels between the two BPF channels above 30 dB within the whole plotted frequency interval are attained.

III. Experimental Results

To practically verify the design concept of the proposed wideband diplexer, a two-layered microstrip prototype is designed and tested. It is fabricated using a Rogers 4003C substrate with relative dielectric constant ε_r = 3.55, dielectric thickness h = 0.813 mm, and dielectric loss tangent of 0.0027. The layout of the conceived diplexer is shown in Fig. 3, in which the open-/short-circuit-ended stubs, and the shunt cascaded transmission-line sections and open-circuit-ended stubs in Fig. 1 are replaced by the open-/short-circuited microstrip lines and the open-circuit-ended slotline SIRs. Here, the open-circuit-ended microstrip line of the lower channel and the short-circuit-ended microstrip line of the upper channel on the bottom layer are designed in folded structures to avoid harmful coupling effects. Fig. 4 depicts the simulated and measured frequency responses, as well as the photographs of the assembled diplexer prototype. The main performance metrics of the measured wideband diplexer are as follows: lower channel centered at 1.52

GHz with minimum insertion loss of 0.84 dB and 3-dB fractional bandwidth of 60%, and upper channel centered at 2.76 GHz with minimum insertion loss of 1.08 dB and 3-dB fractional bandwidth of 24.93%; the power isolation levels are above 26.79 dB from 0.5 to 4 GHz.

IV. Conclusion

A two-layered microstrip diplexer using two third-order high-selectivity wideband BPFs has been reported. From the equivalent circuit of their building vertical-transition networks and other line elements, its theoretical foundations have been detailed. Finally, a proof-of-concept microstrip diplexer prototype has been built and tested for validation, showing a close agreement between measurements and simulations.

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