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OPTIMIZATION AND MODELING OF ESD PROTECTION DEVICES

by

LI SHEN

A THESIS

Presented to the Graduate Faculty of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE

in

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PUBLICATION THESIS OPTION

This thesis consists of the following two articles, formatted in the style used by the Missouri University of Science and Technology:

Paper I, found on pages 2–31, has been published in 44th Annual EOS/ESD Symposium and Exhibits in 2019.

Paper II, found on pages 32–52, to be submitted in 48th Annual EOS/ESD Symposium and Exhibits.

ABSTRACT

Transient voltage suppressors (TVS) are used to protect ICs (integrated circuits) against overvoltage, ESD (Electrostatic Discharge), inductive load switching, and even lightning strikes. In this research, a transient behavior model framework for ESD protection devices is used for modelling four different types of TVS (non-snapback, snapback, spark gap like device and varistor). The System-Efficient ESD Design (SEED) methodology is utilized to strengthen the trust in the model framework by efficient simulation of ESD interaction of the off-chip ESD protection devices with the IC ESD protection device and associated measurement data.

Improvements in the TVS transient response, accounting for conductivity modulation, voltage overshot at the snapback voltage, etc., are required to accurately model the ESD protection device. With this in mind, the unimproved model is presented for various ESD protection device where their transient behavior of single component can be fully described by a quasistatic very fast transmission line pulse (VF)-TLP. The improved model is validated within a sub-system consisting of an off-chip ESD protection device, an IC on-chip protection and a PCB trace in between. Multiple solutions to avoid convergence issues are also proposed for effective simulation.

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1. INTRODUCTION

Transient voltage suppressors (TVS) devices are widely used to protect vulnerable circuits from electrical over-stress. Often, for transient protection, the designer's choice is a TVS. Hence, an accurate TVS model which can capture the transient response of different ESD protection devices is vital for both component level simulaton and system-level ESD simulation. A good model should be able to predict whether the protection device will trigger or not before testing and be able to mimic the time domain waveforms of device within an acceptable error range.

In the first paper, a general TVS model framework is studied. The voltage overshoot and quasi-static IV curve for various ESD protection devices are simulated with comparison to the measured data. System efficient ESD design (SEED) is applied to demonstrate the capabilities of the model. Investigations are implemented when one TVS is at injection input and another TVS acts as an IC protection device during an ESD event. The effect of passive components on race condition between the on- and off-chip TVS devices is studied. The SEED modelling showed good agreement with measurements.

In the second paper, an improved ESD protection device model is presented. On the component level, three different types of TVS (non-snapback, snapback, varistor) are represented using the updated model. these models were validated at the system-level in a system consisting of of an off-chip ESD protection device, an on-chip protection diode and a PCB trace in between.

PAPER

I. TVS DEVICES TRANSIENT BEHAVIOR MODELING FRAMEWORK AND APPLICATION TO SEED

ABSTRACT

The transient behavior for four different types of TVS (non-snapback, snapback, spark gap, varistor) is modeled using the same modeling framework. By a 10 ns VF-TLP, the quasi-static I-V curve and the transient turn on are captured and modeled in ADS. The models are applied in a SEED simulation to investigate the strengths and weaknesses of the modeling frame.

1. INTRODUCTION

Various protection devices have been developed to protect the device under test (DUT) by suppressing voltage transiently during ESD disturbs. A variety of papers have addressed modeling of TVS devices and system-efficient-ESD-design (SEED) simulation [5]-[13]. SEED simulation is still not the industry standard. For the existing models, the model shown in [7] and [8] simulates the TVS I-V curve, they're easy to implement, but the DUT transient behavior is not simulated. The model in [9] and [10] discusses the quasi-static I-V curve, the snapback delay and small signal model, however, conductivity modulation behavior is not studied. In [11] and [12], both the conductivity modulation and the snapback behavior are studied, the overshoot due to the conductivity modulation is well

modeled, however, it's difficult to implement them in SEED simulation. TVS Simulation models need to allow to compare TVS devices from different vendors and different types, thus a simulation modeling frame is needed that is adoptable to different TVS devices and can capture turn on and quasi-static I-V behavior. For the TVS simulation model introduced in this paper, the "black-box" approach is applied to characterize the parameters in the model. This methodology allows the modelling process can be implemented without intimate knowledge and both the quasi-static I-V and transient turn on behavior of TVS are discussed for the model. This paper aims at advancing the state of the art and usage of the SEED simulation by improving the simulation framework shown in [5]. The model framework was tested on four types of TVS devices: the snapback TVS diode; non-snapback TVS diode; varistor, and spark gap like device. The time-domain waveforms and the quasi-static I-V curves are discussed between simulation and measurement.

2. MEASUREMENT SETUP

Figure 1 shows the block diagram of the measurement setup for the very fast transmission line pulse (VF-TLP) tester. This simplified setup is designed to capture both the quasi-static I-V cure for TVS devices and their transient time-domain waveforms. The VF-TLP pulse length is 10 ns long and a voltage rise time filter of 200 ps is used. The current of the TVS is measured at channel 1 in the oscilloscope, and the voltage of the TVS is measured at channel 3 in the oscilloscope. The average window setting from 7 ns to 9 ns of each pulse is applied to calculate the quasi-static voltage and current from the time-

domain waveforms. The VF-TLP voltage range of 0.5 V to 1250 V is applied to the device under test (DUT).

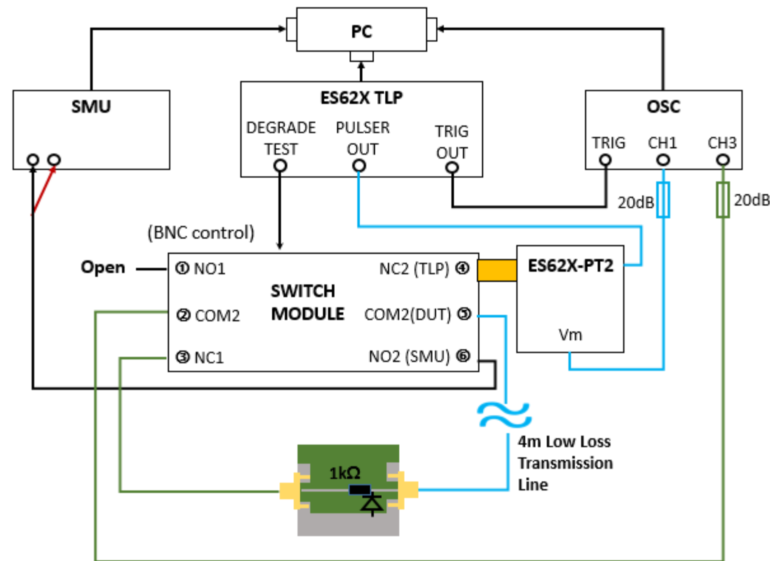

Figure 1. VF-TLP measurement setup.

3. TVS SIMULATION MODEL FRAMEWORK

Figure 2 shows the block diagram of the TVS transient behavior model framework [5]. The model frame is symmetric for both charge polarities. For each polarity, it consists of two large parts: the linear small signal model and the nonlinear large signal model. The non-linear behavior is separated into path selection sub-model (D1 and D2), pre-clamping model (D5 and D6), TVS turn on behavior model (snapback delay model and conductivity modulation mode) and a quasi-static I-V model for the behavior after the device turned on (D3 and D4). The combination of these sub-models describes the transient behavior of the TVS. D1 and D2 are practically ideal diodes. For a positive transient event, the diode D1

turns on to activate the positive current path while the negative current path is activated through diode D2 for a negative ESD event.

For some snapback devices, the TVS current can go up to tens mA before the snapback delay triggers. This preclamping behavior is modeled by D5 for positive current path and D6 for negative current path. After the TVS is turned on, the device can be modeled as a P-N diode, D3 and D4 in Figure 2 are used to model the quasi-static VI curve.

The snapback delay sub-model is for snapback TVS devices, snapback TVS does not go into the snapback once its voltage reaches the snapback threshold voltage “Vt1”. The delay time for the snapback trigger is described by the parameter “Snapback_trigger”. The details about how to tune these two parameters are discussed in model tuning section.

Conductivity modulation sub-model is to describe the conductivity change in device due to the carrier concentration change of a semiconductor device [5]. The conductivity modulation give contribution to the voltage overshoot besides the inductive voltage overshoot. A current-controlled current source (CCCS) is used to simulate this sub-model, the values for two key parameters “Von” and “R_turnoff” need to be determined. The tuning process is discussed in model tuning section.

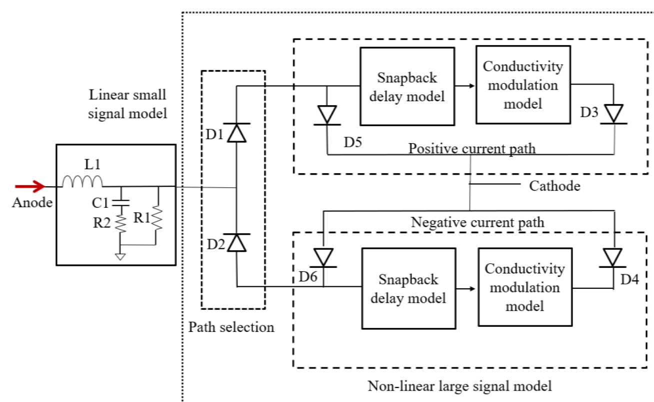

Figure 2. Block diagram of the TVS transient behavior model [5].

4. MEASUREMENT AND SIMULATION COMPARISON

4.1. SNAPBACK TVS DIODE

In this paper, a typical snapback TVS diode is evaluated. Figure 3 illustrates that the simulated I-V curve obtained using the model framework matches the measured result.

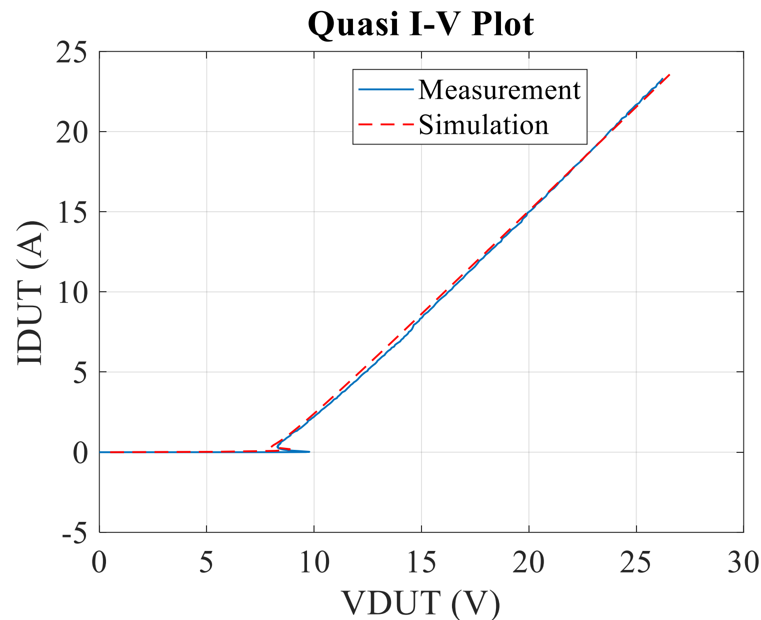

Figure 3. The simulated and measured quasi-static I-V curves for the snapback TVS diode.

As a TVS transient behavioral model, the difference between the simulated TVS voltage overshoot and measured overshoot needs to be quantified. Instead of showing limited time-domain waveforms, the voltage overshoot of DUT1 at each TLP sweeping voltage is plotted to give a statistical comparison between the simulation and measured data. Figure 4 shows the simulated VDUT peak values, and the measured VDUT peak values can match very well up to 1.1 kV TLP sweeping voltage.

The quasi-static DUT voltage (VDUT) is obtained by applying the averaging window setting to the time-domain voltage waveforms. Figure 5 illustrates the simulated VDUT can match with measured VDUT values within 2% error.

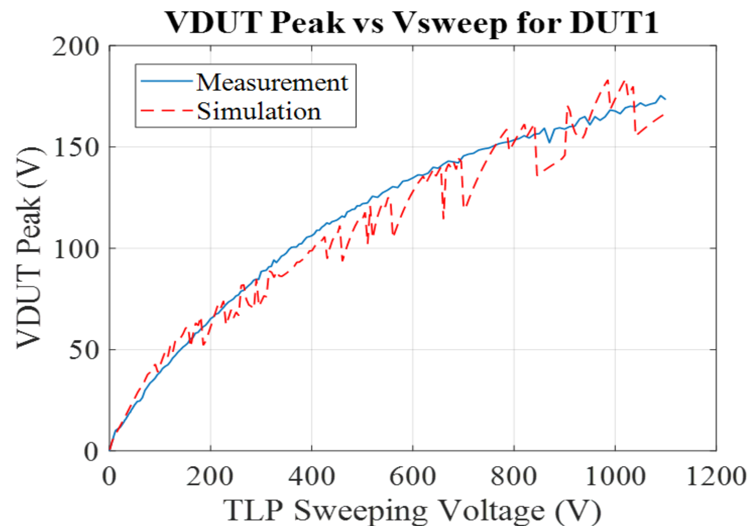

Figure 4. The simulated and measured VDUT peak values at different TLP sweep voltages for the snapback TVS diode.

The robustness and reliability of the model can be verified only after both the VDUT peak values and VDUT at each TLP sweeping voltage are compared with measurements.

Figure 6 illustrates the match between the simulated and measured I-V curve for another snapback TVS diode. The holding voltage of this DUT is around 2 V, which is much lower than the DUT1, and it also has a faster turn-on time. This DUT is used as an off-chip protection TVS diode in the SEED simulation analysis provided in Section VI. Figure 7 and Figure 8 illustrate that the simulated VDUT peak and the quasi-static VDUT values as a function of the TLP sweep voltage match the measured values.

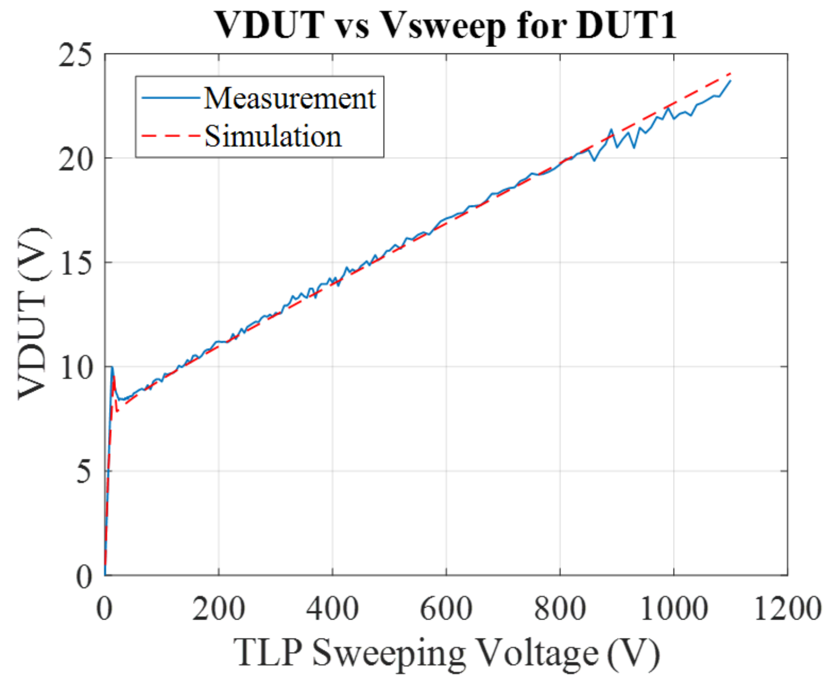

Figure 5. Quasi-static voltage at different TLP sweep voltages for the snapback TVS diode.

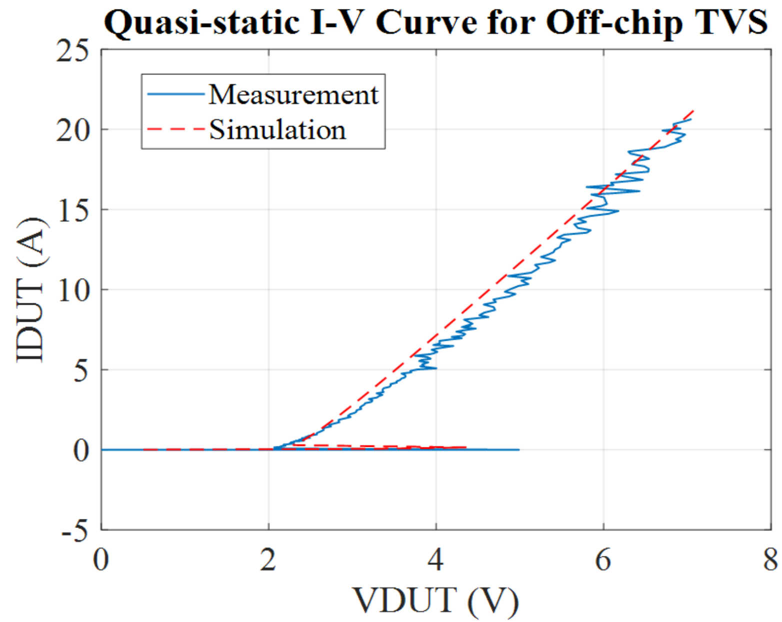

Figure 6. The simulated and measured quasi-static I-V curve for the snapback TVS diode.

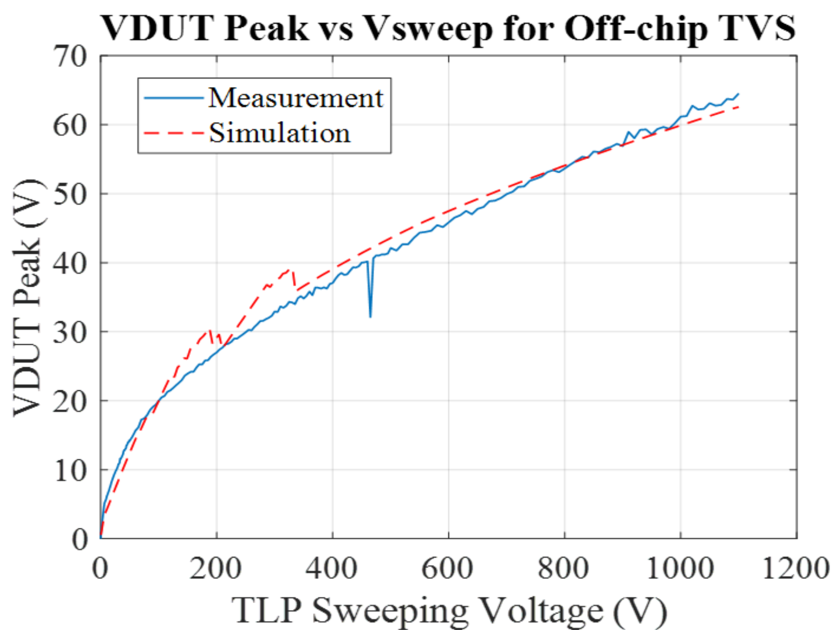

Figure 7. The simulated and measured VDUT peak values at different TLP sweep voltages for the off-chip snapback TVS diode.

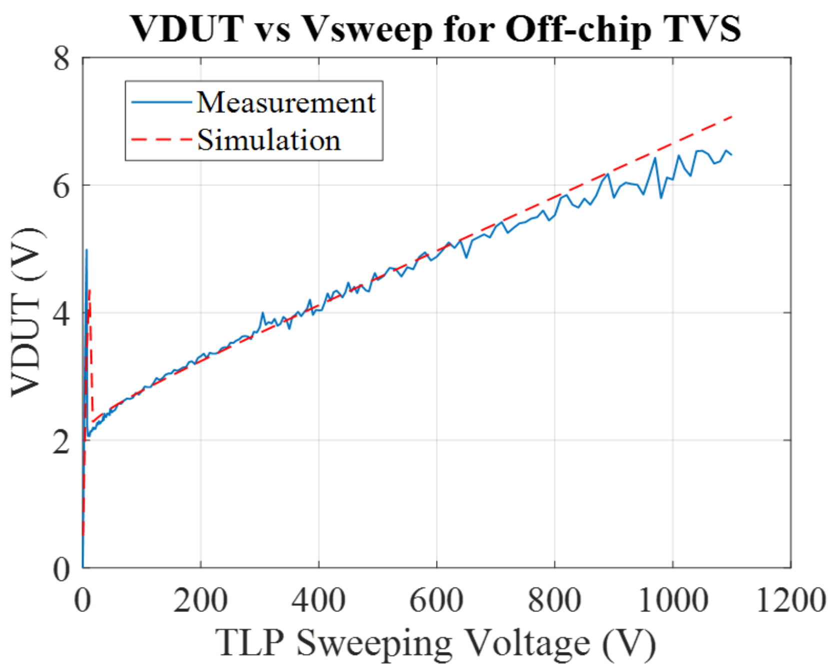

Figure 8. Quasi-static voltage at different TLP sweep voltages for the off-chip snapback TVS diode.

4.2. NON-SNAPBACK TVS DIODE

Figure 9 depicts the simulated and measured I-V curve for a unidirectional non-snapback TVS diode, which is labeled as DUT3. The reverse biased orientation of the unidirectional TVS is depicted in Figures 9 to 11.

The measurement data shows that between 5.5 V and 8.2 V, the I-V curve has a different dynamic resistance (R_{DYN}) which is the device behavior instead of a jump between two widely spaced data points (this information has been confirmed by the TVS component vendor).

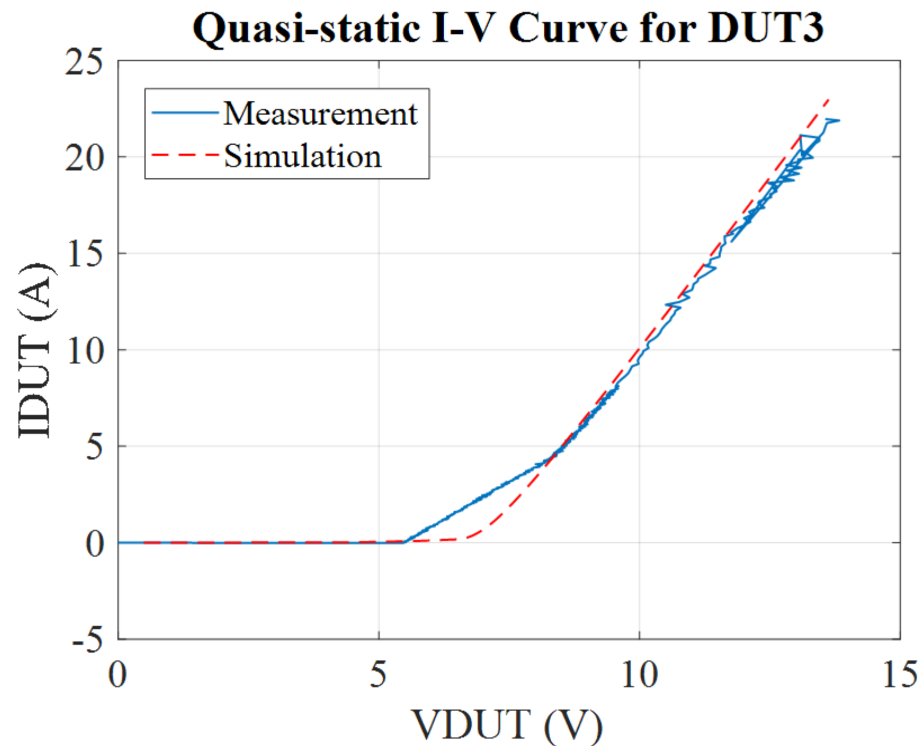

Figure 9. The simulated and measured quasi-static I-V curve for the non-snapback TVS diode.

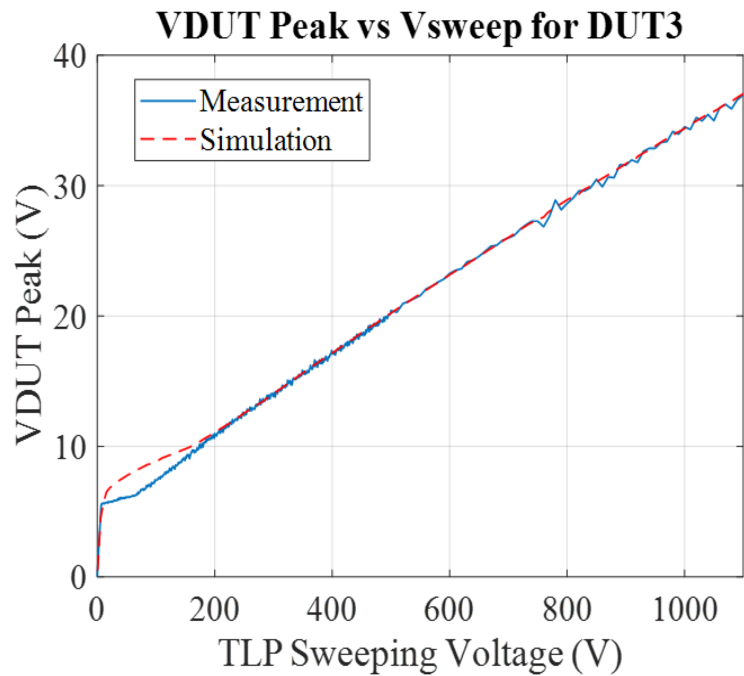

Figure 10. The simulated and measured VDUT peak values at different TLP sweep voltages for the non-snapback TVS diode.

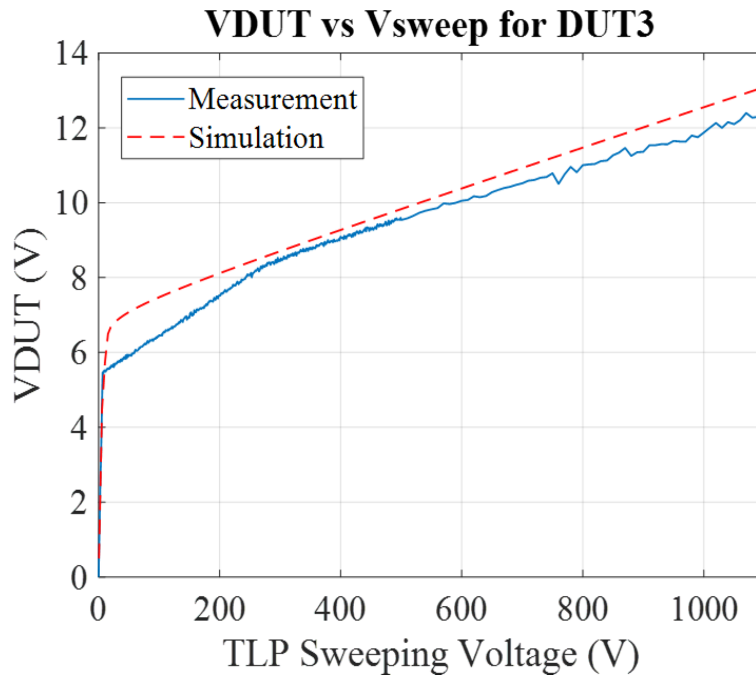

Figure 11. Quasi-static voltage at different TLP sweep voltages for the non-snapback TVS diode.

The TVS may have two breakdown characteristics, leading to two different RDYN values as shown in the measured I-V curve in Figure 9. A small deviation in the simulated VDUT peak values from the measured VDUT peak values is observed at lower TLP sweep voltages (20 V to 200 V) in Figure 10. In Figure 11, a similar deviation is observed in VDUT values at low TLP sweep voltages (up to 250 V). This deviation in the simulated curve can be explained due to the transient behavior modeling framework which can only model one of the two breakdown characteristics.

The forward biased orientation of the unidirectional TVS is also simulated and compared with the measured data. This orientation of the TVS diode is called as the IC diode in this paper. The forward biased response mimics the weak on-chip ESD protection in SEED measurement and simulation discussed in Section VI. Figure 12 shows a good match between the simulated and measured quasi-static I-V curve of the IC diode. Figure 13 and Figure 14 illustrate the results of the simulated transient behaviors of the on-chip IC diode.

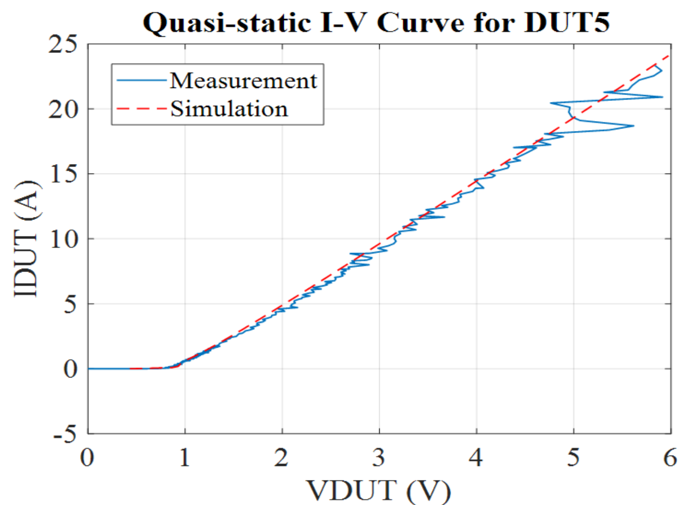

Figure 12. The simulated and measured quasi-static I-V curve for the non-snapback TVS diode.

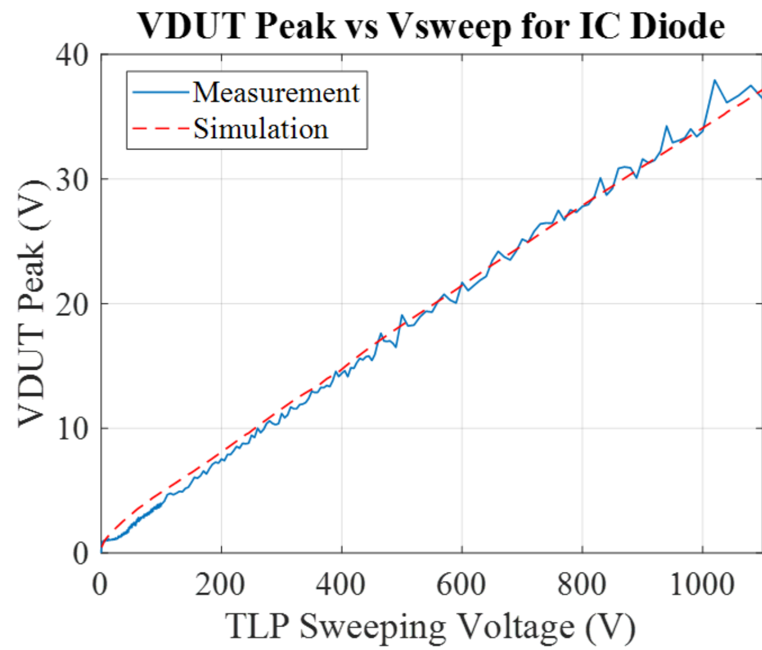

Figure 13. The simulated and measured VDUT peak values at different TLP sweep voltages for the non-snapback TVS diode.

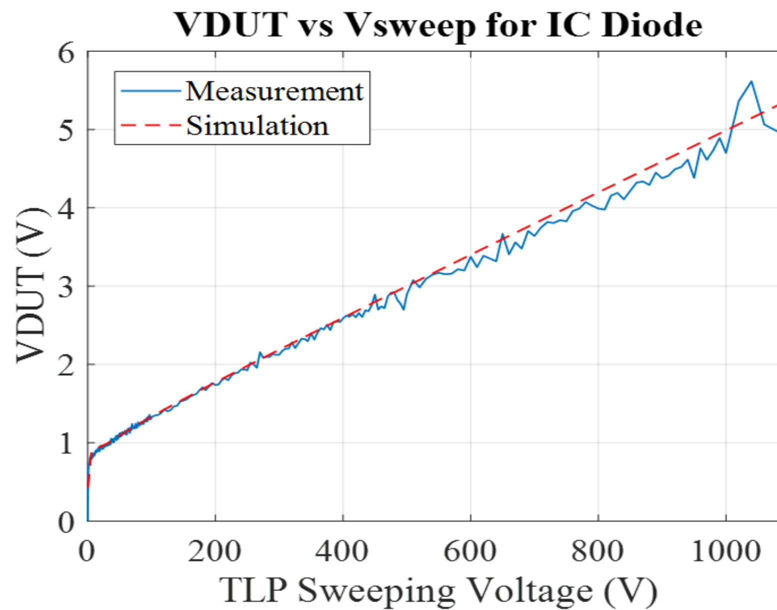

Figure 14. Quasi-static voltage at different TLP sweep voltages for the non-snapback TVS diode.

4.3. SPARK GAP LIKE DEVICE

A spark gap like device labeled as DUT5 shows a strong snapback behavior. This spark gap like device differs from a classical spark gap in two regards: even before breakdown they limit the voltage, somewhat like a Zener diode, and the breakdown delay (statistical time lag) is only in the range of a few nanoseconds. They maintain the advantage of having a very small capacitance (< 0.2 pF) which is not voltage-dependent. Thus, they do not create RF harmonic distortion. The disadvantages are a high turn-on voltage > 100 V, and high holding voltage > 25 V.

They could be especially useful for protecting antennas, as the peak voltage of RF applications can reach > 30 V. Figure 15 shows that the simulated I-V curve has a good match with the measured result.

Simulated and the measured VDUT peak values at different TLP sweeping voltages for the spark gap like device are shown in Figure 16. The simulated voltage overshoot for a spark gap can match the measured data well.

Fine tuning the parameters of pre-clamping diode (D5/D6) in the model framework, can help to reduce the DUT voltage overshoot mismatch between simulation and measurement.

Figure 17 depicts that the simulated VDUT has a good match with the measured result within 10% error. In addition, the conductivity modulation sub-model can also help reduce the voltage overshoot value.

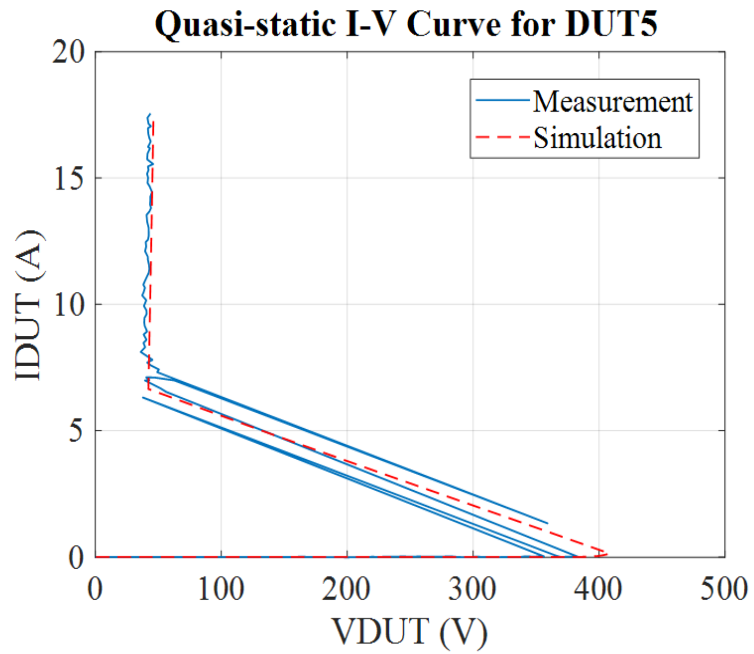

Figure 15. Simulated and measured quasi-static I-V curve for the spark gap like device.

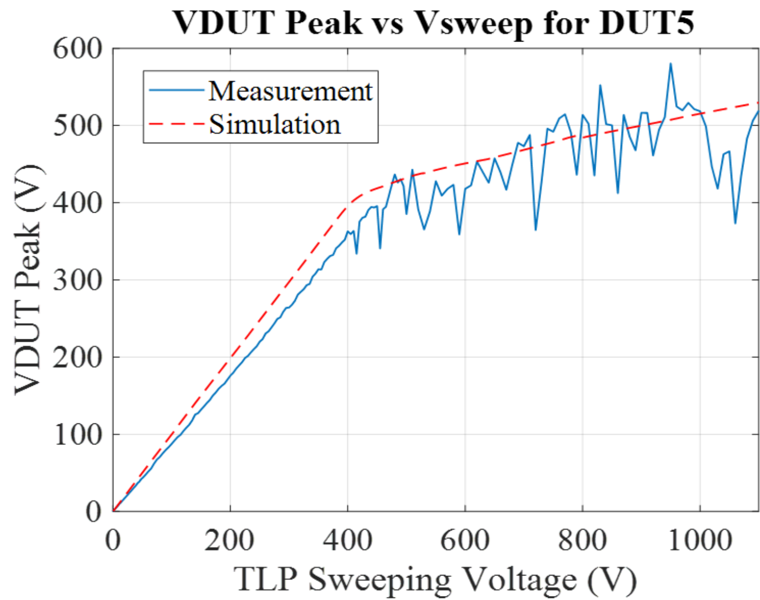

Figure 16. The simulated and measured VDUT peak values at different TLP sweep voltages for the spark gap like device.

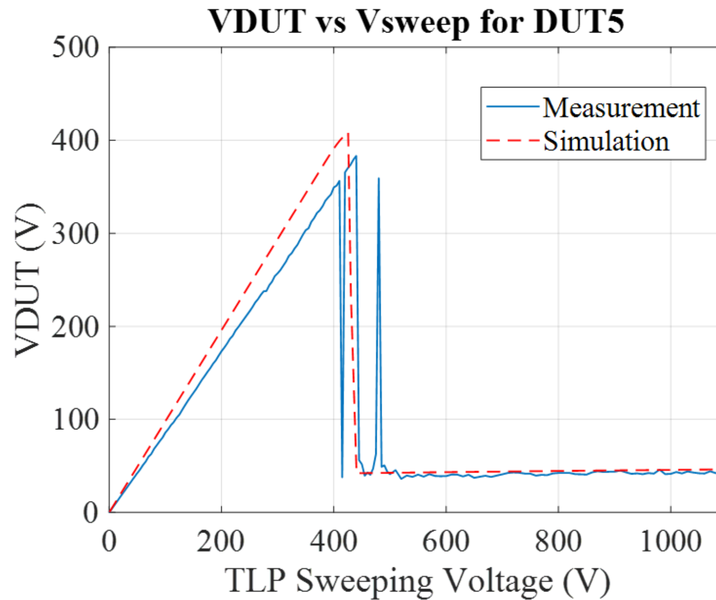

Figure 17. Quasi-static voltage at different TLP incident voltages for the spark gap like device.

These improvements in simulation indicate that the model framework can fit the measured response for spark gap like devices. The model fine tuning process is discussed in Section V.

4.4. VARISTOR

The quasi-static I-V curve of a varistor is similar to a non-snapback TVS diode. However, the curvature of the I-V curve is less steep. Figure 18 presents the simulated I-V curve for a typical varistor, and it shows a good match with the measured result.

When the ESD stress is low, the varistor voltage rising edge can be affected by its small signal capacitance, which can be tuned in the linear small signal sub-model. Here 45 pF (50 pF is reference value from datasheet) is determined as the small signal capacitance value from RF measurement. This value is used in the varistor simulation model. Figure

19 illustrates that the simulated VDUT peak values as a function of the TLP sweep voltage match the measured values. The varistor simulation model overestimates the voltage across the varistor when VTLP is higher than 300 V, as illustrated in Figure 20. Thus, the simulation would overestimate the stress on the IC, leading to a conservative system design.

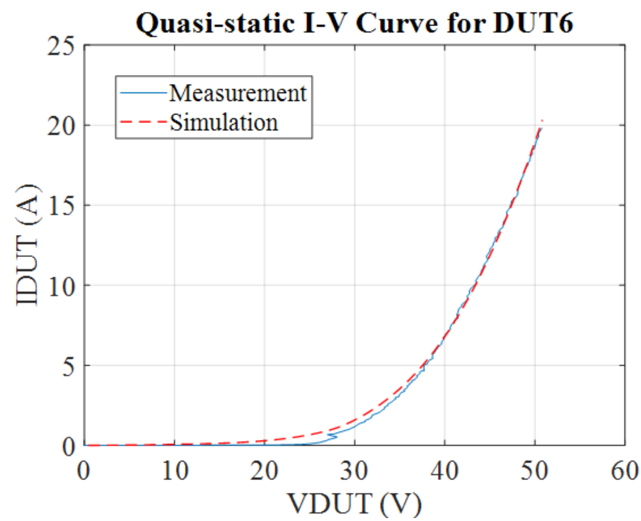

Figure 18. Simulated and measured quasi-static I-V curve for the varistor.

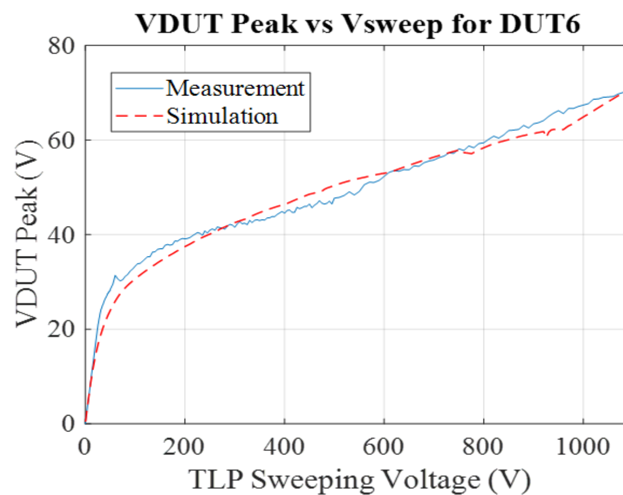

Figure 19. The simulated and measured VDUT peak values at different TLP sweep voltages for the varistor.

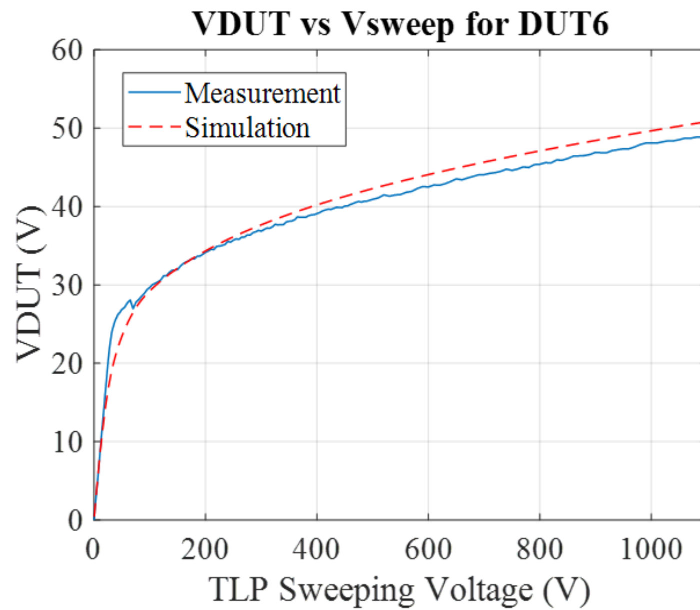

Figure 20. Quasi-static voltage across the varistor at different TLP sweeping voltages.

5. MODEL TUNING

The extraction method for the parameters in the TVS model framework is discussed in [5], but additional discussion on efficient model tuning is still nontrivial to guide people who are interested in this model framework to simulate various TVS components.

5.1. NON-SNAPBACK DEVICE

Only positive polarity injection path is discussed in this paper. For a non-snapback TVS, first leave the pre-clamping diode D5 open, and short the snapback-delay sub-model and the conductivity modulation sub-model. The D3 diode will be tuned first in the model. Three parameters of the D3 diode: Is, N, Rs are tuned. Figure 21 shows how to use the tuning mode in ADS software to tune the D3 diode, until the simulated quasi-static I-V

curve matches the measured curve. The parameter “Rs” helps change the RDYN; “Is” and “N” parameters help shift the curve towards left or right.

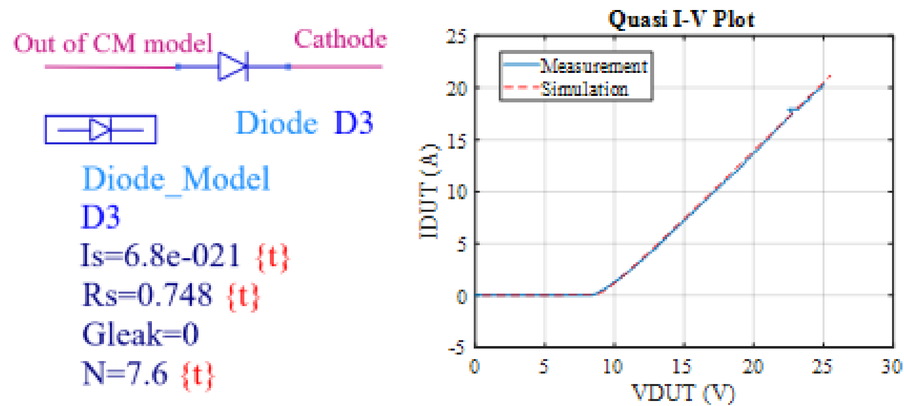

Figure 21. Quasi-static I-V diode model tuning.

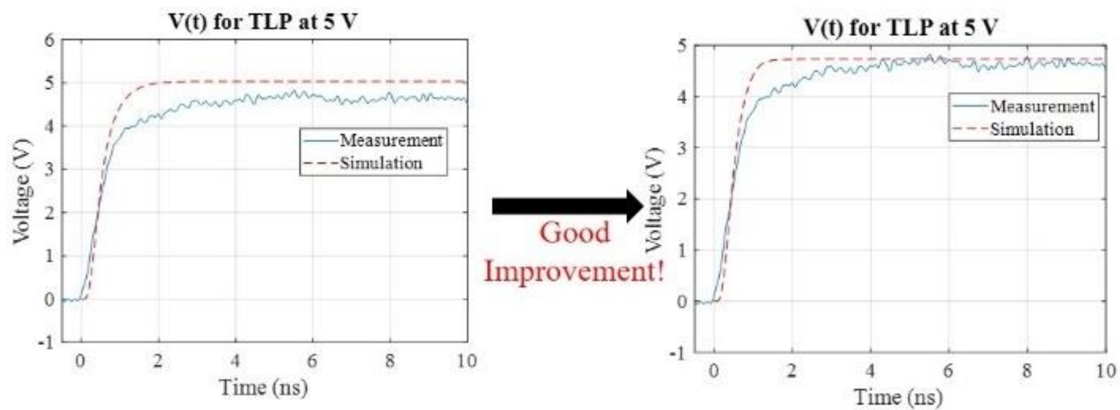

Figure 22. Before and after tuning preclamping diode.

As the diode triggers around 8 V, to determine the parameters for pre-clamping diode D5, plot out one of the time-domain voltage waveforms before it triggers. Tune the “Rs”, “Is”, and “N” parameters for the pre-clamping diode until the time-domain waveform matches the measured waveform as shown in Figure 22.

After tuning the pre-clamping diode parameters, looking at the time-domain voltage waveforms will help to decide if the conductivity modulation sub-model is needed to better match the time-domain waveforms. Figure 23 shows the conductivity modulation sub-model structure.

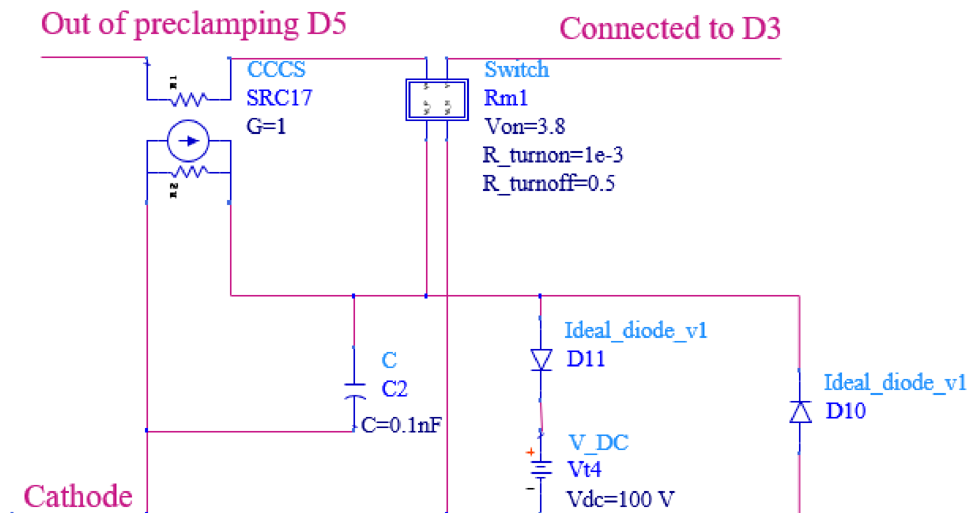

Figure 23. Conductivity modulation sub-model structure.

Figure 24 (a) shows the voltage overshoot magnitude and falling edge both mismatch between the simulation and measurement, although the deviations are not large, to improve the simulation performance, the conductivity modulation sub-model should be added. In the conductivity modulation sub-model except for default settings, “C2”, “Von” and “R_turnoff” are the three parameters which need to be tuned. The capacitor C2 is charged by the current to create a voltage that is used to change the resistance of the switch. Von is the voltage across the capacitor C2, it is used to control the conductivity by changing the value of the variable resistor. The variable resistance was created using a voltage-

controlled switch model, R_turnon is set to 1 mΩ and R_turnoff needs to be tuned manually.

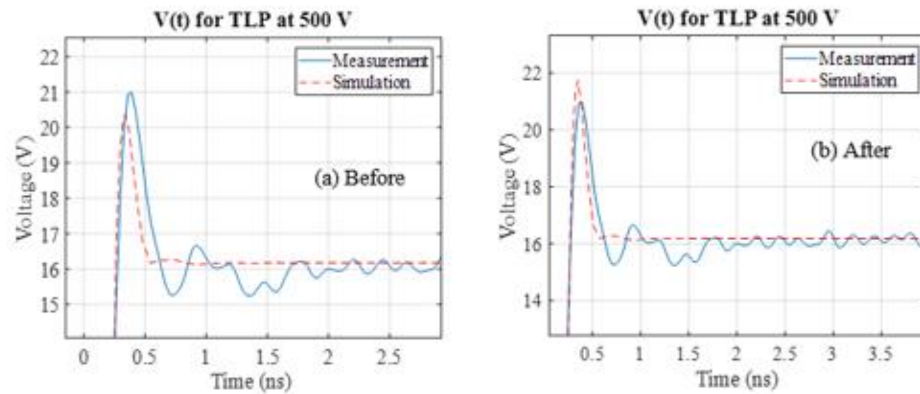

Figure 24. Voltage time-domain waveforms before and after adding the conductivity modulation sub-model.

To tune the parameters in conductivity modulation sub-model, first the C2 is set to 0.1 nF, as the conductivity modulation effect for this DUT is not dominating. Von mirrors how fast the voltage overshoot falls and the R_turnoff helps to fix the voltage peak value mismatch. When the TVS is on, select one of the time-domain voltage waveforms. The charge accumulated in C2 corresponds to a voltage value, which is the Von. If the Von is higher, it leads to a slower voltage overshoot falling edge in the time-domain waveform.

Secondly, assuming the inductance L of the TVS in small signal sub-model is accurate, the R_turnoff can be determined by the equation: Vpeak = Vind + R_turnoff * I [5]. Tuning the R_turnoff parameter value can further help to match the voltage overshoot.

After adding pre-clamping diode and the conductivity modulation sub-model, the quasi-static I-V curve will not have a good match with the measured I-V curve in most

cases. The final step is to fine tune the diode D5 parameters until the quasi-static I-V curve also matches with the measurement as illustrated in Figure 25.

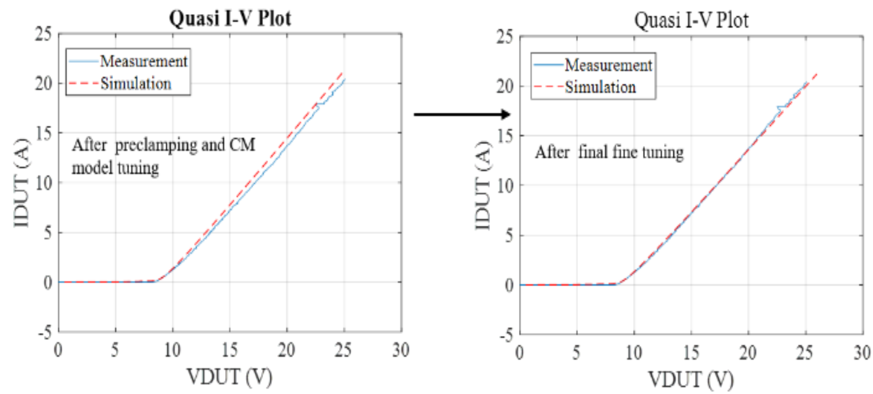

Figure 25. Fine tuning of the quasi-static I-V curve.

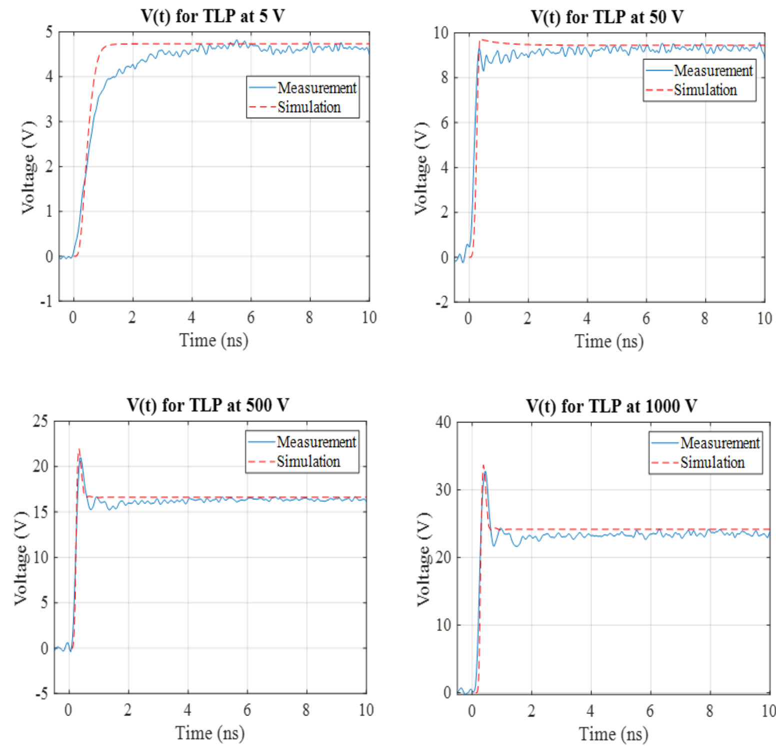

Figure 26. V (t) waveforms after fine tuning of the quasi-static I-V curve.

When the fine tuning of the quasi-static I-V curve is done, time-domain waveforms also need to be checked and can be fine-tuned as well. The time-domain waveforms are depicted in Figure 26.

5.2. SNAPBACK DEVICE

During the tuning process for a snapback TVS device, follow the tuning procedure provided for the non-snapback device by tuning the pre-clamping diode, conductivity modulation sub-model, and the quasi-static I-V diode sub-models.

The I-V curve at this stage should look like the response shown in Figure 27. After tuning these sub-models, then proceed with the tuning of the snapback delay sub-model to further improve the match to the measured data.

Figure 28 illustrates the details of the snapback delay sub-model. Although there are many variables and sources in the snapback delay sub-model, most of them are set at default settings and only “Vt1” and “Snapback_trigger” need to be tuned manually in most cases.

To obtain a better match to the measured I-V curve, snapback delay sub-model tuning is required for this TVS. From Figure 27, it is observed that the “Vt1” is about 25 V, so first set the Vt1 parameter to 25 V. After setting the Vt1 parameter to a fixed value, then proceed with tuning of the “Snapback_trigger” parameter.

When the fine tuning of the snapback delay is done, the time-domain waveforms also need to be checked and can be fine-tuned as well.

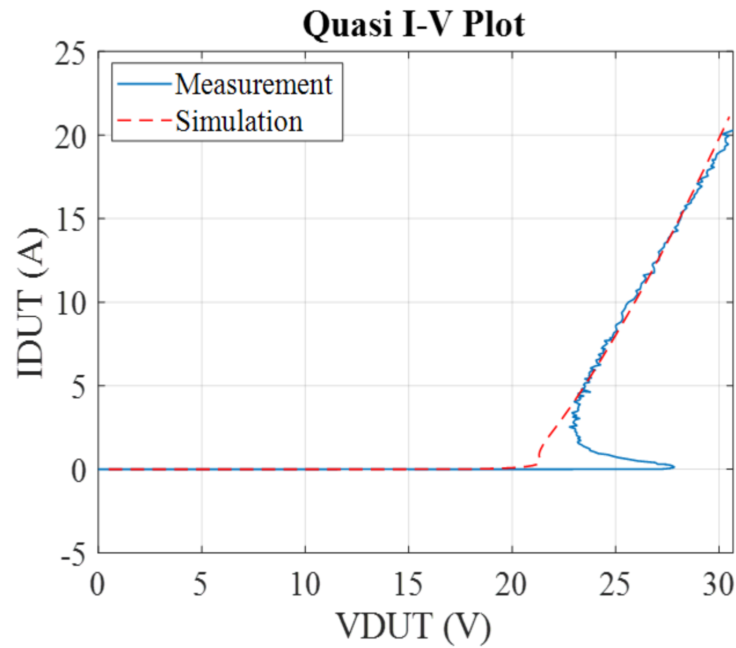

Figure 27. Quasi-static I-V curve of a snapback device without snapback delay sub-model in framework.

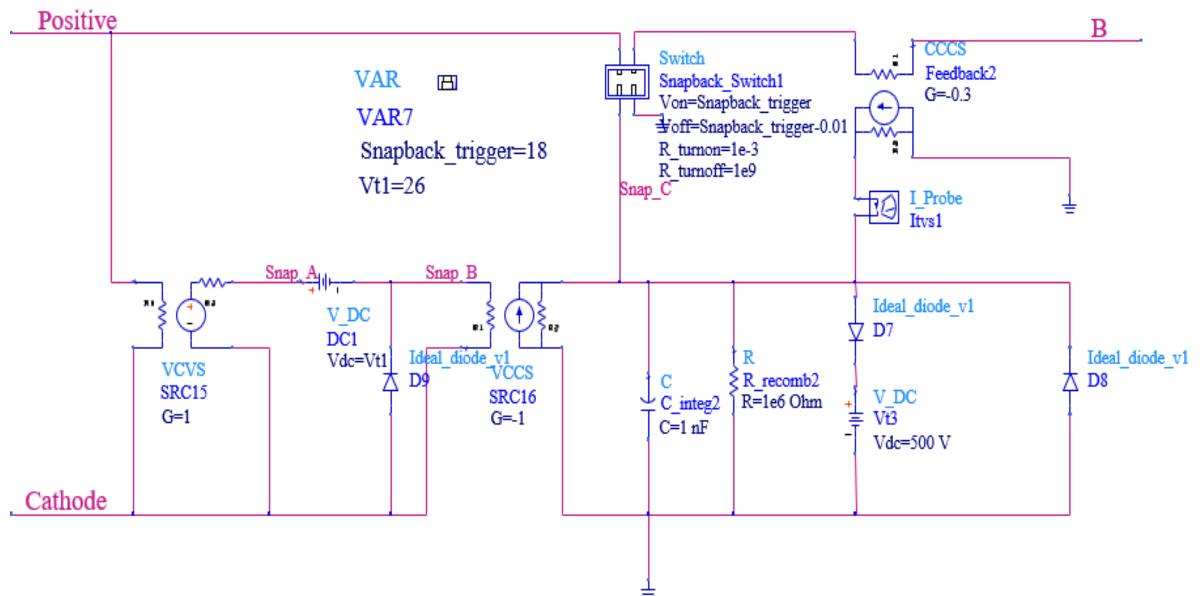

Figure 28. Snapback delay sub-model structure [5].

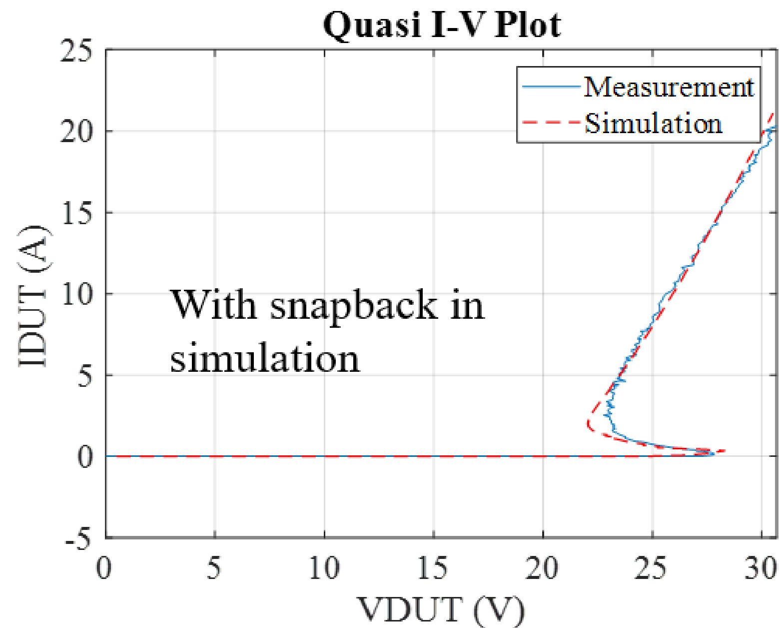

Figure 29. Quasi-static I-V curve of a snapback device after snapback delay tuning.

6. SEED MEASUREMENT AND SIMULATION

The interactions between the on-board protection and on-chip ESD protection can be analyzed by using SEED methodology [15]-[16]. A snapback TVS diode is selected to be the off-chip TVS protection diode. A non-snapback TVS is selected as the IC diode, which represents the on-chip ESD protection. In addition, series elements are introduced in between the off-chip and the on-chip TVS diodes to investigate the impact of the added series elements to improve the protection of the on-chip TVS diode. The TVS transient behavior model allows to investigate the interaction between the on-chip IC diode and the off-chip TVS protection diode during an ESD event.

Figure 30 shows the block diagram of the measurement setup for the standard transmission line pulse tester [6]. This simplified setup is designed to capture both the

quasi-static I-V curve for TVS devices and their transient time-domain waveforms. The standard TLP pulse length is 30 ns long and a voltage rise time filter of 200 ps is used. The current flowing through the TVS is measured at channel 3 in the oscilloscope, and the voltage across the TVS is measured at channel 1 in the oscilloscope. The average window setting from 21 ns to 27 ns of each pulse is applied to calculate the quasi-static voltage and current from the time-domain waveforms. The TLP voltage range of 0.5 V to 1200 V is applied to the DUT.

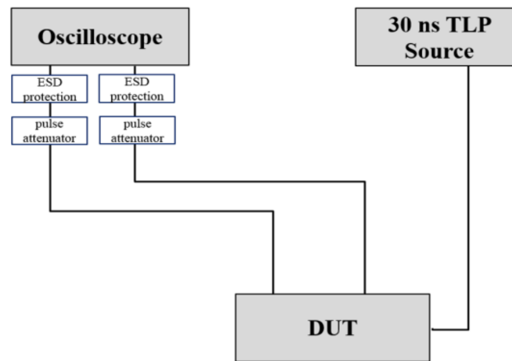

Figure 30. Simplified test setup for SEED measurement.

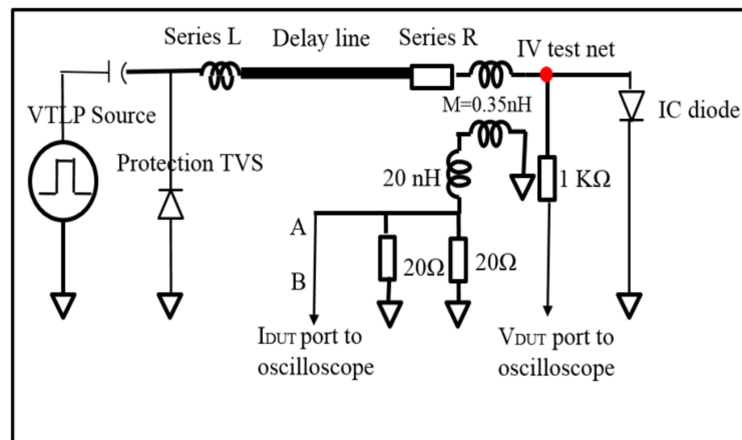

Figure 31. On-board measurement and simulation schematic diagram.

The voltage and current at the IC diode can be measured directly from the board during the TLP testing.

The frequency response of the current deconvolution structure is symmetric to the inductive coupling structure, which is simulated in ADS [6].

A damage threshold criteria for the IC diode is assumed to be at 1.5 V across the diode or at 2 A current through the diode.

To identify if the off-chip TVS and the IC diode combination can limit the input voltage and current sufficiently at the IC diode, the SEED measurement and simulation is performed.

At a maximum setting of 1200 V TLP voltage, it is observed in Figure 32 that the current into the IC diode is above the damage threshold criteria.

In this scenario, a series resistor of 2 Ω was added in between the off-chip TVS diode and the IC diode, but it did not provide sufficient ESD protection.

When the voltage of the IC diode is lower than 1 V, a small mismatch between simulated and measured current is observed. The simulation results show a good match when the IC diode voltage is higher than 1 V.

To help reduce the ESD current flowing into the IC diode, a 30 nH inductor is added in series. Figure 33 shows the current into the IC diode is within the damage threshold criteria at the highest TLP stress voltage.

Both resistor and inductor series elements contribute to limit the current flow into IC diode.

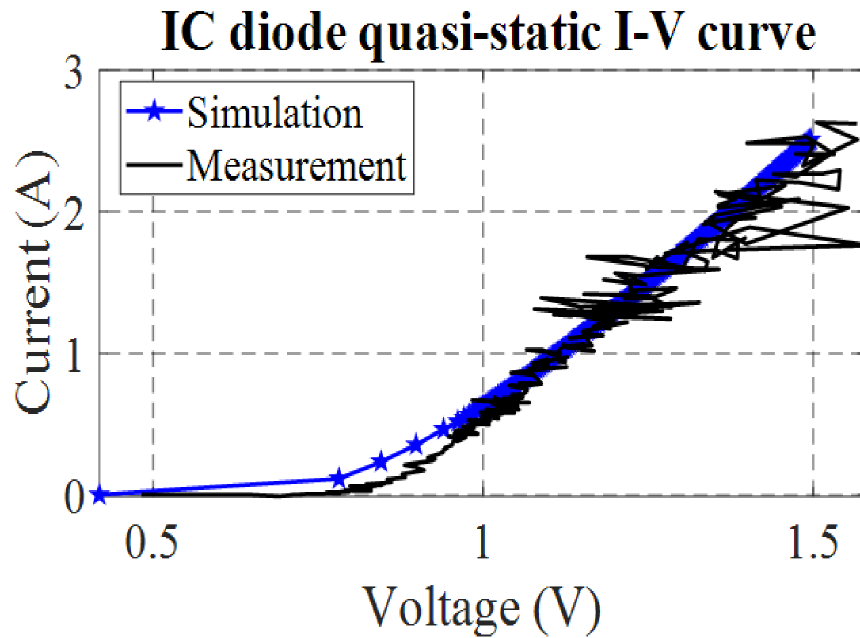

Figure 32. SEED simulation and measurement comparison with series R = 2 Ω and series L = 0 nH.

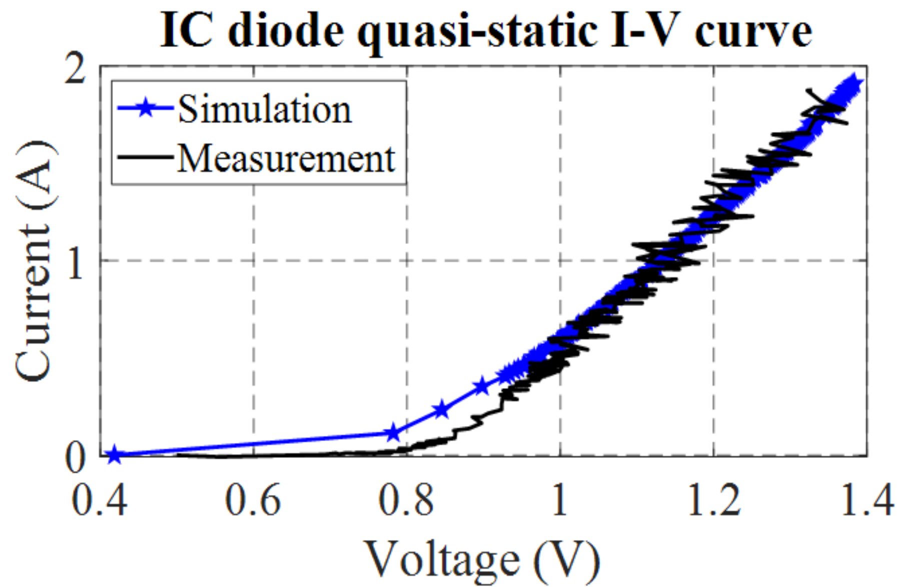

Figure 33. SEED simulation and measurement comparison with series R = 2 Ω and series L = 30 nH.

7. DISCUSSION

With respect to the TVS modeling, the experience with the modeling framework has shown that different classes of TVS devices can be modeled by the framework by adjusting its parameters. The SEED simulation results show the robustness of the simulation model. The protection race condition of the off-chip TVS diode can be studied in detail with this technique. The simulation model has been transferred into other SPICE solvers as it relies only on universal and generalized model elements.

8. CONCLUSION

For the snapback type TVS diode, the model framework was able to match both the transient peak voltage value and the quasi-static I-V curve within 10% error when compared to the measured data. Additionally, the effect of the dynamic conductivity change in the snapback TVS device can be simulated by the current model. For a non-snapback type TVS diode and varistor, overall, the model can simulate both the transient behavior and the quasi-static I-V curve within acceptable errors.

For a spark gap like device, this paper shows that the model can simulate the TVS component very well, as long as the fine tuning is carefully performed. The current pre-clamping diode sub-model is also improved to better fit the spark gap like device. In addition, the process of how to tune the parameters in the ADS model framework is explained in detail.

ACKNOWLEDGMENTS

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II. IMPROVED MODELING OF TRANSIENT VOLTAGE SUPRESSION DEVICES

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ABSTRACT

An improved circuit model for ESD protection devices is presented where the transient behavior of a single component can be fully described by a quasistatic very fast transmission line pulse (VF)-TLP and is applied to a snapback transient voltage suppression (TVS), non-snapback TVS, and varistor. The models are tuned based on characterizations of these protection devices, and then applied in system efficient ESD design (SEED) to predict the voltages and currents throughout a system consisting of an off-chip ESD protection device, an IC on-chip protection and a PCB trace in between, where the TVS was used to protect an on-chip diode. The modified conductivity modulation and updated snapback delay sub-model is valid for circumstances which present the interaction of various off-chip protection devices with the IC ESD protection.

1. INTRODUCTION

ESD protection devices are often placed on board to protect Integrated Circuits (ICs) from electrostatic discharge (ESD). The off-chip and on-chip protection must be designed to ensure the off-chip protection device turns on and shunts the ESD current away from the on-chip protection, so the on-chip protection does not take the full event and fail. A generic circuit model for discrete ESD protection devices which has high stability and broad utility can significantly improve the ability to optimize the ESD protection strategy. The System-Efficient ESD Design (SEED) methodology [1] provides a way to determine the interaction between the off-chip protection, passive components, and the internal protection within the IC. SEED simulations require highly accurate transient device models [2].

Several simulation models for TVS devices have been proposed. The models in [3] and [4] are easy to implement, but only accounts for the steady-state IV curve of the device, and not its transient characteristics. The authors in [5] and [6] proposed an improved model, but its ability to determining the voltage overshoot is limited.

For IC protection, the on-chip ESD protections often turn on quickly within several nano seconds, however, the off-chip devices turn on time can be long for those with a low-doped well, which makes device switching to the on-state status slower [7].

The conductivity modulation in the silicon was accounted for in [8], which presents a physics-based conductivity modulation sub-model which accurately describes the modulation of resistance. The improved conductivity modulation sub-model recognizes

that a threshold charge value must be reached within the low-doped region to enable conduction of the trigger current.

Here, on the premise of retaining the modular sub-models, an improved device model framework is used to capture the behavior a variety of TVS devices. A VF-TLP is used to characterize the turn-on behavior and quasi-static I-V curves are captured for simulation on component level in ADS.

The paper demonstrates how the improved model can be used to model not a prominent example device but discrete common ESD protection devices: non-snapback TVS, snapback TVS and varistor on component level. The model is valid in a SEED simulation to improve system level robustness for a test board consisting of consists of an off-chip ESD protection device, an IC on-chip protection and a PCB trace in between.

This paper is organized in the following way: Section II describes the models for ESD protection device. Section III presents the experimental characterization and modeling of the ESD protection devices. SEED simulation of the interaction of the off-chip TVS devices with an on-chip ESD protection diode is studied in Section IV. Section V discusses possible simulation convergence problems and their solution. The conclusions are presented in Section VI.

2. MODELS FOR ESD PROTECTION DEVICE

Figure 1 [9] shows a block diagram of the TVS model. For bipolar ESD protection devices, this model is symmetric for positive and negative injections. D1 and D2 are ideal diodes which determine if the positive or negative current path is activated. The nonlinear

large-signal model contains a pre-snapback model (D5 and D6), TVS turn-on behavior model (snapback delay model, and conductivity modulation model), and a quasi-static I-V model for holding characteristics after snapback (D3 and D4). The pre-snapback diodes allow for current flow before the voltage reaches Vt1, the snapback trigger voltage. In I-V curves, this is visible as a curvature of the IV curve for voltages below Vt1 and before snapback. Conductivity modulation model is to describe the conductivity change in a device due to the carrier concentration change of a semiconductor device.

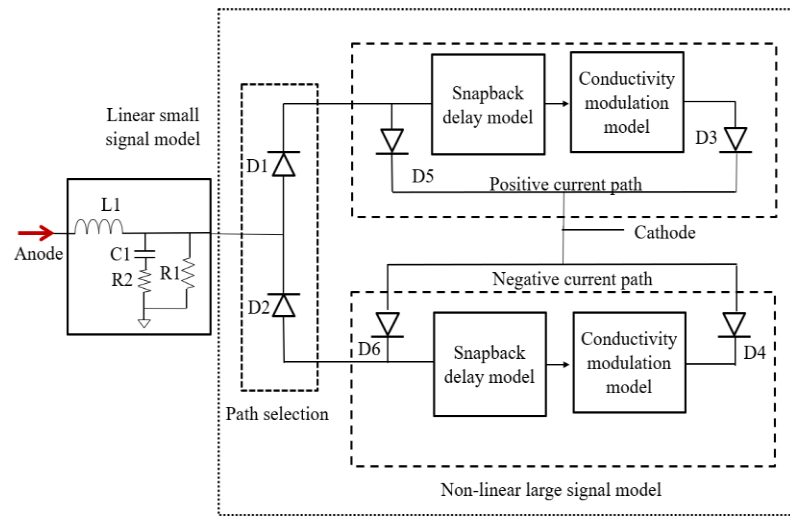

Figure 1. Block diagram of the protection device model.

The conductivity modulation sub-model is used to describe the change in conductivity in the device due to the change in the carrier concentration within low-doped regions. The initially lower conductivity of these regions will increase the voltage across the TVS beyond the value predicted by the quasi-static IV curve during the time of the transition. Figure. 2 shows the original structure of the conductivity modulation sub-model prior to modification. The on resistance, Ron, is small to allow other components to

determine the IV curve of the device. After the device is fully turned on, the P-N diodes D3 and D4 (Figure. 1) dominate the device behavior. Roff is tuned to mimic conductivity modulation after the snapback switch has been thrown. The current-controlled current-source (CCCS - Figure. 2) produces a current to charge the capacitor C2. The voltage across C2 determines when the conductivity modulation switch will switch from Roff to Ron. When the switch is thrown (and how long conductivity modulation is active) is determined by the amount of charge passing through the TVS device as set by the gain of the CCCS, the size of the capacitor, and the switch trigger voltage Von [10]. This circuit mimics the requirements that a minimum charge must be injected into the low-doped region of the protection device to increase its conductivity to its steady-state value.

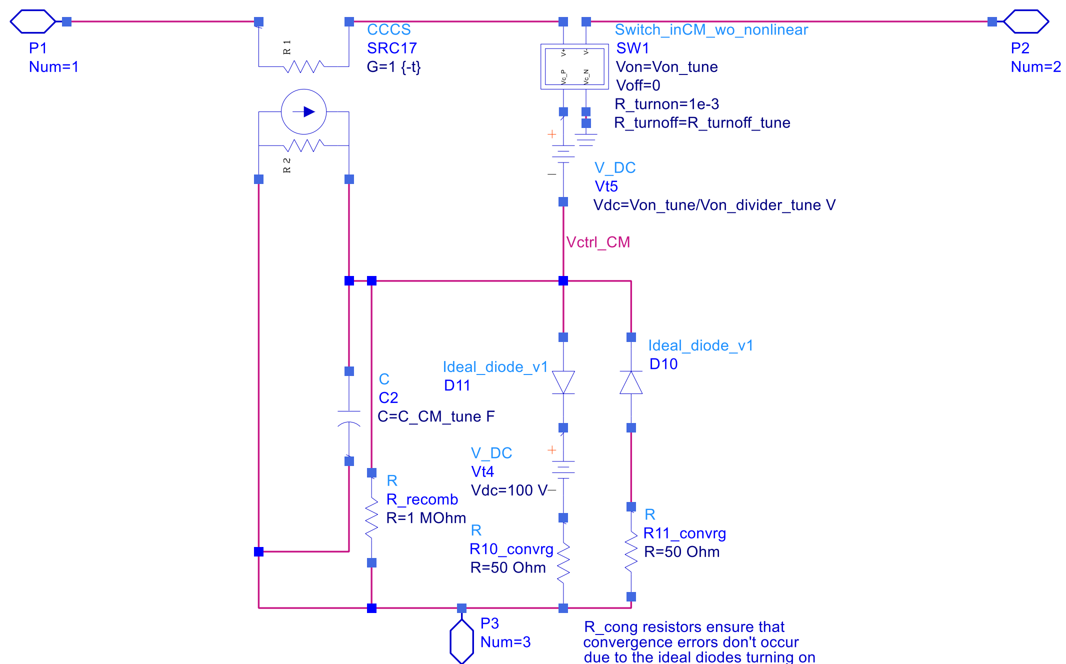

Figure 2. Conductivity modulation sub-model.

The advantage of this sub-model is that it simplifies understanding and the tuning of parameters. The user defined switch (Figure. 3) controlling conductivity modulation follows a numerical function which is not based on physics, however, which may not fully represent device behavior and may cause other problems during implementation. Equation (1) shows the relationship dictating the transition between turn on and off of the switch before improvement:

$$R_{Switch} = exp\left\{ln\left(\sqrt{R_{on}R_{off}}\right) + 3\,ln\left(\frac{R_{on}}{R_{off}}\right)\cdot\frac{V_{control}-\frac{V_{on}+V_{off}}{2}}{2(V_{on}-V_{off})} - 2\,ln\left(\frac{R_{on}}{R_{off}}\right)\cdot\left(\frac{V_{control}-\frac{V_{on}+V_{off}}{2}}{V_{on}-V_{off}}\right)^3\right\} \quad (1)$$

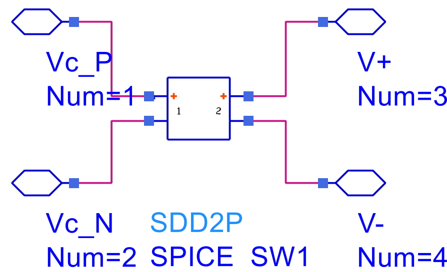

Figure 3. Switch used in conductivity modulation sub-model.

The improved model for conductivity modulation directly modulates the conductivity of the according to the delivered charge according to Equation (2) [7]:

$$R_{modulated(t)} = \frac{R_{off}}{1+\frac{Q_{charge(t)}}{Q_0}} \quad (2)$$

where R_off is the resistance when current first starts to flow, Q_(charge(t)) and Q_0 represent the total injected charge and the threshold charge the device must reach to trigger the conduction, respectively.

The modified circuit model for conductivity modulation is shown in Figure. 4. The changing resistance R_(modulated(t)) in the sub-model is controlled by the voltage

$Vcontrol_$CM across capacitor $C17$. The capacitor is charged by a current-controlled current-source, so that the voltage across the capacitor is directly proportional to the charge injected into the system.

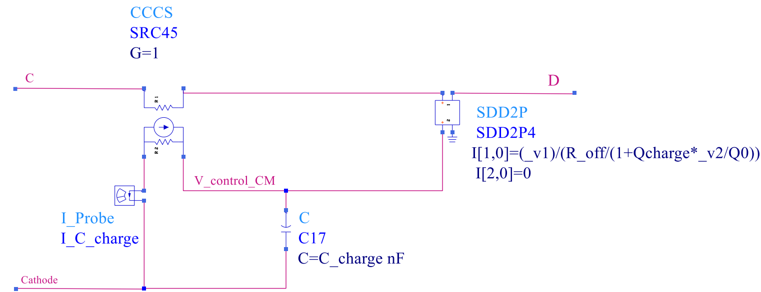

Figure 4. Improved conductivity modulation model.

A second modification was added to the snapback model further improve the transient behavior of the model [11]. With only a single switch the fall time of the voltage across the model is much faster than is observed in practice. A second switch and RC-control circuit, highlighted switch in Figure. 6, was added to better capture the snap-back turn-on behavior.

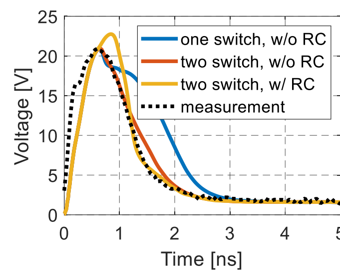

Figure 5. Snap-back delay sub-model requires a second switch [11].

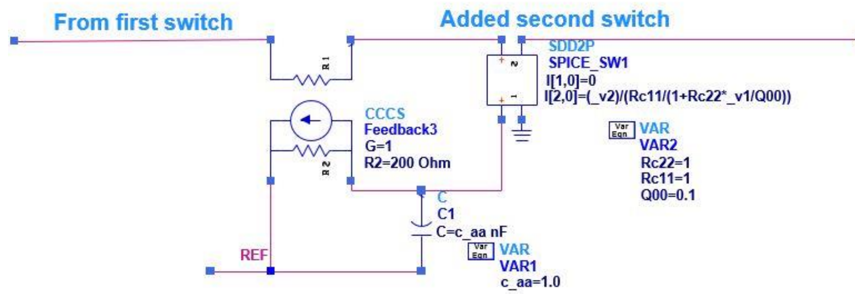

Figure 6. Improved snapback sub-model.

The ability of the improved model to accurately represent a variety of ESD protection devices is investigated in the following sections by comparing measurement and simulation data of a snapback TVS device, a non-snapback diode, and a varistor.

3. DEVICE CHARACTERIZATION AND MODELING

3.1. SNAPBACK TVS DIODE: PESD3V3Y1BSF

A bidirectional TVS with a low trigger-voltage and low clamping voltage was selected for investigation. This device also had a low parasitic inductance associated with it. Figure 7 shows the measured I-V curve for this device.

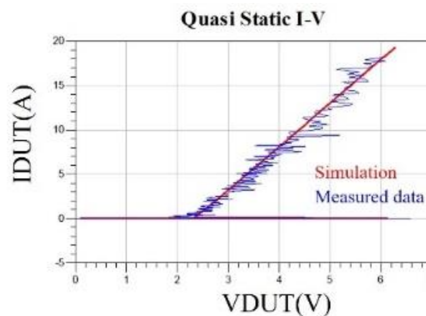

Figure 7. I-V curve of a snapback TVS device.

Figure 8 shows the simulated transient response of the snapback diode before modification of the device model. The old model correctly captures the IV curve of the device and reasonably captures the transient voltage overshoot, but the falling edge of the voltage waveform is not captured well and some improvement in the capture of the transient peak is possible. Figure 9 shows the simulated transient voltage using the improved device model. Both the magnitude of the peak and the shape of the waveform are better captured.

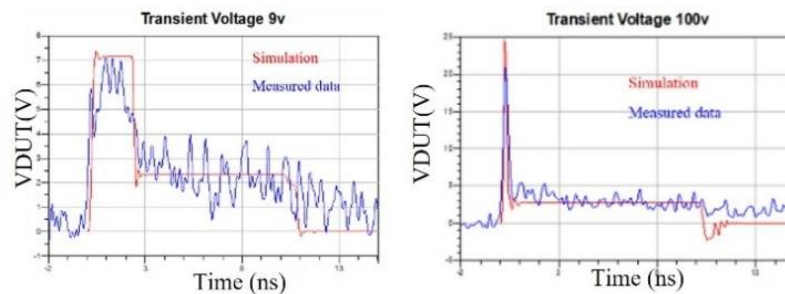

Figure 8. Measured and simulated transient response of TVS snapback device using the old device model.

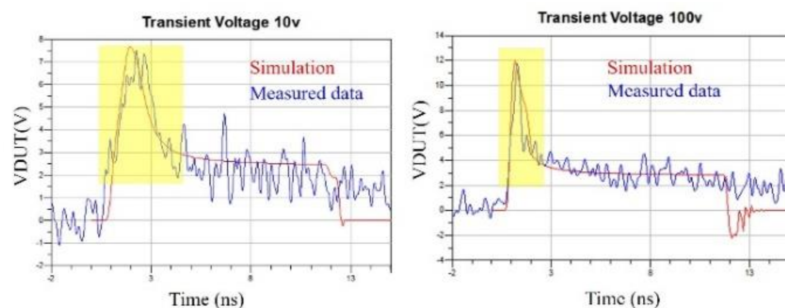

Figure 9. Measured and simulated transient response of TVS snapback device using the improve device model.

3.2. NON-SNAPBACK TVS DIODE

Figure 10 shows the simulated and measured I-V curves for a non-snapback TVS diode. Results are shown for both the old and the improved device models. Both capture the quasi-static behavior of the device well.

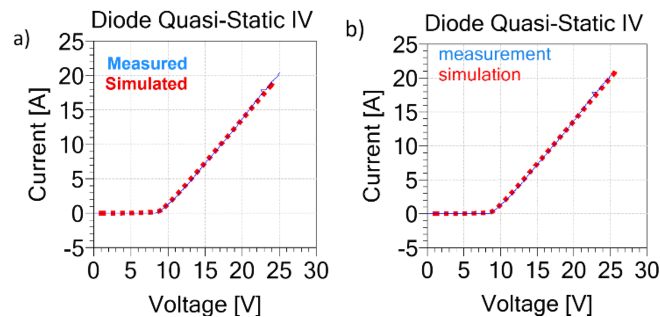

Figure 10. Measured and simulated IV curves of a non-snapback TVS diode using the (left) old model and (right) improved model.

A comparison of the simulated and measured transient response of the non-snapback diode is addressed in Figure 11.

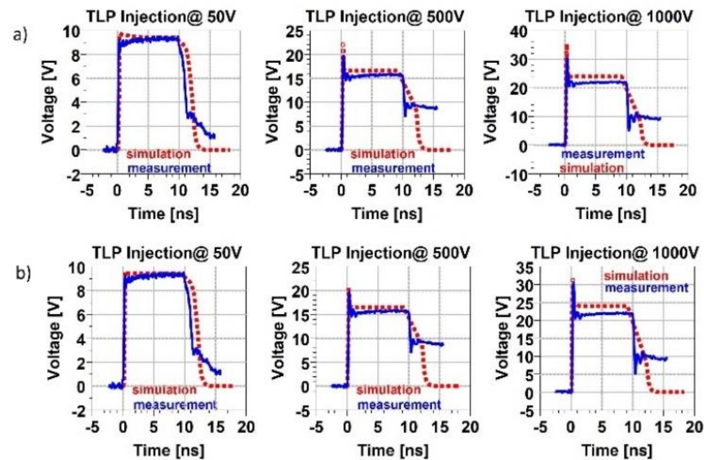

Figure 11. Measured and simulated transient response of non-snapback TVS device (top row) using the old TVS model and (bottom row) using the improved TVS model.

The improved model better captures the transient voltage overshoot. For this non-snapback TVS, the impact of the snapback switches on the transient response is negligible since there is no snapback to speak of.

3.3. VARISTOR

The “quasi-static” I-V curve of a metal-oxide varistor (Figure 12) is similar to the non-snapback TVS diode, but the current rises more slowly with voltage due to their slow response time.

Here, the current and voltage was measured 10 nS after the onset of the TLP pulse, and the varistor may not have reach its full current at that point. Comparison of the simulated and measured I-V curves in Figure 12 show both the old and improved device models predict the curve well.

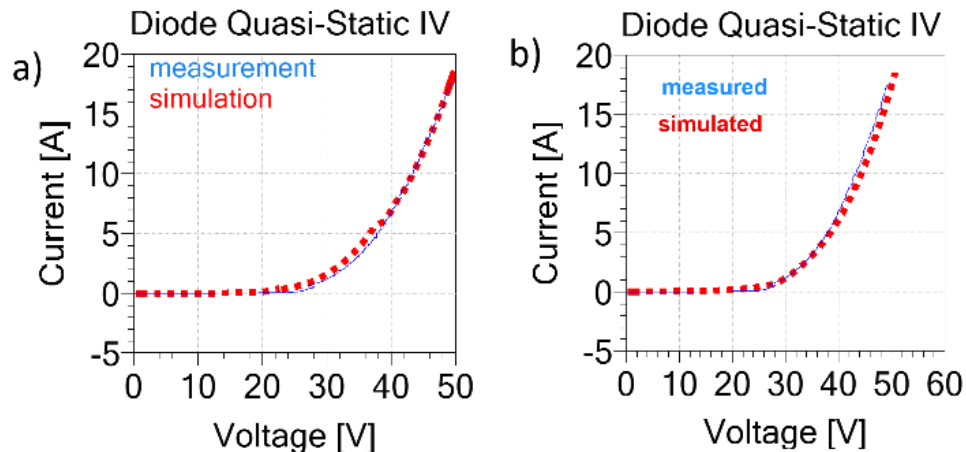

Figure 12. Measured and simulated IV curve for a varistor using (left) the old model and (right) the improved model.

Figure 13 shows a comparison between the simulated and measured transient response of the varistor. During conduction, the varistor voltage remains relatively constant even when the current changes by several orders of magnitude.

The impact of conductivity modulation effect on a varistor is therefore significant. The improved model was able to better capture the transient voltage response as demonstrated in Figure 13.

Setting the parameters for the conductivity modulation sub-model was particularly important for this device.

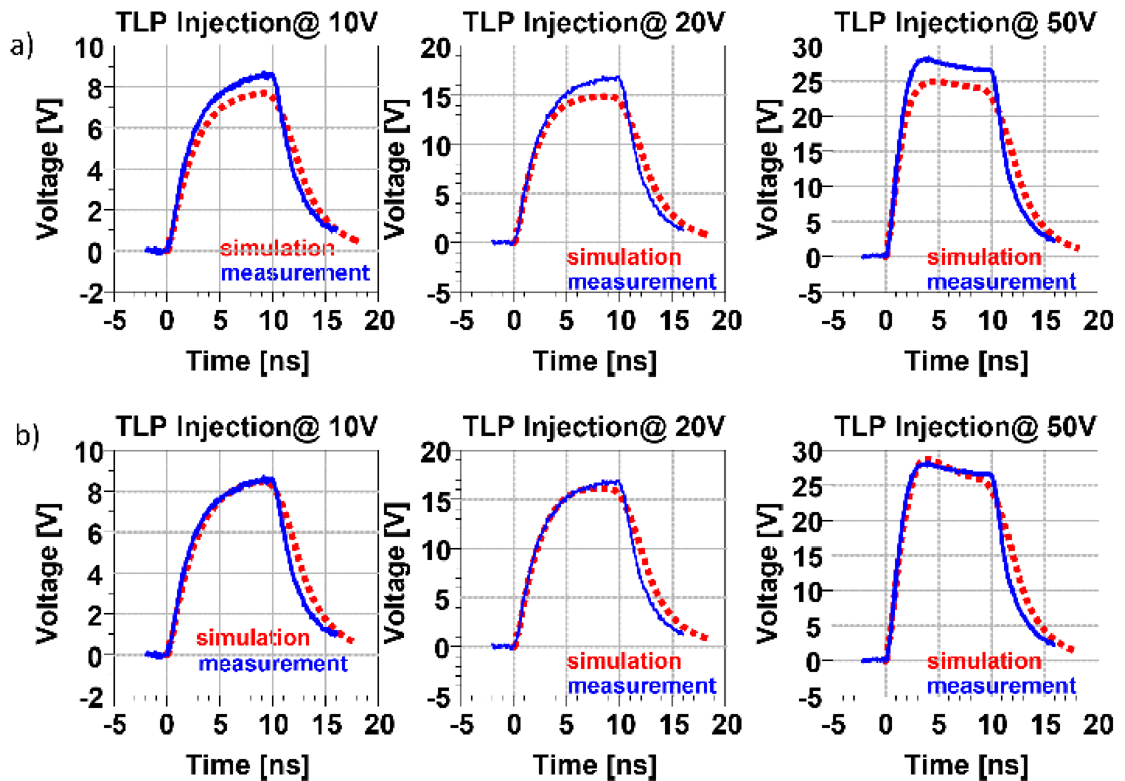

Figure 13. Transient response of varistor a) w/o and b) with modified TVS model.

4. PREDICTING INTERACTION OF OFF-CHIP ESD PROTECTION AND ON-CHIP DIODE

The ability to predict the interaction between two ESD protection devices is more challenging than capturing the behavior of one device alone. This ability was validated for each device using a SEED simulation where an off-chip ESD protection device protected an IC with an on-chip protection diode, with a PCB trace in between (Figure 14).

Measurements were performed on a customed PCB board [11]. Instead of using a real IC, the IC was replaced by a simple diode, which was also modeled using the improved modeling approach (Figure 15).

Between the TVS device and the IC there was a 50-ohm PCB trace. The ESDEMC TLP was connected via an SMA connector to the input of the board. The voltages and currents on the board were captured using one 12 GHz Agilent DSO81204B oscilloscope with 40 GSa/s and one 2 GHz 10 GSa/s Rohde & Schwarz oscilloscope. The length of the TLP pulse was set to 20 ns. The rise-time of the VF-TLP pulse was varied from 0.65 ns to 5 ns.

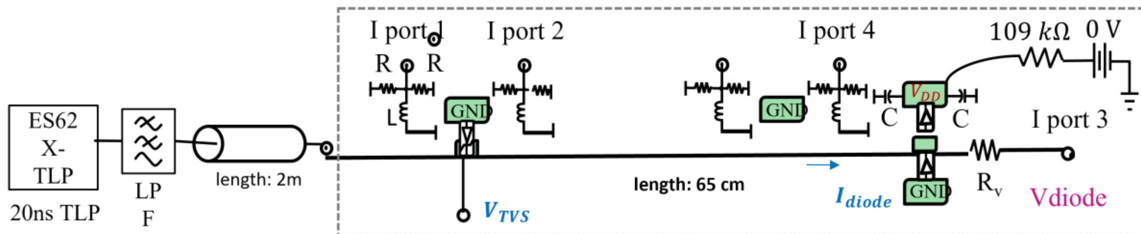

Figure 14. SEED test configuration.

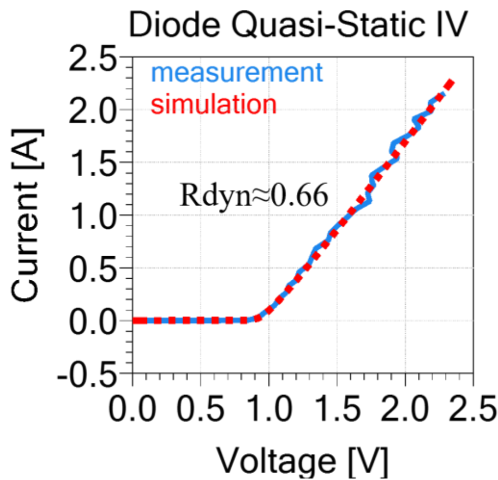

Figure 15. Measured and simulated I-V curve for the “on-chip” ESD protection.

Measurements were performed using 20 ns wide TLP pulses with levels from 10 V to 94 V with a linear step size of 6 V. Voltage and current waveforms at the off-chip and on-chip protection devices were captured during each pulse and saved to disk. Information regarding the quasi-static and peak and current through each device was extracted to demonstrate the performance of the device models. The measured TLP voltage when injecting into a 50-ohm load (Figure 16) was used in the SEED simulations.

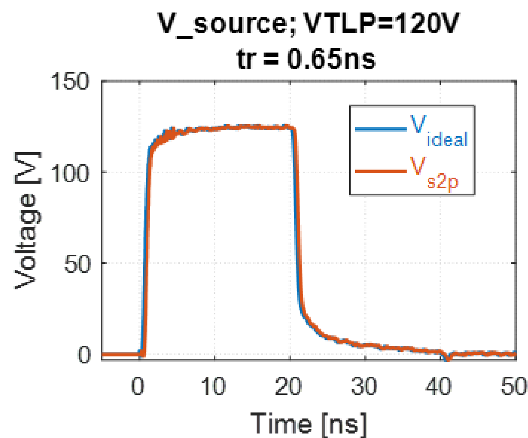

Figure 16. Example for measured TLP source.

4.1. SNAPBACK TVS DIODE WITH ON-CHIP DIODE

Figure 17 shows the measured and simulated results when the snapback TVS was used to protect the on-chip diode. In most cases, the quasi-static and peak currents were predicted within a few percent. The peak TVS and diode current was more challenging to capture for a slow rise time, but overall was acceptable (generally within 5%).

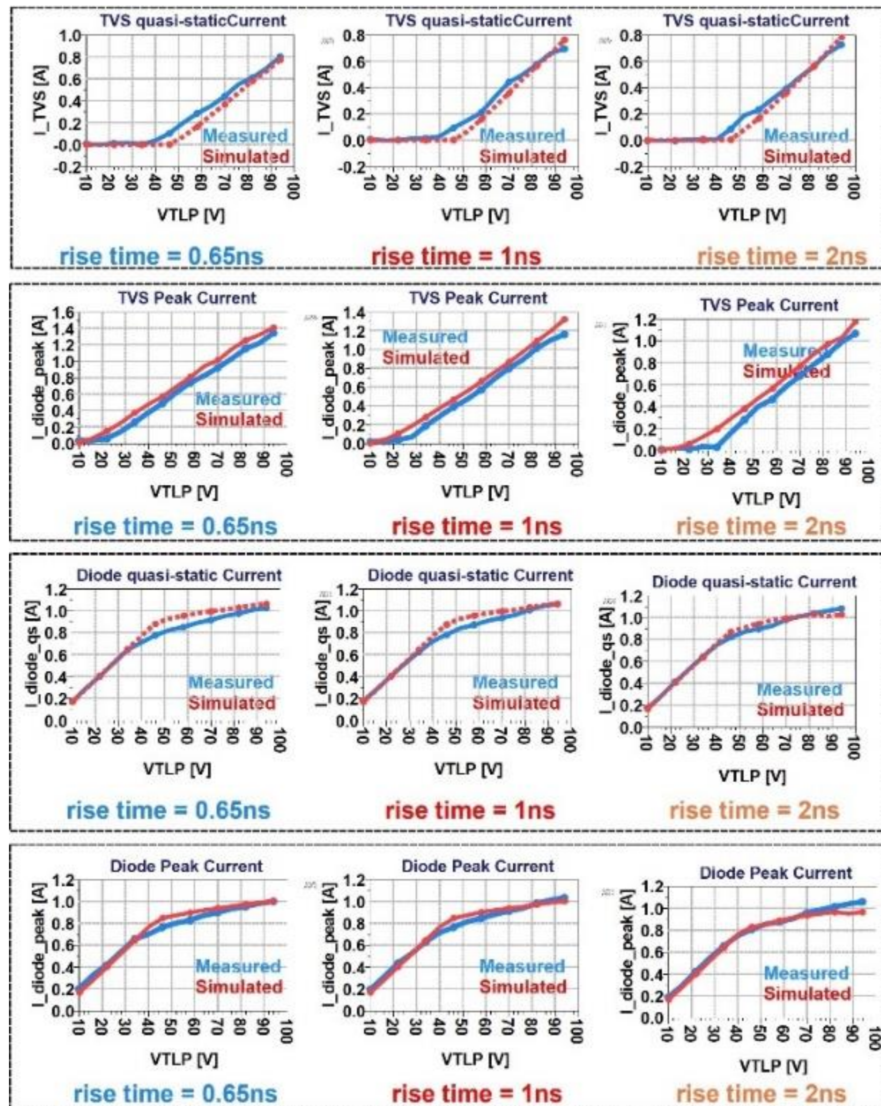

Figure 17. Simulated and measured voltages and currents when the snapback TVS diode was used with the on-chip diode.

4.2. NON-SNAPBACK TVS DIODE WITH ON-CHIP DIODE

The 20 ns TLP injection with levels from 120 V to 400 V with a linear step size of 20 V was used to test the non-snapback TVS protecting the on-chip diode.

An example for the transient response of off-chip non-snapback TVS and the IC protection are given as well (Figure 18).

Figure 18 presents the comparison between the simulation and measured data from low injection level to high injection level for both the IC diode and the TVS.

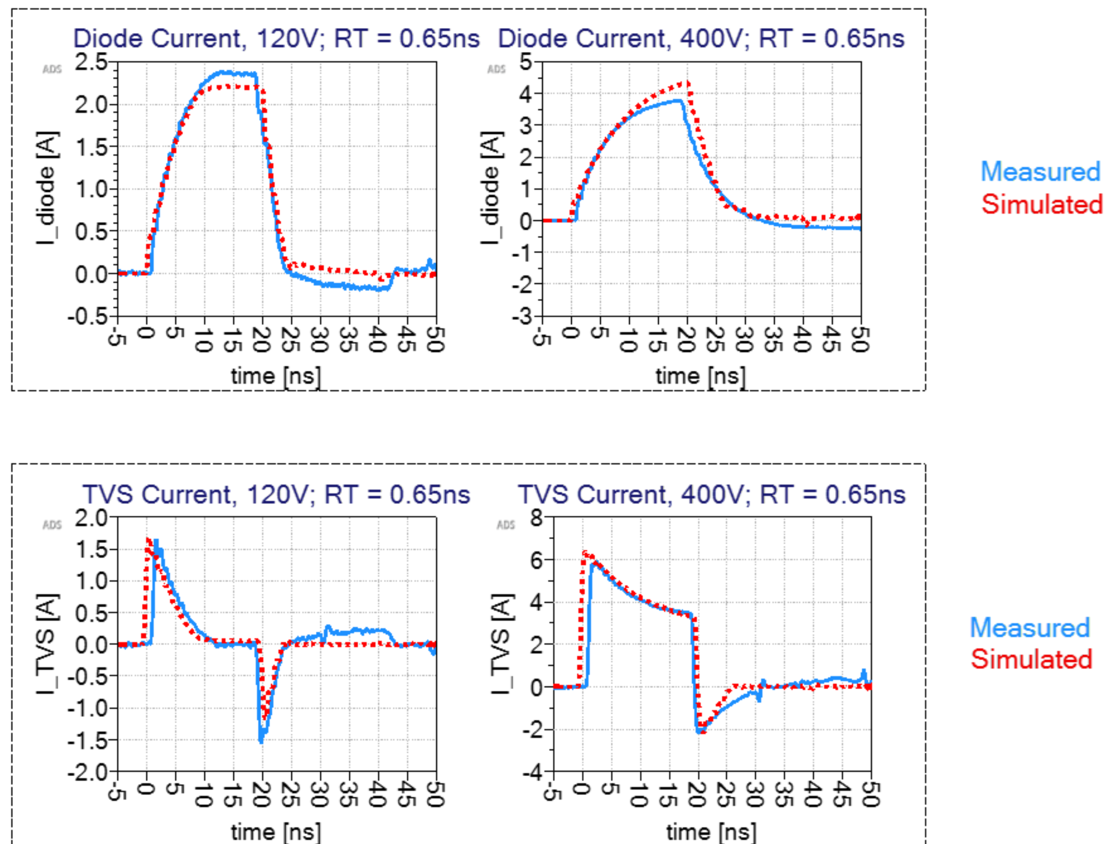

Figure 18. Transient response for the off-chip non-snapback TVS and IC protection diode.

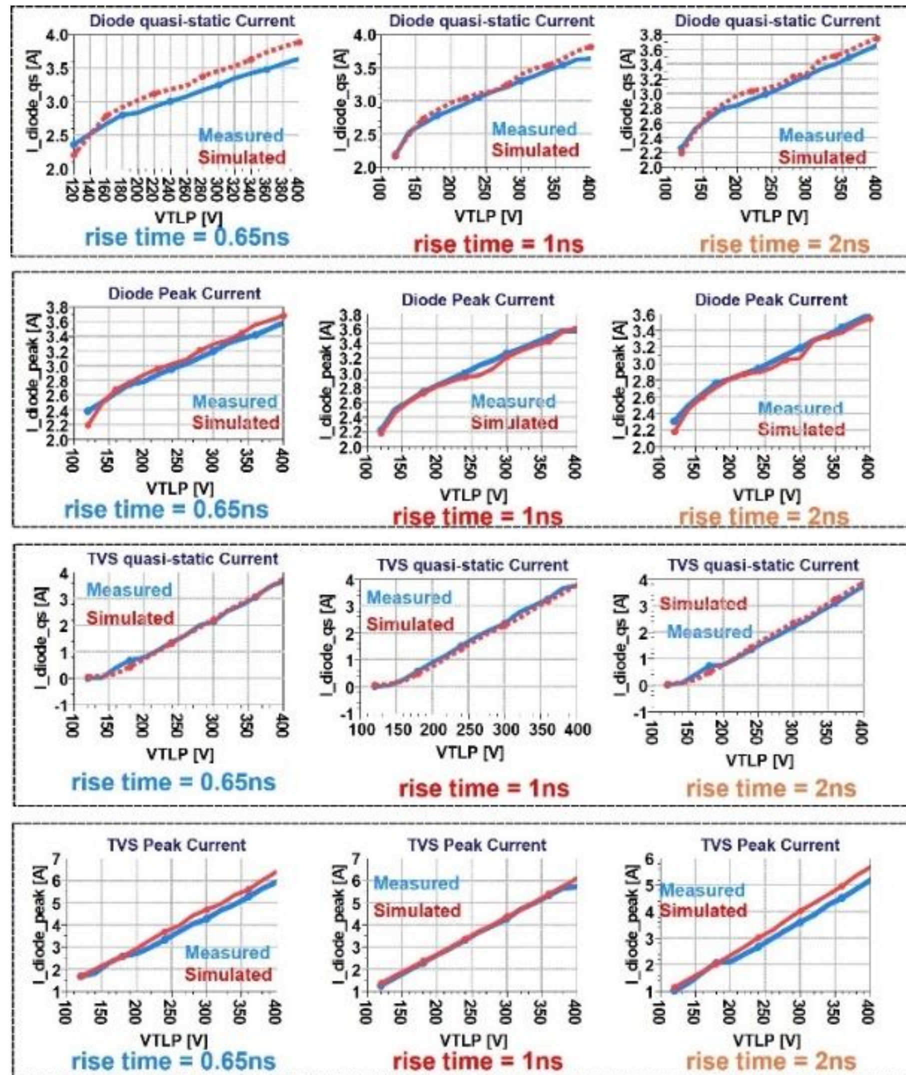

Figure 19. Simulated and measured voltages and currents when the non-snapback TVS diode was used with the on-chip diode.

Figure 19 shows the simulated and measured results. Quasi-static currents and peak current with rise times up to 2 ns were captured within a 2% error range.

4.3. VARISTOR WITH IC PROTECTION

Figure. 20 shows the simulated and measured results when a varistor was protecting an on-chip diode. While results are acceptable, the model performance with the varistor

was modestly worse than with the other devices, in particular when predicting the peak current through the varistor itself. This error results when the rise time of the current associated with the varistor turn-on varies between the measurement and the simulation, since the current often does not reach its peak level over the duration of the 20 ns TLP.

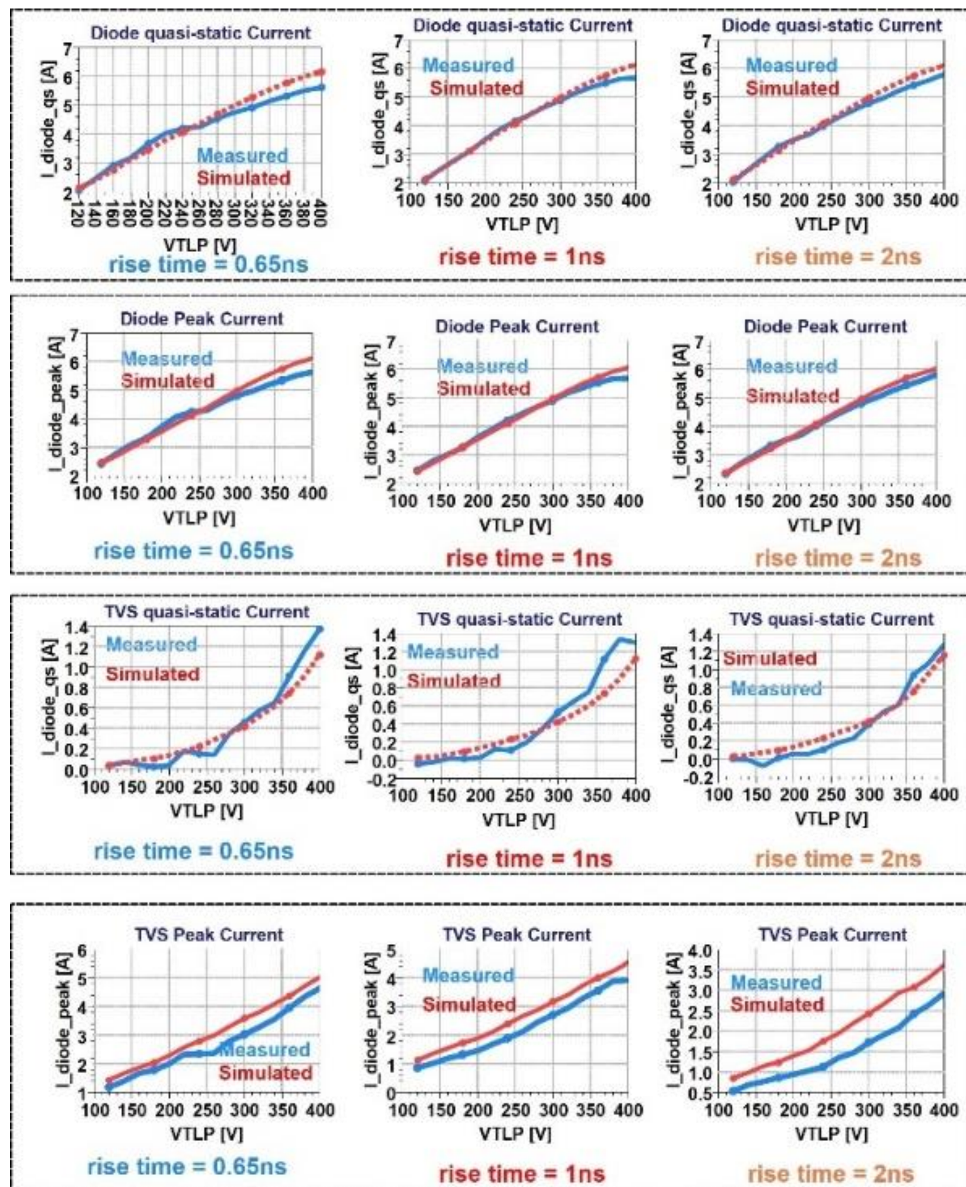

Figure 20. Simulated and measured voltages and currents when the varistor was used with the on-chip diode protection.

5. CONVERGENCE PROBLEMS

The fast non-linear responses of the ESD protection device working and the diode working in parallel can cause SPICE simulation convergence issues. The complexity of the device model and value of the model parameters can increase the risk of non-convergence. Controlling the V_off value in Snapback_Switch1 at a reasonable value is important. Secondly, tuning the value of the RC low pass filter (Figure. 21) parameters will also help slow down the snapback.

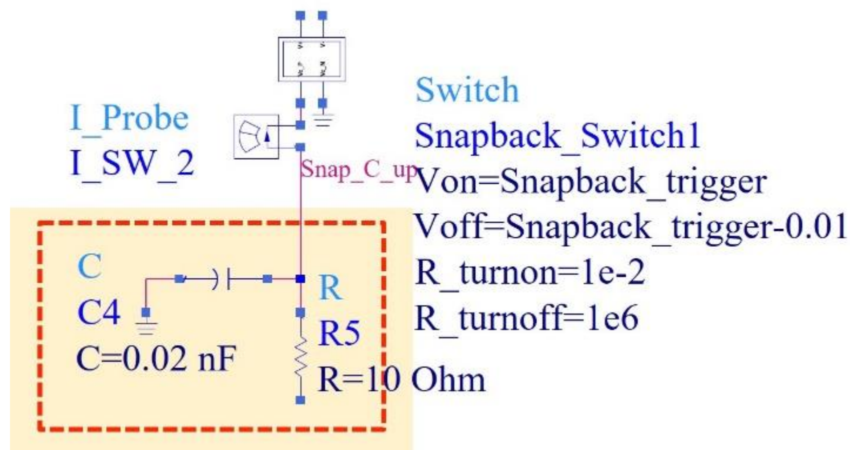

Figure 21. First snapback switch in sub-model structure.

There is no single solution for solving convergence problems. If the above suggestions do not allow the simulation to converge, one may also:

- Vary the SPICE integration coefficient, mu.
- Increase the time-point iteration limit.
- Adjust the current and voltage relative and absolute tolerances.

6. CONCLUSIONS

The improved model for ESD protection devices shows it can closely predict measured results for a variety of different protection devices, and when two models are used together to predict the behavior of an off-chip protection device protecting an on-chip diode. Performance was worst for slow rise times, but still within 10% of measurements for nearly all of the cases studied, considering both peak and quasi-static currents through both the diode and the TVS, which is well within the acceptable levels of accuracy. Where the model performs best depends somewhat on how the model is tuned. The additional components added here do not add substantially to the overall tuning effort, but make can make significant improvements to performance, particularly when modeling snapback devices. The improvement to a non-snapback diode is modest-to-negligible since both improvements primarily address the snapback behavior of the protection device. Convergence can be an issue when simulating multiple models together in the same system, as was done here, but can be addressed by either slowing down the switching of parts of the model or by modifying SPICE simulation parameters. Overall, the improved model appears useful for predicting the transient behavior of a wide variety of ESD protection devices.

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SECTION

2. CONCLUSIONS

A comparison of the improved ESD protection devices with measurement results shows very good agreement. The simulation work also is valid for the stability of the model and broad ESD protection elements the model can fit. This research emphasizes the generic utility of the modified device model and addresses the tuning required for using the device model.

VITA

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