Spring 2022

Modeling strategy for EMI filter and flyback transformer

Ruijie He

Department: Electrical and Computer Engineering

MODELING STRATEGY FOR EMI FILTER AND FLYBACK TRANSFORMER

by

RUIJIE HE

A DISSERTATION

Presented to the Graduate Faculty of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

DOCTOR OF PHILOSOPHY

in

ELECTRICAL ENGINEERING

2022

Approved by:

Chulsoon Hwang, Advisor
Victor Khilkevich, Co-Advisor
Jun Fan
Daryl Beetner
Daniel Fischer

PUBLICATION DISSERTATION OPTION

This dissertation consists of the following three articles, formatted in the style used by the Missouri University of Science and Technology.

Paper I: found on pages 5-25; Modelling Strategy for Film Capacitors in EMI Filters, has been accepted by 2019 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+SIPI).

Paper II: Pages 26-50; Modeling Strategy for EMI Filters, has been accepted by IEEE Transactions on Electromagnetic Compatibility 2020.

Paper III: Pages 51-71; Study on the root cause of the variation in conducted emissions of flyback converters, will be submitted to IEEE Letters on Electromagnetic Compatibility Practice and Applications 2022.

ABSTRACT

The switch-mode power supply is key to miniaturizing power adapters. However, the switching nature of the circuit introduces issues in conducted emissions. In a flyback converter, the transformer serves as the path for common mode current flowing from the primary side to the secondary side. Different winding technologies have been invented and implemented to reduce the capacitance between the primary side and the secondary side. But the repeatability of the winding is still poor due to the fluctuations of the winding machine. Thus, the resulting conducted emission has a fluctuation that can lead to failure in the compliance tests. EMI filter is another module implemented to reduce the conducted emissions. Due to the miniaturization, the components inside a filter are closely placed, therefore, strong mutual parasitics. These parasitics degrade the performance of the EMI filter. Overall, it would be beneficial if the performance of the EMI filter and the fluctuation of the transformer can both be analyzed through pre-design simulation. In this dissertation, a model strategy for EMI filters is developed and validated through comparison with measurement. The strategy covers different types of film capacitors, common mode chokes, and circuit topologies. This dissertation also provides an approach to asserting the parasitic capacitance of transformers through 2D analysis. Contradictory to the existing models that relate the parasitic capacitance and conducted emissions, the best-performance capacitance is found not zero. A simplified circuit model is developed to associate the conducted emissions with the parasitic capacitance of the transformer. This circuit model leads to an analytical formulation for evaluating the best-performance parasitic capacitance of the transformer, and its prediction matches with the observed relationship in the measurement. In conclusion, the research in this dissertation clarified the procedure for utilizing computer-aided simulation to guide the design of EMI filters and flyback converters in compact designs.

ACKNOWLEDGMENTS

The pursuit for PhD degree is a road full of obstacles. Fortunately, I have received all kinds of support during this journey.

I would like to thank my advisor, Dr. Chulsoon Hwang, and my co-advisor, Dr. Victor Khilkevich for their priceless inspiration, guidance, and inclusiveness.

I would like to thank Dr. Jun Fan, Dr. Daryl Beetner, and Dr. Daniel Fischer for serving on my doctoral committee and providing helpful feedback on my research work.

In addition, I would like to extend my appreciation to all the faculty members, staffs, and students in the UMR/MST EMC Lab.

Finally, my deepest love and gratitude to my family, who unconditionally love me and support me through the ups and downs during my pursuit for PhD degree.

This dissertation is based upon work supported partially by the National Science Foundation (NSF) under Grant No. IIP-1916535.

TABLE OF CONTENTS

Page

LIST OF ILLUSTRATIONS

PAPER II

PAPER III

LIST OF TABLES

1. INTRODUCTION

With the miniaturization of electronic products and trend of unibody design, the components inside a product become more and more compact. At the same time, demands for faster charging becomes higher and higher. Consequentially, the conducted emissions of the consumer electronics becomes a more challenging issue. This work studies the modeling for both the EMI filter and the noisy component on a consumer electronics product. The locations of the EMI filter and the noisy component are shown in Figure 1.1

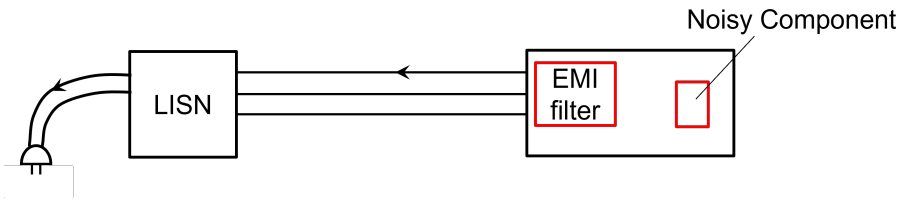


Figure 1.1. A typical setup for conducted emission test.

1.1. CHALLENGES WITH EMI FILTER DESIGN

The intent of the conducted emission limits is to restrict the noise current passing out through the product's ac power cord. EMI filters are dedicated to reducing the noise current passing out through the AC power cord. Therefore, the EMI filter performance is key to success in the EMC design. Figure 1.2 shows the components of a typical EMI filter.

The performance of an EMI filter is subject to the self parasitics of individual components and mutual couplings among the components. During the design of an EMI filter, the first step is usually looking for components that have effective nominal values (Figure 1.3.a.). Then the self parasitics of the components are includes into the circuit model. For products that the components can be sparsely placed, the design of the EMI

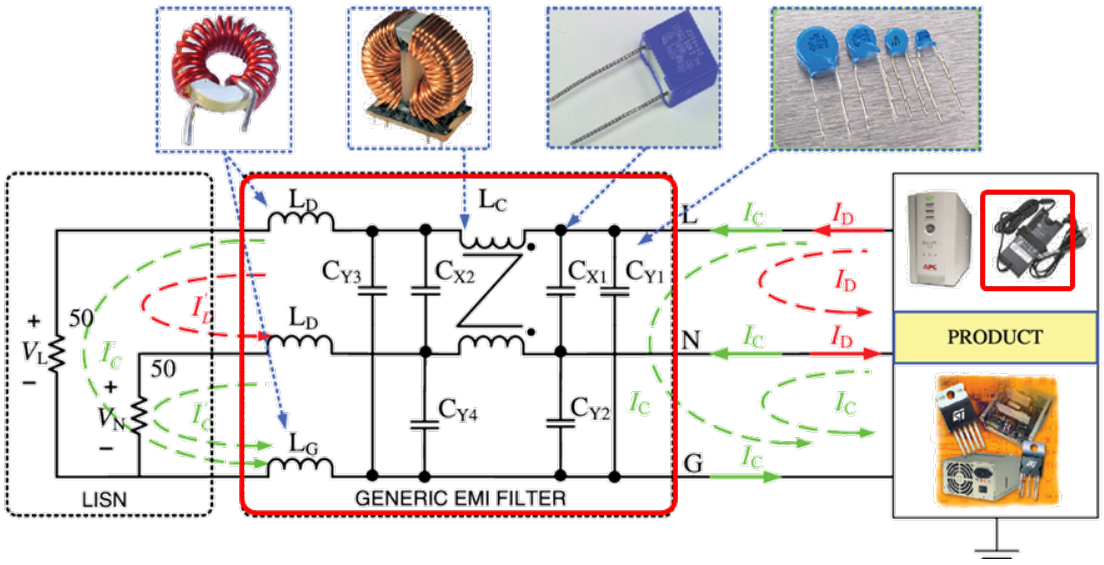


Figure 1.2. Components inside an EMI filter.

filter can be concluded. However, in a compact design, the mutual coupling among the components become ineligible and play an important role in the final performance of the EMI filter.

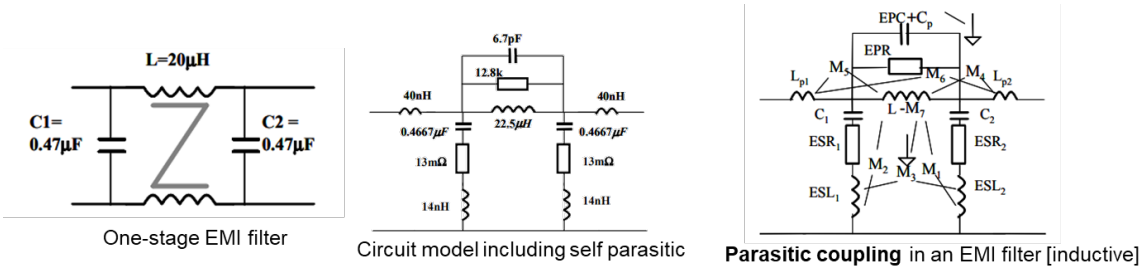


Figure 1.3. The evolution of circuit model during the EMI filter design.

The performance of the EMI filter can be drastically different from the circuit model that neglect the mutual couplings. (Figure 1.4)

1.2. VARIATIONS AMONG FLYBACK TRANSFORMERS

Isolated power converters are commonly used in power adapters for consumer electronics. The flyback converter is a popular type of such converters. (Figure 1.5)

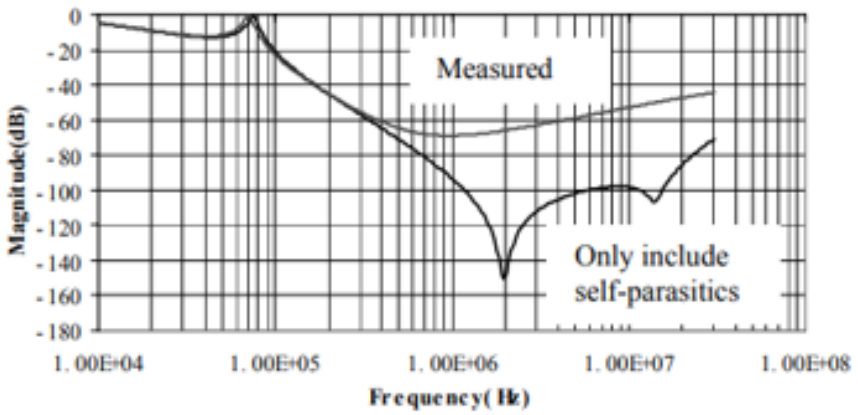


Figure 1.4. The comparison of performance of EMI filter between measurement and design that neglects mutual couplings.

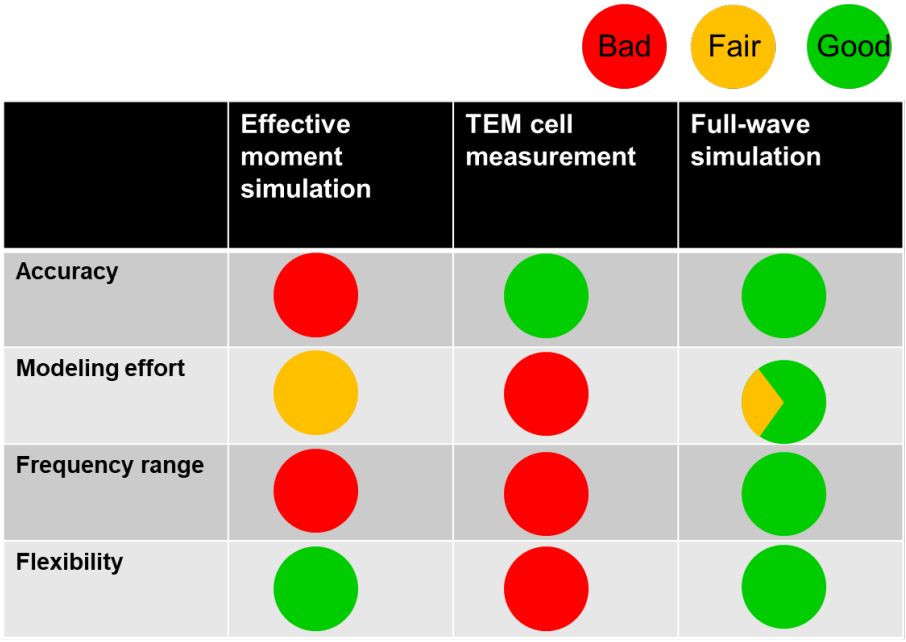


Figure 1.5. The on and off state of a flyback adapter.

In a flyback converter, the MOSFET on the primary side of the transformer serves as a voltage controlled switch. The control voltage is modulated by an IC that also receives feedback from the secondary side. On the secondary side of the transformer, there is a diode and a capacitor. During the on-state, the MOSFET is closed and the secondary winding is charged. But due to the secondary side diode, there will be no current going out from the

secondary winding. The capacitor serves as a current source and for the resistive loading. During the off state, the secondary winding discharges. The output current charges both the output capacitor and the resistive load. The controller IC regulates the PWM of the gate voltage of the MOSFET, therefore adjusting the output voltage level. The transformer is a key component for the common mode current path during the conducted emissions test. Due to lack of control during the winding procedure, it is common that two transformers have different interwinding capacitance, therefore, different performance in the conducted emissions tests.

1.3. CONTENTS AND CONTRIBUTIONS

The outline and contributions of this dissertation are summarized.

In the first paper, a modeling strategy for film capacitors in EMI filters is proposed and validated. In the following paper, a modeling strategy for common mode choke is developed.

The proposed modeling strategy both aim at computational efficiency and accuracy. The modeling effort and the flexibility of the model is also considered.

The proposed modeling strategy is put to test under different scenarios and is validated through comparison between the simulation and measurement results. A general indication of the advantage of the proposed strategy is shown in Figure 1.5

In the last two papers, the challenges in core loss characterization are discussed, and two-probe characterization based methods are proposed to release the requirement for resonance tuning in real practices.

PAPER

I. MODELLING STRATEGY FOR FILM CAPACITORS IN EMI FILTERS

ABSTRACT

The performance of the EMI filters on power-electronics applications is limited by the parasitic coupling between the components of the filters. While this coupling can be partially taken into account on the circuit level by including mutual inductance and capacitance elements to the filter circuit, it is difficult to estimate the values of these elements. In this work, a full-wave modeling strategy is proposed to estimate the parasitic coupling of film capacitors to other components of the filters and to other elements of the electronic system such as wires and enclosures. Information about the internal structure of the capacitors is taken into account to create accurate and computationally efficient 3D models.

Keywords: EMI filter, film capacitor, Mutual Coupling, full-wave modeling.

1. INTRODUCTION

EMI filters are commonly used for the purpose of suppressing conductive noise. It is often seen that densely populated filter components will result in a degraded attenuation performance of the filter [1]. Study in [2] has shown the effect of magnetic coupling among components. Several papers have proposed different methods to improve the performance by decreasing the mutual inter-component coupling [2, 3, 4].

Availability of the filter model at the design stage allows to predict the filter's performance and make a design process more efficient. In [2] a circuit model has been used to represent the components in EMI filter, including self-parasitic and mutual inductances

between the components (capacitor-to-capacitor, capacitor-to-CMC). But the values of the mutual inductances aren't evaluated. In [3] 3D modelling is used to determine the mutual inductance value. In [5] TEM cell measurements for individual components are implemented to obtain the mutual inductance between every two components. In [6], 3D full-wave model was constructed for film capacitors, and the inductive couplings were well captured, but the capacitive coupling is left out.

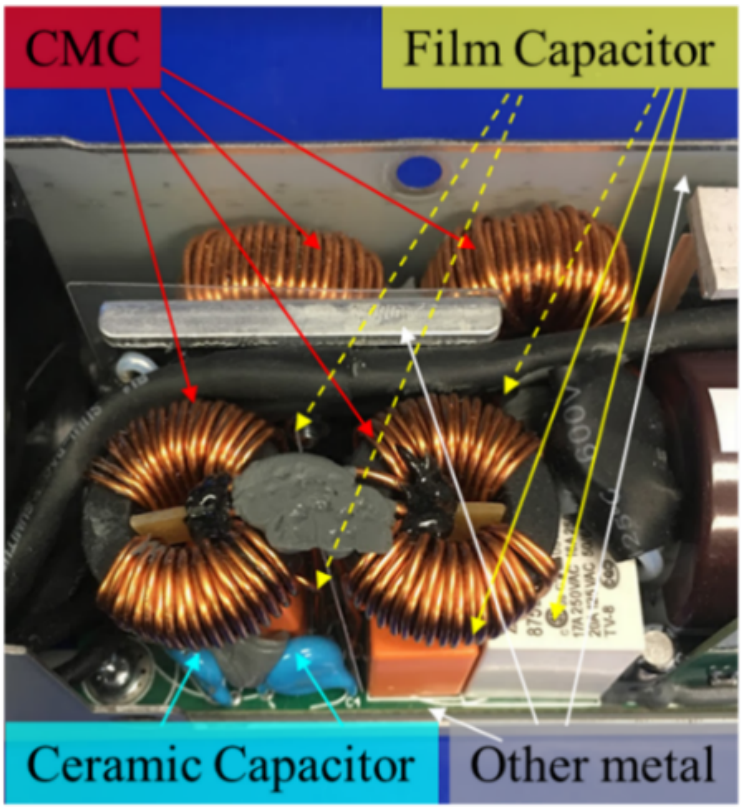


Figure 1. Example of a compact EMI filter design.

2. MODEL CONSTRUCTION

As shown in Figure 1, a compact EMI filter design includes not only the individual electrical components such as capacitors and common mode chokes (CMC), but also wires, PCB board, chassis, and other metallic parts for mechanical purposes. The inductive

and capacitive coupling co-exist between the electrical components and between them and external elements, such as chassis and wires. Many previous studies have been concentrating on modelling and predicting the inductive mutual coupling, while few investigations were done upon the capacitive couplings. In this work, a 3D model is constructed, allowing to predict both types of coupling, including coupling to arbitrary 3D structures such as wires Besides, the model is constructed without reproducing the multi-layer structure of the capacitors, making it easy to use and computationally efficient.

This paper is organized as follows. In Sect. II the capacitors are anatomized to provide information for constructing a 3D model. In Sect. III the 3D model results are compared against measurement results for validation purposes. In Sec. IV the modelling strategy is summarized.

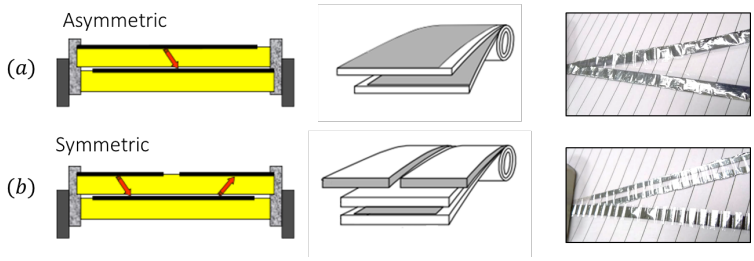


Figure 2. (a) Asymmetric winding, (b) Symmetric winding.

The film capacitor model construction can be broken down to several steps. Firstly it needs to be determined whether the interior structure is symmetric or asymmetric. Then the interior and exterior dimensions need to be measured to form a 3D model with correct physical dimensions. Thirdly, the electrical properties need to be correctly set in the 3D model, to produce an exact performance as the actual component.

2.1. INTERNAL STRUCTURE OF THE CAPACITOR

In most of the cases, the core of a film capacitor is made out of two pieces of plastic film covered with metallic electrodes. The two pieces are wound into a cylindrically shaped winding, with terminals attached at the sides. In this work, we focus on two winding technologies shown in Figure 2. They can be called symmetric and asymmetric winding, respectively.

On the third column of Figure 2, two actual capacitors are unwrapped. The asymmetric case has two electrodes with the same width. The symmetric case has three electrodes, two of them located on the same piece of film. In the symmetrical design, the capacitor actually consists of two capacitors in series, which allows decreasing the voltage applied to the dielectric, and hence increase the voltage rating of the capacitor at the expense of capacitance.

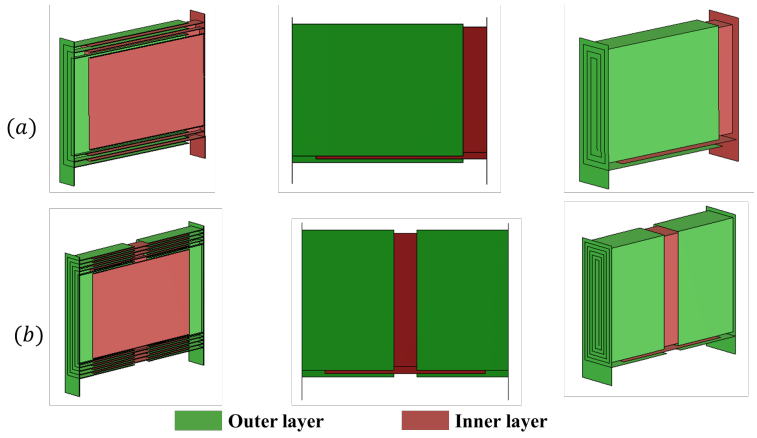


Figure 3. The layers of a film capacitor.

In the asymmetric case, one of the terminals will be connected to the film that dominates the outer surface of the core, while the other terminal is connected to the film that occupies a smaller portion of the outer surface of the core (Figure 3.*a*). As for the symmetric case, the two terminals are connected to two electrodes that have the same width, and together occupy almost the entire outer surface of the capacitor (Figure 3.*b*).

The winding strategy can be determined without dissecting a capacitor. An S-parameter measurement using a voltage probe can be implemented to identify the winding technology. As shown in Figure 4, port 1 and port 2 of a vector network analyzer (VNA) are connected with the capacitor and the voltage probe HP 85024A, respectively. The level of S_{21} at the lowest possible frequency (100 kHz) is recorded, along with the location of the probe tip. Notice that the S_{21} level is proportional to the potential measured at the location of the probe tip.

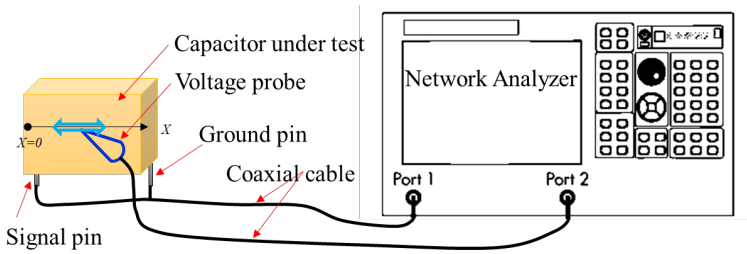


Figure 4. Measurement setup to identify the winding technology.

The level of S_{21} indicates whether the film beneath the probe tip is connected to the 'signal', or 'ground' pin. The voltage trend along the x-axis will be measured again after exchanging the signal pin and the ground pin of the capacitor under test. The difference in the trend of potential along the capacitor after exchanging signal pin and ground pin indicates asymmetry.

This effect is illustrated in the simulation model shown in Figure 5. The potential along the side of the asymmetric capacitor is significantly different when the outer or inner layer is connected to a high potential (1 V). Whereas if the capacitor is symmetrical the potential does not depend on the capacitor orientation.

To demonstrate this in the measurement, two capacitors using different winding technologies were selected. The resulting S_{21} curves are shown in Figure 6. From the results, we can tell that the capacitor with 10 nF nominal capacitance is asymmetric. The

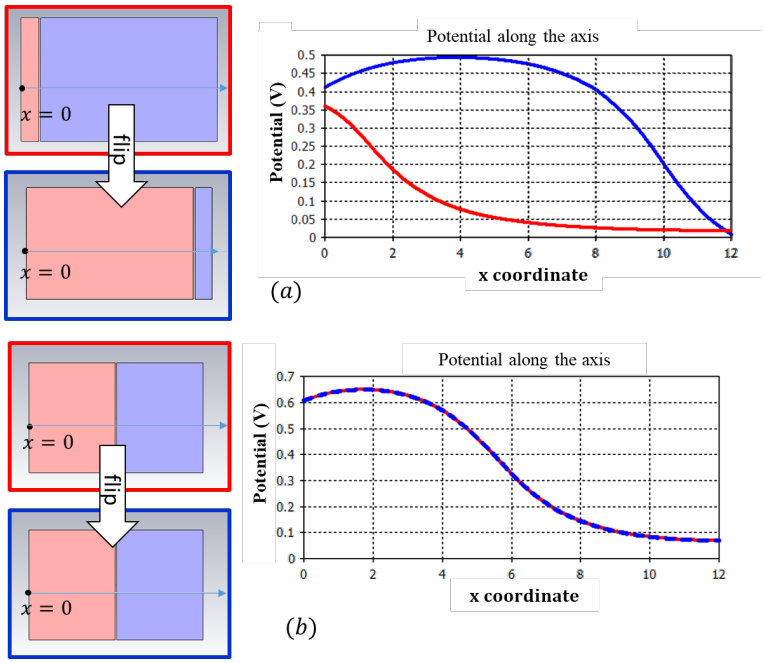


Figure 5. Potential along the capacitor (represented by metal blocks) with asymmetrical and symmetrical winding. Pink color indicates non-zero potential, blue color indicates zero potential. Colors of the plot frames on the left correspond to the colors of the curves.

capacitor with 1 nF nominal capacitance is symmetric since no significant difference is observed in the potential trend after exchanging the signal pin and ground pin. From the evolution of potential along the capacitor, we can identify the winding technology.

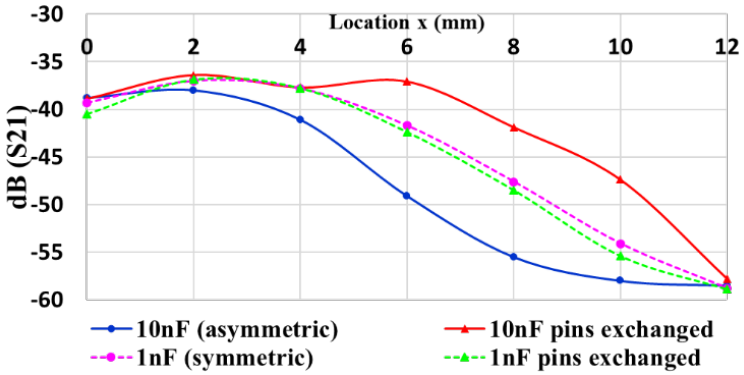


Figure 6. Potential trend along two different capacitors.

2.2. INTERIOR DIMENSIONS OF FILM CAPACITOR

The interior dimensions of the capacitor can be obtained by cutting the capacitor as shown in Figure 7, the dimensions that need to be measured are marked.

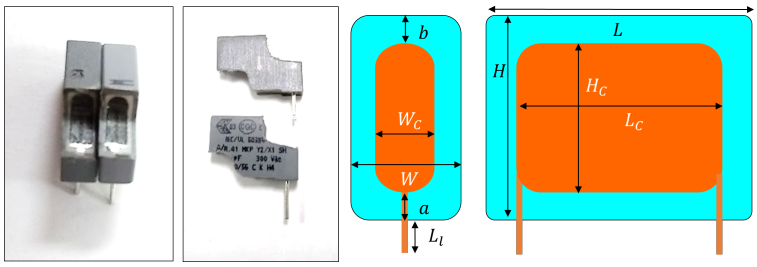


Figure 7. The cross section and dimensions measurement.

If one of the winding technologies illustrated in Figure 3 is used, the outer body of the capacitor will consist of two parts having different electric potentials. This leads to the modelling strategy that considers the entire capacitor body as two conductive blocks, instead of two windings. Such simplification leads to reduced calculation and modelling effort. Figure 8 shows the dramatically decreased mesh cell number when modelling a film capacitor with blocks instead of actual winded sheets even in the case when just 8 layers in the roll are used. For more realistic capacitors geometries with tens of layers, the mesh count reduction is expected to be even greater.

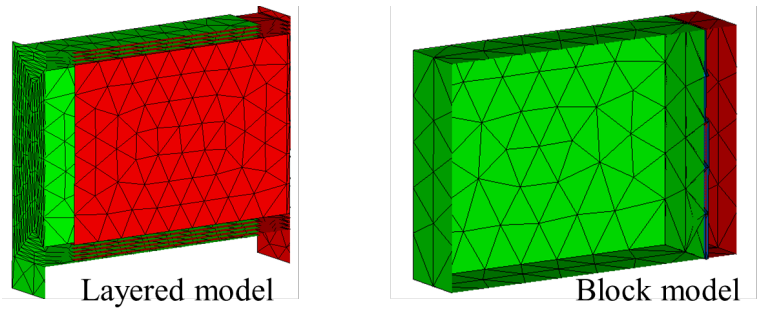


Figure 8. Layered model with 24211 mesh cells, versus block model with 3864 mesh cells.

Figure 9 shows examples of the 3D model for both asymmetric and symmetric winding. The core of an asymmetric capacitor is modeled with two blocks, a larger one and a smaller one. While for the symmetric capacitor, its core is represented with two blocks with identical dimensions. The properties of the materials used in these 3D models will be discussed in the next section.

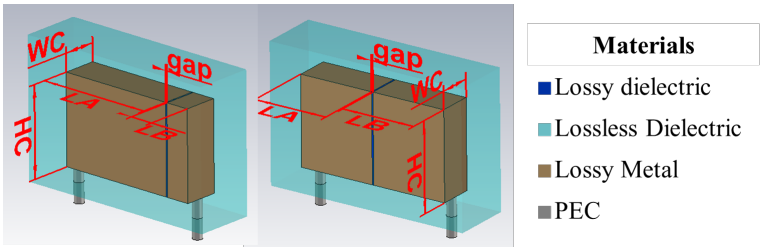


Figure 9. 3D models of the film capacitor.

2.3. ELECTRICAL PROPERTIES IN 3D MODELLING

In Figure 10, an equivalent circuit model of a capacitor is shown. Dielectric and metal loss of the capacitor is represented by resistors R_d and R_c, and the parasitic inductance is represented by an inductor L. The equivalent circuit can be transformed to have just 3 components [7]: Equivalent Series Resistance (ESR), Equivalent Series Inductance (ESL), and Equivalent Series Capacitance (ESC). The ESL value is dictated predominantly by the capacitor geometry and the way it is mounted on the PCB (the lead length, trace geometry, etc), while the ESC and ERS are the properties of the capacitor itself.

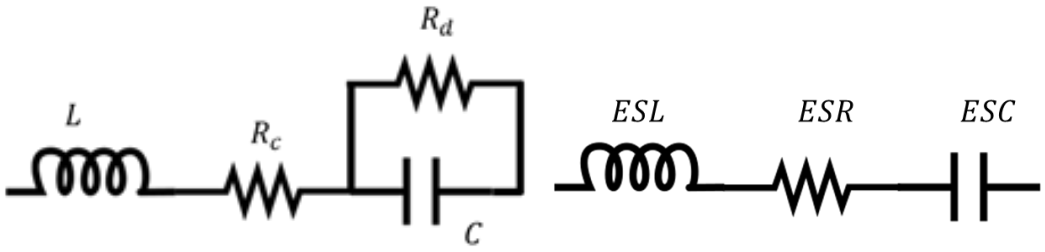


Figure 10. Equivalent circuit of a film capacitor.

Majority of the dielectric materials used for film capacitors can be approximated as having frequency independent loss tangent $\tan\delta_d$. Then we have a -20 dB/dec behavior of the dielectric loss:

$$R_d = \frac{1}{\omega C \tan\delta_d} \tag{1}$$

The ESR can be expressed as:

$$ESR = R_c + \frac{\tan\delta_d}{\omega C(1+\tan^2\delta_d)} \tag{2}$$

Since the capacitor dielectric usually has low loss such that $\tan\delta_d \ll 1$, we can further write

$$ESR \approx R_c + \frac{\tan\delta_d}{\omega C} \tag{3}$$

The conductive resistance R_c is frequency dependent, due to skin effect. However, the skin effect will not be dominating until relatively high frequency, so the R_c will be almost constant at lower frequencies. Overall, the ESR over frequency is shown in Figure 11.

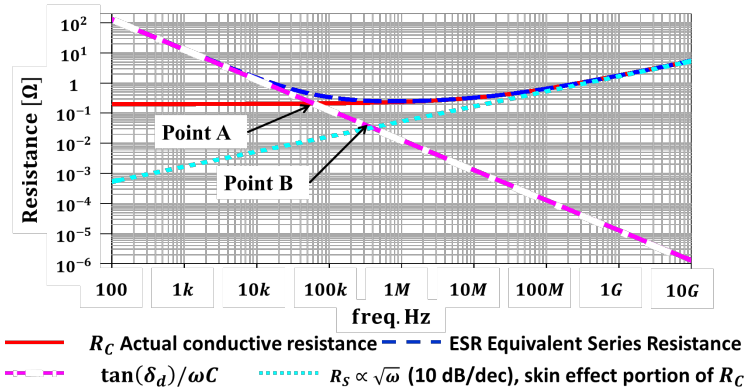


Figure 11. The resistances composing ESR.

There are generally two regions in the curve – at low frequencies the dielectric loss dominates, and at high frequencies the conductor loss dominates.

Notice, however, that there is a 'flat region' in the ESR curve. Whether it appears in the curve depends on the relative position of two crossing points A and B. Point A is when $R_c = R_d$, while Point B is when the R_d curve crosses the $\sqrt{\omega}$ (10 dB/dec) line describing the skin effect at high frequencies. If the frequency of point A is lower than the frequency of point B, the ESR curve will have a flat region, otherwises the transition happens directly from the $1/\omega$ (-20 dB/dec) curve (dielectric loss dominates) to $\sqrt{\omega}$ (10 dB/dec) curve (skin effect loss dominates). Capturing the flat region of the ESR curve in the 3D model presents a significant challenge. The reason is twofold. First of all, many high-frequency solvers (like CST microwave studio frequency domain solver) do not support mesh inside conductors, and use a boundary condition instead, which exclude the possibility of modelling the flat region (since the current inside the conductor is not modelled). Secondly, even if the metals could be meshed, it would require a high mesh count. For example, the skin depth in copper at 1 MHz is 65 μm. To capture the field penetration into metal the mesh cell size needs to be comparable to the skin depth, which gives 3641 cubic mesh cells with 65 um edges per 1 cubic mm. considering that the volume of film capacitor rolls can reach hundreds of cubic mm, the mesh count increase due to internal conductor mesh can become prohibitive.

To come up with a more computationally efficient model, a lumped element is added between the metal parts representing the resistor to model the flat region, and a tuned conductivity is assigned to the body of the capacitor. The two metal blocks in the 3D model form a parallel plate capacitor. Filling the gap between them with a specifically assigned dielectric layer allows modelling the nominal capacitance C.

$$C = \frac{\varepsilon_d W_C H_C}{gap}, \tag{4}$$

Figure 9 shows the model of the 1 nF (symmetric), and the 10 nF (asymmetric) capacitors. These two capacitors have identical exterior geometry. Both of them are made of four materials: PEC for the leads, lossy metal for the capacitor core (conductivity σ),

lossless dielectric for the capsule (permittivity ε_c), and lossy dielectric for the dielectric layer between the two metal blocks (permittivity ε_d, loss tangent tanδ_d). The loss tangent tanδ_d of the lossy dielectric layer can be determined by using (1) on the low-frequency part ($1/\omega$) of the resistance curve (where the resistance due to the dielectric loss dominates) and its permittivity ε_d by using the parallel-plate capacitor formula (4) and the nominal value of capacitance. The 3D model of the 10 nF capacitor also has a lumped resistor inserted between the two metal blocks to account for the 'flat region' in the ESR curve.

The values of the series resistor, as well as the conductivity of the capacitor body, are determined by matching the ESR of the model to the measured ESR curve. All relevant parameters of the models of 1 nF and 10 nF capacitors are listed in Table 1.

Table 1. Paramters in 3D model.

Nominal Capacitance		**10nF**	**1nF**
Geometry	L_A	$8.9mm$	$4.5mm$
	L_B	$1mm$	$4.5mm$
	gap	$100\mu m$	$1\mu m$
	W_C	2.3mm	2.3mm
	H_C	6.7mm	6.7mm
Material	σ	60000 S/m*	2000 S/m*
	ε_d	80	8
	tanδ_d	0.08	0.0015
	ε_c	2#	2#
Lumped element		0.17 Ω	No lumped element

*Obtained by tuning. #Roughly estimated.

3. VALIDATION WITH MEASUREMENTS

In the following paragraphs, we will demonstrate that a 3D model constructed following the strategy described in the previous sections can represent both the self-parameters of the film capacitor and coupling. Three cases that demonstrate the inter-component coupling will be discussed: coupling to a wire, coupling to a metal plate, coupling to another capacitor. All simulations are conducted in the CST Microwave Studio, using the fre-

quency domain (FEM) solver with tetrahedral mesh. Lumped ports are used to obtain the S-parameters. For the single capacitor case, the port is defined between the capacitor leads. For coupling cases, the ports are defined between the PCB traces and solid ground planes on the bottom sides of the PCBs.

3.1. THE SINGLE CAPACITOR CASE

The impedance of the capacitor is measured using two impedance analyzers HP4294A and HP4291A, so that a wide frequency range from 100 Hz to 1 GHz can be achieved. The magnitude and the real part of the measured and modelled impedances are shown in Figure 12. As can be seen, the simulated and the measured results are well matched.

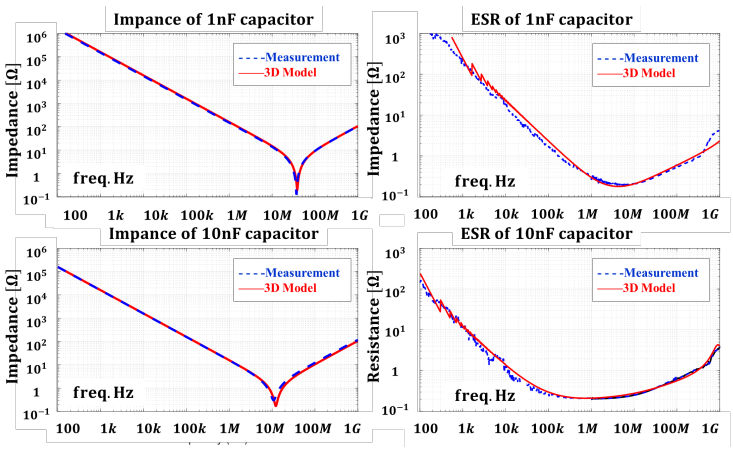


Figure 12. Self impedance and ESR of the 1 nF and 10 nF capacitors.

3.2. COUPLING TO WIRE CASE

As shown in Figure 1, there are wires routing through the EMI filter. Also, there are traces routing on the PCB. A test case is built to validate the ability of the 3D model to predict the coupling between the film capacitor and a wire. Correspondingly, a 3D model of the test case is also constructed (Figure 13).

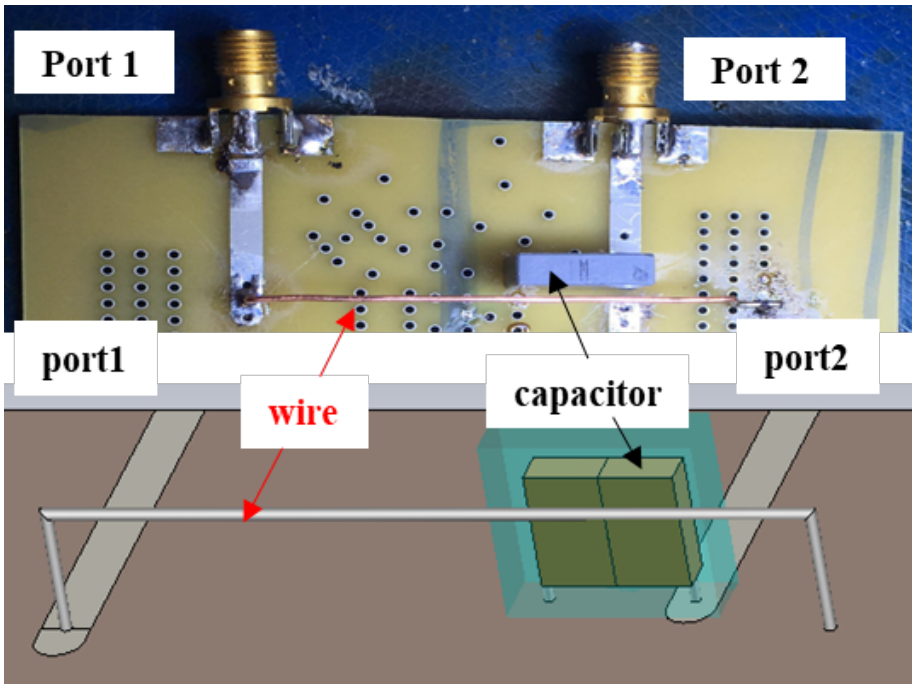


Figure 13. Test case: Coupling between capacitor and wire.

The coupling between the capacitor and a wire depends on the loading conditions of the wire and the capacitor. In this work, only 'open', and 'short' loading conditions are considered. To distinguish the loading conditions the results are labeled. For example 'open loaded capacitor, short loaded wire' case is denoted as 'OS', 'short loaded capacitor, open loaded wire' case is denoted as 'SO', and so on. Circuit diagrams in Figure 14 illustrate the coupling mechanisms between the capacitor and the wire, under different loading conditions. Notice that even for 'open' loading conditions, a small parasitic capacitance still exists between the component and the ground. The simulations and measurements cover the frequency range of 100 kHz ~1GHz (same for all test cases).

As can be seen, the agreement is good in all cases and the trends are captured correctly for all loading conditions.

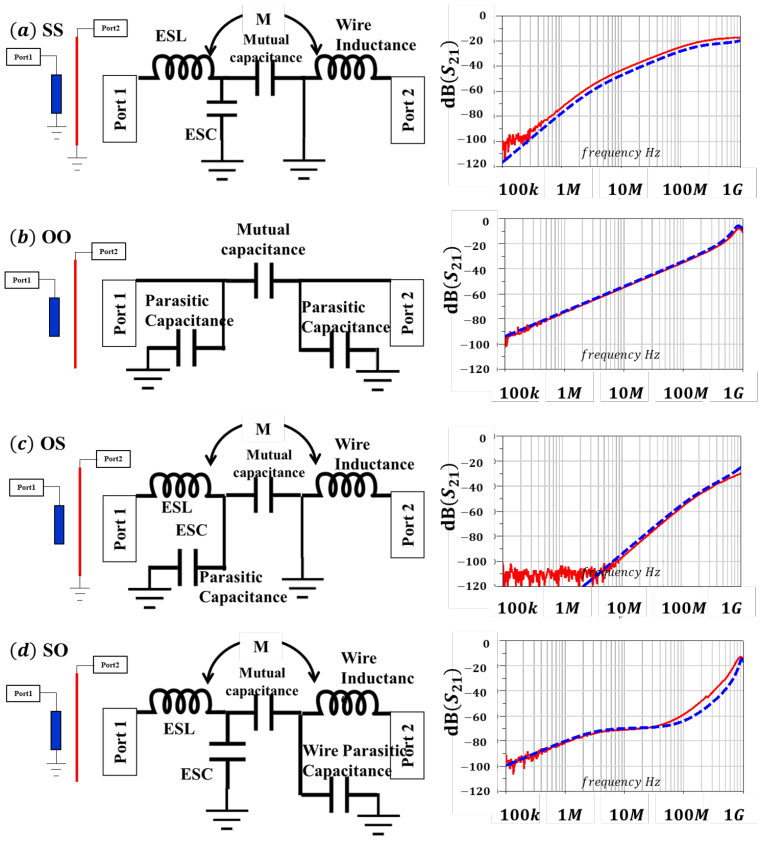


Figure 14. Capacitor to wire coupling. Comparison between simulation and measurement results.

3.3. COUPLING TO PLATE CASE

As shown in Figure 1, there are metal plates for mechanical or reference purposes in an EMI filter. Capacitive coupling between the capacitor and the metal body of the plate is more significant, when compared with the capacitive coupling between capacitor and wire. This lead to a noticeable difference in results when studying an asymmetric capacitor, depending on whether the larger or the smaller block of the capacitor body is connected to the load. A test case is built to validate the ability of the 3D model to predict the coupling between the film capacitor and a metal plate. Correspondingly, a 3D model of the test case is also constructed (Figure 15).

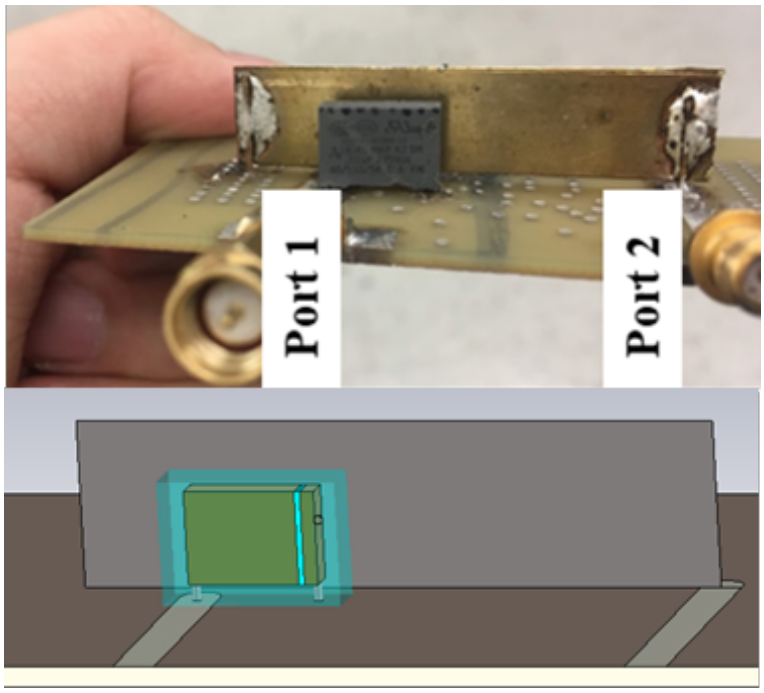


Figure 15. Test case: Coupling between capacitor and metal plate.

The coupling between the capacitor and a metal plate also depends on the loading conditions of the plate and the capacitor. The coupling mechanisms are of little difference compared to the capacitor-to-wire coupling case. However, due to the increased parallel surface area, the mutual capacitance becomes larger. Because of that, a larger difference will appear in the mutual capacitance between an asymmetric capacitor and the plate, depending on the capacitor orientation. To begin with, the asymmetric capacitor is placed as in Figure 15 (the smaller block is connected to the load). The 3D simulation results are compared against measurement results in Figure 16, under all four loading combinations.

As can be seen, the simulation and measurement results are well matched. The results of SO case will become different in levels when the larger block is connected to the load. Such phenomenon can be found in both the measurement results and 3D model results. The comparison is shown in Figure 17.

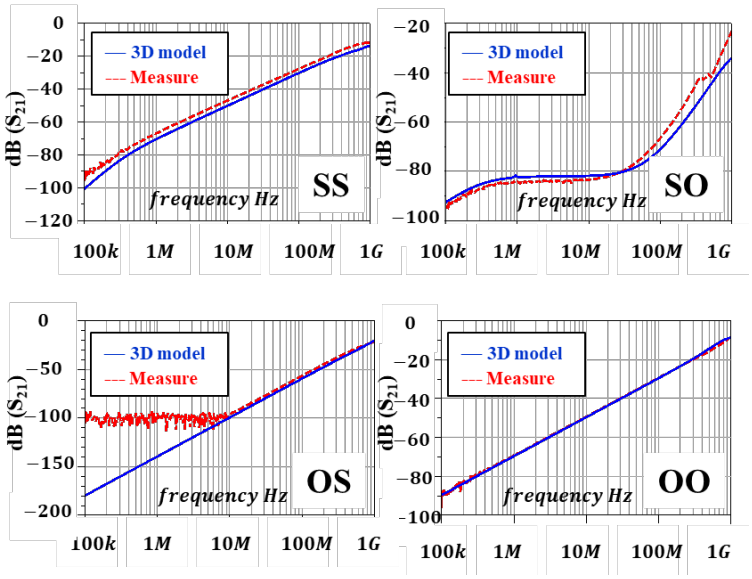


Figure 16. The coupling between an asymmetric capacitor and a metal plate.

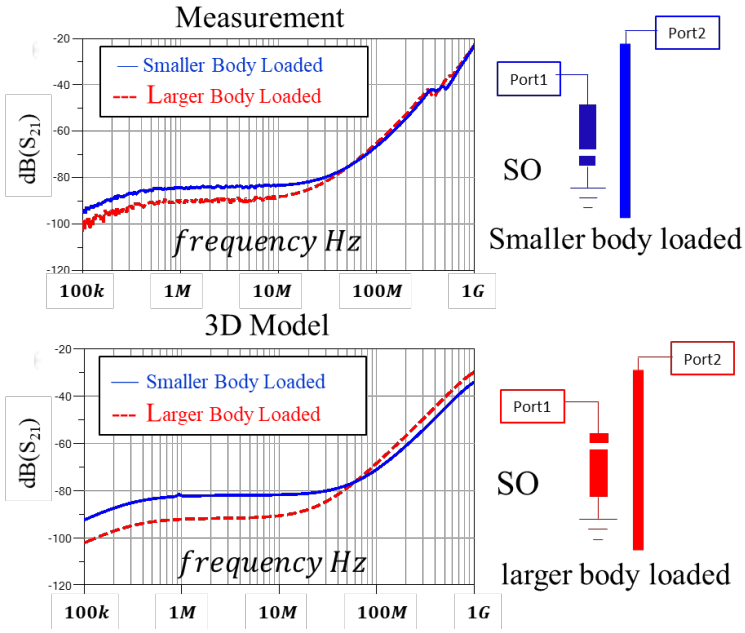


Figure 17. 'SO' case coupling comparison, for two orientations of the asymmetric capacitor.

3.4. CAPACITOR TO CAPACITOR COUPLING

When two capacitors are closely placed, their metal bodies form capacitive couplings, and also the current flowing through them leads to inductive couplings. The 3D model is able to reproduce both coupling mechanisms under various loading conditions for both symmetric and asymmetric capacitors.

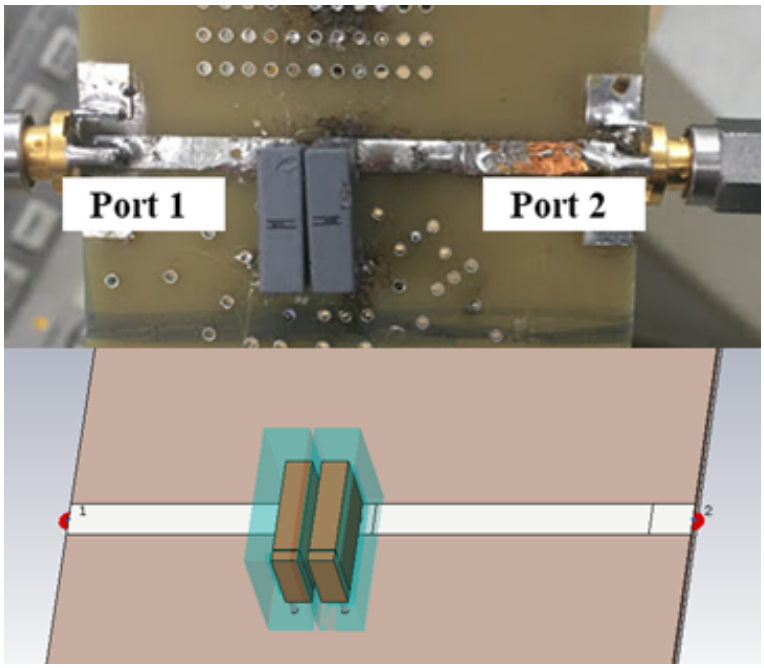


Figure 18. Validation case: Closely placed capacitors.

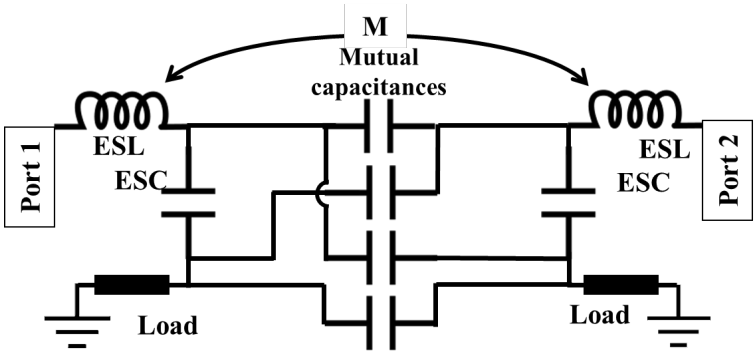


Figure 19. Equivalent circuit of capacitor to capacitor coupling test case.

A test case is shown in Figure 18, where both symmetric and asymmetric capacitors were put to test. An equivalent circuit is shown in Figure 19, where the load can be either a short circuit or a small parasitic capacitor (open loaded). There are 4 mutual capacitances, formed by every two metal blocks that do not belong to the same capacitor.

Figure 20 displays a good match between the simulation and measurement results for the symmetric capacitor. Three different loading combinations are checked.

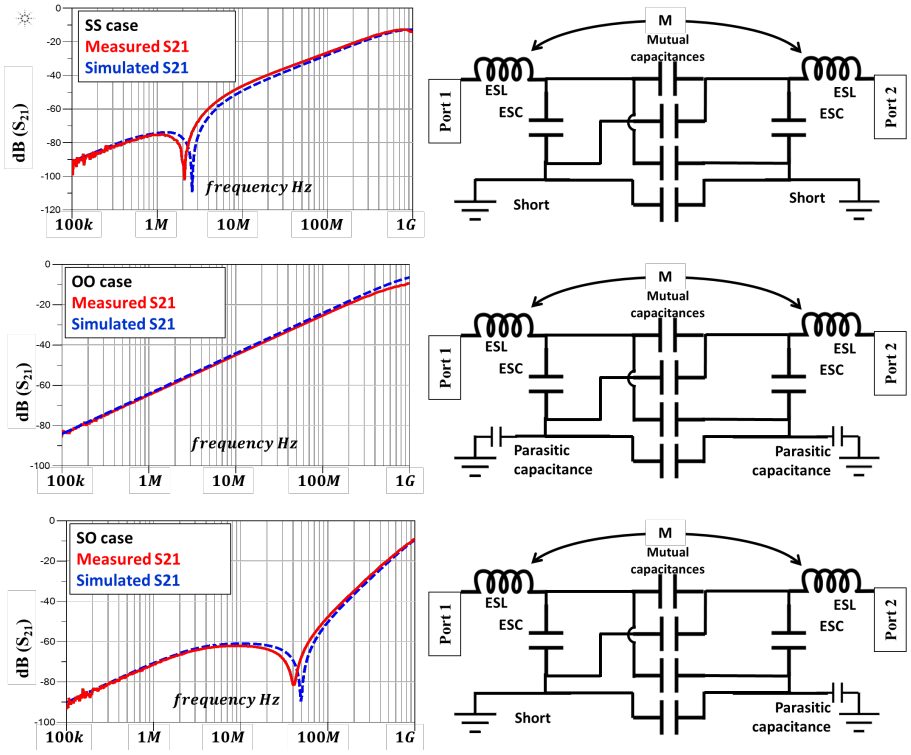


Figure 20. Coupling between two symmetric capacitors.

When the capacitors are asymmetric, there can be again a combination of loading and orientation conditions. Different orientation combination means different mutual capacitance between the two asymmetric capacitors. Measurement and simulation results for different orientations and loading conditions are presented in Figure 21. Capacitor orientation is encoded by letters X and Y, such that X means that the small part of the body is connected to the load, and Y means that the large part of the body is connected to the load (for example XYSS means that in the first capacitor the small part is shorted, and in the second capacitor – the large part is shorted). As can be seen, the comparison shows good agreement between simulated and measured results in all configurations. Small mismatches are due to inaccuracy in the geometry, especially the distance between the two capacitors.

The S_{21} level indicates how strong the mutual coupling between the two capacitors is. In Figure 21 (a), the capacitive coupling is the main coupling mechanism at the lower frequency (below 500 kHz). Adjacent asymmetric capacitors can have a different amount

of mutual capacitance, depending on how the capacitors are oriented. The 3D model can predict the coupling levels in all orientation combinations. Comparisons in (b) and (c) also demonstrate the validity of the 3D model in predicting the coupling between capacitors, under different loading and alignment conditions.

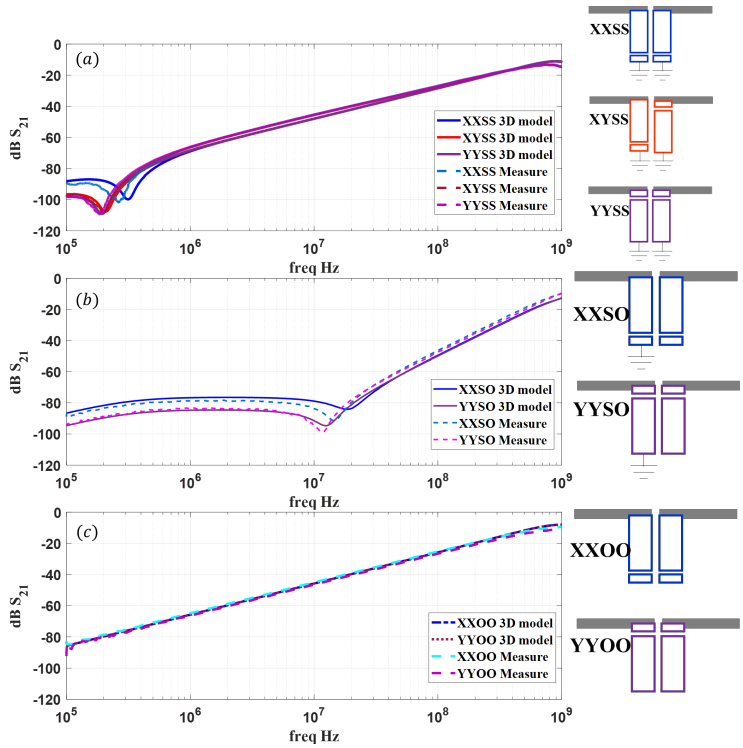


Figure 21. Coupling between asymmetric capacitors. (a) Both capacitors are short loaded. (b), One capacitor is short loaded, another is open loaded; (c). Both capacitors are open loaded.

4. CONCLUSIONS

The proposed 3D modelling strategy takes into account the internal structure of the film capacitor. Two most widely used winding technologies are investigated. The resulting modelling strategy can handle both types of winding of films.

In the proposed model two metal blocks represent the core of the capacitor; a dielectric layer with calculated properties is inserted between the two blocks to capture the nominal capacitance. The conductivity of the metal blocks is tuned to reproduce the ESR of the capacitor. Under certain conditions, a lumped series resistor element is required.

In the three mutual coupling cases that were investigated, the 3D simulation results show good correlation with the measurement results. The models are computationally efficient using CST Microwave Studio, frequency domain solver. The typical simulation times cost is several minutes in the two capacitors test case. The mesh count is typically within 10,000~30,000. The models are suitable to be imbedded into more complicated filter models with many other components, including wires, metal walls, and other capacitors. Presented work is a part of the ongoing EMI filter modeling effort, which will eventually result in the complete filter model including the common mode chokes.

ACKNOWLEDGEMENT

This work was supported in part by the National Science Foundation (NSF) under Grant IIP-1916535.

REFERENCES

[1] Wang, S., van Wyk, J. D., and Lee, F. C., 'Effects of interactions between filter parasitics and power interconnects on emi filter performance,' IEEE Transactions on Industrial Electronics, 2007, **54**(6), pp. 3344–3352.

[2] Wang, S., Lee, F., and Odendaal, W., 'Controlling the parasitic parameters to improve emi filter performance,' in 'Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC'04.', volume 1, IEEE, 2004 pp. 503–509.

[3] Moonen, N., Buesink, F., and Leferink, F., 'Optimizing capacitor placement in emi-filter using back annotation of 3d field coupling parameters in circuit models,' in '2016 International Symposium on Electromagnetic Compatibility-EMC EUROPE,' IEEE, 2016 pp. 576–580.

[4] Stojanovic, M., Lafon, F., Perdriau, R., and Ramdani, M., 'Accurate analytical prediction of emi filter attenuation by considering intercomponent coupling phenomena,' IEEE Transactions on Electromagnetic Compatibility, 2018, **61**(4), pp. 1042–1051.

[5] Stojanovic, M., Lafon, F., Op't Land, S., Perdriau, R., and Ramdani, M., 'Determination of equivalent coupling surface of passive components using the tem cell,' IEEE Transactions on Electromagnetic Compatibility, 2017, **60**(2), pp. 298–309.

[6] Zhou, A., *Modèles de composants passifs et couplage électromagnétique pour filtres HF de puissance: optimisation du placement*, Ph.D. thesis, Université Claude Bernard-Lyon I, 2013.

[7] Paul, C. R., *Introduction to electromagnetic compatibility*, volume 184, John Wiley & Sons, 2006.

II. MODELING STRATEGY FOR EMI FILTERS

ABSTRACT

Performance of EMI filters in power-electronics applications is limited by the parasitic coupling between the components of the filters and the self-parasitic of each component. While these parasitic effects can be partially taken into account on the circuit level, it is difficult to estimate their values. In this work, a full-wave modeling methodology is proposed to predict the performance of a complete EMI filter up to 1 GHz. Following the proposed methodology, the mutual couplings among the EMI filter components are taken into account as well as the self-parasitics of each individual component. Experiments and simulations are carried out to validate the modeling methodology. A self-parasitic cancellation technique is also applied to demonstrate the benefits of 3D modeling methodology in EMI filter design.

Keywords: EMI filter, film capacitor, Common Mode Choke, Mutual Coupling, full-wave modeling

1. INTRODUCTION

EMI filters are commonly used to address conducted emission issues. With the process of miniaturization, modularization, and integration in power electronic systems, the EMI filters are required to have smaller volume and better performance [1]. At the design stage of an EMI filter, however, parasitic behavior and mutual coupling among the components are hard to predict accurately. These effects are responsible for degradation of the filter performance, as reported in [2]. Different methodologies have been proposed to estimate parasitics and coupling. A circuit model has been proposed in [3], which contains both self and mutual parasitics of an EMI filter (capacitor-to-capacitor and capacitor-to-CMC mutual inductances). But the values of these mutual inductances are determined using

measurements which require to have filter prototypes. A 3D model in [4] uses a simple structure to represent two coupled current paths. The mutual inductance obtained from the 3D model is back-annotated into a circuit model to predict the filter performance. TEM cell measurements for individual components are implemented in [5] to obtain the mutual inductance between every two components.

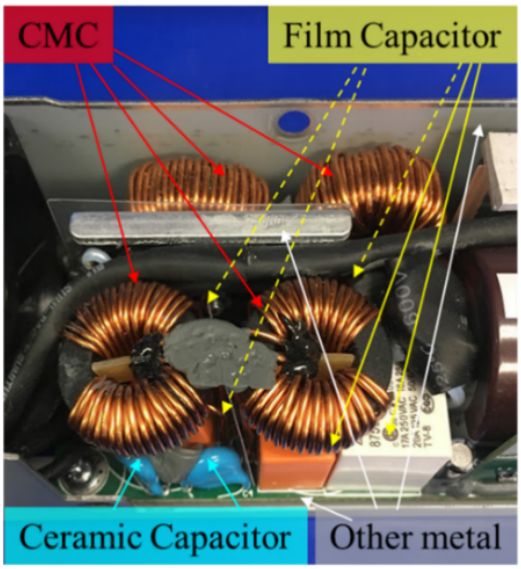


Figure 1. Example of a compact EMI filter design.

However, as the filter geometry gets more and more complicated, the reliability of these methods becomes questionable. As shown in Figure 1, a compact EMI filter design can include not only the individual electrical components such as capacitors and common mode chokes (CMC), but also wires, PCB board, chassis, and other metallic parts for mechanical purposes. Therefore, identifying all coupling mechanisms in such structures can become difficult as inductive and capacitive coupling exists not only between the electrical components but also between them and external elements, such as chassis and wires. Besides this, previous studies have been concentrating mainly on modeling and predicting the inductive mutual coupling, while few investigations were done upon the capacitive couplings.

On the other hand, during the iterative stage of EMI filter design, the methods mentioned above require re-measurement and re-calculating each mutual parasitics even if only the geometry of the filter has changed.

Several different techniques have been proposed to reduce the self or mutual parasitics [1, 2, 6, 7]. These techniques can help to improve filter performance. However, they all introduce other parasitics. The study in [6] has shown that the combination of different parasitic-cancellation techniques may lead to degraded filter performance.

3D modeling of the whole EMI filter can, therefore, provide a solution for both predicting the filter performance and validating different parasitic-cancellation techniques. The 3D model of an EMI filter can help at both initial and iterative design stages.

Using 3D models for EMI filter is not new. For example in [8, 9, 10], the authors modeled the parasitics and mutual coupling in EMI filters using 3D-PEEC-BIM method. Results obtained by the 3D-PEEC-BIM method were presented for frequency range up to 30MHz. Authors of [11, 12, 13] reported the modeling procedure for individual components such as mlti-layer ceramic capacitors (MLCC) and common mode chokes. However, 3D modeling of complete EMI filters up to 1GHz based on a more common and readily commercially available method such as FEM has not been reported in the literature. Full-wave simulations up to 1GHz reveal not only the performance of the EMI filter in suppressing conducted EMI but potentially can also predict the role of the EMI filter in radiated EMI tests, increasing the value of the model for EMC-aware design.

In [14] a 3D modeling strategy for film capacitors has been proposed and validated. The mentioned modeling strategy uses a simple structure to avoid explicit modeling of the film roll inside the film capacitor. In this way, the model is easy to build and is computationally efficient. The FEM based solver is able to perform full-wave simulation for the film capacitors with good accuracy up to 1GHz in a relatively short time (up to tens of minutes maximum).

In this paper, a full-wave modeling strategy for an entire EMI filter (including capacitors and CMCs) is proposed and validated. The filter performance is correctly predicted by the 3D full-wave model up to 1 GHz including common and differential mode responses. Besides this, a parasitic-cancellation technique is implemented in 3D modeling to demonstrate the benefit brought by the model at the iterative stage of the filter design.

This paper is organized as follows. In Section 2, a typical EMI filter is presented. The components are anatomized to provide information for constructing a 3D model. In Section 3, the modeling procedure for each component is described. In Section 4 an example is shown to display the advantages of using 3D model to help improve the EMI filter design. The modeling strategy is summarized in Section 5.

2. EMI FILTER AND COMPONENTS

A one-stage EMI filter is analyzed in this work. The layout of the EMI filter is demonstrated in Figure 2. This filter uses two film-capacitors as X-capacitors and 2 ceramic capacitors as Y-capacitors.

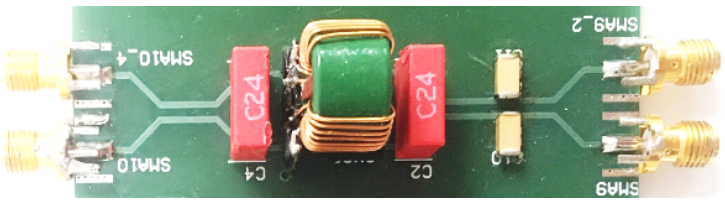


Figure 2. The EMI filter under investigation.

The Y-capacitors are relatively far away from the other components, thus the mutual coupling between other components and the Y-capacitors is of less relevance. As for the X-capacitors, they are inductively and capacitively coupled to the common-mode choke (CMC). Taking this into account, a circuit diagram for the filter containing self and mutual parasitics can be drawn (Figure 3).

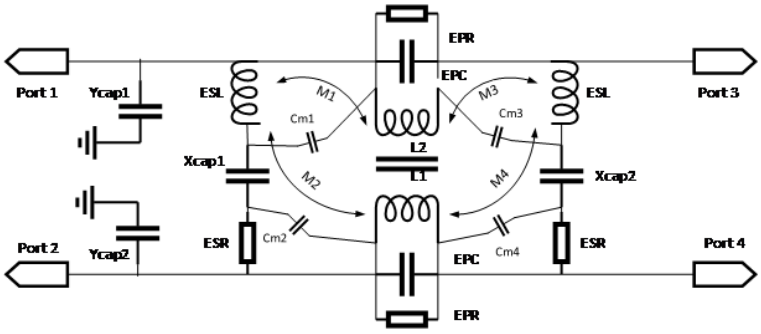


Figure 3. The equivalent model of the EMI filter under investigation.

In the proposed methodology the self-parasitics of the components are captured by 3D modeling their geometry (in some cases measurements are needed to determine model parameters, such as the permeability of the CMC core). The mutual parasitics are modeled in a 3D model exclusively, without relying on measurements. The following sub-sections demonstrate how 3D models of every EMI filter component can be created.

2.1. INTERNAL STRUCTURE OF FILM CAPACITORS

In most cases film capacitors are made of two pieces of plastic film covered with metallic electrodes rolled into a cylindrically shaped winding. The capacitor is finalized by attaching terminals and encapsulation [15]. The electrodes are interchangeable because the film capacitors are not polarized. However, as demonstrated in [14], the film capacitor is not necessarily electrically symmetric. The capacitive coupling between the film capacitor and another film capacitor may be dependent on the film capacitor's orientation. Two winding technologies – symmetric and asymmetric – have been investigated in [14]. These two technologies are shown in Figure 4. The symmetric winding in film capacitors effectively forms multiple smaller capacitors connected in series. In this way, the effective breakdown voltage of the film capacitor is raised.

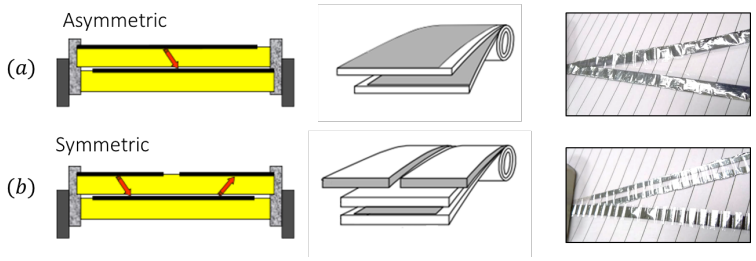


Figure 4. Asymmetric and symmetric winding of film capacitors. The film of capacitor from each type is unwound to show the difference.

Correspondingly, two modeling structures were proposed in [14] for electrically symmetrical and asymmetrical film capacitors (Figure 5). It's essential to determine which type of winding technology is applied in the film capacitors especially when they are mounted close to other components to capture the capacitive coupling effects correctly and what is the actual orientation of the capacitor mounted on the PCB. The winding type and orientation can be determined by dissecting the capacitor or non-destructively by measuring the electric potential on the capacitor surface as described in [14].

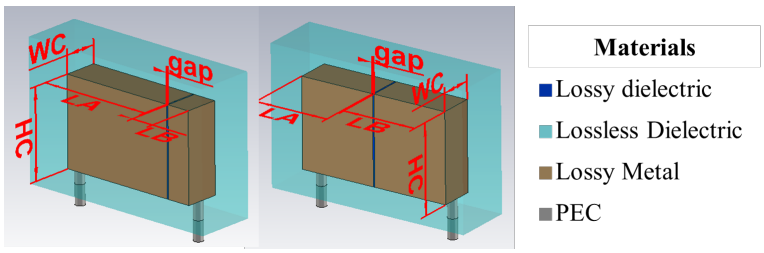


Figure 5. 3D model for film capacitors. (a) Asymmetric winding. (b) Symmetric winding.

The models in Figure 5 represent capacitors as solid metal blocks and its nominal capacitance is modeled by inserting a dielectric material between the metal blocks. The permittivity of the dielectric layer is calculated using a parallel plate capacitor formula [14].

2.2. INTERNAL STRUCTURE OF THE TOROIDAL CMC

A group of toroidal common mode chokes commonly used in EMI filters is shown in Figure 6. These common mode chokes, although they share the same shape of core, could have different properties. Three types of core material are used: Nanocrystalline, Mn-Zn ferrite, and Ni-Zn ferrite. The Nanocrystalline core is highly conductive and usually is placed inside a plastic shell with relatively large gaps (up to several mm) between the core and the shell. Thus the capacitive coupling to the core is small or even negligible. Other than a difference in the core material, the CMCs can differ in the number of the winding layers. Besides this, they can be mounted on a PCB in either standing or flat fashion. The modeling procedure proposed in this paper can cover all these variations.

The windings of the CMCs will exhibit a transmission line effect at high frequencies [16], similar to the transmission line effect found in film capacitors [17]. A 3D model following the strategy proposed in this paper can reproduce the transmission line effect since the model for CMC is very close to the actual structure, with little geometrical features discarded.

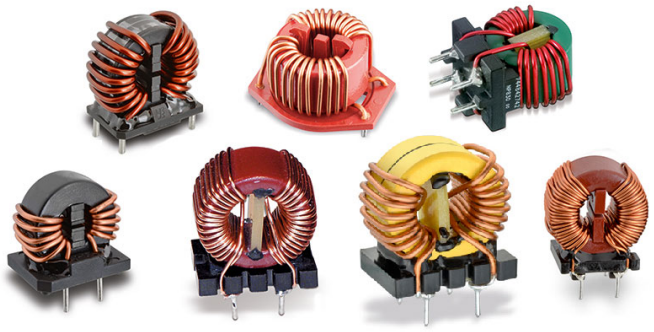


Figure 6. A group of common mode chokes used in EMI filer applications.

2.3. INTERNAL STRUCTURE OF CERAMIC CAPACITORS

Ceramic capacitors usually have small package size. However, their parasitic inductance and inductive coupling with other components could be still relevant. Mutual capacitances contributed by the ceramic capacitors — although small — can still be measured. To create a 3D model a multi-layer ceramic capacitor (MLCC) was cut open. The cross-section shows that the capacitor can have a complicated internal structure (Figure 7). Other than laminated electrodes, the capacitor can consist of several smaller capacitors, connected in series to increase the voltage rating of the capacitor.

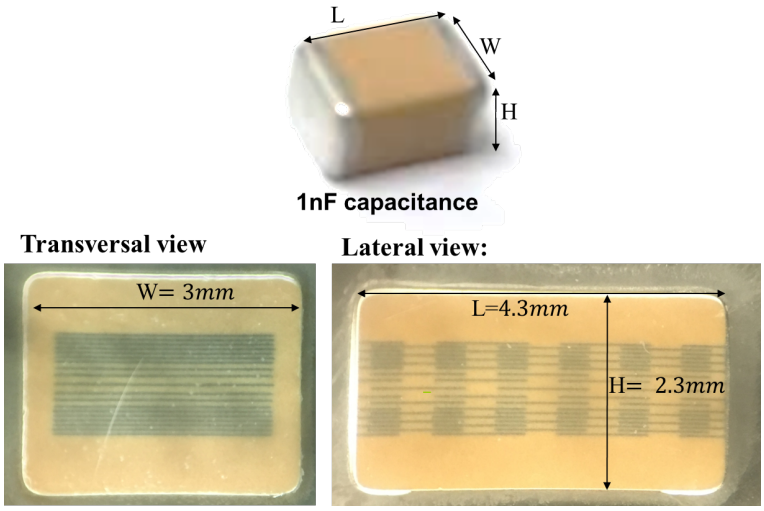


Figure 7. The cross-section of a 1 nF MLCC. Multiple smaller capacitors are found inside the MLCC, connected in series. The length L, width W, and height H are measured.

3. EMI FILTER MODELING PROCEDURE

The primary goal of the modeling strategy is to predict the filter performance accurately. Saving computational resources comes secondly. In this section, the modeling procedure is broken down into the modeling of each component. The component models are

validated separately before being inserted into the filter model. Paper [14] has described the film capacitor modeling in detail. As for the modeling of CMCs, characterization through simple measurements is required before the modeling procedure starts.

3.1. CHARACTERIZATION OF CMC

Common mode choke WE7448252311 [18] is used in the EMI filter shown in Figure 2. The dimensions of this CMC are measured and displayed in Figure 8. and Table 1.

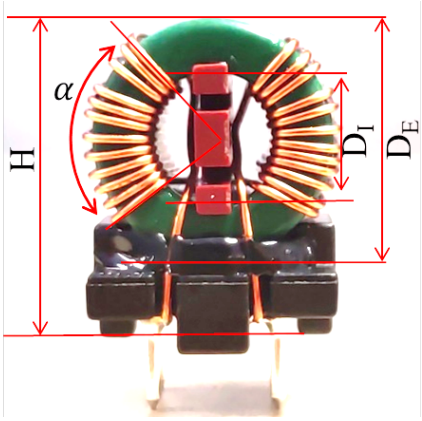


Figure 8. Dimensions of a common mode choke.

Table 1. Dimensions of the common mode choke.

H	20.0 mm	Wire radius (α)	0.3 mm
α	107°	Core Width(W_E)	9.3 mm
D_I	14.2mm	Number of turns (N)	12
D_E	18.6mm	Single/Multi-layer winding	Single Layer

Other than physical dimensions, the electrical properties are also measured under two configurations: single-winding configuration and cross-winding configuration [19]. The measurement circuits and the equivalent circuits of the choke in two configurations are presented in Figure 9.

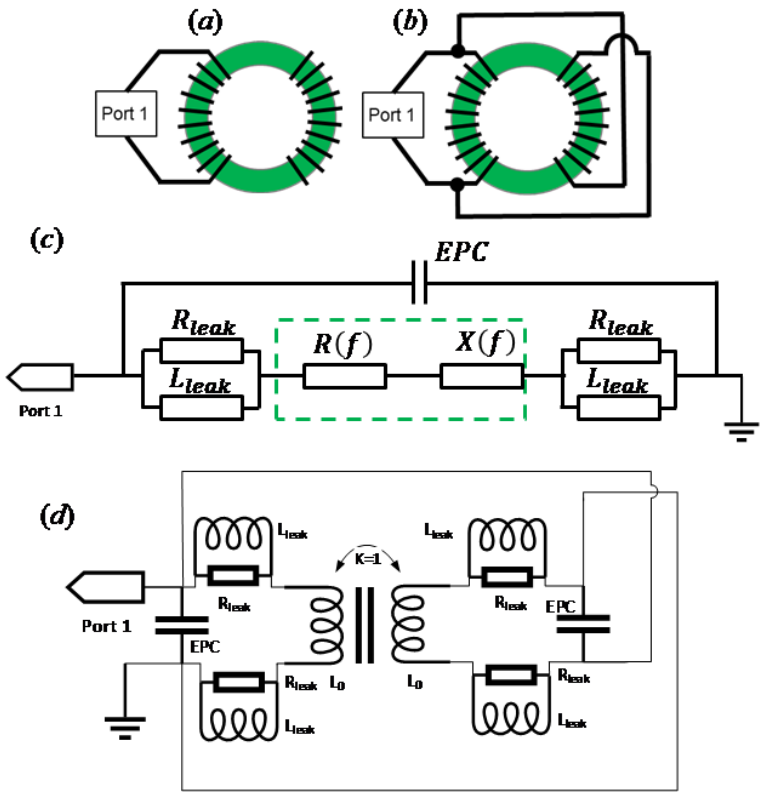


Figure 9. CMC configurations for characterization. (a) Single-winding CMC configuration. (b) Cross-winding CMC configuration. (c) Equivalent circuit for Single-winding configuration. (d) Equivalent circuit for cross-winding configuration.

The equivalent circuit shown in Figure 9 (c) is used in [20] to extract the permeability of the core material. EPC denotes the equivalent parallel capacitance of the winding on CMC. The green box in Figure 9 (c) represents the actual inductance and magnetization loss contributed by the flux inside the core material with a total impedance equal to

$$\boldsymbol{Z_{core}} = jX\,(f) + R\,(f) \tag{1}$$

Where the impedance $Z_{leak} = \frac{j\omega L_{leak} R_{leak}}{j\omega L_{leak} + R_{leak}}$ represent the leakage inductance and its loss.

The real and imaginary part of the core material permeability can be related to the core geometry [20]:

The real and imaginary part of the core material permeability can be related to the core geometry [20]:

$$\mu' = \frac{2\pi X(f)}{\omega N^2 \mu_0 W_E \ln\left(\frac{D_E}{D_I}\right)} \mu'' = \frac{2\pi R(f)}{\omega N^2 \mu_0 W_E \ln\left(\frac{D_E}{D_I}\right)} \tag{2}$$

Where W_E, D_E, and D_I are the width, outer diameter, and inner diameter of the core, respectively, N is the number of turns in the winding.

The measured impedance following the single-winding configuration is denoted as Z_{meas}. According to the equivalent circuit diagram in Figure 9 (c), the relationship between measured impedance and Z_{core} is :

$$Z_{meas} = \frac{Z_c \bullet (Z_{core} + 2Z_{leak})}{Z_c + (Z_{core} + 2Z_{leak})} \tag{3}$$

Where

$$Z_c = \frac{1}{j\omega \bullet EPC} \tag{4}$$

Thus, the leakage impedance Z_{leak} needs to be determined before obtaining Z_{core}. As suggested in [19], the cross-winding configuration needs to be measured to obtain Z_c and Z_{leak}. The configuration and the corresponding equivalent circuit diagram is shown in Figure 9 (b). The circuit in Figure 1. (d) can be simplified into the circuit in Figure 10, as the cross-winding configuration let the perfectly coupled portion of the inductances to cancel each other.

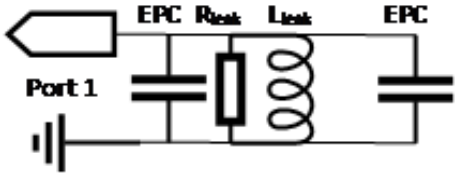


Figure 10. The simplified circuit for cross-winding configuration.

According to the circuit, the Z_{leak} can be obtained from the measurement result under cross-winding configuration. The procedure is straightforward since the measured impedance shows a clear RLC parallel resonance pattern.

The measured impedances from both configurations are shown in Figure 11. Both the magnitude and phase are displayed. Substituting the parameters obtained from the cross-winding measurement into (refp2e2), along with the dimensions from Table 1, the real and imaginary parts of the core permeability μ', μ'' are extracted and plotted in Figure 12.

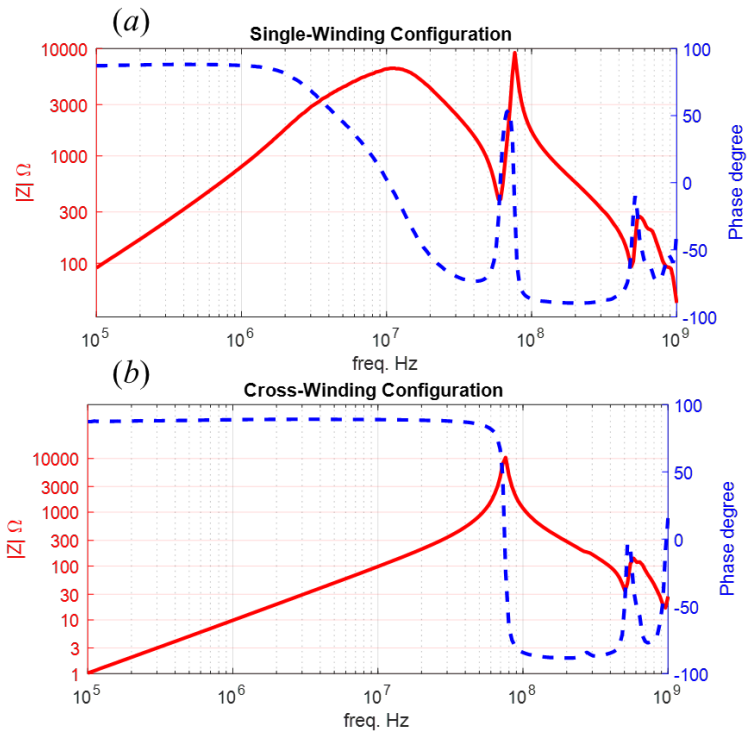


Figure 11. Measured impedance magnitude and phase.(a) Single-winding configuration impedance magnitude and phase. (b) Cross-winding configuration impedance magnitude and phase.

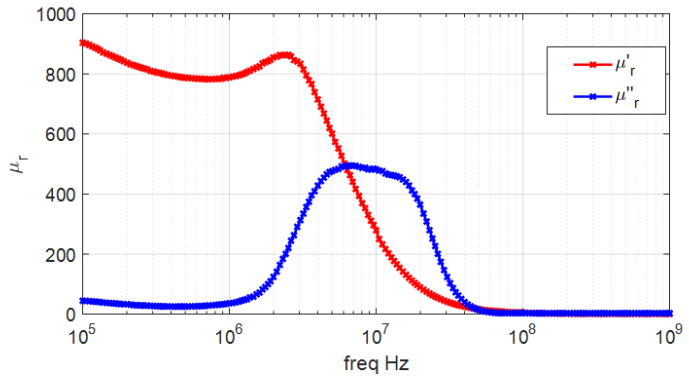


Figure 12. Extracted permeability of the Ni-Zn core.

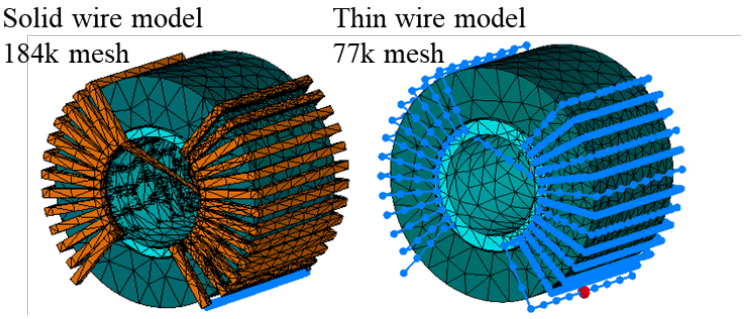


Figure 13. User interface of the macro program.

3.2. MODELING OF CMC

With the dimensions listed in Table 1, a 3D model of the CMC can be constructed. A macro program is developed to generate the model in CST STUDIO SUITE, in frequency domain solver environment. (Figure 13)

In the entry of the macro, there are two options for the wire, either a thin wire model or a solid wire model. To reduce the mesh count required to represent solid wires, the wires are built to have square cross-section instead of round cross-section. The difference in wire settings leads to a difference in the parasitic capacitance.

In order to save computation resources, wires in the 3D model have no insulation coating. Besides this, the wires in the model are not wound as tight as in the real CMC (due to difficulty of calculating the wire geometry needed to achieve tight winding). As

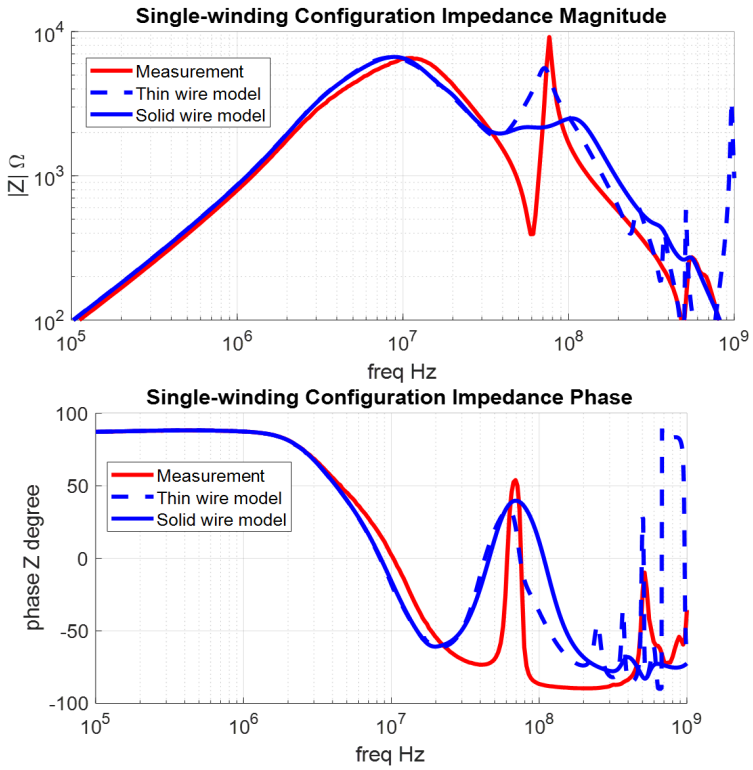


Figure 14. The CMC model and its impedance (cross-winding configuration). The comparison is between measurement and simulation results.

a result of this, the distance between wires is larger than that in reality - which can be as low as tens of micrometers, and the permittivity of the dielectric between the wires is lower. These differences lead to a mismatch in the parallel capacitance of the winding. To compensate for this difference, an additional insulation layer is added into the inner opening of the torus covering all turns. The permittivity of this insulation layer is tuned to match the target parasitic capacitance. As mentioned in the previous section, the cross-winding configuration results show a clear LC resonance, which makes it an ideal target for parameter tuning. The tuning procedure is simple, since the EPC is dominated by the wire-to-wire capacitance in the winding, which is linearly proportional to the permittivity of the additional insulation layer.

Two versions of the CMC model (solid and thin wire) are displayed in Figure 14 and Figure 15, followed by their impedances under single-winding and cross-winding configurations, in comparison with the impedances obtained through measurement.

Both models demonstrate relatively good agreement with the measured parameters. However, since the mesh count of the thin wire model is significantly lower, this model will be used henceforth as more computationally efficient.

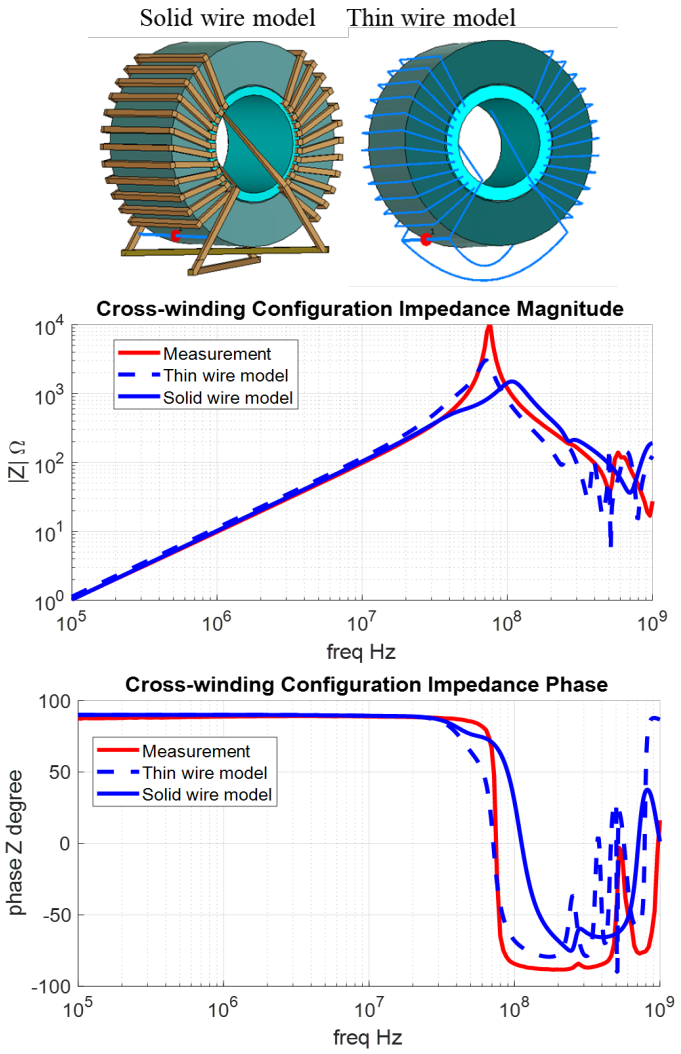


Figure 15. The CMC model and its impedance (single-winding configuration). The comparison is between measurement and simulation results.

3.3. MODELING FOR THE CERAMIC CAPACITOR

An extreme case where two identical MLCCs are closely placed (0.3mm apart) has been tested to validate the MLCC model. The cross-section of the capacitor is shown in Figure 7. One side of these two capacitors are connected to port 1 and port 2, respectively. The other side of the capacitors are connected to the ground plane by a 0.01 Ω lumped resistance. In the corresponding measurement setup one end of the capacitors is mounted on the microstrip trace (having the gap in the middle) and the other end is connected to the ground plane by vias. The coupling between these two capacitors are evaluated by measuring and simulating the transmission coefficient S_{21} between the ports. Two models of the capacitors were created: the explicit model reproducing the internal structure of the capacitors and the simplified model, modeling the capacitors as solid blocks (similar to the film capacitors in Figure 5). The results from both explicit model and simplified model are compared against measurement results (Figure 16).

The mechanism of the coupling between the two MLCCs is capacitive at lower frequencies, inductive at higher frequencies (above the resonance). The inductive coupling between the capacitors would be almost identical for both models because the current path geometry is practically the same in both cases. Capacitive coupling potentially could be different (due to a difference in electric field potential between the models), but for the configuration in Figure 16 it happens to be very similar.

As can be seen from Figure 16, building an explicit model for the ceramic capacitor does not improve the accuracy when compared with a simplified model. The relevance of coupling would be even less significant for the filter in Figure 2 due to the increased distance between the capacitors relative to Figure 16. At the same time the self-impedance of the capacitors is modeled accurately (Figure 16 (c)).

In the simplified model for MLCC, a thin dielectric layer is inserted between the two solid blocks. The permittivity ε_r of this thin layer is obtained from parallel plate capacitance formula.

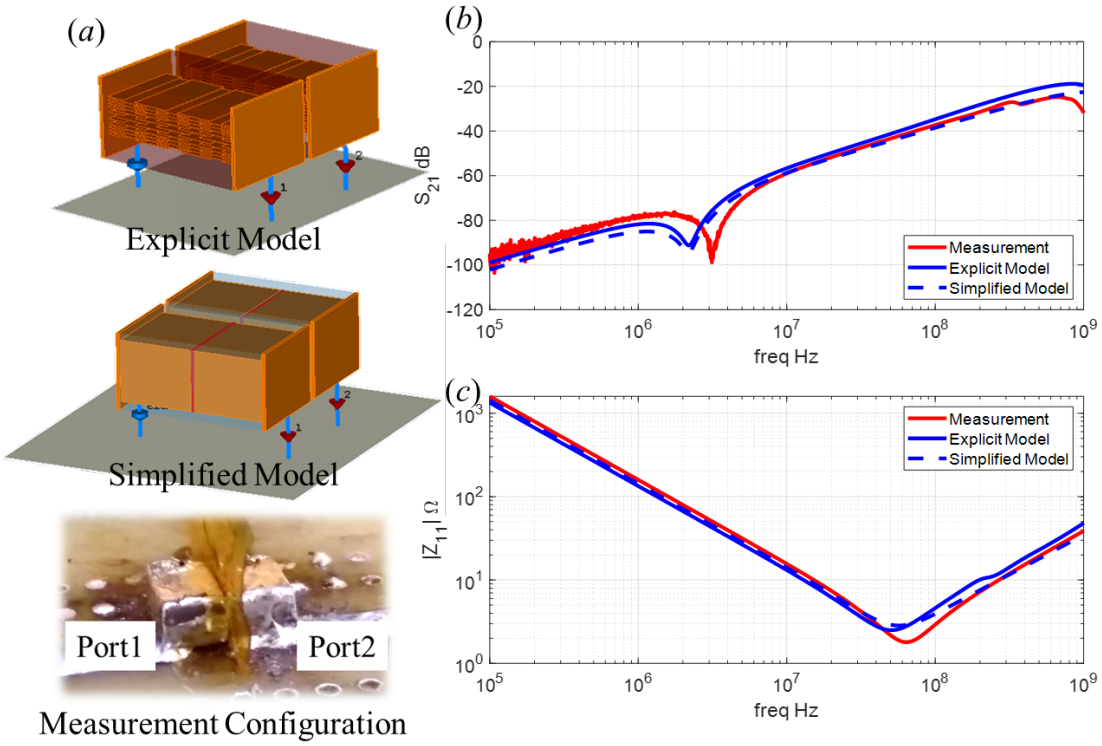


Figure 16. MLCC model. (a) The 3D models for MLCC capacitors and the measurement configuration for the coupling between the two capacitors.
(b) S_{21} results obtained from explicit model, simplified model and measurement.
(c) Impedance of a single MLCC from explicit model, simplified model, and measurement.

$$\varepsilon_r = \frac{C}{S} d \tag{5}$$

Where C is the nominal value of the MLCC; S is the cross-section area of the two solid blocks; d is the thickness of the thin dielectric layer.

3.4. MODELING FOR THE FILTER

The filter model integrates the models of the individual components. Other items such as the board, the traces, etc. are also included. Figure 17 illustrates the final filter model. The CMC is mounted upright on the PCB, the X-capacitors have symmetric winding, and the Y-capacitors are MLCCs modeled as two solid blocks separated by a dielectric layer.

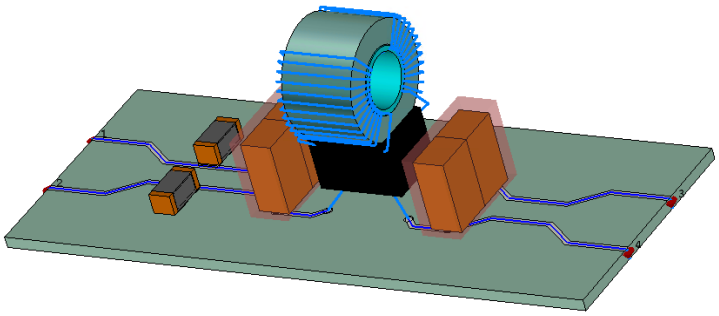


Figure 17. 3D model for the EMI filter.

The performance of this filter model is displayed in Figure 18 together with the measured curves. Coefficients S_{cc21} and S_{dd21} are the mix-mode scattering transmission coefficients for common and differential modes respectively. Filter performance is predicted very accurately up to 10 MHz. Above 10 MHz the accuracy of the differential mode suffers, probably due to inaccurate modeling of leakage inductance of the CMC (a similar effect of the leakage inductance is observed in a circuit model in Figure 3). Relatively large discrepancies are observed above 100 MHz but even in that frequency range, the tendency is captured correctly. At the same time, frequencies where the filter performance changes qualitatively (50 MHz and 100 MHz for the differential mode and 100 MHz for the common mode) are predicted relatively accurately. Because of this, the model can be useful for filter optimization despite quantitative inaccuracies.

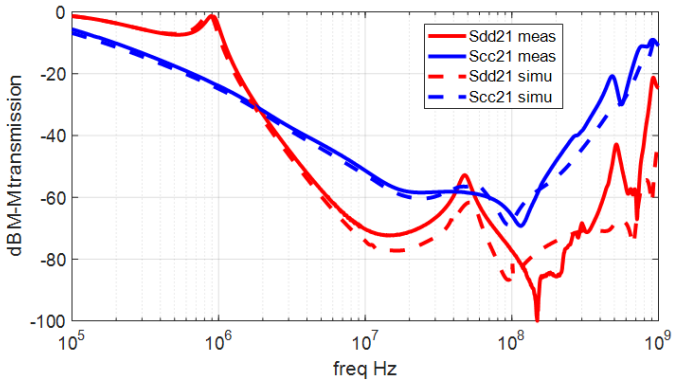


Figure 18. Performance of the EMI filter. Results are compared between 3D simulation and measurement.

4. PRACTICAL APPLICATION OF THE 3D MODEL

In this section, an example of applying parasitic cancellation technique to the filter design is discussed. The purpose of this discussion is to give an example of the scenarios where the 3D modeling strategy for EMI filters can be used.

The goal of the filter mentioned in Section 3 is to suppress both DM noise and CM noise, especially for the frequency range of 10MHz~100MHz. Since the EPC of the CMC dictates the performance of S_{cc21} in this range, an EPC cancellation technique (Figure 19) proposed in [21] is therefore implemented and evaluated through the 3D modeling.

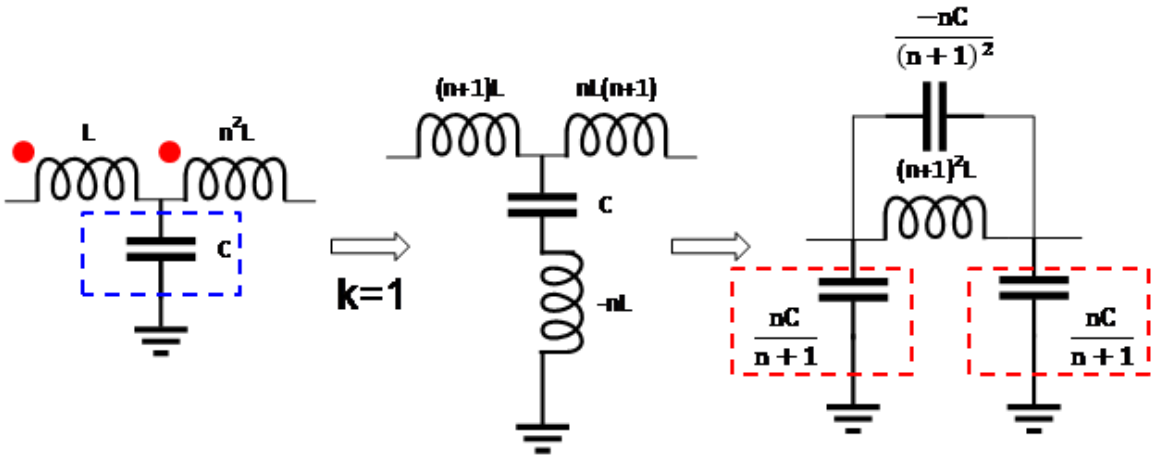


Figure 19. An EPC cancellation technique using a tapping capacitor.

This approach adds a tapping capacitor (marked in blue box) to the windings on the CMC. This tapping capacitor – when set at the right value – will cancel the EPC of the winding. The performance of the filter is maximized when the following criterion is met:

$$\frac{nC}{(n+1)^2} = EPC \tag{6}$$

However, the EPC of the winding often varies from unit to unit. Besides this, the cancellation technique itself introduces additional capacitances (marked in red dashed boxes in Figure 19), and the tapping capacitors themselves will be parasitically coupled to the CMC. Because of this, the circuit in Figure 19 is a relatively rough approximation of the

actual situation. The 3D model provides a solution to find the best tapping capacitor value and evaluates the influence introduced by the added parasitics. A group of simulation results can quickly be obtained from a 3D simulation with different values of tapping capacitance. Figure 20 shows the 3D model, where the tapping capacitor (modeled as a lumped element) is added between the first turn of the windings and the ground plane.

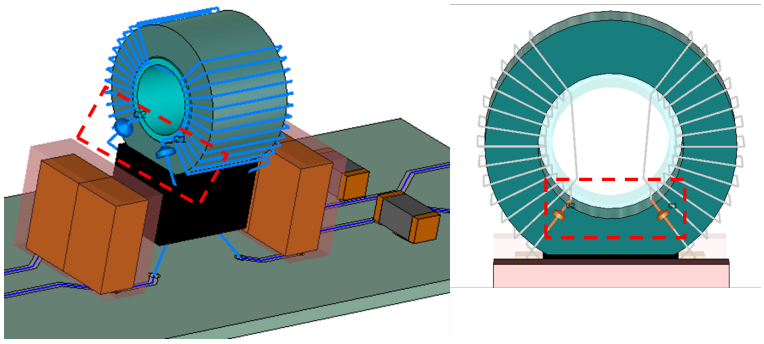


Figure 20. 3D model of the filter after applying the EPC cancellation technique.

The effect of the tapping capacitor can be observed in the frequency range from 10 to 100 MHz. We selected a frequency of 70 MHz as a reference point to compare the effect of different capacitor values on the magnitude of S_{cc21}. A parameter sweep is then implemented in 3D solver, sweeping the tapping capacitance value from 0.1pF to 10pF at a step of 0.5pF. The improvement in S_{cc21} at 70MHz is then plotted against the tapping capacitance in Figure 21, while the S_{cc21} at certain capacitance values are plotted in Figure 22.

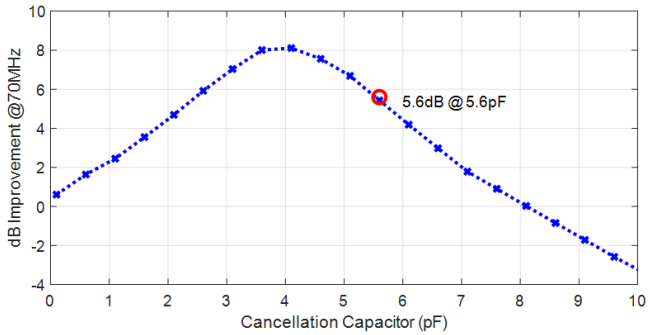


Figure 21. Improvement of S_{cc21} at 70MHz as a function of tapping capacitance.

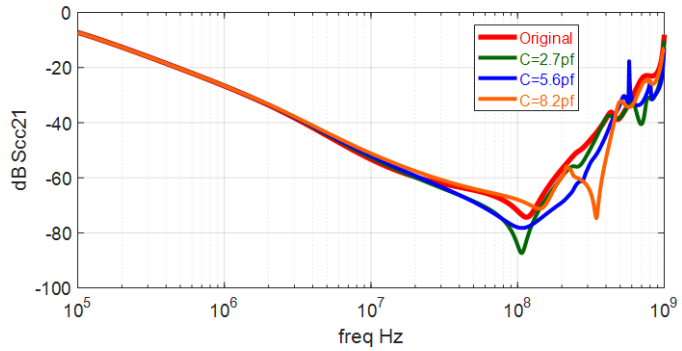


Figure 22. Simulated performance of the filter (S_{cc21}) with different tapping capacitor values.

At the same time, simulation results also show that adding a tapping capacitor will not affect S_{dd21} (Figure 23). Adding a tapping capacitor cancels the EPC of the coupled windings and introduces two equivalent Y-caps and a negative capacitor that cancels EPC of coupled inductors as shown in Figure 19. Therefore, the taping capacitor only affects the CM attenuation of the EMI filter (since no asymmetry is added). DM transmission can be affected if additional degrees of freedom are used, such as different tapping points for the windings.

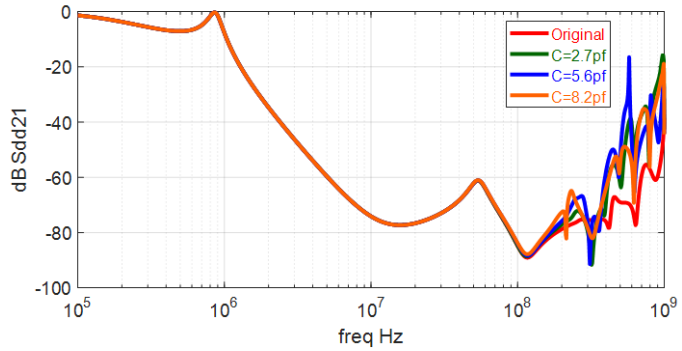


Figure 23. Simulated S_{dd21} of the filter with different tapping capacitor values.

From the curves above, it can be determined that the capacitance around 4 pF will yield the largest improvement of the CM suppression at 70MHz. The tapping capacitance within the range of 2~6 pF leads to at least 5dB improvement in S_{cc21} at 70MHz. The tapping technique is then put to measurement (Figure 24), with a 5.6 pF additional capacitance added

to the first turns of the CMC windings. The measurement shows 10dB improvement in the S_{cc21} at 70MHz, which is close to the predicted value in Figure 21. (5.6dB improvement). The DM attenuation in the range of 10MHz~100MHz is not affected, as shown in both simulation and measurement. At higher frequencies introducing the tapping capacitors reduces the DM attenuation which is correctly predicted by simulation.

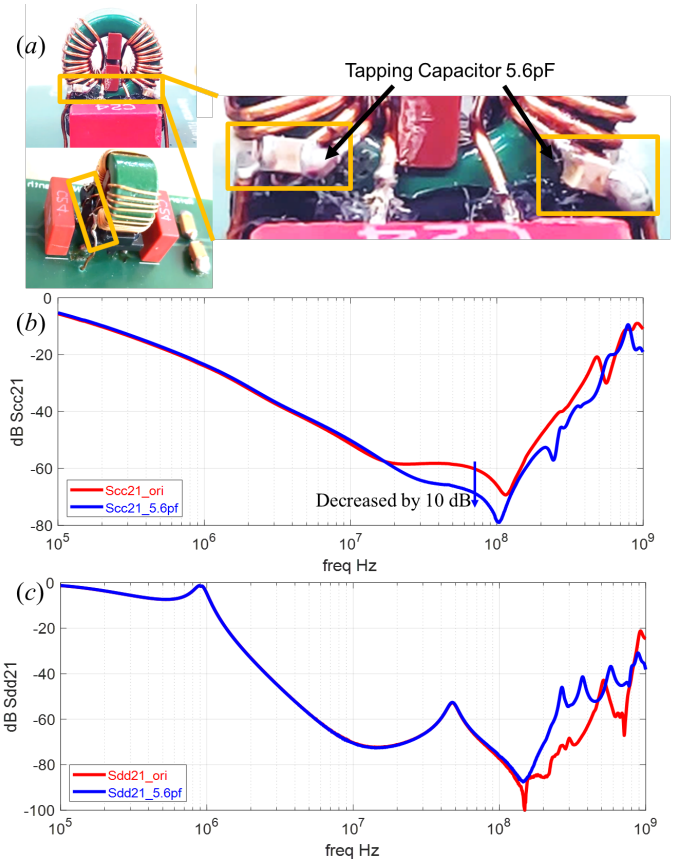


Figure 24. Tapping capacitor. (a) Installation of the tapping capacitor on the windings of the CMC. (b) Performance of the filter S_{cc21} in comparison with the original filter configuration. (c) Performance of the filter S_{dd21} in comparison with the original filter configuration.

5. SUMMARY

In this work, a 3D modeling strategy for EMI filters is proposed and evaluated. The model takes into account the internal structure of the film capacitor, the common mode choke, and the ceramic capacitor. Blocks and thin-wires are implemented to avoid explicit

modeling of the internal structure of the capacitors and simplify the CMC model, relieving the burden of the solver and mesh generator. The need for model parameter tuning is also minimized in the proposed strategy. The only parameter that requires tuning is the equivalent parallel capacitance of the choke (through the permittivity of the equivalent dielectric layer in the model).

A 3D model is built for an example EMI filter, the model demonstrated the ability of the proposed strategy to predict the filter performance up to 1 GHz (with various accuracy across the frequency range, but qualitatively correctly). An example of the procedure of improving the filter design utilizing the 3D model is presented.

Section 4 demonstrates that the effect of the tapping capacitors on the filter performance is correctly predicted up to 1 GHz for both common and differential modes. The proposed modeling strategy is therefore useful to not only the early design stage of EMI filters, but also at the iterative stage where multiple parameters need to be changed to fine-tune the filter performance.

ACKNOWLEDGEMENT

This work was supported in part by the National Science Foundation (NSF) under Grant IIP-1916535.

REFERENCES

[1] Zhenyang, Y., Shishan, W., Zheng, S., and Lee, B.-L., 'The reviews of integrated emi filters applied in power electronic system,' in '2015 Asia-Pacific Symposium on Electromagnetic Compatibility (APEMC),' IEEE, 2015 pp. 227–230.

[2] Wang, S., Odendaal, W., and Lee, F., 'Extraction of parasitic parameters of emi filters using scattering parameters,' in 'Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting.', volume 4, IEEE, 2004 pp. 2672–2678.

[3] Wang, S., Lee, F., and Odendaal, W., 'Controlling the parasitic parameters to improve emi filter performance,' in 'Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC'04.', volume 1, IEEE, 2004 pp. 503–509.

[4] Moonen, N., Buesink, F., and Leferink, F., 'Optimizing capacitor placement in emi-filter using back annotation of 3d field coupling parameters in circuit models,' in '2016 International Symposium on Electromagnetic Compatibility-EMC EUROPE,' IEEE, 2016 pp. 576–580.

[5] Stojanovic, M., Lafon, F., Op't Land, S., Perdriau, R., and Ramdani, M., 'Determination of equivalent coupling surface of passive components using the tem cell,' IEEE Transactions on Electromagnetic Compatibility, 2017, **60**(2), pp. 298–309.

[6] Wang, S., Lee, F. C., and van Wyk, J. D., 'A study of integration of parasitic cancellation techniques for emi filter design with discrete components,' IEEE transactions on Power Electronics, 2008, **23**(6), pp. 3094–3102.

[7] Yoneda, S., Hirose, K., Kobayashi, A., Sasaki, Y., and Miyazaki, C., 'A study for designing an esl-cancelling circuit for shunt capacitor filters based on the biot-savart law,' in '2017 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI),' IEEE, 2017 pp. 17–21.

[8] Kovačević, I. F., Friedli, T., Müsing, A. M., and Kolar, J. W., '3-d electromagnetic modeling of parasitics and mutual coupling in emi filters,' IEEE Transactions on Power Electronics, 2013, **29**(1), pp. 135–149.

[9] Kovačević, I. F., Friedli, T., Muesing, A. M., and Kolar, J. W., '3-d electromagnetic modeling of emi input filters,' IEEE Transactions on Industrial Electronics, 2013, **61**(1), pp. 231–242.

[10] Kovačević, I. F., Friedli, T., Muesing, A. M., and Kolar, J. W., 'Electromagnetic modeling of emi input filters,' in '2012 7th International Conference on Integrated Power Electronics Systems (CIPS),' CIPS, 2012 pp. 1–9.

[11] Moonen, N., Vogt-Ardatjew, R., Roc'h, A., and Leferink, F., '3-d full-wave high frequency common mode choke modeling,' IEEE transactions on electromagnetic compatibility, 2019, **62**(3), pp. 707–714.

[12] Asmanis, A., Stepins, D., Dzenis, A., and Asmanis, G., '3d modeling of surface-mount capacitors and mutual couplings between them,' in '2017 International Symposium on Electromagnetic Compatibility-EMC EUROPE,' IEEE, 2017 pp. 1–6.

[13] Asmanis, A., Stepins, D., Asmanis, G., and Ribickis, L., '3d modelling and analysis of parasitic couplings between surface-mount components of emi filters,' in '2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC),' IEEE, 2018 pp. 496–501.

[14] He, R., Walunj, S. A., Yong, S., Khilkevich, V., Pommerenke, D., Aichele, H., Boettcher, M., Hillenbrand, P., and Klaedtke, A., 'Modelling strategy for film capacitors in emi filters,' in '2019 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+ SIPI),' IEEE, 2019 pp. 259–265.

[15] Vuillermet, Y., Chadebec, O., Lupin, J., Saker, A., Meunier, G., and Coulomb, J.-L., 'Optimization of low-voltage metallized film capacitor geometry,' IEEE transactions on magnetics, 2007, **43**(4), pp. 1569–1572.

[16] Dubickas, V. and Edin, H., 'High-frequency model of the rogowski coil with a small number of turns,' IEEE Transactions on Instrumentation and Measurement, 2007, **56**(6), pp. 2284–2288.

[17] Sullivan, C. and Kern, A., 'Capacitors with fast switching require distributed models,' CR Sullivan, AM Kern, 2001, pp. 1497–1503.

[18] Elektronik, W., 'Wurth elektronik we-cmb nizn common mode power line choke 744842311 datasheet, [revision 002.007].' 2016, accessed on: Jan. 1, 2020.

[19] Kotny, J.-L., Margueron, X., and Idir, N., 'High-frequency model of the coupled inductors used in emi filters,' IEEE Transactions on Power Electronics, 2011, **27**(6), pp. 2805–2812.

[20] Cuellar, C., Tan, W., Margueron, X., Benabou, A., and Idir, N., 'Measurement method of the complex magnetic permeability of ferrites in high frequency,' in '2012 Ieee international instrumentation and measurement technology conference proceedings,' IEEE, 2012 pp. 63–68.

[21] Wang, S. and Lee, F. C., 'Analysis and applications of parasitic capacitance cancellation techniques for emi suppression,' IEEE Transactions on Industrial Electronics, 2009, **57**(9), pp. 3109–3117.

III. STUDY ON THE ROOT CAUSE OF THE VARIATION IN CONDUCTED EMISSIONS OF FLYBACK CONVERTERS

ABSTRACT

Flyback converters are commonly used in low voltage power adapters. The conducted emissions performance of the flyback converters is essential for meeting the timeline for the publication of consumer electronic devices. The flyback transformers have been reported to be responsible for the variation in conducted emissions results. Massive simulation and measurements are implemented to reveal the relationship between the winding variation and the variation in CE. A SPICE model is proposed to explain the observed relationship between the interwinding capacitance of the transformer and the conducted emission results. A good correlation between the variation among simulated results and measurement results is presented.

Keywords: Flyback converter, Conducted Emissions, Design of Experiments, Interwinding Capacitance

1. INTRODUCTION

Isolated power converters are commonly used in power adapters for consumer electronics. The transformer is a key part of voltage transformation and isolation [1]. The common mode (CM) coupling capacitance of the transformer is one of the main contributors of the CM noise, as has been verified in many previous studies ([2][3][4][5]). Different approaches has been brought up and implemented to reduce the interwinding capacitance. ([4][5][6]). In [7] , a two-capacitance model was introduced to simplify the evaluation of a transformer. The conducted emission path and the equivalent model based on the two-capacitor transformer model are illustrated in Figure 1. b. C_{AD} and C_{BD} are the two

capacitors that represent the transformer in the common mode current path ([8]). The two-capacitor model leads to an analytical formula that relates the capacitance of the transformer with the CE.

$$V_{CM} = \frac{V_{SW} \bullet Z_{LISN} \bullet \frac{C_{BD}}{C_{Total}+C_y+C_{q2}}}{\frac{1}{j\omega\left(C_{Total}+C_y+C_{q2}\right)} + Z_{LISN} + Z_{ED} + Z_{SG}} \tag{1}$$

Where C_y and C_{q2} stands for the deliberate Y-capacitor and parasitic capacitance between the primary side ground and secondary side ground. C_{Total} is the sum of $C_{BD}$and C_{AD}. V_{SW} is the switching noise of the MOSFET. Z_{LISN} is the common mode impedance of the LISN, Z_{SG} is the impedance between the secondary ground and earth. and Z_{ED} is the impedance of the common mode choke in the EMI filter.

Studies in [5] considered the turns in a transformer as a well-controlled uniform distribution inside the winding. However, due to the winding procedure, the variance in the turns' distribution is inevitable. The variation can be so large that different winding techniques not only provide different common mode CE performance, but also different fluctuation range and passing rate. Analyzing different winding techniques requires massive simulation and measurements, which make the analysis tedious.

On the other hand, due to the fine-tuned shielding winding technique, the interwinding capacitance of a flyback transformer is usually very small. Following (1), considering $C_{BD} \ll C_y$,$C_{BD} \ll C_{AD}$, and $C_{q2} \ll C_y$, the common mode conducted emissions is approximated as (2).

$$|V_{CM}| \approx |C_{BD}| \frac{V_{SW} \bullet Z_{LISN} \bullet j\omega}{1 + \left(C_{AD} + C_y\right)\left(Z_{LISN} + Z_{ED} + Z_{SG}\right)} \tag{2}$$

The above approximations are valid since C_{BD} studied in this work is in sub-pF range, C_{AD} in tens of pF range, while C_y is an intended capacitor, usually above 100 pF.

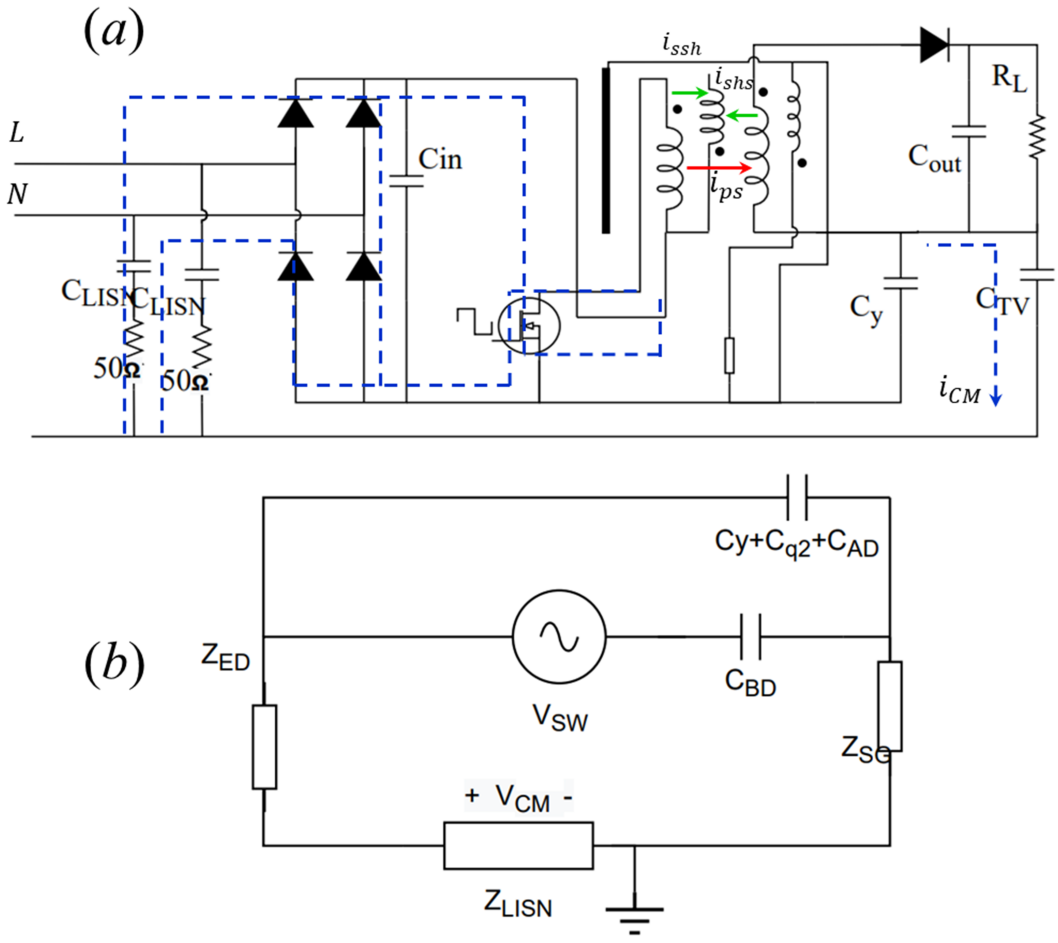


Figure 1. SPICE model for analyzing the conducted emissions in a flyback converter. (a). Common Mode current path through a flyback transformer with shielding winding. (b) Simplified model for common mode conducted emissions based on two-capacitor model for the flyback transformer.

This works presents a simulation approach aiming at 2D analysis of the transformer based on reuse of mesh

Which reduces the time cost for massive simulation (Sec. II). Massive measurement aiming at evaluation of the transformers and conducted emissions are conducted with the help of pluggable test fixtures. The results are presented and analyzed in Sec. III. The CE and interwinding capacitance relationship found in Sec. III does not fit the formula (1).

Therefore, an updated SPICE model is proposed in IV. The proposed SPICE model leads to an analytical formula that predicts the CE based on the interwinding capacitance of the transformer and matches the relationship between both CE vs. C_{BD} and CE vs. C_y.

2. CROSS SECTION OF TRANSFORMER

The cross-section of the transformer studied in this work is illustrated in Figure 2. The transformer has 4 windings: Primary winding (4 layers, 93 turns), shielding winding (12 turns), Secondary winding, and Auxiliary winding.

There is also a shielding copper tape in the most inner layer of the bobbin. The purpose of the shielding winding is to adjust the primary to secondary inter-winding capacitance. [4] analyzed the influence of the shielding winding, [5] introduces an analytical formula that provides the best performance shielding winding configuration. [6] calculated the idea width for the shielding layer that isolates the ferrite and the primary winding in a transformer.

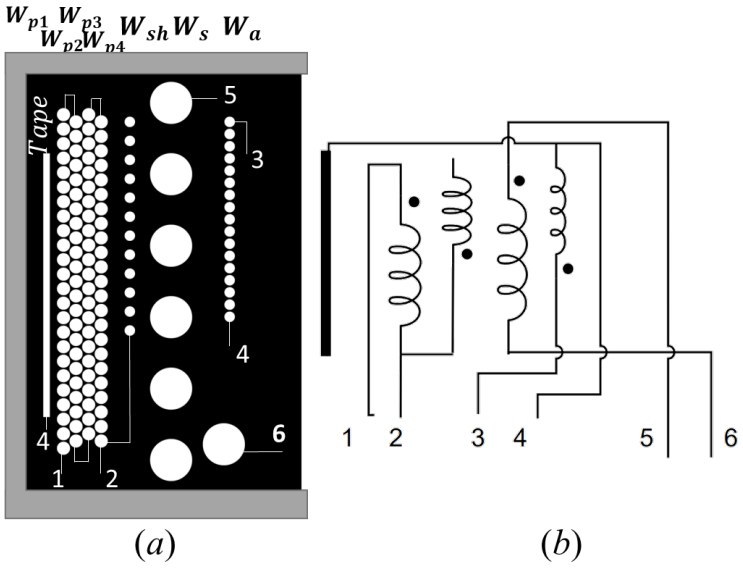


Figure 2. Cross Section of the transformer studied. (a) CT images of a transformer.

All above techniques lead to a small interwinding capacitance of the transformers. However, the variation between the shielding winding is large since the winding procedure is hard to control.

Figure 3.a shows the CT image of 4 different transformers that follow the same winding configuration. By stacking the four images together and have the copper tape shielding aligned, it is shown in Figure 3. b that the repeatability of the windings is poor. If the repeatability were good, most of the circles in the stacked image should be white color.

A digital image processing (DIP) is introduced to convert the CT image into a 2D cross-section recognizable for the 2D solver. There are 129 round cross-sections in total, and a piece of copper shielding that is connected to the primary ground. The potential of each turn in the cross-section is assigned according to its position in the winding. (Figure 4). The different color annotates different winding. The darkness of the turn cross-section indicates how close the potential is to zero. The extracted cross-section is then converted to 2D simulation in Q2D.

The primary output of the 2D solver is a per unit length capacitance matrix. In this matrix. The turn-to-turn capacitance C_{tt} is acquired by approximating the turns as translational invariant parallel wires. The total length of each turn is $l = 2\pi r$, where r is the radius of the layer in which the turn is in. The turn-to-turn capacitances can then be developed into interwinding capacitance C_q in (3)-(5). The $C_q$is a behavioral capacitance that stands for the admittance in the path of the common mode current that flows from the primary winding to the secondary windinng. The C_q value becomes negative when the overall common mode current flows from secondary side to the primary side.

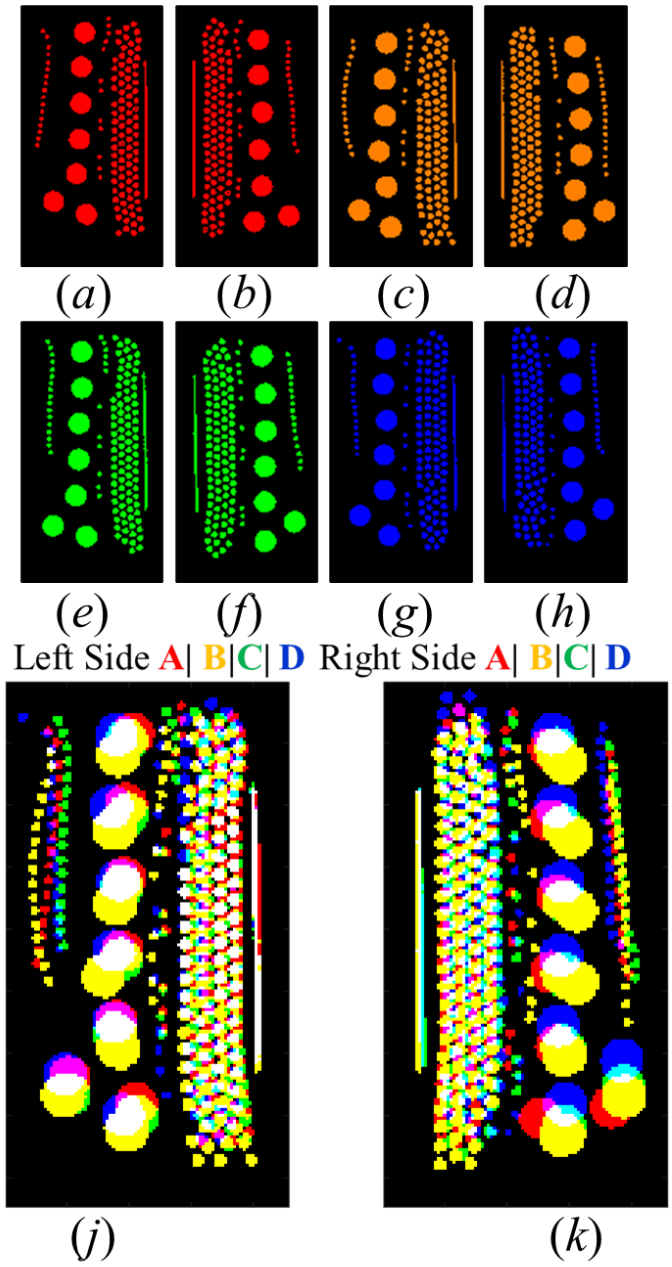


Figure 3. CT image of 4 different transformers. (a) – (f) Individual transformers' cross-section, on the left and right side. (b) Stackup image of the 4 cross-sections. The alignment is based on the position of the shielding copper tape.

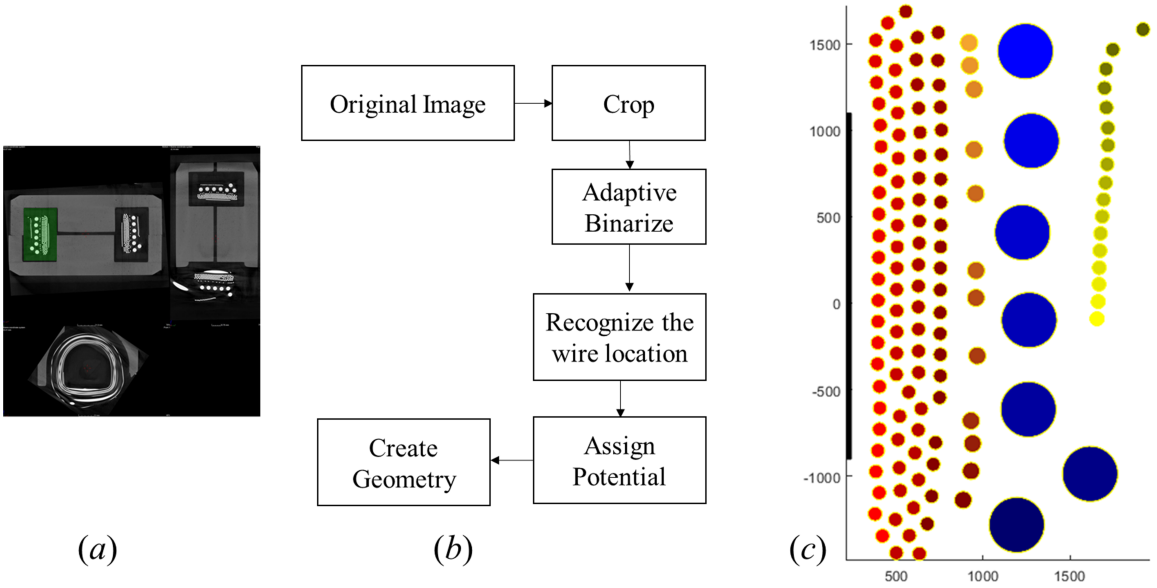


Figure 4. Digital image process that converts the CT image into 2D cross-section. (a) Input of the image processing. (b) Flow chart of the image processing. (c) Output of the image processing.

$$C_q = \frac{i_{CM}}{j\omega V_{sw}} = \frac{i_{shs} - i_{ssh} + i_{ps}}{j\omega V_{sw}} \tag{3}$$

$$i_{ps} = \int_0^{H_s} \int_0^{H_p} C_{pxsy} \frac{\mathrm{d}\left(V_{px} - V_{sy}\right)}{\mathrm{d}t} \mathrm{d}x\mathrm{d}y \tag{4}$$

$$i_{shh} - i_{ssh} = \int_0^{H_s} \int_0^{H_{sh}} C_{shzsy} \frac{\mathrm{d}\left(V_{shz} - V_{sy}\right)}{\mathrm{d}t} \mathrm{d}z\mathrm{d}y \tag{5}$$

In (4) and (5), the two components of the common mode current is calculated through integration of distributed turn to turn capacitance paths. C_{pxsy} is the capacitance from turn at height x in the primary winding to turn at height y in the secondary winding. C_{shzsy} is the capacitance from turn at height z in the shielding winding to turn at height y in the secondary winding. Both C_{pxsy} and C_{shzsy} can be found in the turn to turn capacitance matrix C_{tt} . The integration boundary H_s, H_p, H_{sh} are the total height of the secondary

winding, primary winding, and shielding winding, respectively. The C_{tt} matrix leads to a lumped interwinding capacitance. Although the authors of [1] used C_q to denote the interwinding capacitance during common mode noise modeling, while the authors of [9] used C_{BD}, derivations in.(6)-(10) show that $C_{BD} = C_q$ for the transformer. Following the derivations in [1] and [9]:

$$k_1 = C_{AD} + C_{BD} \tag{6}$$

$$\frac{1}{2}k_7 = (n-1)\,C_{AD} - C_{BD} \tag{7}$$

$$k_1 = \sum_{i=1}^{N}\sum_{j=1}^{M} C_{PiSj} \tag{8}$$

$$k_7 = 2n\sum_{i=1}^{N}\sum_{j=1}^{M} C_{PiSj}\frac{N-i}{N-1} - 2\sum_{i=1}^{N}\sum_{j=1}^{M} C_{PiSj}\frac{M-j}{M-1} \tag{9}$$

The C_{BD} is solved as (10) in the two-capacitor model for fly back transformer.

$$\begin{aligned} C_{BD} &= \sum_{i=1}^{N}\sum_{j=1}^{M} C_{PiSj}\left(\frac{n-1}{n} - \frac{N-i}{N-1} - \frac{1}{n}\frac{M-j}{M-1}\right) \\ &\approx \sum_{i=1}^{N}\sum_{j=1}^{M} C_{PiSj}\left(\frac{i}{N} - \frac{1}{n}\frac{M-j}{M}\right) \\ &= \int_0^{H_s}\int_0^{H_p} C_{pxsy}\left(V_{px}/V_{sw} - V_{sy}/V_{sw}\right)\mathrm{d}x\mathrm{d}y \end{aligned} \tag{10}$$

The integration form of C_{BD} is similar to (4). Therefore, in a two-capacitor model of a two-winding transformer:

$$i_{CM} = i_{ps} = j\omega C_{BD} V_{sw} \tag{11}$$

A multi-winding flyback transformer can be modeled with two capacitors C_{BD} as well. The expression of C_{BD} becomes more complicated since more windings and voltage distributions are involved. But as long as $j\omega C_{BD}$ stands for the admittance in the path for the common mode current flowing from primary side to secondary side of the transformer, the two annotations from different authors are equivalent.

The interwinding capacitance then can be acquired for all four CT images. As listed in Table 1, the interwinding capacitance has large variation among the four transformers.

Table 1. Interwinding capacitance.

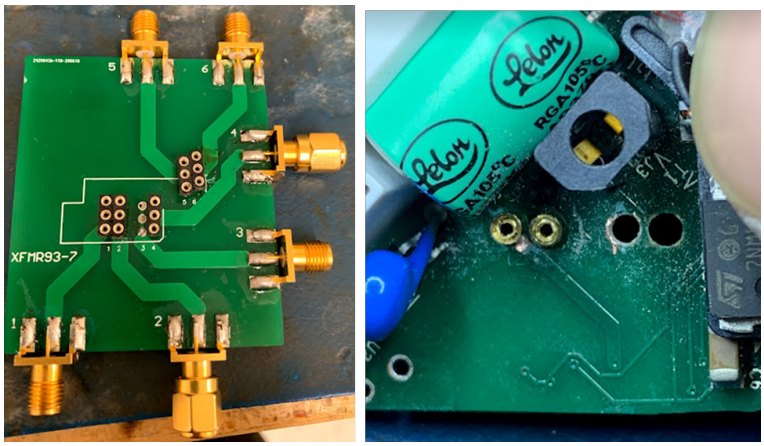
ID	Capacitance (pF)	CE Test Result
A	0.226	Fail
B	0.153	Fail
C	-0.127	Pass
D	-0.165	Pass

In order to reveal the variation of the winding capacitance, analysis on several samples is far from enough. Due to lack of samples and the time-consuming nature of the measurement, massive simulations are helpful for revealing such variation and makes other statistical analysis feasible. The interwinding capacitance can be estimated through 2D analysis, approximating the turns as translational invariant structure. [10].

Commercial 2D solvers such as Q2D utilizes FEM to acquire the turn-to-turn capacitance. Despite the reliability of this solver, small tuning in the statistical analysis leads to regeneration of mesh and thus unnecessary cost of time. The number of conductors exceeds 100, which leads to tens of minutes of solving time for each cross-section. Therefore, a 2D solver that reuses mesh and utilizes MoM is developed. Utilizing this solver reduces the time cost for each cross-section to less than a minute and makes the massive simulation feasible.

3. EVALUATION OF TRANSFORMER

A test vehicle is developed to evaluate the interwinding capacitance of the transformers. (Figure 5). On the test vehicle, pin sockets are used to hold the transformer in place. The microstrips that connect from the SMA connectors to the pin sockets are of same length. Another modified circuit board is used to measure the conducted emissions using different transformers. Reusing the same test vehicle avoids fluctuations in the inter-component coupling.



(*a*) (*b*)

Figure 5. Pluggable test vehicle for the transformer evaluation. (a) Evaluation board for the interwinding capacitance. (b) Evaluation board for the conducted emissions (two sockets have been installed).

3.1. MEASUREMENTS ON INTERWINDING CAPACITANCE

Since the device under test (DUT) has 6 ports, multi-port measurement is required. Given the small value of the target capacitance, the measurement must be conducted with either oscilloscope and source or a vector network analyzer (VNA). [1] suggested that VNA has higher accuracy, while the oscilloscope measurement setup is more suitable for capacitances with larger values. The transformers studied in this work have very small interwinding capacitance due to the shielding winding. Therefore, a calibrated VNA is

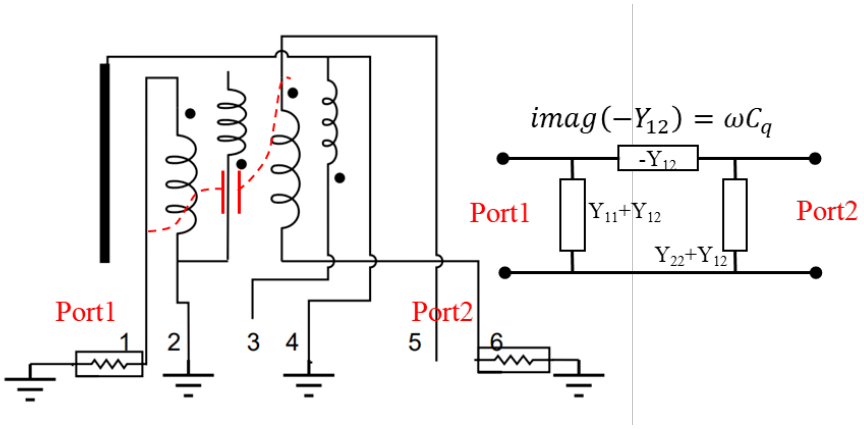


Figure 6. Configuration for evaluating the transformer's interwinding capacitance from primary to secondary winding.

needed. With the measured 6-port S-parameters, different terminations can be applied to the S-parameters, leading to different parasitics of the transformer. (12)- (18) derives of the capacitance between the primary and secondary winding, following the termination configuration shown in Figure 6.

$$[\boldsymbol{I}] = \left[\overline{\overline{\boldsymbol{Y}}}\right]\left[\overline{\overline{\boldsymbol{V}}}\right] \tag{12}$$

Since terminal 2 and 4 are shorted to ground, while port 3 and 5 are left open:

$$V_2 = V_4 = 0 I_3 = I_5 = 0 \tag{13}$$

$$\begin{bmatrix} I_1 \\ I_6 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{16} \\ Y_{61} & Y_{66} \end{bmatrix} \begin{bmatrix} V_1 \\ V_6 \end{bmatrix} + \begin{bmatrix} Y_{13} & Y_{15} \\ Y_{63} & Y_{65} \end{bmatrix} \begin{bmatrix} V_3 \\ V_5 \end{bmatrix} \tag{14}$$

$$\begin{bmatrix} I_3 \\ I_5 \end{bmatrix} = \begin{bmatrix} Y_{31} & Y_{33} & Y_{35} & Y_{36} \\ Y_{51} & Y_{53} & Y_{55} & Y_{56} \end{bmatrix} \begin{bmatrix} V_1 \\ V_3 \\ V_5 \\ V_6 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{15}$$

Rewrite (15):

$$-\begin{bmatrix} Y_{33} & Y_{35} \\ Y_{53} & Y_{55} \end{bmatrix}\begin{bmatrix} V_3 \\ V_5 \end{bmatrix} = \begin{bmatrix} Y_{31} & Y_{36} \\ Y_{51} & Y_{56} \end{bmatrix}\begin{bmatrix} V_1 \\ V_6 \end{bmatrix} \tag{16}$$

The relationship between I_1, I_6 and V_1, V_6 then leads to a new Y matrix in (17).

$$\begin{aligned} \begin{bmatrix} \overline{\overline{Y'}} \end{bmatrix} &= \begin{bmatrix} I_1 \\ I_6 \end{bmatrix}\begin{bmatrix} V_1 \\ V_6 \end{bmatrix}^{-1} \\ &= \begin{bmatrix} Y_{11} & Y_{16} \\ Y_{61} & Y_{66} \end{bmatrix} - \begin{bmatrix} Y_{13} & Y_{15} \\ Y_{63} & Y_{65} \end{bmatrix}\begin{bmatrix} Y_{33} & Y_{35} \\ Y_{53} & Y_{55} \end{bmatrix}^{-1}\begin{bmatrix} Y_{31} & Y_{36} \\ Y_{51} & Y_{56} \end{bmatrix} \end{aligned} \tag{17}$$

$$C_q = \frac{\text{imag}\left(-Y'(2,1)\right)}{\omega} \tag{18}$$

In the beginning, the terminations are assigned to terminals 2,3,4,5 as short, open, short, open, respectively. Consequentially, I_3=I_5= 0, V_2=V_4= 0. Therefore, (12) is broken down into (14) and (15). And then (15) is rewritten as (16) Substituting (16) back to (14), the new Y matrix is expressed as (17). The new Y matrix directly leads to C_q, as expressed in (18).

To measure the 6-port network, 15 measurements are needed when using a 2-port VNA, since $\binom{2}{6} = 15$. The VNA is calibrated to the SMA cables used for the measurements. The six microstrips on the test vehicle are of the same length. Following the calculation in (17)(18) , the C_q acquired from the empty fixture is around 10 fF, while the acquired C_q from the transformers are in the range of 100 fF (Figure 7).

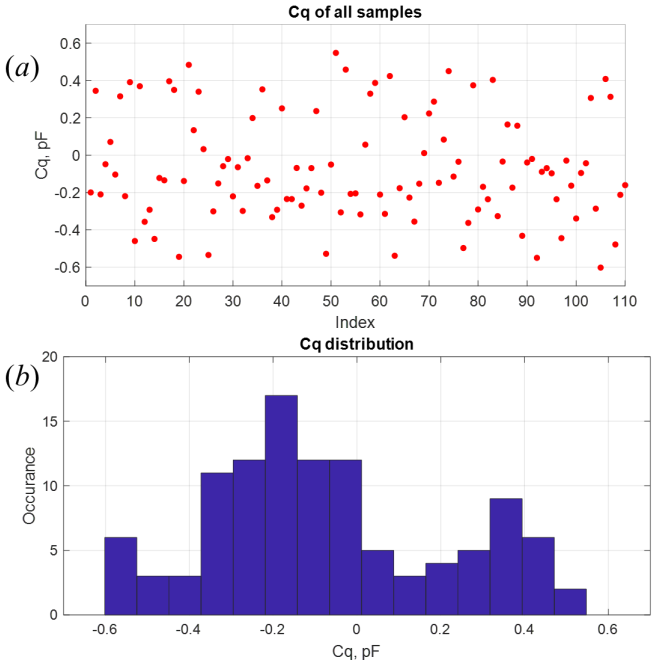


Figure 7. Interwinding capacitance measurement results. (a) C_q values of the 18 samples. (b) Histogram of the C_q values.

The capacitance distribution of the tested 18 samples fall in the range of -0.6~0.6 pF. According to (2), the CE should have the similar distribution: half of the CE fall into the lower range (corresponding to the values between -0.2pF~0.2pF) and other half fall into the higher range.

3.2. CONDUCTED EMISSION ASSESSMENT

The measurement of the conducted emission follows the CISPR 16 standard [11]. A TV is set facing a vertical wall. The distance and height of the TV is fixed according to the standard.

An oscilloscope is used to capture the conducted emissions. The post-processing procedure proposed in [12] was used to apply Quasi-peak function. This approach takes much less acquisition time compared to a spectrum analyzer. The acquisition time of the oscilloscope can be reduced to 1s for one measurement. The setup of the measurement is sown in Figure 8.

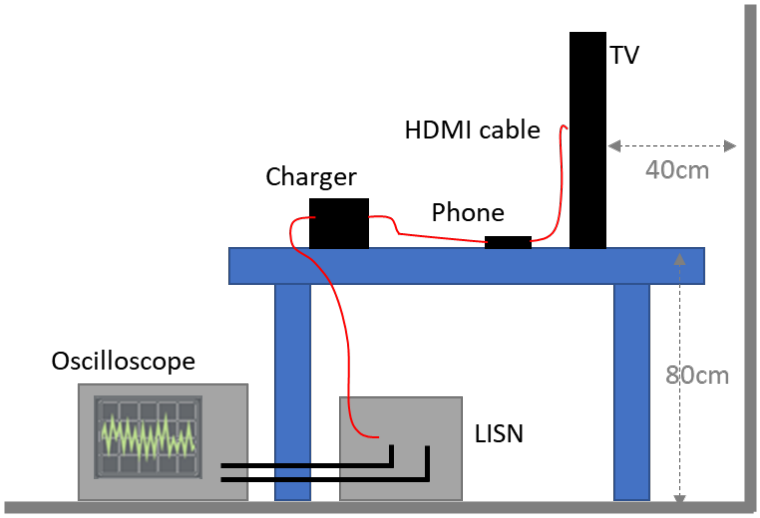


Figure 8. Measurement setup of conducted emissions.

Part of the common mode CE results are presented in Figure 9.a. The frequency range of 300 kHz~1 MHz is of most interest since some units failed to meet the compliance. By stacking the results together, the peak value at around 670 kHz becomes the main focus due to the large variation. Figure 9.c. shows the variation is as large as 10dB. Some units can not pass the compliance test due to such variation.

With the assessment on both interwinding capacitance and CE of the flyback transformers, the relationship between capacitance and the CE is revealed in Figure 10. Following (1), the CE vs. C_q should follow a V-shape function that has turning point at $C_q = 0$. It has been proven to work well in a scenario where the capacitance is in tens of pF range. In this

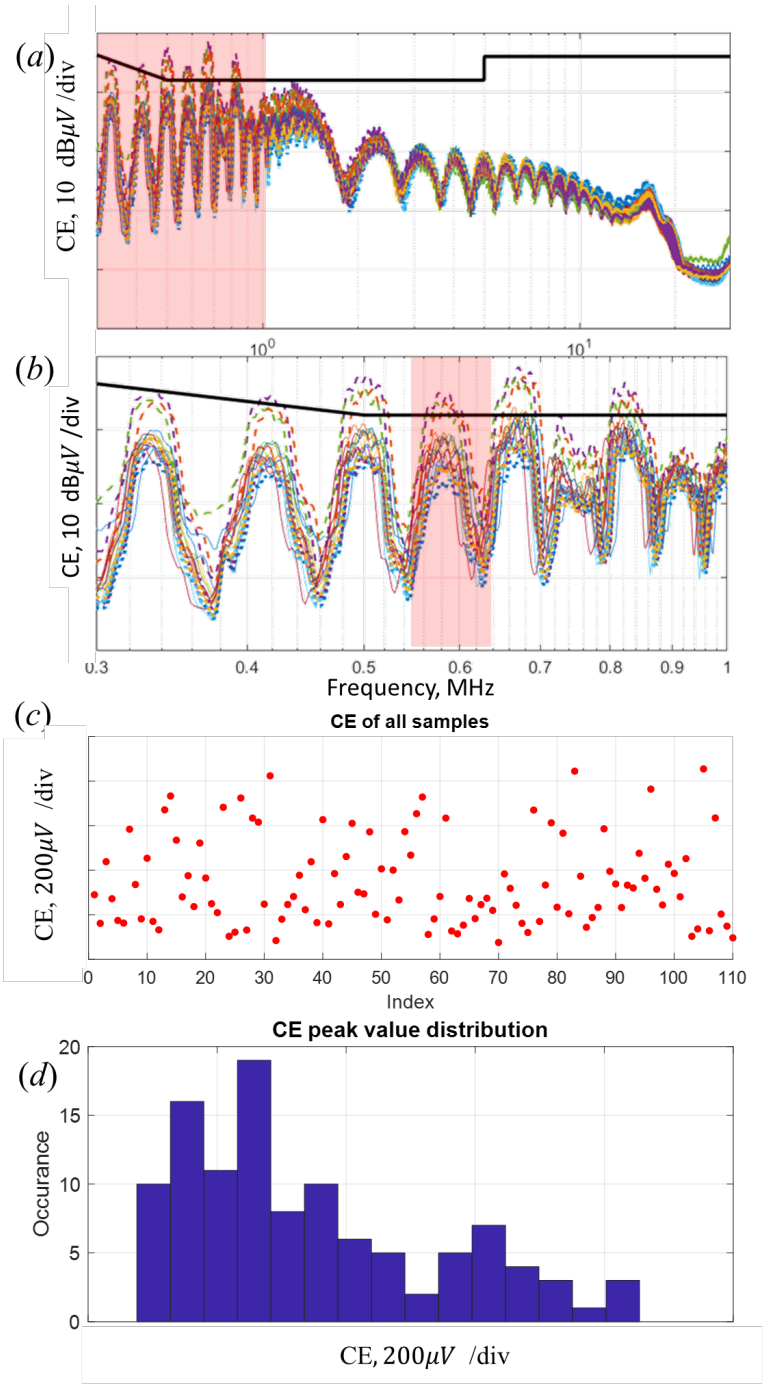


Figure 9. CE results. (a) Quasi peak results within 0.3 30 MHz. (b) Quasi peak results within 0.3 1 MHz. (c) Peak level in the range 0.63 0.7 MHz. (d) Histogram of the peak level in the range 0.63 0.7 MHz.

paper, however, thanks to the shielding winding, the C_q value is below 1 pF. Therefore, the relationship between the capacitance and CE is not well represented by the proposed circuit model in (1).

4. SPICE MODEL FOR CE VS. C_Q

The primary ground to earth capacitance (C_{pg}) is usually omitted due to its small value and the difficulty in extracting its value. In this section, a SPICE model is brough up and provides an analytical solution for the relationship between the CE and capacitance. The updated SPICE model is shown in Figure 11.

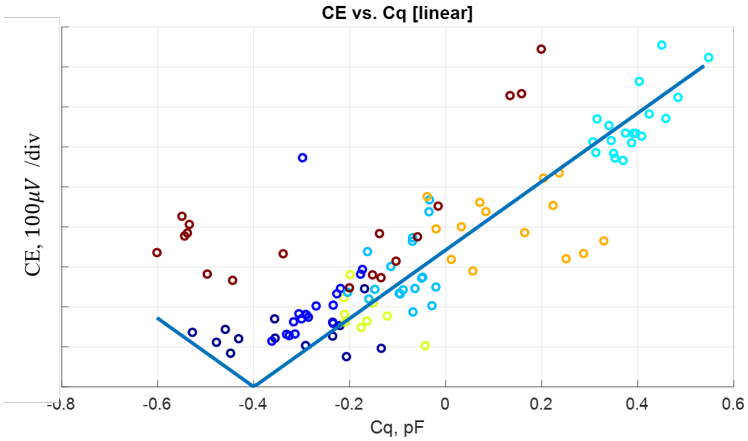


Figure 10. Interwinding capacitance and conducted emissions. Different colors of dots indicate different batch of samples.

The C_{tv} is the capacitance between the TV and ground, which is related to Z_{SG} in Figure 1 by $j\omega C_{tv} = Z_{SG}^{-1}$. In the SMPS, the purpose of the C_y capacitor is to form a virtual ground for the secondary side, thus reduce conducted emissions([13]). An analytical form for common mode conducted emissions can then be derived. The first step for the derivation is to convert the Δ shape tri-capacitor circuit (C_{tv}, C_{BD}, C_{pg}) into a Y shape circuit (Figure 12.a).

The $\Delta - Y$ conversion is expressed in 19.

$$C_1 = \frac{\Sigma_{CC}}{Ctv}, C_Y = \frac{\Sigma_{CC}}{Cpq}, C_Z = \frac{\Sigma_{CC}}{Cq} \tag{19}$$

The equivalent current source is expressed as:

$$\boldsymbol{I_{eq}} = V_{sw} \bullet j\omega C_X = V_{sw} \bullet j\omega \frac{\Sigma_{CC}}{C_{tv}} \tag{20}$$

Where $\Sigma_{CC} = C_{pg}C_q + C_{pg}C_{tv} + C_qC_{tv}$ is a common term. Since $C_{pg} \ll C_{tv}, C_q \ll C_{tv}$, Σ_{CC}can be reduced to

$$\Sigma_{CC} \approx C_{pg}C_{tv} + C_qC_{tv} \tag{21}$$

The common mode current that flows through the LISN impedance is then expressed as:

$$\boldsymbol{i_{CM}} = \frac{I}{Y_Z + Y_C} \bullet Y_Z = V_{SW} \bullet j\omega \frac{\Sigma_{CC}}{C_{tv}} \bullet \frac{Y_Z}{Y_Z + j\omega\Sigma_C} \tag{22}$$

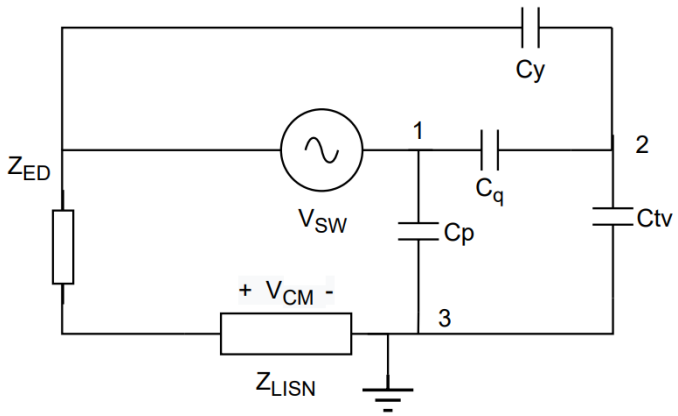


Figure 11. Updated circuit model for CE and C_q.

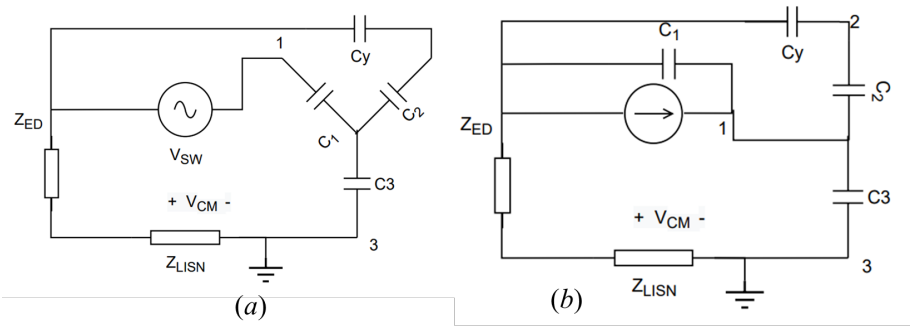


Figure 12. Y shape circuit converted from the Δ shape circuit (C_{tv}, C_{BD}, C_{pg}). (a). The Y shape circuit. (b). Norton equivalent of the Y shape circuit.

Where Σ_C is the equivalent capacitance of C_1, C_2, C_y together. Y_Z is the admittance of the serial components C_3, Z_{ED},and Z_{LISN}.$Y_C$is the admittance of Σ_C.

$$\begin{aligned} \Sigma_C &= \frac{\Sigma_{CC}}{C_{tv}} + \frac{C_y \Sigma_{CC}/C_{pq}}{C_y + \Sigma_{CC}/C_{pq}} \\ Y_C &= j\omega\Sigma_C \\ Y_Z &= \frac{1}{(j\omega C_3)^{-1} + j\omega L + r} = \frac{j\omega\Sigma_{CC}}{C_q - j\omega^2 L\Sigma_{CC} + j\omega\Sigma_{CC} r} \end{aligned} \tag{23}$$

The expansion of (22) is too long, therefore omitted. The final form is expressed in (25). The condition of $C_{pg} \ll C_{tv}, C_q \ll C_{tv}$ for another time during the expansion.

$$i_{CM} = V_{SW} \bullet \frac{j\omega\Sigma_{CC}}{C_{tv} + \Sigma_C \frac{C_q C_{tv}}{\Sigma_{CC}} + Z_s\,(j\omega\Sigma_C C_{tv})} \tag{24}$$

$$i_{CM} = V_{SW} \bullet \frac{m + C_q}{n + Z_S C_q} \tag{25}$$

$$m = C_{pg}\left(1 + C_y/C_{tv}\right) n = \frac{\left(C_y/C_{tv} + 1\right)}{j\omega} + mZ_s + Z_s C_y \tag{26}$$

Where impedance of Z_{LISN} is expressed as $r + j\omega L$.

Following the derivation of (19)-(26) the C_q that leads to the lowest CE is $C_q = -C_{pg}(1 + Cy/C_{tv})$. In this case, the capacitance C_{pg} although small, becomes significant with a factor of $1 + Cy/C_{tv}$. Following the formula in (2) where C_{pg} has been omitted, the relationship curve is a V-shape function symmetrical to C_q=0, CE = 0. However, a V shape function that turns at $C_q = -0.3pF$ can be found and fits the measurement results well (Figure 10). According to (26), the turning point location means C_{pg} = 15 fF. This value is so small that it can't significantly affect the relationship for CE vs. C_y. Figure 13 demonstrates the relationship between CE and C_y from measurement results. The alternation of C_y values is accomplished by changing the value of the Y-capacitor on the circuit board for CE measurement. The measurement results fit well with the prediction based on the proposed SPICE model.

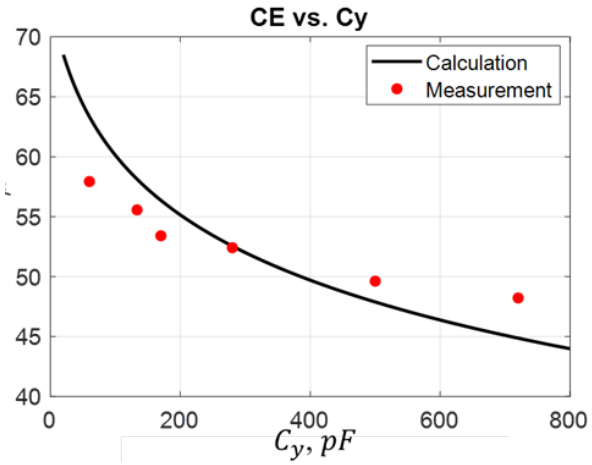


Figure 13. CE relationship with Cy capacitance and conducted emissions.

5. RESULTS ANALYSIS

In this work, a transformer with very small interwinding capacitanceC_q is studied. Lack of control in the winding procedure leads to variations among the transformers in terms of C_q.The small variation in the C_q value result in variation in the CE results. 2D

analysis were carried out to reveal the variation of the parasitic capacitance of the transformers. Massive measurements were conducted to extract the interwinding capacitance of the transformers.

An analytical formula is derived from an updated SPICE model that includes C_{pg}. The derivation indicated that the C_q that leads to best CE performance is not necessarily at 0 pF. This finding well-explained the trend of the CE vs. C_q found in measurements and doesn't violate the relationship between the CE and another importance capacitance C_q.

ACKNOWLEDGEMENT

This work was supported in part by the National Science Foundation (NSF) under Grant IIP-1916535.

REFERENCES

[1] Zhenyang, Y., Shishan, W., Zheng, S., and Lee, B.-L., 'The reviews of integrated emi filters applied in power electronic system,' in '2015 Asia-Pacific Symposium on Electromagnetic Compatibility (APEMC),' IEEE, 2015 pp. 227–230.

[2] Fu, K. and Chen, W., 'Evaluation method of flyback converter behaviors on common-mode noise,' IEEE Access, 2019, **7**, pp. 28019–28030.

[3] Fu, K. and Chen, W., 'Balance winding scheme to reduce common-mode noise in flyback transformers,' Journal of Power Electronics, 2019, **19**(1), pp. 296–306.

[4] Chen, H., Zheng, Z., and Xiao, J., 'Determining the number of transformer shielding winding turns for suppressing common-mode noise in flyback converters,' IEEE Transactions on Electromagnetic Compatibility, 2017, **60**(5), pp. 1606–1609.

[5] Chen, H., Zhao, C., and Zheng, Z., 'Design of the number of transformer shielding winding turns for minimizing low-frequency common-mode noise in flyback converters,' IEEE Transactions on Electromagnetic Compatibility, 2019, **61**(6), pp. 1961–1966.

[6] Chen, H. and Xiao, J., 'Determination of transformer shielding foil structure for suppressing common-mode noise in flyback converters,' IEEE Transactions on Magnetics, 2016, **52**(12), pp. 1–9.

[7] Zhang, H., Wang, S., Li, Y., Wang, Q., and Fu, D., 'Two-capacitor transformer winding capacitance models for common-mode emi noise analysis in isolated dc–dc converters,' IEEE Transactions on Power Electronics, 2017, **32**(11), pp. 8458–8469.

[8] Li, Y., Zhang, H., Wang, S., Sheng, H., Chng, C. P., and Lakshmikanthan, S., 'Investigating switching transformers for common mode emi reduction to remove common mode emi filters and y-capacitors in flyback converters,' IEEE Journal of Emerging and Selected Topics in Power Electronics, 2018, **6**(4), pp. 2287–2301.

[9] Li, Y., Zhang, H., Wang, S., Sheng, H., Lakshmikanthan, S., and Chng, C. P., 'Techniques of the modeling, measurement and reduction of common mode noise for a multi-winding switching transformer,' in '2017 IEEE Applied Power Electronics Conference and Exposition (APEC),' IEEE, 2017 pp. 2511–2518.

[10] Wilton, D., Rao, S., Glisson, A., Schaubert, D., Al-Bundak, O., and Butler, C., 'Potential integrals for uniform and linear source distributions on polygonal and polyhedral domains,' IEEE Transactions on Antennas and Propagation, 1984, **32**(3), pp. 276–281.

[11] Commission, I. E. *et al.*, 'Specification for radio disturbance and immunity measuring apparatus and methods-part 1-2: Radio disturbance and immunity measuring apparatus-ancillary equipment-conducted disturbances,' CISPR16-1-2, 2006.

[12] Sun, M., Hu, J., He, J., Wu, C., Zhao, H., and Kim, H., 'Emi receiver model to evaluate conducted emissions from time-domain waveforms,' in '2020 IEEE International Conference on Computational Electromagnetics (ICCEM),' IEEE, 2020 pp. 166–168.

[13] Jha, M. M., Naik, K. B., and Das, S. P., 'Types of electro magnetic interferences in smps and using y-capacitor for mitigation of mixed mode noise,' in '2010 International Conference on Power, Control and Embedded Systems,' IEEE, 2010 pp. 1–6.

SECTION

2. SUMMARY AND CONCLUSIONS

In the first paper, a modeling strategy for film capacitors in EMI filters is proposed and validated. The proposed model is based on the anatomy of the film capacitor. The potential distribution along the film capacitor is reproduced by the proposed model. Meanwhile the computation efficiency is maintained. Compared to an ordinary block model or lumped model for capacitor, the proposed model can satisfy the need for both accurate impedance, and accurate mutual coupling with nearby components.

In the following paper, a modeling strategy for common mode choke is developed. The proposed procedure computes the permeability of the core material of the commo mode choke utilizing measurement results. The wire model of the common mode choke is simplified so that the computational efficiency is ensured. Together with the first paper, a modeling strategy for EMI filter is proposed. The proposed strategy delivers accurate self-impedance and mutual coupling among the components, and eventually an accurate performance of the EMI filter. The model is computationally effective and makes optimization and topology tuning feasible.

In the third paper, the relationship between the interwinding capacitance of a transformer and the conducted emission performance is studied. Simulation tools are developed to analyze the cross-section of a certain winding configuration with affordable time cost. Measurement vehicles are developed to allow for fast evaluation of the transformers in large quantity. The massive measurement results reveal a relationship between the conducted emissions and interwinding capacitance. The observed relationship doesn't match earlier literatures. Therefore, an update was proposed to the existing models. An analytical formula

is derived and validated. The work in the third paper reveals a fact that smaller interwinding capacitance doesn't necessarily lead to smaller conducted emissions. The tools developed in this work also are very helpful for the design of transformers.

REFERENCES

[1] Wang, S., van Wyk, J. D., and Lee, F. C., 'Effects of interactions between filter parasitics and power interconnects on emi filter performance,' IEEE Transactions on Industrial Electronics, 2007, **54**(6), pp. 3344–3352.

[2] Wang, S., Lee, F., and Odendaal, W., 'Controlling the parasitic parameters to improve emi filter performance,' in 'Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC'04.', volume 1, IEEE, 2004 pp. 503–509.

[3] Moonen, N., Buesink, F., and Leferink, F., 'Optimizing capacitor placement in emi-filter using back annotation of 3d field coupling parameters in circuit models,' in '2016 International Symposium on Electromagnetic Compatibility-EMC EUROPE,' IEEE, 2016 pp. 576–580.

[4] Stojanovic, M., Lafon, F., Perdriau, R., and Ramdani, M., 'Accurate analytical prediction of emi filter attenuation by considering intercomponent coupling phenomena,' IEEE Transactions on Electromagnetic Compatibility, 2018, **61**(4), pp. 1042–1051.

[5] Stojanovic, M., Lafon, F., Op't Land, S., Perdriau, R., and Ramdani, M., 'Determination of equivalent coupling surface of passive components using the tem cell,' IEEE Transactions on Electromagnetic Compatibility, 2017, **60**(2), pp. 298–309.

[6] Zhou, A., *Modèles de composants passifs et couplage électromagnétique pour filtres HF de puissance: optimisation du placement*, Ph.D. thesis, Université Claude Bernard-Lyon I, 2013.

[7] Paul, C. R., *Introduction to electromagnetic compatibility*, volume 184, John Wiley & Sons, 2006.

[8] Zhenyang, Y., Shishan, W., Zheng, S., and Lee, B.-L., 'The reviews of integrated emi filters applied in power electronic system,' in '2015 Asia-Pacific Symposium on Electromagnetic Compatibility (APEMC),' IEEE, 2015 pp. 227–230.

[9] Wang, S., Odendaal, W., and Lee, F., 'Extraction of parasitic parameters of emi filters using scattering parameters,' in 'Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting.', volume 4, IEEE, 2004 pp. 2672–2678.

[10] Wang, S., Lee, F., and Odendaal, W., 'Controlling the parasitic parameters to improve emi filter performance,' in 'Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC'04.', volume 1, IEEE, 2004 pp. 503–509.

[11] Moonen, N., Buesink, F., and Leferink, F., 'Optimizing capacitor placement in emi-filter using back annotation of 3d field coupling parameters in circuit models,' in '2016 International Symposium on Electromagnetic Compatibility-EMC EUROPE,' IEEE, 2016 pp. 576–580.

[12] Stojanovic, M., Lafon, F., Op't Land, S., Perdriau, R., and Ramdani, M., 'Determination of equivalent coupling surface of passive components using the tem cell,' IEEE Transactions on Electromagnetic Compatibility, 2017, **60**(2), pp. 298–309.

[13] Wang, S., Lee, F. C., and van Wyk, J. D., 'A study of integration of parasitic cancellation techniques for emi filter design with discrete components,' IEEE transactions on Power Electronics, 2008, **23**(6), pp. 3094–3102.

[14] Yoneda, S., Hirose, K., Kobayashi, A., Sasaki, Y., and Miyazaki, C., 'A study for designing an esl-cancelling circuit for shunt capacitor filters based on the biot-savart law,' in '2017 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI),' IEEE, 2017 pp. 17–21.

[15] Kovačević, I. F., Friedli, T., Müsing, A. M., and Kolar, J. W., '3-d electromagnetic modeling of parasitics and mutual coupling in emi filters,' IEEE Transactions on Power Electronics, 2013, **29**(1), pp. 135–149.

[16] Kovačević, I. F., Friedli, T., Muesing, A. M., and Kolar, J. W., '3-d electromagnetic modeling of emi input filters,' IEEE Transactions on Industrial Electronics, 2013, **61**(1), pp. 231–242.

[17] Kovačević, I. F., Friedli, T., Muesing, A. M., and Kolar, J. W., 'Electromagnetic modeling of emi input filters,' in '2012 7th International Conference on Integrated Power Electronics Systems (CIPS),' CIPS, 2012 pp. 1–9.

[18] Moonen, N., Vogt-Ardatjew, R., Roc'h, A., and Leferink, F., '3-d full-wave high frequency common mode choke modeling,' IEEE transactions on electromagnetic compatibility, 2019, **62**(3), pp. 707–714.

[19] Asmanis, A., Stepins, D., Dzenis, A., and Asmanis, G., '3d modeling of surface-mount capacitors and mutual couplings between them,' in '2017 International Symposium on Electromagnetic Compatibility-EMC EUROPE,' IEEE, 2017 pp. 1–6.

[20] Asmanis, A., Stepins, D., Asmanis, G., and Ribickis, L., '3d modelling and analysis of parasitic couplings between surface-mount components of emi filters,' in '2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC),' IEEE, 2018 pp. 496–501.

[21] He, R., Walunj, S. A., Yong, S., Khilkevich, V., Pommerenke, D., Aichele, H., Boettcher, M., Hillenbrand, P., and Klaedtke, A., 'Modelling strategy for film capacitors in emi filters,' in '2019 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+ SIPI),' IEEE, 2019 pp. 259–265.

[22] Vuillermet, Y., Chadebec, O., Lupin, J., Saker, A., Meunier, G., and Coulomb, J.-L., 'Optimization of low-voltage metallized film capacitor geometry,' IEEE transactions on magnetics, 2007, **43**(4), pp. 1569–1572.

[23] Dubickas, V. and Edin, H., 'High-frequency model of the rogowski coil with a small number of turns,' IEEE Transactions on Instrumentation and Measurement, 2007, **56**(6), pp. 2284–2288.

[24] Sullivan, C. and Kern, A., 'Capacitors with fast switching require distributed models,' CR Sullivan, AM Kern, 2001, pp. 1497–1503.

[25] Elektronik, W., 'Wurth elektronik we-cmb nizn common mode power line choke 744842311 datasheet, [revision 002.007].' 2016, accessed on: Jan. 1, 2020.

[26] Kotny, J.-L., Margueron, X., and Idir, N., 'High-frequency model of the coupled inductors used in emi filters,' IEEE Transactions on Power Electronics, 2011, **27**(6), pp. 2805–2812.

[27] Cuellar, C., Tan, W., Margueron, X., Benabou, A., and Idir, N., 'Measurement method of the complex magnetic permeability of ferrites in high frequency,' in '2012 Ieee international instrumentation and measurement technology conference proceedings,' IEEE, 2012 pp. 63–68.

[28] Wang, S. and Lee, F. C., 'Analysis and applications of parasitic capacitance cancellation techniques for emi suppression,' IEEE Transactions on Industrial Electronics, 2009, **57**(9), pp. 3109–3117.

[29] Zhenyang, Y., Shishan, W., Zheng, S., and Lee, B.-L., 'The reviews of integrated emi filters applied in power electronic system,' in '2015 Asia-Pacific Symposium on Electromagnetic Compatibility (APEMC),' IEEE, 2015 pp. 227–230.

[30] Fu, K. and Chen, W., 'Evaluation method of flyback converter behaviors on common-mode noise,' IEEE Access, 2019, **7**, pp. 28019–28030.

[31] Fu, K. and Chen, W., 'Balance winding scheme to reduce common-mode noise in flyback transformers,' Journal of Power Electronics, 2019, **19**(1), pp. 296–306.

[32] Chen, H., Zheng, Z., and Xiao, J., 'Determining the number of transformer shielding winding turns for suppressing common-mode noise in flyback converters,' IEEE Transactions on Electromagnetic Compatibility, 2017, **60**(5), pp. 1606–1609.

[33] Chen, H., Zhao, C., and Zheng, Z., 'Design of the number of transformer shielding winding turns for minimizing low-frequency common-mode noise in flyback converters,' IEEE Transactions on Electromagnetic Compatibility, 2019, **61**(6), pp. 1961–1966.

[34] Chen, H. and Xiao, J., 'Determination of transformer shielding foil structure for suppressing common-mode noise in flyback converters,' IEEE Transactions on Magnetics, 2016, **52**(12), pp. 1–9.

[35] Zhang, H., Wang, S., Li, Y., Wang, Q., and Fu, D., 'Two-capacitor transformer winding capacitance models for common-mode emi noise analysis in isolated dc–dc converters,' IEEE Transactions on Power Electronics, 2017, **32**(11), pp. 8458–8469.

[36] Li, Y., Zhang, H., Wang, S., Sheng, H., Chng, C. P., and Lakshmikanthan, S., 'Investigating switching transformers for common mode emi reduction to remove common mode emi filters and y-capacitors in flyback converters,' IEEE Journal of Emerging and Selected Topics in Power Electronics, 2018, **6**(4), pp. 2287–2301.

[37] Li, Y., Zhang, H., Wang, S., Sheng, H., Lakshmikanthan, S., and Chng, C. P., 'Techniques of the modeling, measurement and reduction of common mode noise for a multi-winding switching transformer,' in '2017 IEEE Applied Power Electronics Conference and Exposition (APEC),' IEEE, 2017 pp. 2511–2518.

[38] Wilton, D., Rao, S., Glisson, A., Schaubert, D., Al-Bundak, O., and Butler, C., 'Potential integrals for uniform and linear source distributions on polygonal and polyhedral domains,' IEEE Transactions on Antennas and Propagation, 1984, **32**(3), pp. 276–281.

[39] Commission, I. E. *et al.*, 'Specification for radio disturbance and immunity measuring apparatus and methods-part 1-2: Radio disturbance and immunity measuring apparatus-ancillary equipment-conducted disturbances,' CISPR16-1-2, 2006.

[40] Sun, M., Hu, J., He, J., Wu, C., Zhao, H., and Kim, H., 'Emi receiver model to evaluate conducted emissions from time-domain waveforms,' in '2020 IEEE International Conference on Computational Electromagnetics (ICCEM),' IEEE, 2020 pp. 166–168.

[41] Jha, M. M., Naik, K. B., and Das, S. P., 'Types of electro magnetic interferences in smps and using y-capacitor for mitigation of mixed mode noise,' in '2010 International Conference on Power, Control and Embedded Systems,' IEEE, 2010 pp. 1–6.

VITA

Ruijie He was born in Chibi, Hubei, China. He received his bachelor of science Degree in Electrical Engineering from Huazhong University of Science and Technology, Wuhan, China in 2015. He then joined the EMC Laboratory in the Missouri University of Science and Technology, Rolla, MO, USA. He received his doctor of philosophy in Electrical Engineering from the Missouri University of Science and Technology in May 2022.

His research interests included the modeling of EMI problems in consumer electronics and their solutions such as EMI filter, shielding and absorbing materials.