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SEED MODELING OF AN ESD GUN DISCHARGE TO A USB CABLE

by

YANG XU

A THESIS

Presented to the Graduate Faculty of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE

in

ELECTRICAL ENGINEERING

2021

Approved by:

Dr. Daryl Beetner, Advisor
Dr. Victor Khilkevich
Dr. Donghyun Kim

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PUBLICATION THESIS OPTION

This thesis consists of the following two articles, formatted in the style used by the Missouri University of Science and Technology.

Paper I: Pages 3-21; SEED Modeling of an ESD Gun Discharge to a USB Cable Surrogate, has been published in 2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium.

Paper II: Pages 22-48; Transient Modeling of an ESD Gun Discharge Event Through a USB Cable, will be submitted to IEEE Transactions on Electromagnetic Compatibility.

ABSTRACT

An IC protected by a transient voltage suppression (TVS) diode may fail if the TVS device does not turn on or does not turn on quickly enough, causing the IC to take the full brunt of the electrostatic discharge (ESD) event. Transient simulation models have been developed for ESD protection devices for the purpose of system-efficient ESD design (SEED). The TVS modeling methodology has been improved to better represent the physics that occurs during the TVS response and more accurately predict the interactions between off-chip and on-chip protection devices. Moreover, a complicated test scenario – an ESD gun discharge through a USB cable - was investigated and simulated, to demonstrate the impact of position, grounding condition, and quality of the USB cable. Test and design guidelines are proposed for incorporating a USB cable in a contact-discharge ESD test.

At the beginning, a hybrid simulation approach was proposed, which uses a full-wave model of the ESD gun, cable, and enclosure combined with the ESD protection devices and test board's circuit-level models. The voltage and current of ESD protection devices are captured within 24-35% compared to the measurements, under various cable configurations.

To further improve the simulation accuracy, physics-based modeling methodologies were proposed to improve the previously developed TVS model, especially on the falling edge after the overshoot. The ESD protection device's response was studied in simulation and measurement for various cable configurations. And the overall discrepancy is within 30%. The modeling process can help engineers to evaluate the design effectiveness under various complicated test scenarios.

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1. INTRODUCTION

The USB interface is one of the most commonly-used high-speed interfaces on a wide range of electrical devices, with connectors easily accessible to users – more susceptible to ESD events. Besides, the increasing data rate brings more concern, 480 Mbit/s for USB 2.0 and 5 Gbit/s for USB 3.0 interface, which is of high requirement of the signal integrity, leading to more challenges on the robust ESD protection design. The high-speed requires on-chip ESD protection of pF range low-capacitance; however, the low-capacitance structure will bring high voltage overshoots during ESD strikes, and even cause a hardware failure. Usually, transient voltage suppression (TVS) diodes are added to a circuit to improve the system's immunity to ESD, with a limited acceptable impact on the signal integrity. TVS devices can shunt most of the ESD current away from sensitive ICs during a transient over-voltage event. Ensuring the TVS diode turns on during an ESD event, and the on-chip protection device does not take the entire charge can be challenging, however, as many on-chip ESD protection structures will turn on faster at lower voltages than the off-chip TVS.

System Efficient ESD Design (SEED) is an approach to modeling the response of a system to an ESD event. SEED has previously been used to predict the interaction between the TVS and on-chip ESD protection during a transmission-line pulse (TLP) event [1]. Methods are developed in the following work to predict the system's response to a more complicated scenario – when an ESD gun discharges to the pin of a USB cable connected to a test board that contains an IC protected by a TVS diode. Moreover, the impact of position, grounding condition, and quality of the USB cable was investigated and simulated. Two methods were proposed to capture the impact of a specific cable configuration: (1) the S-parameter extracted from the full-wave simulation was applied, (2) the measurement-based current source was used to account for the different cable configurations. Transient simulation models for the TVS and on-chip protection devices were developed in the

beginning. In addition, the TVS modeling methodology was improved to represent better the physics that occurs during the TVS response and more accurately predict the interactions between off-chip and on-chip protection devices. Finally, test and design guidelines are proposed for incorporating a USB cable in a contact-discharge ESD test.

PAPER

I. SEED MODELING OF AN ESD GUN DISCHARGE TO A USB CABLE SURROGATE

Yang Xu
Department of Electrical and Computer Engineering
Missouri University of Science and Technology
Rolla, Missouri 65409–0050
Tel: 573–341–6622, Fax: 573–341–4115
Email: xuy1@mst.edu

ABSTRACT

An IC protected by a transient voltage suppression (TVS) diode may fail if the TVS device does not turn on or does not turn on quickly enough, causing the IC to take the full brunt of the ESD event. System Efficient ESD Design (SEED) simulation can help predict when the TVS will turn on and the level of ESD stress seen by the IC. In the following work, models are developed to predict the voltage and current through a TVS and on-chip protection diodes connected to a USB cable when an ESD gun discharges to a pin at the end of the cable. A hybrid simulation methodology is proposed, which uses a full-wave model of the ESD gun, cable, and enclosure combined with the ESD protection devices and test board's circuit-level models. The response of the ESD protection is studied in simulation and measurement for a variety of cable configurations. Simulations of the voltage and current waveforms match measurements 24-35%. The total charge delivered to the on-chip diode as a function of ESD gun voltage was predicted within 21%.

Keywords: Electrostatic discharge (ESD), system-efficient ESD design (SEED), USB, cable discharge, electromagnetic compatibility (EMC).

1. INTRODUCTION

Protection devices like transient voltage suppression (TVS) diodes are often added to a circuit to improve its immunity to electrostatic discharge (ESD). TVS devices are used for shunting the majority of the ESD current away from sensitive ICs during a transient over-voltage event. Ensuring the TVS diode turns on during an ESD event, and the on-chip protection device does not take the entire charge can be challenging, however, as many on-chip ESD protection structures will turn on faster and at lower voltages than the off-chip TVS. System Efficient ESD Design (SEED) is an approach to modeling the response of a system to an ESD event. SEED has previously been used to predict the interaction between the TVS and on-chip ESD protection during a transmission-line pulse (TLP) event [1]. Methods were developed to predict the system's response to a more complicated scenario – when an ESD gun discharges to the pin of a USB cable connected to a test board that contains an IC protected by a TVS diode.

A number of SEED models have previously been developed to assist with this problem. The static VI curve of a TVS is modeled in [2]. The transient turn-on behavior is modeled in [3], [4] to account for the importance of the TVS turn-on time in system-level ESD simulations. The TVS simulation framework is further improved in [5] and applied in SEED simulation to investigate the interaction between a TVS and on-chip protection devices in [1] during a TLP event. A number of models for ESD guns have also been developed [6, 7, 8], as summarized in [9]. However, system-level simulation of a system's response to an ESD event is still challenging, considering the many interactions between ESD and protection circuits and variations in the ESD pulse that occur due to interactions between the ESD gun and the surrounding environment – particularly when the injection occurs at the end of a cable and not into a typical "ground plane" structure.

Though several publications provide an analysis of ESD immunity with protection devices, less information is available on the impact of a cable on an ESD gun discharge event. It was noticed that the circuit simulation approach fails when the cable has an

electrical long distance from the reference plane if discharging with an ESD generator [6]. The work in [10] shows the importance of modeling the USB cable, as the ESD stress differs significantly with the type and length of the USB cable.

Simulation models are developed in the following work to predict the ESD stress on an I/O line when an ESD gun is discharged to one pin of a USB cable. The resulting model is used with models of an on-chip ESD diode and an external TVS device to predict the resulting current and voltage seen by the IC. Measurements used to characterize the ESD event seen when discharging with an ESD gun to a cable and characterize the resulting reaction of on-chip and off-chip ESD protection is given in Section 2. Simulation models of the overall system (ESD gun, cable, board, TVS, and on-chip diode) are developed in Section 3, followed by conclusions. Results demonstrate the overall model can do a good job of predicting the charge delivered to the on-chip diode during an ESD discharge to the cable, suggesting these models will be a useful tool for engineers trying to evaluate the effectiveness of their ESD protection strategy early in the design process.

2. EXPERIMENTAL MEASUREMENTS

The setup used to characterize the ESD gun and the response of the TVS and on-chip diode is shown in Figure 1. An ESD gun was discharged to a single pin of a 1.2 m long USB cable whose shield was connected to an enclosure. Inside the enclosure, the wire carrying the ESD event was either connected to a 50 Ω load or was connected to a test board containing a TVS and a pair of on-chip diodes. The board also included probes or probe points for measuring voltages and currents within the circuit.

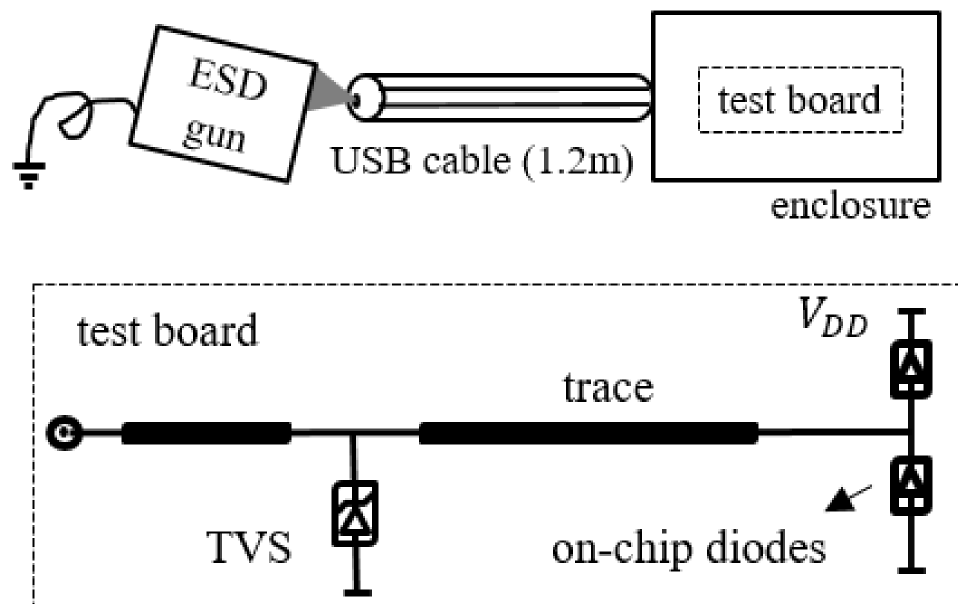


Figure 1. Set up for characterizing ESD event and the response of the TVS and on-chip diodes.

2.1. CABLE CONFIGURATIONS

The test board and other measurement hardware were put inside a shielded enclosure to avoid coupling between the ESD gun and the measurement instruments. One end of the cable shield was always connected to this enclosure. The other end, at the ESD gun injection point, may or may not be connected to the enclosure, depending on the cable configuration. The cable configuration was found to have a significant impact on the ESD waveform.

Four cable configurations were studied, as shown in Figure 2. In all cases, the USB cable's internal wires were well shielded along the entire length of the cable. In Case 1 (Figure 2a), the ESD gun was discharged directly into the test board with no cable in between. This case serves as a reference for the other tests. In Case 2, the cable was run along with the enclosure, and the cable shield was connected to the enclosure at both ends. In Case 3, the cable was run in the same way as in Case 2, but the cable shield was only connected to the enclosure at the location of the test board. Case 2 and Case 3 help demonstrate how common mode currents flowing on the cable shield's outer surface

influence the ESD waveform. In Case 4, the cable was run straight out from the enclosure, normal to the enclosure wall, and parallel to the “ground” plane. Here the cable shield could only be connected to the enclosure at one location, where the cable connected to the test board.

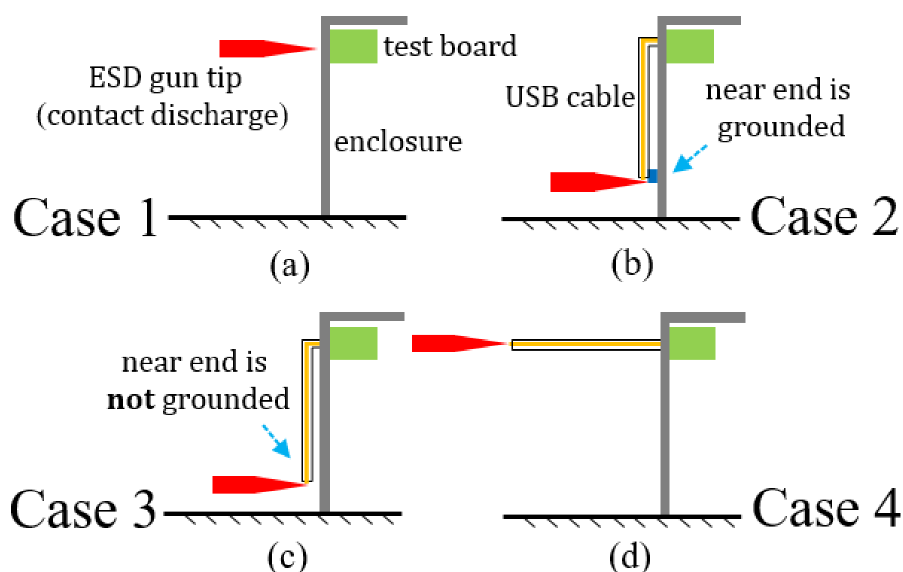


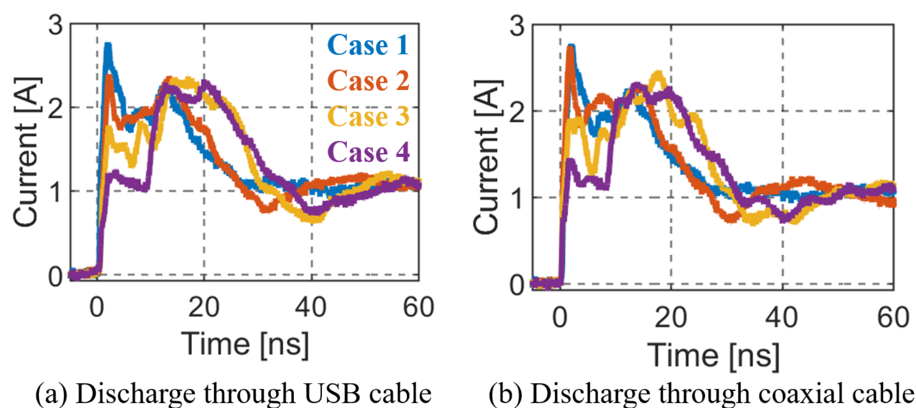
Figure 2. Cable configuration: Case 1(no cable), Case 2(cable both ends shielded), Case 3(near end not shielded), and Case 4(cable straight out).

2.2. DISCHARGE TO A 50 Ω LOAD

The first experiments were done with the USB cable connected to a 50 Ω load inside the enclosure rather than the test board and the ESD protection devices. This test helps demonstrate the impact of the cable configuration and will later be used to validate the setup models. Tests were performed using a 1 kV contact mode ESD injection to the D+ pin of the USB cable and when using a standard coaxial cable.

Figure 3 shows the measured results when discharging to a 50 Ω load. Figure 3a shows results when using a USB cable, and Figure 3b when using a coaxial cable. The measured waveforms for Case 1 and Case 2 are similar since the load, and the interaction

between the ESD gun and enclosure are similar at the injection site. In Case 3 and Case 4, where the shield is only connected to the enclosure at the test board, there is a considerable delay between the start of the ESD event and when the ESD event peaks. In a rough (but not entirely accurate) way, one can think of the first part of the pulse as resulting from an interaction between the gun and the cable shield, followed shortly after by the added contribution of the interaction between the gun and the enclosure, delayed by twice the length of the "transmission line" created between the cable shield and the enclosure or ground plane. The initial peak is much lower for Case 3 and 4 than for Case 1 and 2 because the impedance between the ESD gun and the cable shield is much higher than between the ESD gun and the enclosure. The interaction is more complicated than indicated here, for example, because more than just TEM modes are present between the shield and ground plane in Case 4. Still, simulations suggest this explanation is reasonably close to reality.



(a) Discharge through USB cable (b) Discharge through coaxial cable

Figure 3. Measurement results when discharging to a 50 Ω load.

Discharging to a coaxial cable yielded similar waveforms as when discharging to a USB cable. This result is not surprising since a TDR test of the USB cable shows the impedance between D+ and the cable ground wire is very close to 50 Ω. Considering the

close match between results when using the two cables, the ease of using a coaxial cable, and the typical variations between ESD gun tests, the coaxial cable can be used to simplify the simulation model.

2.3. DISCHARGE TO ESD PROTECTION DEVICES

The subsequent tests were performed when discharging to a test board containing ESD protection circuitry. The test setup is shown in Figure 4. Tests were performed using a USB cable laid out as shown in Figure 2.

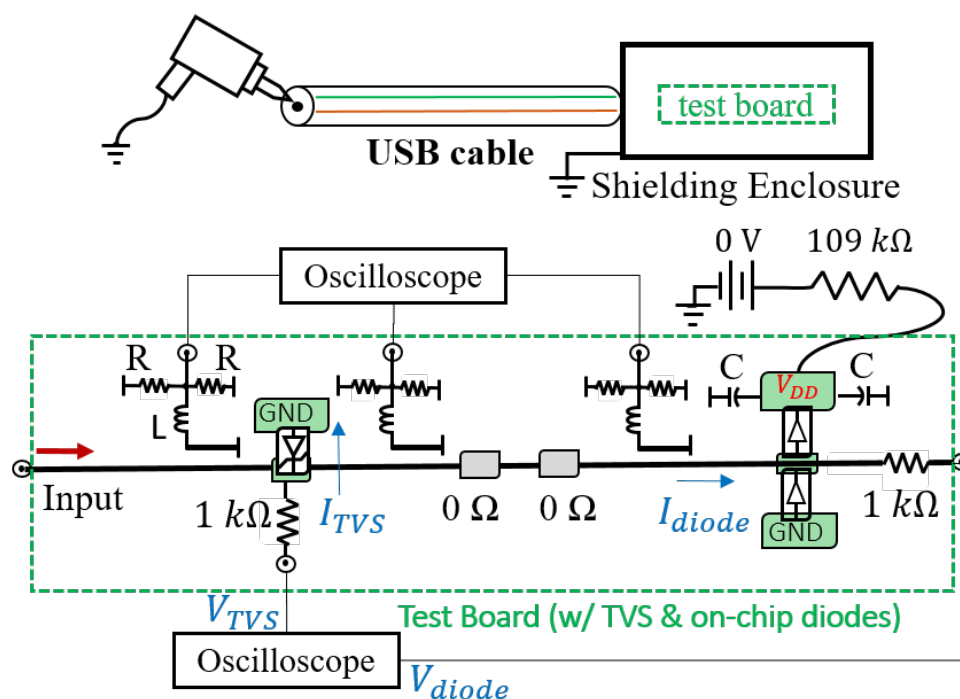


Figure 4. Discharge to a test board connected to a 1.2 m long cable.

The test board includes a TVS device, a pair of “on-chip” diodes, and probes for measuring the current and voltage associated with each device, as shown in Figure 4. The DC bias (Vdd, Figure 1) was set to 0 V. A 1 kΩ resistor connected to the location of the TVS, and the on-chip diode serves as a 21:1 voltage probe of each device. The current was monitored using an FCC F65 current probe at the ESD generator’s front tip and using three

on-board current probes built from shorted traces located very close to the trace carrying the ESD current [1]. A current probe was placed just before and after the TVS, so the TVS current could be determined from the difference in currents measured by the two probes. Another current probe was placed just before the on-chip diode to capture the current to the on-chip diode. Current waveforms were reconstructed by performing a full S-parameter calibration of each probe and using the frequency domain compensation technique given in [11].

The total current injected into the test board, Itotal, is shown in Figure 5 for Case 2 (cable shield grounded at both ends) and Case 4 (cable straight out). As when discharging to 50 Ω, the initial peak disappears when one end of the cable is not connected to the enclosure. This result is further confirmation that the ESD stress seen on-PCB will differ significantly when the board is connected to a cable compared to the case when it is not. This phenomenon and other configuration measurement results will be addressed further in Section 3.

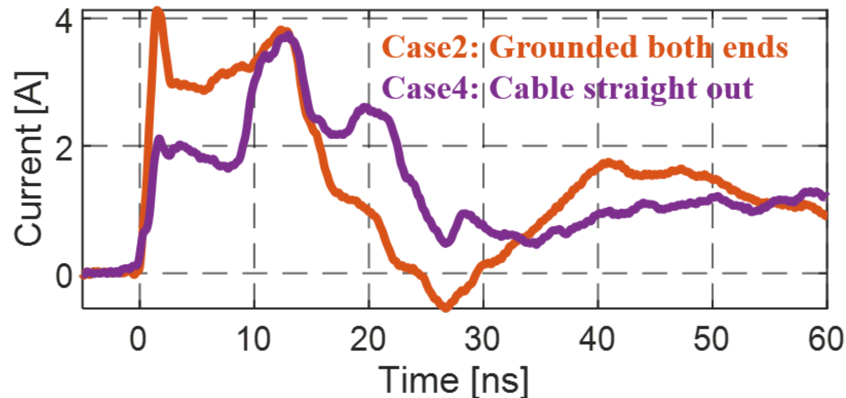


Figure 5. Total current injected into the test board.

3. SIMULATION

The complicated interactions between the ESD gun, cable, and enclosure make it challenging to represent the ESD gun using a simple model. Traditional circuit models will not accurately capture this interaction and will give incorrect results [6]. To better capture the impact of the cable, a hybrid simulation approach was used. The first step of this simulation strategy was to find an S-parameter block capturing the impedance between the ESD gun source and the input to the test board when accounting for the ESD gun, cable, and enclosure. The second step was to use this S-parameter block along with models of TVS and on-chip diode to capture the board's response to this cable-guided ESD event.

3.1. FULL-WAVE SIMULATION OF ESD GENERATOR AND COAXIAL CABLE

The full-wave simulation model of the ESD gun, cable, and enclosure is shown in Figure 6a. This model was built using CST Microwave Studio. A coaxial cable was used to represent the USB cable to simplify the model since the measurement results are similar (see Figure 3). The ESD gun model is based on the model in [6], as shown in Figure 6a. Metal blocks were used to represent large conductive portions of the ESD gun, and lossy material to represent lossy portions of the discharge path. Lumped elements were also included to tune the ESD gun response better. The gun, cable, and enclosure model can be used to find the ESD input pulse to the board as shown in Figure 6b by measuring the S-parameter response of the 3D model and using a step-function approximation of the ESD gun input [6]. The ESD gun model was tuned by calibrating its output to measurement data when discharging to the ground directly.

Figure 7 shows the simulated and measured waveforms when the cable is terminated with a 50 Ω load, for each of the cable configurations shown in Figure 2. While the majority of the waveform is captured well in each case, there is some discrepancy in results within the first 20 ns for Cases 1 and 2, after the first peak. This discrepancy is not entirely unexpected

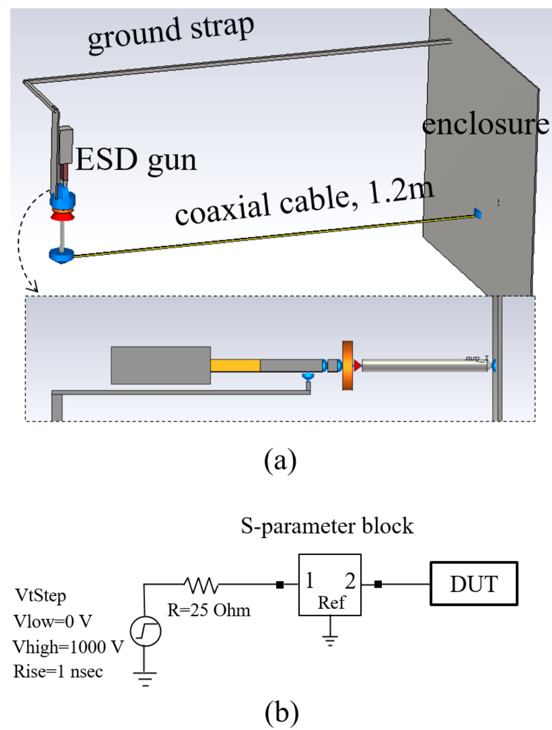


Figure 6. Hybrid simulation approach.

given the simplicity of the ESD gun model, and is not so significant as to warrant the development of a much more sophisticated model. The simulation captures the initial peak in the waveform for all cases within 18%. The delay and magnitude of the peak when the cable is grounded only at the test board location (Case 3 and 4) are captured accurately. Further simulations demonstrate that this delay is proportional to the cable length. The magnitude of the peak in Case 4 is captured within 20% and is even better for Case 3.

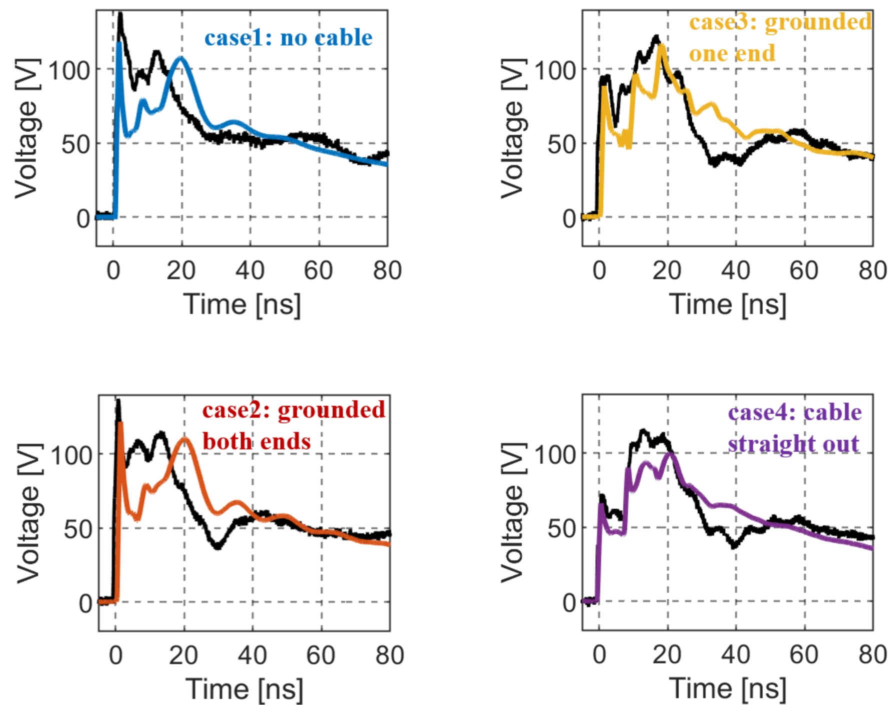


Figure 7. Simulated and measured waveforms when injecting into a 50 Ω load.

3.2. SEED MODELS OF BOARD AND ESD PROTECTION DEVICES

A high-level model of the test board is shown in Figure 8. The TVS and on-chip diode were modeled using a behavioral model like that shown in [1]. Each device was modeled to capture its small-signal input parameters (e.g., inductance, resistance, capacitance), its IV characteristics (turn-on voltage, snapback, on-resistance, etc.), and transient behavior (conductivity modulation, turn-on delay, etc.). Characterization was done by measuring the device response using a TLP, and then tuning the model to achieve a good match between the simulated and measured current and voltage waveforms in terms of their peak and steady-state values. Some modifications were made to the conductivity modulation model in [5] to ensure a smooth turn-on during a fast rise-time event. Similar modifications were made to the snapback delay model.

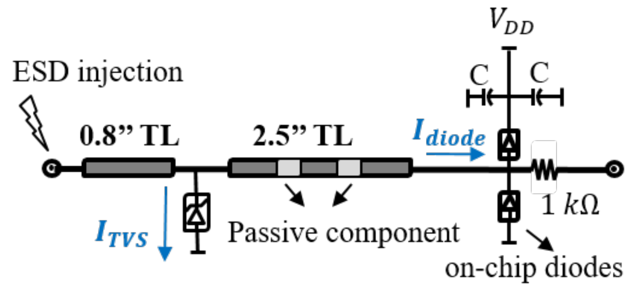


Figure 8. Circuit diagram of the test board.

Measured and simulated voltage and current waveforms for the on-chip diode and TVS are shown in Figure 9 and Figure 10 as examples to demonstrate the model's performance. The on-chip diode was tested with TLP voltages of 20, 32, and 50 V and with rise-times of 0.4, 2, and 5 ns. The TVS was tested with TLP voltages of 20, 27, and 92 V and with rise-times of 0.4, 2, and 5 ns. The waveforms match within about 10% for each tested stimulation. Models were developed using a TLP injection rather than an ESD injection, given the lower complexity and better repeatability of the TLP.

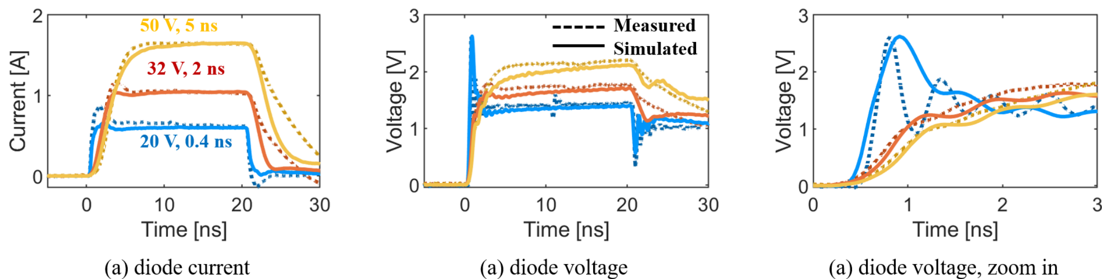
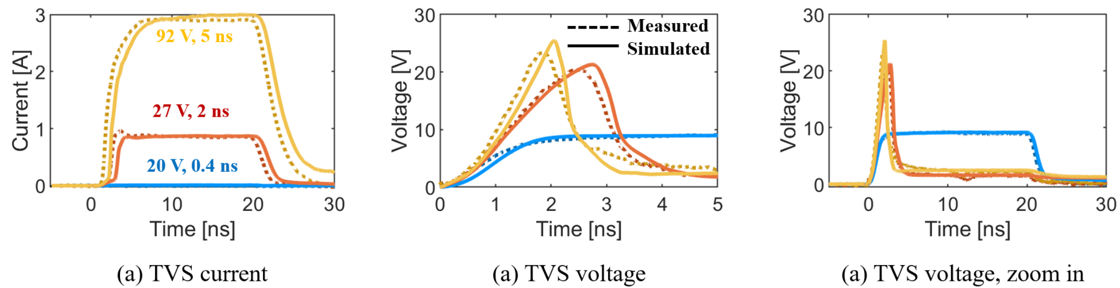


Figure 9. Simulated (dashed line) and measured current and voltage waveforms for the on-chip diode during a TLP injection.

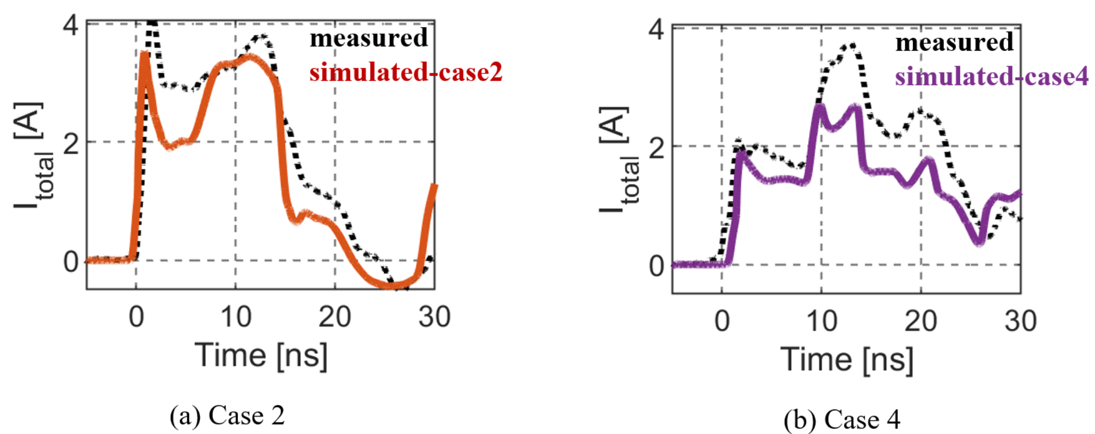


(a) TVS current (a) TVS voltage (a) TVS voltage, zoom in

Figure 10. Simulated (dashed line) and measured current and voltage waveforms for the TVS during a TLP injection.

3.3. SYSTEM-LEVEL SIMULATION

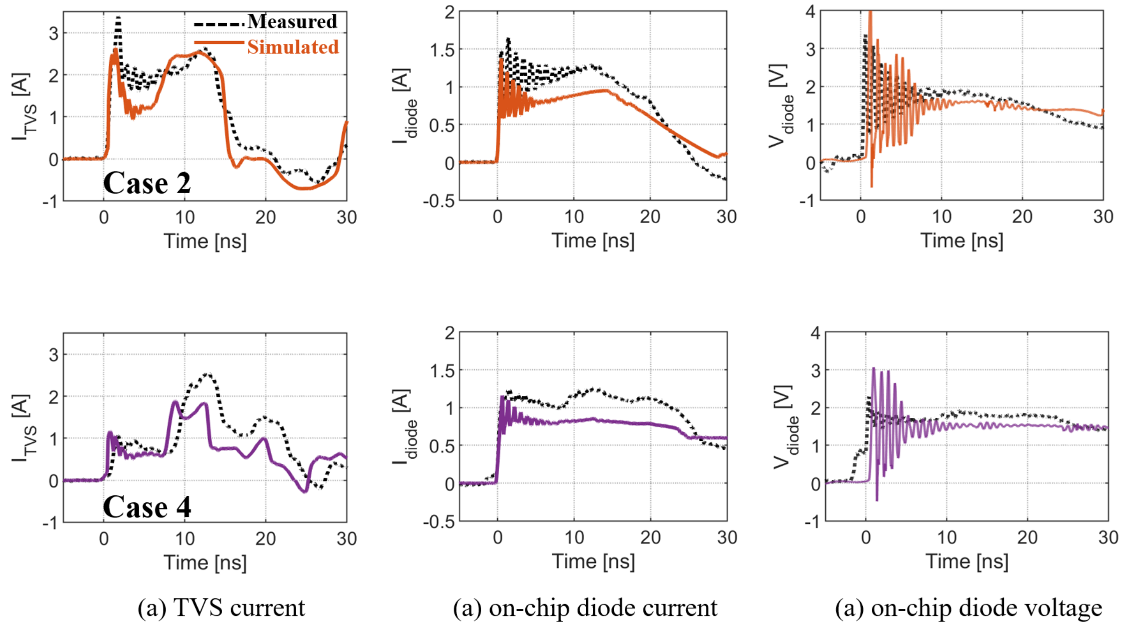
The response of the system to an ESD discharge to a USB cable was simulated using a coaxial cable as a USB cable surrogate shown in Figure 6b. The source and S-parameter block represent the ESD gun, cable, and enclosure, and the DUT is described by the circuit models of the board, TVS, and on-chip diode. Figure 11 shows a comparison of the total current entering the test board as found in measurement and simulation for Case 2 (cable shield grounded on both ends) and for Case 4 (cable straight out). The predicted current matches the measurement within 35% and captures the waveform's major features well.



(a) Case 2 (b) Case 4

Figure 11. The total current injected into the test board.

Case 2 and Case 4 were selected for detailed discussion since Case 1 generates results similar to Case 2, and Case 3 generates results similar to Case 4 (see Figure 3). The voltages at, and currents through, the TVS and on-chip diode are shown in Figure 12 for Case 2 and Case 4 (both sides of cable grounded and cable straight out, respectively). The TVS current was determined by the difference between currents measured by the left and central current probes, as depicted in Figure 4. The ringing in the waveforms is caused by the reflections between the diode and TVS after they turn on, at which point they essentially create shorts at both ends of the transmission line between them. The ringing frequency is 1 GHz as predicted by the transmission line's electrical length, as is seen in both measurement and simulation. Peak values of currents and voltages predicted by the simulation are captured within 24% of those found through measurements, while the steady-state is captured within 30%. The steady-state diode current is modestly underestimated, in part because the ESD gun model under-predicts current by about 18% within the first 20 ns, as shown in Figure 7d.



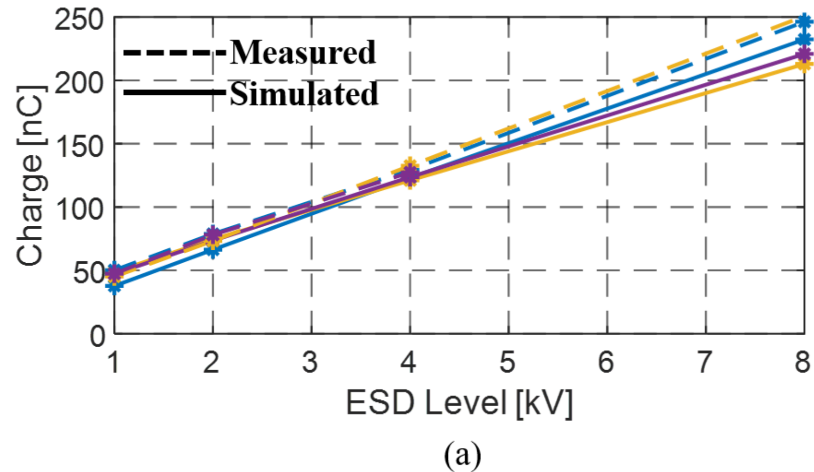
(a) TVS current (a) on-chip diode current (a) on-chip diode voltage

Figure 12. Current and voltage waveforms for the TVS and on-chip diode.

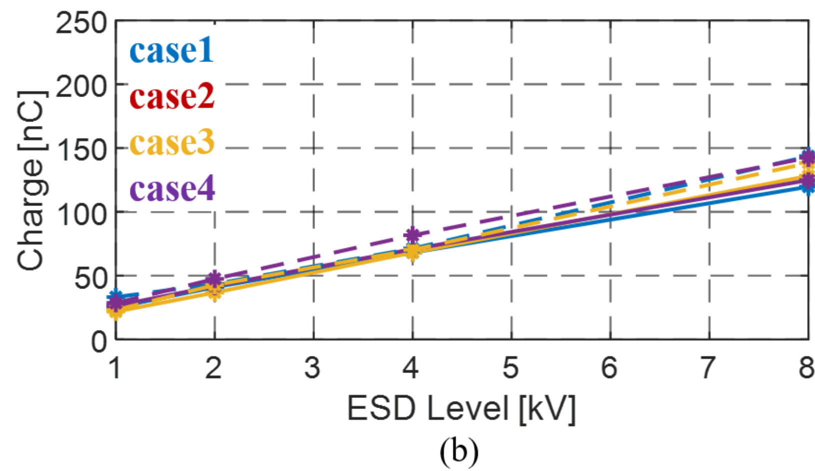
To further capture the performance of the model, the total charge that passes through the on-chip diode was found as a function of the ESD gun voltage under two conditions. The first was when the TVS and on-chip diode were set up, as shown in Figure 8. In the second, an additional 10 nH inductor and a 1 Ω resistor are added between the TVS and on-chip diode to simulate added parasitic inductance or resistance that may be present in an actual application. Results are shown in Figure 13 for ESD gun voltage from 1-8 kV and for cases 1, 2, 3, and 4. The total charge is calculated within the first 40 ns starting from the rising edge. Simulation and measurements match within 21%. The total charge delivered to the diode does not change much between cable configurations, though the presence of parasitics between the TVS and on-chip diode substantially reduces the total charge seen by the diode. In the condition of the added 10 nH inductor and 1 Ω resistor, the total charge was reduced by 48%. If there is additional impedance in series with the on-chip ESD protection, the current division between on-chip protection and TVS will change, and less current will flow through the on-chip protection.

4. DISCUSSION AND CONCLUSIONS

Methods were developed to predict the response of a TVS device and on-chip diode connected to a USB cable, when an ESD gun was discharged to one of the USB cable pins. The simulation approach used a hybrid technique where the interactions between the ESD gun, cable, and enclosure were captured with a 3D full-wave model, and the response of the TVS and on-chip diode were captured with a SPICE model. The simulation model was able to predict the steady-state current and voltage within 30% and capture the peak current and voltage within 24%. The total charge through the diode during a cable-guided ESD event was predicted within 21% for 1-8 kV contact injection level. The simplicity of the ESD gun model was one cause for errors in results, though improving the gun model will take substantial effort and may not be warranted given the likely improvement in results. Errors in the overall current and voltage waveforms may have also been caused by small



(a)



(b)

Figure 13. Total charge seen by the on-chip diode without (a) or with (b) passive components in between.

errors in the diode or TVS device's turn-on time, which can significantly change the overall waveform. It was found particularly difficult to predict the diode voltage across system configurations accurately.

The characteristics of the ESD waveform change substantially depending on the cable configuration. When the cable shield is only connected to the enclosure at the point where the enclosure connects to the test board, there is a substantial delay between the

beginning of the pulse and the first peak, and the waveform loses the sharp, high-magnitude initial peak that is associated with a human metal model event. A qualitative description can be given for the first peak. The first peak is likely determined by the impedance of the gun, in series with the (instantaneous) 50 Ω impedance looking into the cable, in parallel with a capacitance between the gun, ground, and the cable shield. The delay in the prominent peak is associated with the delay in electromagnetic energy traveling between the gun to the enclosure and back to the input of the coaxial cable. At lower frequencies, transmission line theory provides a qualitative explanation; however, the complexity of this 3D structure is too high to explain further details by an equivalent circuit containing transmission lines when the cable is straight out from the enclosure. Regardless, capturing the interaction between the gun, cable, and enclosure is critical to properly model the waveform generated by a discharge to a cable.

As suggested by the complexity of the interaction between the ESD gun, cable, and enclosure, and by the changes in the ESD gun current for each case, traditional methods of modeling the ESD gun as a simple current source will not be effective unless measurements are made using the correct system configuration. Even in those cases, care should be taken to properly represent the ESD gun's source impedance, which could substantially impact reflections from the board to the ESD gun and back.

Overall, the methods shown here were able to accurately predict the voltage and current waveforms seen at the TVS and on-chip diode resulting from an ESD discharge at the end of a USB cable surrogate. These methods will help ESD engineers evaluate and optimize their ESD protection strategies' effectiveness in this and other similar situations.

ACKNOWLEDGEMENTS

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II. TRANSIENT MODELING OF AN ESD GUN DISCHARGE EVENT THROUGH A USB CABLE

Yang Xu
Department of Electrical and Computer Engineering
Missouri University of Science and Technology
Rolla, Missouri 65409–0050
Tel: 573–341–6622, Fax: 573–341–4115
Email: xuy1@mst.edu

ABSTRACT

An IC protected by a transient voltage suppression (TVS) diode may fail if the TVS device does not turn on or does not turn on quickly enough, causing the IC to take the full brunt of the ESD event. The USB IC is more susceptible to ESD events and demands a more robust protection design due to the high-speed interface and regularity of connecting and disconnecting operations by users. System-efficient ESD Design (SEED) simulation can help predict when the TVS will turn on and the level of ESD stress seen by the IC. Previously reported TVS model was improved with physics-based conductivity modulation, based on which models are developed to predict the voltage and current through a TVS and on-chip protection diodes connected to a USB cable when an ESD gun discharges to a cable pin. The ESD protection device's response is studied in simulation and measurement for various cable configurations, and the overall discrepancy is within 30%. The modeling process outlined here can help engineers to evaluate the design effectiveness under various complicated test scenarios.

Keywords: Electrostatic discharge (ESD), system-efficient ESD design (SEED), System-level ESD, USB cable, transient voltage suppressor.

1. INTRODUCTION

Protection devices like transient voltage suppression (TVS) diodes are often added to a circuit to improve its immunity to electrostatic discharge (ESD). TVS devices are used to shunt most of the ESD current away from sensitive ICs during a transient over-voltage event. Ensuring the TVS diode turns on during an ESD event, and the on-chip protection device does not take the entire charge can be challenging, however, as many on-chip ESD protection structures will turn on faster at lower voltages than the off-chip TVS. System Efficient ESD Design (SEED) is an approach to modeling the response of a system to an ESD event. SEED has previously been used to predict the interaction between the TVS and on-chip ESD protection during a transmission-line pulse (TLP) event [1]. Methods are developed in the following work to predict the system's response to a more complicated scenario – when an ESD gun discharges to the pin of a USB cable connected to a test board that contains an IC protected by a TVS diode

The USB cable was selected since the USB interface is one of the most commonly-used high-speed interfaces on a wide range of electrical devices, with connectors that are easily accessible to users – more susceptible to ESD events. Besides, the increasing data rate brings more concern, 480 Mbit/s for USB 2.0 and 5 Gbit/s for USB 3.0 interface, which is of high requirement of the signal integrity, leading to more challenges on the robust ESD protection design. The high-speed requires on-chip ESD protection of pF range low-capacitance, however, the low-capacitance structure will bring high voltage overshoots during ESD strikes, and even cause a hardware failure, as reported in [2]. Usually, advanced external ESD protection of low clamping voltage, low dynamic resistance, and low capacitance are demanded. Moreover, a careful system-level ESD design is needed, with a good understanding of the characteristics and limitations of ESD protection devices, together with the PCB parasitics [3]. Accordingly, a thorough simulation in the early design stage is essential.

A number of SEED models have previously been developed. The static I-V curve of a TVS is modeled in [4]. The transient turn-on behavior is modeled in [5], [6] to account for the importance of the TVS turn-on time in system-level ESD simulations. The TVS simulation framework is further improved in [7] and applied in SEED simulation to investigate the interaction between a TVS and on-chip protection devices [1] during a TLP event. A number of models for ESD guns have also been developed, for either circuit-based or full-wave simulation based, as summarized in [8]. However, system-level simulation of a system's response to an ESD event is still challenging, considering the many interactions between ESD and protection circuits and variations in the ESD pulse that occur due to interactions between the ESD gun and the surrounding environment – particularly when the injection occurs at the end of a cable and not into a typical "ground plane" structure.

Though several publications provide an analysis of ESD immunity with protection devices, less information is available on the impact of a cable on an ESD gun discharge event. It was noticed that the circuit simulation approach fails when the cable has an electrical long distance from the reference plane if discharging with an ESD generator [9]. The work in [10] shows the importance of modeling the USB cable, as the ESD stress differs significantly with the type and length of the USB cable. The cable discharge events with a USB cable were studied in [11], while only the impact to the whole system was discussed, without investigating the interaction between the off-chip and on-chip protection devices.

Simulation models were developed to predict the ESD stress on an I/O line when an ESD gun is discharged to one pin of a USB cable. The TVS and on-chip diode transient models are developed in Section 2 and validated against TLP measurements. Section 3 describes the measurements characterizing the transient repose of the ESD protection devices under different USB cable configurations. In Section 4, a simulation model taking considering the whole system (the ESD gun, USB cable, test board, TVS, and on-chip diode) is presented, together with the discussion on the impact of cable configurations. Results

demonstrate the overall model's effectiveness, suggesting the modeling methodology is helpful for engineers trying to evaluate the effectiveness of their ESD protection strategy early in the design process.

2. TRANSIENT MODELING OF ESD PROTECTION DEVICES

The diagram in Figure 1 shows the test scenario to be investigated. A general system-level ESD protection strategy was implemented on a test board, including the off-chip (TVS) and on-chip ESD protection devices. The dual-diodes structure represents the simplified ESD protection structure of the I/O on an IC.

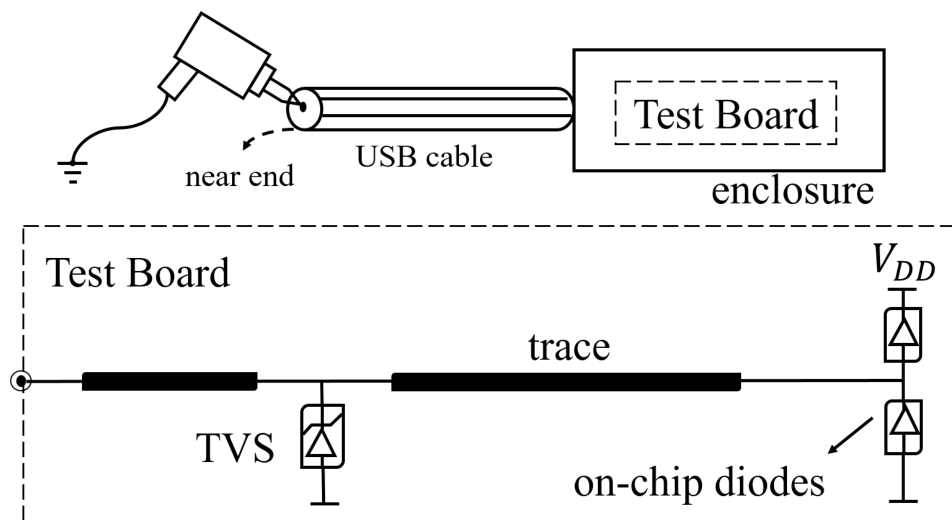

Figure 1. Set up for characterizing ESD event with a USB cable.

The TVS was modeled using a behavioral model like that shown in [7]. As depicted in Figure 2, the TVS was modeled to capture its small-signal input parameters (e.g., inductance, resistance, capacitance), its IV characteristics (turn-on voltage, snapback, on-resistance, etc.), and the transient behavior (conductivity modulation, turn-on delay, etc.). Notice that the negative path is simplified with an ideal diode in series with a resistor, considering the device is a unidirectional TVS. Characterization was done by measuring

the device response using a TLP and then tuning the model to achieve a good match between the simulated and measured current and voltage waveforms in terms of their peak and steady-state values. Models were developed using a TLP injection rather than an ESD gun injection, given the lower complexity and better repeatability of the TLP.

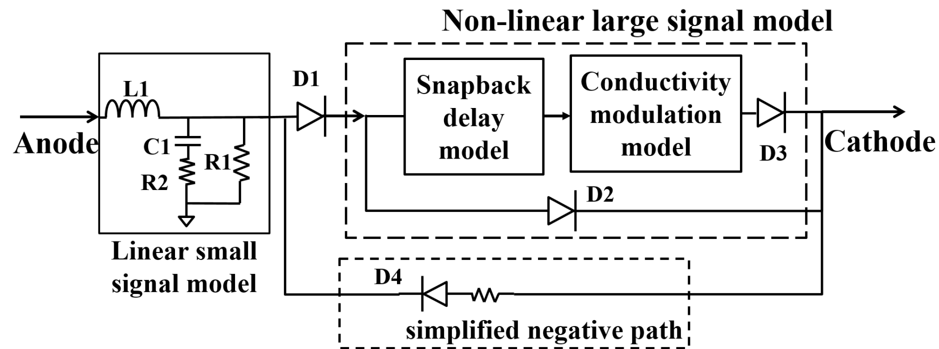

Figure 2. TVS model framework.

During the TVS modeling process, it was found that the conductivity modulation module's working range is limited, leading to bad performance after the overshoot. Two examples are illustrated in Figure 3: the TVS was tested with TLP of 0.6ns rise time and 50, 800 V injection voltage. The simulation shows a good match at low injection level – 50V; however, much underestimation at high injection level – 800 V, the corresponding current level is around 30 A – due to the limitation of the conductivity modulation, which dominates the falling edge after the overshoot. Note that the falling edge is vital in the system-level simulation together with the on-chip ESD protection devices, because the residual pulse [12] might be higher than the on-chip protection can withstand. For example, at 800 V TLP injection (Figure 3b), the remaining TVS voltage is only tens of volts at 0.5 ns, suggesting that there will be less ESD stress at the on-chip protection device. However, the measured TVS voltage is much higher – around 100 V, this residual pulse may cause the failure of the IC. To better evaluate the ESD protection design in a system, the accurate modeling of the conductivity modulation is necessary.

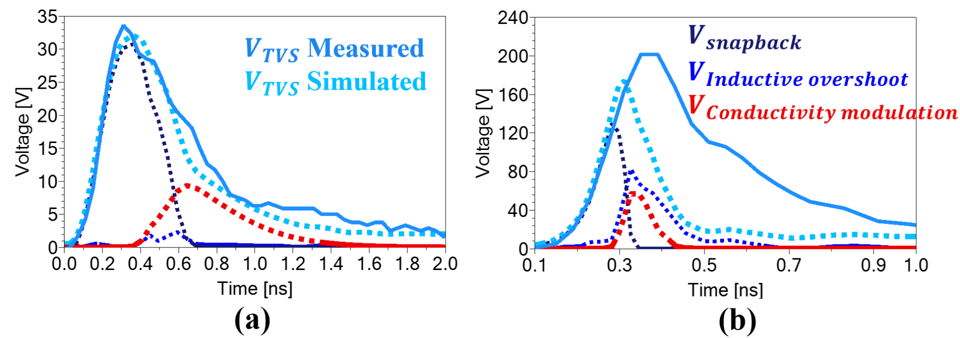

Figure 3. Measured and simulated TVS voltage with the reference TVS model at (a) 50 V and (b) 800 V TLP injection of 0.6 ns rise time.

The circuit diagram of the conductivity modulation [7] is shown in Figure 4. The TVS has a high resistance at the beginning, as the minority carries accumulates and excess of charge needed, the resistance decreases and conductivity increases, denoted as conductivity modulation [5], [13]. The conductivity modulation (Figure 4a) was modeled as a changing resistor controlled by the voltage over a constant capacitor, resulting in a narrower voltage response with increasing injection current (Figure 4b). However, the measurements suggest that the voltage response of conductivity modulation shall be of similar overshoot width. As shown in Figure 5a, the measured falling edge after the overshoot is of similar duration among different injection levels. Similar behavior was found with a different rise time case – 1 ns rise time (Figure 5b). While the conductivity modulation dominates the falling edge, so it can be concluded that the conductivity modulation model needs to be improved to have a similar voltage response duration over a wide injection range. Correspondingly, two physics-based methods are proposed to implement the improvement.

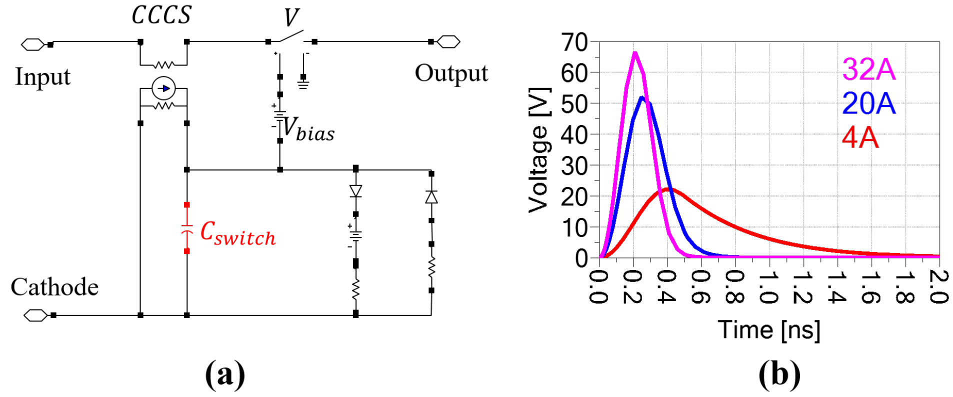

Figure 4. Reference conductivity modulation model and its voltage response.

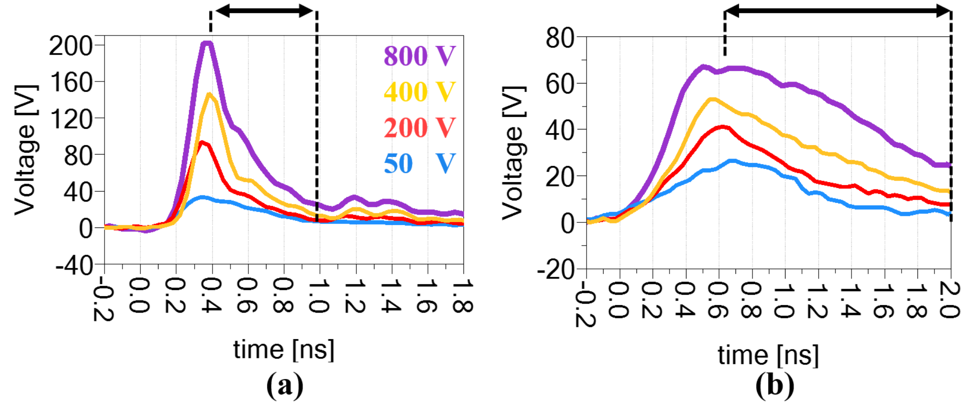

Figure 5. Measured TVS Voltage at 50, 200, 400, 800 V, and with 0.6, 1 ns rise time.

2.1. IMPROVED CONDUCTIVITY MODULATION MODEL WITH PHYSICS-BASED CHANGING RESISTOR

The simplified physics-based expression for the modulation of resistance was presented in [13], based on which the conductivity modulation overshoot was modeled in [14]. Similarly, the resistance change R_{CM} can be modeled as:

$$R_{CM} = \frac{R_{off}}{1 + Q_C/Q_0} \tag{1}$$

where R_{off} is the resistance when the TVS is at 'off' status; Q_C and Q_0 represent the total injected charge and the charge threshold needed to establish the conduction.

Accordingly, a circuit was implemented, as shown in Figure 6a. The changing resistor R_{CM} is developed in the Advanced Design System (ADS) as a symbolically defined resistor (1) whose value is controlled by the voltage $V_{control}$ over the constant charging capacitor C_{charge}. Since the C_{charge} is charged by the current flowing through the system, so $V_{control}$ represents the total charge into the system – Q_C. Ultimately, the resistance is modulated by the charge injected to the system (2).

$$R_{CM(t)} = \frac{R_{off}}{1 + C_0 \times I_{TVS(t)} \times \left(1 - e^{\frac{t}{R_2 \times C_{\text{charge}}}}\right) / Q_0} \tag{2}$$

Figure 6b shows the module's voltage response: similar duration over different injection levels, which can help to improve the modeling of the falling edge after the overshoot (Figure 3).

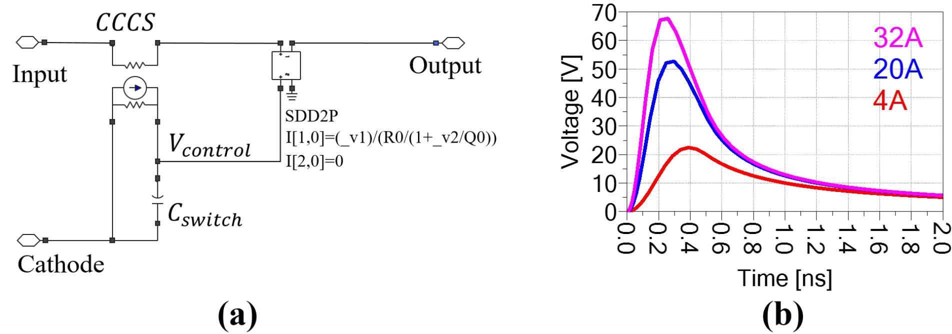

Figure 6. Improved physics-based conductivity modulation model and its voltage response.

2.2. TRANSIENT RESPONSE OF TVS AND ON-CHIP DIODE

The TVS model was enhanced based on the improved conductivity modulation methodology. The quasi-static IV (Figure 7a) is well-matched, together with the snapback behavior, based on the D2 and D3 in Figure 2. As for the transient response, the TVS' current and peak voltage are summarized in Figure 7b, with TLP of 0.6 ns and 1 ns rise time. The simulation matches the measurement primarily within 5% over a wide injection range. The peak voltage is not linearly proportional to the current; due to that, the snapback delay overshoot dominates instead of the inductive overshoot. The TVS behaves like a pure resistor after complete turn-on, so one can assume that the dI/dt is linearly proportional to the TLP injection voltage. In that case, if the inductive overshoot dominates, the current and peak voltage shall be linearly proportional to each other.

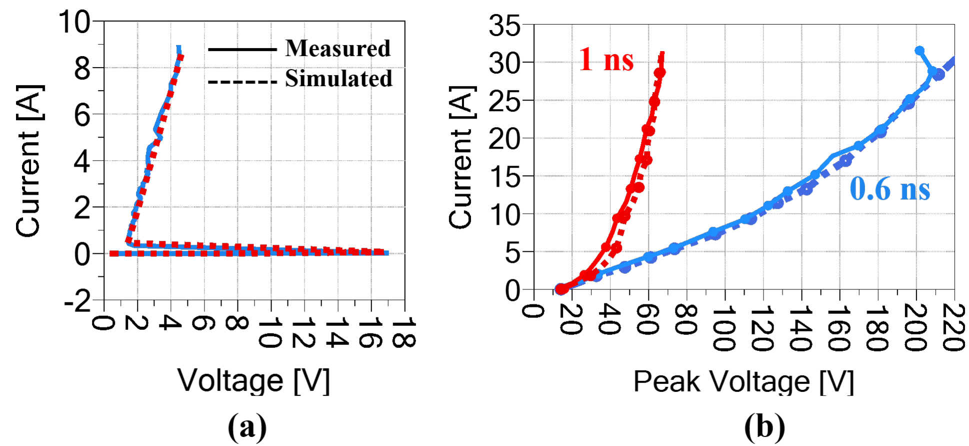

Figure 7. Quasi-static I-V curve and peak voltage versus current curve.

Figure 8 shows the measured and simulated TVS transient waveforms under a low injection level of 50 V and a high injection level of 800 V, and with rise time of 0.6, 1 ns. Note that the voltage waveforms are zoom into the first 2 ns for a better view of the rising edge and falling edge following the overshoot, which is important in the system-level

simulation with other ESD protection devices [12]. The underestimation issue of the falling edge in Figure 3b was fixed; the falling edge can be reasonably well modeled over a wide range.

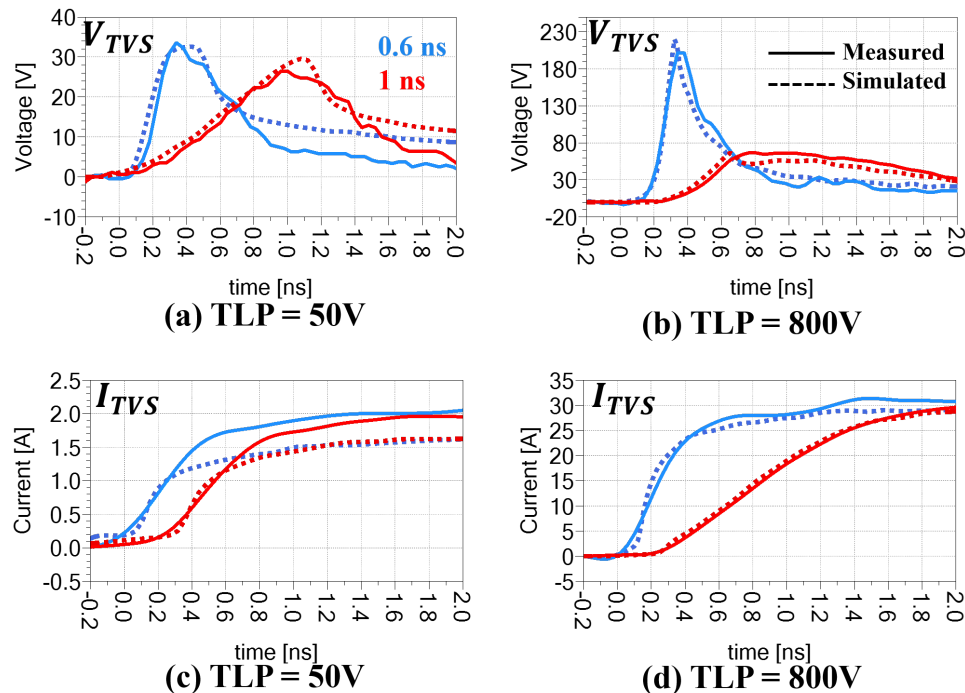

Figure 8. Transient waveforms for the TVS under TLP injection with 0.6 ns and 1 ns rise time at different levels.

To have a better view of the improved falling edge, the voltage level – 0.3 ns away from the overshoot happens – is summarized for both the reference model (the conductivity modulation was implemented with a constant charging switch, Figure 4) and the improved model, and compared to the measurement for the rise time of 0.6 ns (Figure 9a) and 1ns (Figure 9b) separately. Noticeable improvement was achieved with the physics-based conductivity modulation model.

The transient model of the on-chip diode was built with a similar methodology as the TVS, without the complicated snapback module. Measured and simulated voltage and current waveforms for the on-chip diode are shown in Figure 10 as examples to demonstrate

the model's performance, with TLP voltages of 20, 32, and 50 V and with rise-times of 0.4, 2, and 5 ns. The on-chip diode is characterized at a low TLP level, considering the IC ESD protection structure is typical of low robustness – 2 kV HBM for a USB 3.1 repeater IC (PI3EQX1002B1). The waveforms match within about 10% for each tested stimulation.

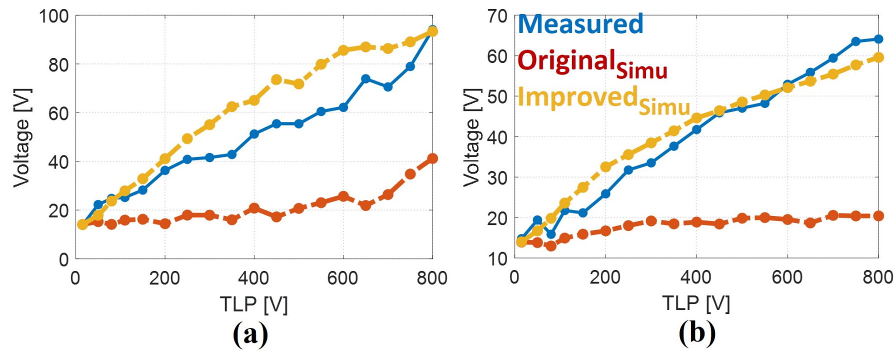

Figure 9. TVS voltage response at the falling edge with TLP rise time of 0.6 ns and 1 ns.

3. EXPERIMENTAL MEASUREMENTS

The setup used to characterize the response of the TVS and on-chip diode is shown in Figure 1. An ESD gun was discharged to a single pin of a 1.2 m long USB cable whose shield was connected to an enclosure. Inside the enclosure, the wire carrying the ESD event was either connected to a 50 Ω load or was connected to a test board containing a TVS and a pair of on-chip diodes. The board also included probes or probe points for measuring voltages and currents within the circuit.

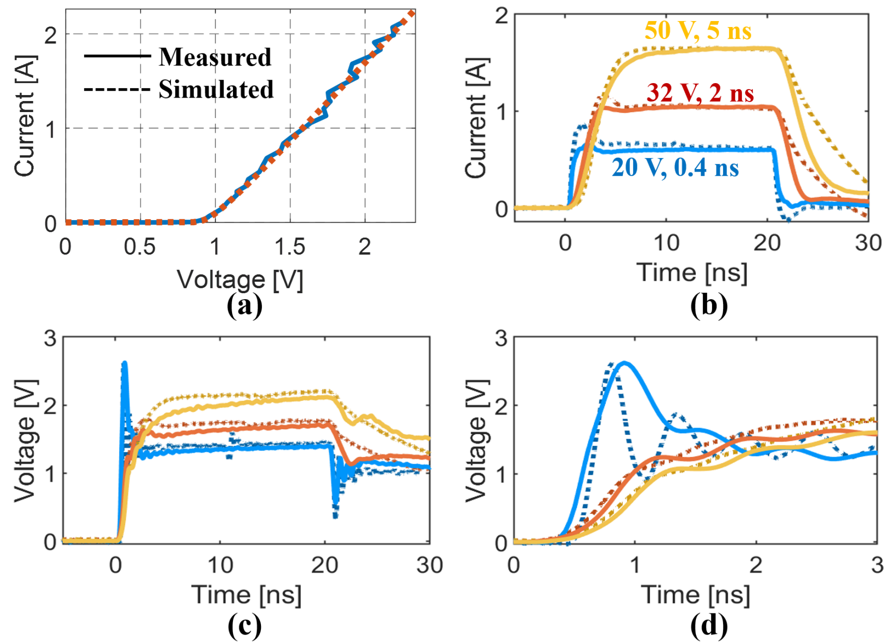

Figure 10. The quasi-static I-V behavior and the transient response of the on-chip diode model with different TLP levels and rise times.

3.1. USB CABLE CONFIGURATIONS

The test board and other measurement hardware were put inside a shielded enclosure to avoid coupling between the ESD gun and the measurement instruments. One end of the cable shield was always connected to this enclosure. The other end, at the ESD gun injection point, may or may not be connected to the enclosure, depending on the cable configuration. The cable configuration was found to have a significant impact on the ESD waveform.

Four cable configurations were studied, as shown in Figure 11. In all cases, the USB cable's internal wires were well shielded along the entire length of the cable. In Case 1 (Figure 11a), the ESD gun was discharged directly into the test board with no cable in between. This case serves as a reference for the other tests. In Case 2, the cable was run along with the enclosure, and the cable shield was connected to the enclosure at both

ends. In Case 3, the cable was run in the same way as in Case 2, but the cable shield was only connected to the enclosure at the location of the test board. Case 2 and Case 3 help demonstrate how common mode currents flowing on the cable shield's outer surface influence the ESD waveform. In Case 4, the cable was run straight out from the enclosure, normal to the enclosure wall, and parallel to the "ground" plane. Here the cable shield could only be connected to the enclosure at one location, where the cable connected to the test board.

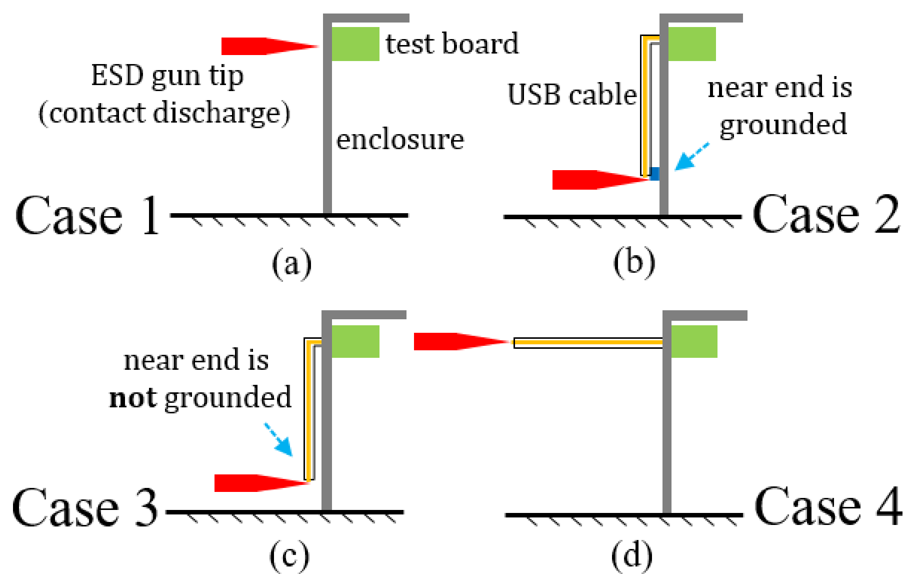

Figure 11. USB cable configurations.

3.2. DISCHARGE TO 50 Ω LOAD

The first experiments were done with the USB cable connected to a 50 Ω load inside the enclosure rather than the test board and the ESD protection devices, as shown in Figure 12. This test helps demonstrate the impact of the cable configuration and will later be used to validate the setup models. Tests were performed using 1 ~ 8 kV contact mode ESD injection to the D+ pin of the USB cable.

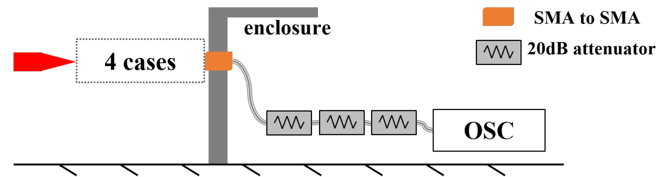

Figure 12. Measurement setup of the ESD gun contact discharge to a 50 Ω load.

Figure 13 shows the measured results when discharging to a 50 Ω load. The measured waveforms for Case 1 and Case 2 are similar since the load, and the interaction between the ESD gun and enclosure are similar at the injection site. In Case 3 and Case 4, where the shield is only connected to the enclosure at the test board, there is a considerable delay between the start of the ESD event and when the ESD event peaks – the 'peak delay' phenomenon. It is not just the interaction between the ESD gun and the cable that causes the 'peak delay', because more than just TEM modes are present between the shield and ground plane in Case 4. The root cause of the 'peak delay' will be explained in Section 4.

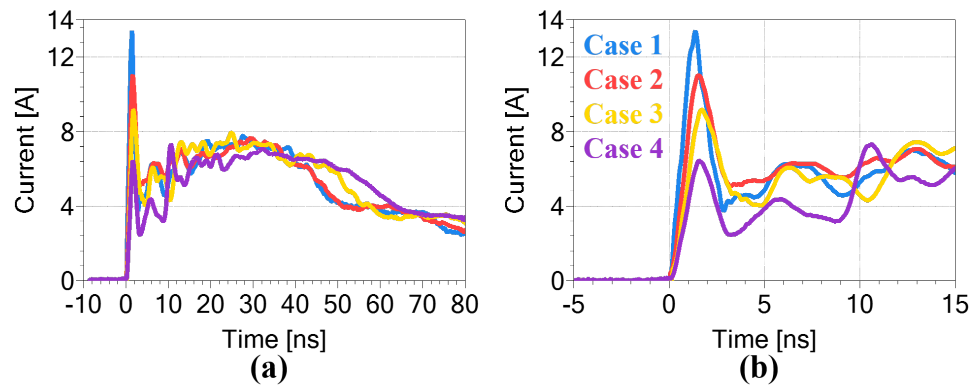

Figure 13. Measurement currents when discharging to a 50 Ω load at 4 kV contact discharge.

3.3. DISCHARGE TO ESD PROTECTION DEVICES

The subsequent tests were performed when discharging to a test board containing ESD protection circuitry. The test setup is shown in Figure 14. Tests were performed using a USB cable laid out, as shown in Figure 11.

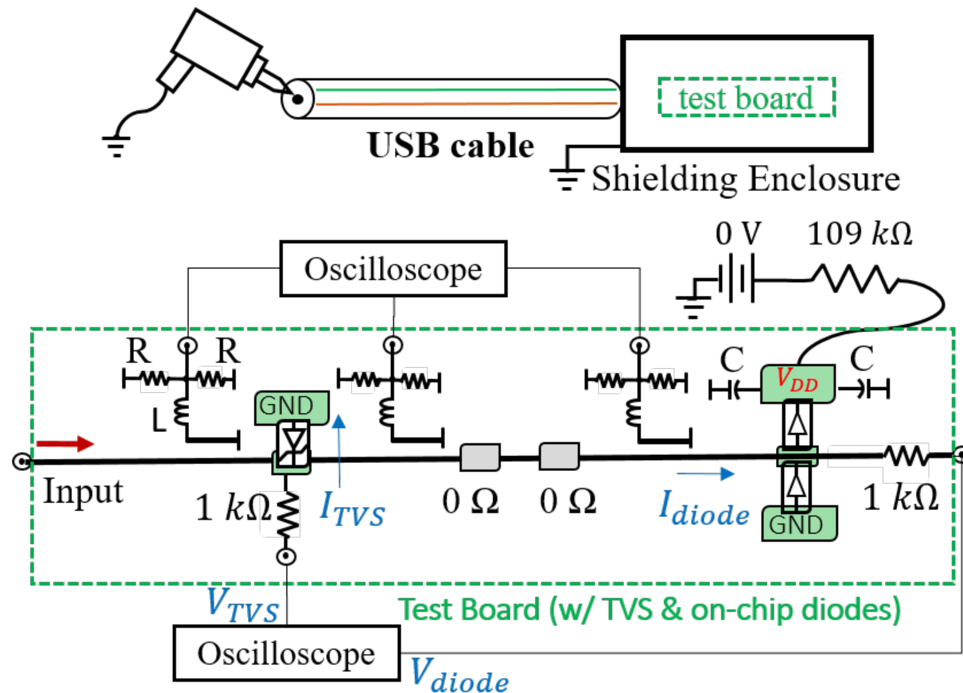

Figure 14. Discharge to a test board connected to a 1.2 m long USB cable.

The test board includes a TVS device, a pair of "on-chip" diodes, and probes for measuring the current and voltage associated with each device, as shown in Figure 4. The DC bias (VDD) was set to 0 V. A 1 kΩ resistor connected to the location of the TVS, and the on-chip diode serves as a 21:1 voltage probe of each device. The current was monitored using an FCC F65 current probe at the ESD generator's front tip and using three on-board current probes built from shorted traces located very close to the trace carrying the ESD current [1]. A current probe was placed just before, and after the TVS, so the TVS current could be determined from the difference in currents measured by the two probes. Another

current probe was placed just before the on-chip diode to capture the current to the on-chip diode. Current waveforms were reconstructed by performing a full S-parameter calibration of each probe and using the frequency domain compensation technique [15].

The total current injected into the test board, Itotal, is shown in Figure 15 for Case 2 (cable shield grounded at both ends) and Case 4 (cable straight out). When discharging to 50 Ω, the initial peak disappears when one end of the cable is not connected to the enclosure. This result further confirms that the ESD stress seen on PCB will differ significantly when the board is connected to a cable compared to when it is not. This phenomenon and other configuration measurement results will be addressed further in Section 4.

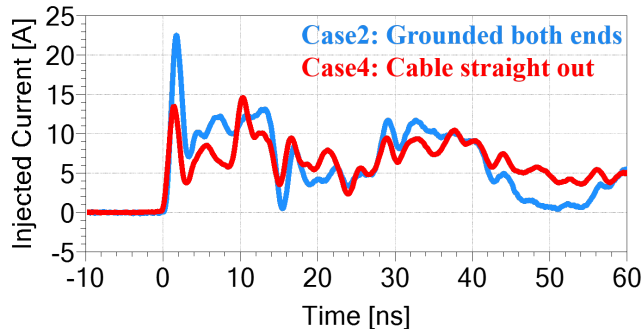

Figure 15. Measured total current injected into the test board at 4 kV contact discharge.

4. SIMULATION

The complicated interactions between the ESD gun, cable, and enclosure make it challenging to represent the ESD gun using a simple model. Traditional circuit models will not accurately capture this interaction and will give incorrect results [9]. To better capture the impact of a specific cable configuration, two methods are proposed: 1) using the S-parameter (Figure 16a) extracted from the full-wave simulation to represent the test setup [16]; 2) applying the measurement-based current source (Figure 16b), which best account for any factor in the test.

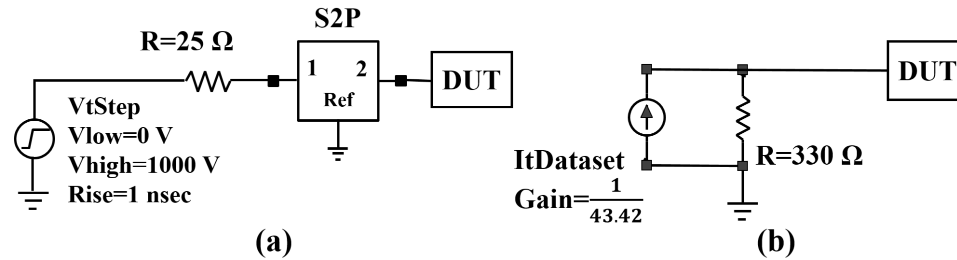

Figure 16. The hybrid simulation approach and measured-based simulation approach to account for different cable configurations.

In the full-wave-simulation-based approach, by building the 3D model according to the test setup, the extracted model can mostly represent various cable configurations' impact [16], such as the two-peak behavior in Case 4 (Figure 13). However, it is challenging to achieve good accuracy, as discussed in [8]. Moreover, the simulation time is a concern, typically taking hours, especially for a complicated structure [8].

On the other hand, the measurement-based approach is of great accuracy and easy to implement. As Figure 16b shows, the 'ItDataset' is measured current source according to the setup in Figure 12 when discharging to a 50 Ω load. The 330 Ω represents the ESD gun's impedance, and the source current magnitude can be extracted based on the measured voltage divided by the parallel resistance (43.42 Ω) of 330 Ω and 50 Ω load. Considering the load effect of the ESD gun discharge [17], 50 Ω was chosen since a TDR test of the USB cable shows the impedance between D+ and the cable's ground is very close to 50 Ω. Accordingly, in the test with a USB cable, the ESD gun sees a 50 Ω path in the beginning, and only sees the load impedance after two times the cable delay (6 ns for a 1.2 m long USB cable). One may be concerned about the low-impedance condition of ESD protection devices after turn-on, while the impact is limited. Figure 17 shows the measured and estimated current when discharging to a 2 Ω ESD target, where the estimation is based on the source model in Figure 16b, and the DUT is set as 2 Ω load correspondingly. Only

the peak current shows a 10% discrepancy, while the remaining discharging current was mostly well captured. Given the above, the measured source (with a 50 Ω load) reasonably works well for the discharging event through a USB cable.

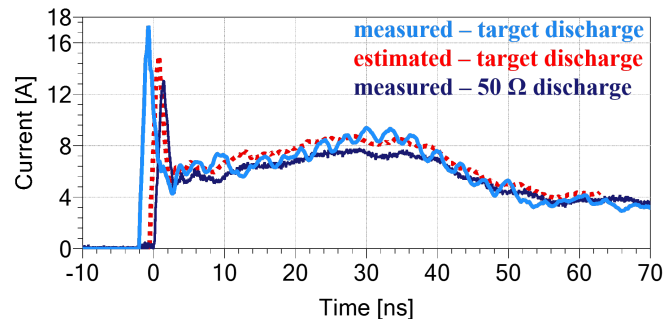

Figure 17. Current at 4 kV contact discharge (Case 1) to a 50 Ω load or the 2 Ω ESD target.

4.1. SYSTEM-LEVEL SIMULATION

The system's response to an ESD discharge to a USB cable was simulated with the measurement-based source current representing the ESD gun and different cable configurations, and the DUT is described by the circuit models of the board, TVS, and on-chip diodes. In addition, there is a 50 Ω transmission path between the source and the DUT, whose delay is determined by the SMA adapter length in Case 1 and the cable length in Case 2 ~ 4.

Figure 18 shows a comparison of the TVS current found in measurement and simulation for Case 2 (cable shield grounded on both ends) and for Case 4 (cable straight out). The predicted current matches the measurement within 30% and captures the waveform's major features well – much less current in Case 4, especially for the beginning 12 ns. Similar behavior as Figure 13, since the dominant current path is the TVS, whose current magnitude is similar to the total injected current.

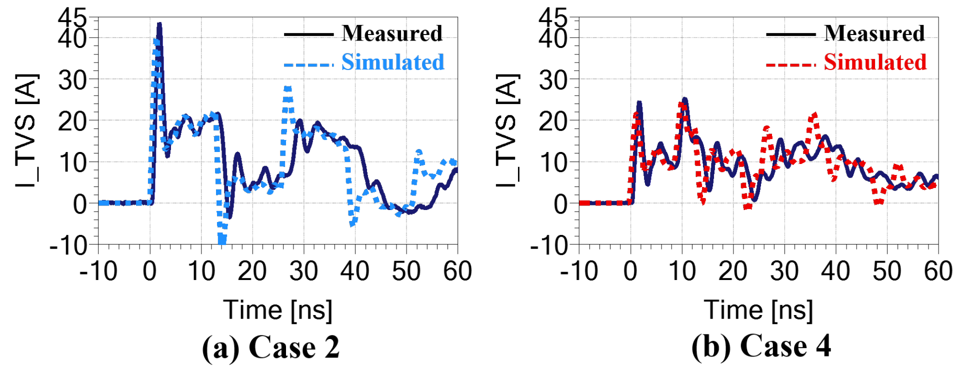

Figure 18. Measured and simulated TVS currents in Case 2 and Case 4.

Case 2 and Case 4 were selected for detailed discussion since Case 1 generates results similar to Case 2, and Case 3 generates results similar to Case 4 (see Figure 13). The current through, and voltages at, the on-chip diode are shown in Figure 19 (Case 2, both ends grounded) and Figure 20 (Case 4, cable straight out). The lowest ESD gun discharge level – 1kV and the highest level – 8 kV are selected as they are the extreme conditions which can best represent the model's performance. The ringing is caused by the reflections between the diode and TVS after they turn on, at which point they essentially create shorts at both ends of the transmission line between them. The ringing frequency is 1 GHz as predicted by the transmission line's electrical length, as is seen in both measurement and simulation. Peak currents and voltages predicted are captured within 25% of those found through measurements, while the steady-state is captured within 30%.

Moreover, the comparison between Case 2 and Case 4 are summarized in Figure 21, together with the simulations, including the on-chip diode's current and voltage at 10ns (assumed to be its quasi-static current, averaged from 9 ~ 11 ns), together with the peak current and voltage. It was observed that there is less ESD stress at the on-chip diode in Case 4, which is not surprising since the total injected current is much lower in the beginning pulse (Figure 13) due to the property of Case 4. The following Section will dig into Case 4 and discuss the impact of cable configuration.

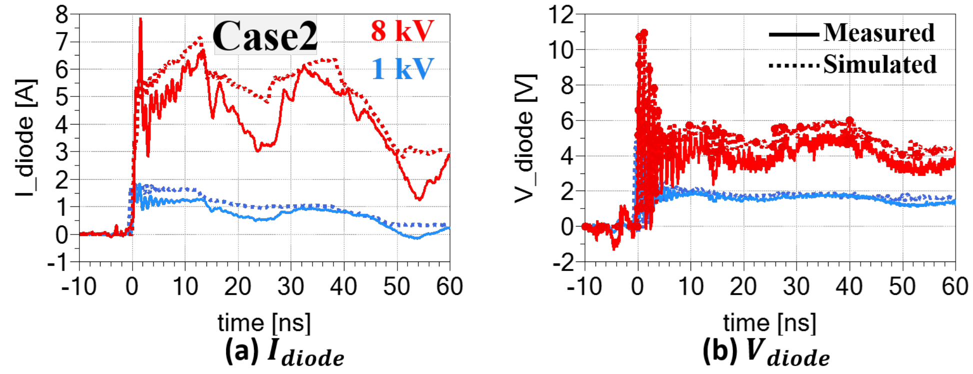

Figure 19. Measurements and simulations for the on-chip diode in Case 2.

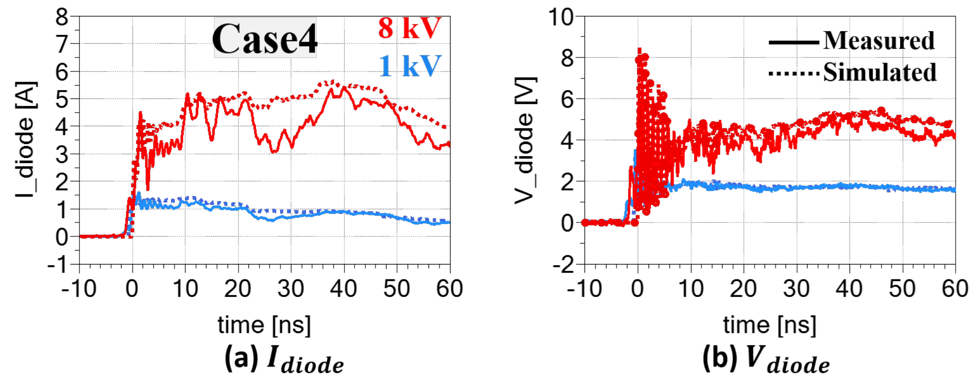

Figure 20. Measurements and simulations for the on-chip diode in Case 4.

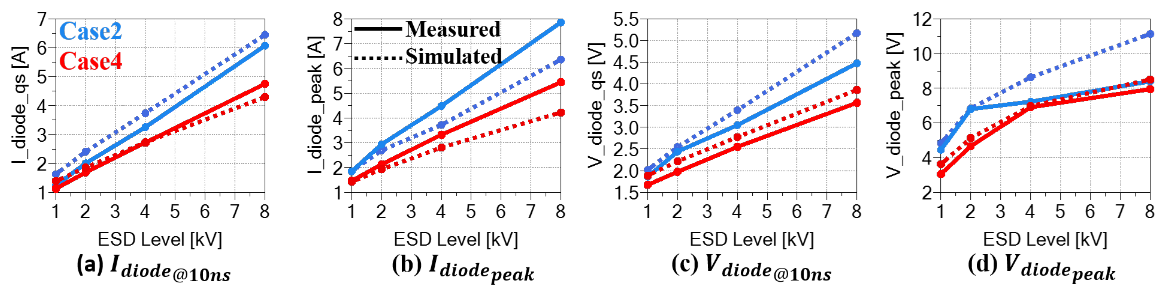

Figure 21. Simulation performance for Case 2 and Case 4 as a function of injection levels.

To further capture the model's performance, also for Case 1 and Case 3, the ESD stress at the on-chip diode under two conditions was investigated. The first was when the TVS and on-chip diode were set up, as shown in Figure 14. In the second, an additional 10 nH inductor and a 1 Ω resistor are added between the TVS and on-chip diode to simulate added parasitic inductance or resistance that may be present in an actual application. Results are shown in Figure 22 (Case 1, no cable) and Figure 23 (Case 3, grounded one end) for ESD gun discharge from 1-8 kV. Simulation and measurement mostly match within 30%. The additional impedance between the TVS and on-chip diode did reduce the ESD stress seen by the diode.

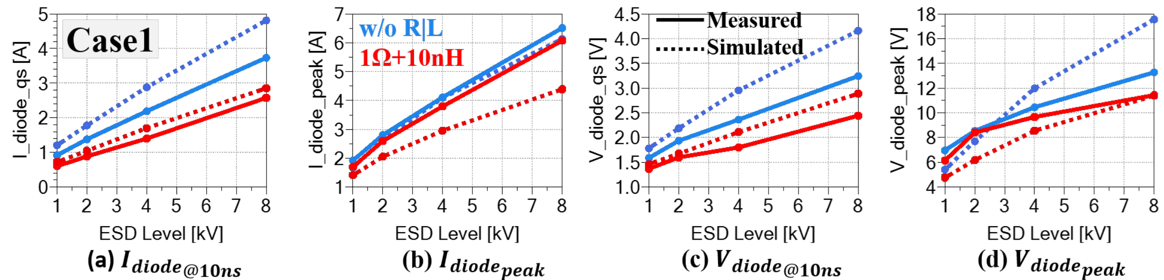

Figure 22. Simulation performance for Case 1 with or without passive components.

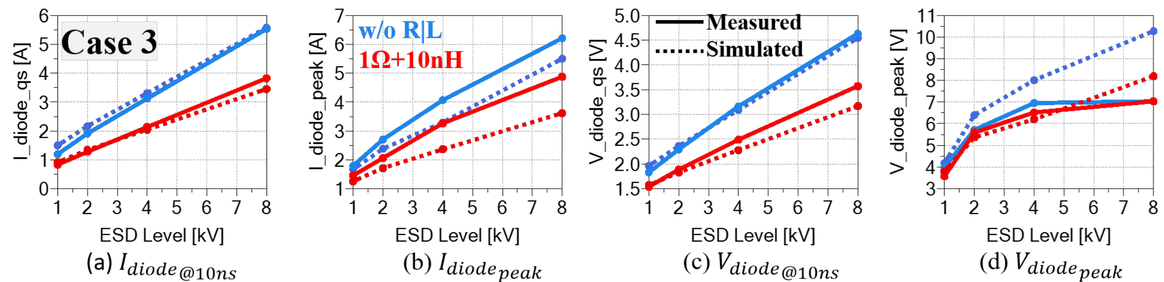

Figure 23. Simulation performance for Case 3 with or without passive components.

4.2. IMPACT OF CABLE CONFIGURATIONS

In the ESD immunity test with a contact discharge like the IEC 614000-4-2, the discharge waveform is expected to follow the standard; however, the resulting discharge waveform is far from expectation due to the cable configuration causing the wrong test conclusion. In particular, case 4 (cable straight out) leads to the most significant change of the discharge waveforms. With the help of full-wave simulation and some experiments (e.g., additional common mode chokes over the USB cable substantially change the discharge waveform), it was identified that the 'peak delay' effect of Case 4 is due to the additional common mode path caused by the none-grounded condition at the near end. The cable's outer shield, together with the big ground plane that is 1.2 m below (Figure 11), causing the additional common mode path, which is around 377 Ω (wave impedance in air). The moment the pulse starts at the inner conductor of the USB cable, the current will see two paths that are in series connected: one path is the inner system – 50 Ω, the other is the common mode path – 377 Ω. Another support is that the 'peak delay' duration is 8 ns (two times of transmission delay in the air for a 1.2 m cable) instead of 12 ns (two times of transmission delay in dielectric for the 1.2 m USB cable). Moreover, the 'peak delay' duration is proportional to the cable length, verified with measurements.

Given the above, Case 4 can be simulated as a 50 Ω transmission path with an additional high-impedance common mode path, as shown in Figure 24. The coaxial cable 'TL1' is of 50 Ω characteristic impedance, representing the inner path ('D+') of the USB cable; the 'TL2' is common mode path with air as the dielectric, and the diameter of the outer conductor ('Do') is set as 1.2 m according to the cable height. 'TL2' is terminated with short since the cable shield's far end is always connected to the shielding enclosure. The source current was measured in Case 1 (no USB cable) when discharged to a 50 Ω load.

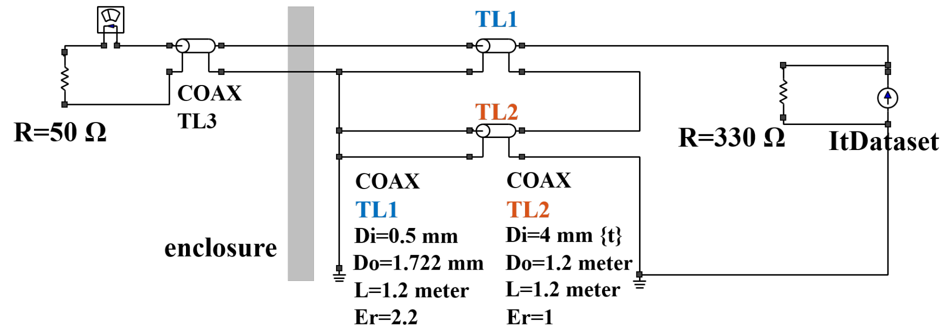

Figure 24. An approximation of Case 4 with 50 Ω inner path (TL1) and 377 Ω common-mode path (TL2).

The simulated current for Case 4 is compared to the measurement in Figure 25 at 4 kV contact discharge. The ‘peak delay’ effect is well captured, while the peak current needs fine-tuning of the inner conductor diameter of the common mode path ‘TL2’. Considering that more than just TEM modes are present between the cable shield and the ground plane, the estimation is good enough. In addition, the simulated Case 4 current was further used as the input of system-level simulation. The simulation can still match the measurement within 30%.

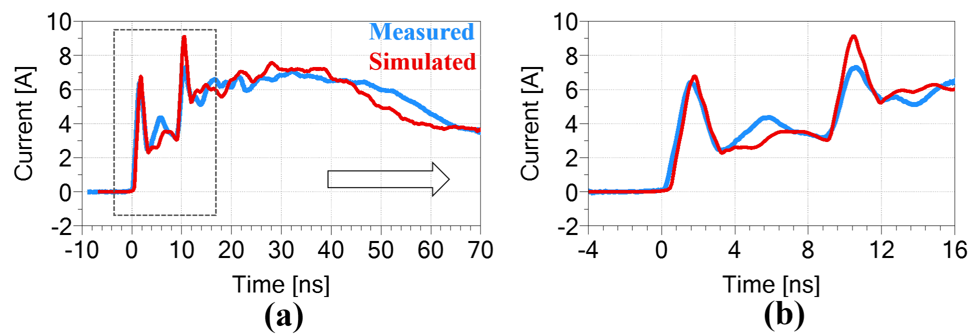

Figure 25. Simulation performance of Case 4 at 4 kV discharge.

Similarly, the lower peak current (Figure 13) in Case 3 can be explained by the additional common mode path since the near-end shield is not grounded. While the USB cable is set just above the shielding enclosure in Case 3, so the common-mode impedance is much lower than Case 4, around 100 Ω. Besides, the measured current of Case 3 can be reproduced by setting the additional common mode path as 100 Ω in the circuit shown in Figure 24.

As can be seen, care should be taken in tests with a USB cable regarding the cable position and grounding condition. The un-grounded condition will lead to less current going to the system. The higher the distance between the cable and the ground plane, the lower the peak current and the current level in the beginning pulse, whose duration is proportional to the cable length. If one needs the worst case (with the most ESD stress) in a test with a USB cable, then Case 2 (both ends grounded) shall be implemented.

4.3. DISCUSSION AND CONCLUSIONS

The transient response of the off-chip ESD protection device (TVS) and on-chip protection in an ESD gun contact discharge event through a USB cable was studied with measurements and simulations. The SEED model for the TVS was improved with physics-based conductivity modulation, whose voltage response is of similar duration over various injection levels – as the measurements indicated. The improved modeling methodology helps to accurately predict the falling edge (follow the overshoot) under a wide range of ESD stress, which is essential to accurately model the possible race condition between the off-chip and on-chip protections.

The USB cables' position and grounding condition are easily ignored in tests, leading to much different ESD stress into the system or bad repeatability among labs. Accordingly, four cable configurations were investigated. It was found that when the cable shield is only connected to the enclosure at the point where the enclosure connects to the test board, an additional common mode path will be formed, resulting in a much lower current level in

the beginning pulse, and the waveform loses the sharp, high-magnitude initial peak that is associated with a human metal model event. For example, the initial peak loses almost 50% in Case 4 (cable straight out) compared to Case 2 (both ends grounded). Moreover, the higher the cable from the ground plane, the smaller the beginning pulse. The SEED models presented here can well capture the currents and voltages of protection devices in all cable configurations over a wide range of ESD gun injection, and when adding passive components between the off-chip and on-chip protection. Moreover, the overall discrepancy between measurement and simulation is within 30%. Errors in the overall current and voltage waveforms may have been caused by small errors in the diode or TVS device's turn-on time, which can significantly change the overall waveform. It was found particularly difficult to predict the diode voltage across system configurations accurately.

Overall, the modeling process outlined here can help engineers evaluate the design effectiveness under various complicated test scenarios and optimize their ESD protection strategy accordingly.

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SECTION

2. SUMMARY AND CONCLUSIONS

This thesis has presented a transient modeling process in a complicated test scenario - ESD gun contact discharge to a USB cable. The SEED model for the TVS was improved with physics-based conductivity modulation, which allows a more accurate prediction of the interactions between the off-chip and on-chip protection devices. Besides, the impact of USB cables' position and grounding condition were discussed. It was found that when the cable's near end is not grounded; an additional common mode path will be formed, resulting in a much lower current level in the beginning pulse. The higher the cable from the ground plane, the smaller the beginning pulse.

The SEED models presented here can well capture ESD protection devices' current and voltage response under a wide discharge range over various cable configurations, even when passive components are added between the off-chip and on-chip ESD protection. Overall, this modeling process can help engineers to evaluate the design effectiveness under complicated test scenarios.

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VITA

Yang Xu received his B.S. degree in Electronic and Information Engineering from Huazhong University of Science and Technology, China, in June 2019. He received his M.S. degree in Electrical Engineering from the Missouri University of Science and Technology, Rolla, MO, USA, in December 2021. His research interests included ESD testing, RF interference, and EMI modeling.