Missouri University of Science and Technology
Scholars' Mine

Opportunities for Undergraduate Research Experience Program (OURE)

Student Research & Creative Works

16 Apr 1992

# Thermally Induced Stresses in Micro-Chip Mounting Devices

K. J. Mikulcik

Follow this and additional works at: https://scholarsmine.mst.edu/oure

Part of the Mechanical Engineering Commons

## Recommended Citation

Mikulcik, K. J., "Thermally Induced Stresses in Micro-Chip Mounting Devices" (1992). *Opportunities for Undergraduate Research Experience Program (OURE)*. 65.
https://scholarsmine.mst.edu/oure/65

This Report is brought to you for free and open access by Scholars' Mine. It has been accepted for inclusion in Opportunities for Undergraduate Research Experience Program (OURE) by an authorized administrator of Scholars' Mine. This work is protected by U. S. Copyright Law. Unauthorized use including reproduction for redistribution requires the permission of the copyright holder. For more information, please contact scholarsmine@mst.edu.

# THERMALLY INDUCED STRESSES IN MICRO-CHIP MOUNTING DEVICES

K. J. Mikulcik
Mechanical Engineering Department

## ABSTRACT

Microchip thermal stress due to the temperature change related to the mounting of a chip to its lead frame was investigated by moire interferometry. Large scale models were made, and the problems of applying a grating to this model at high temperature were addressed without success. Further possibilities, however, remain to be attempted. Moire interferometry was successfully used at room temperature by examining mechanically relieved residual stresses. The results agreed with an analytical approach to stress analysis and also to a finite element analysis. A practical solution to the problem of peeling was found.

## INTRODUCTION

Thermal stresses in microchips present a problem when microchips are large, which creates a high aspect ratio, and when there is a large temperature drop. The microchip which is made of silicon has a very low coefficient of thermal expansion, whereas the lead frame to which it is mounted is usually a metal with a high coefficient of thermal expansion. In the case of this research the lead frame is copper which has a relatively high coefficient of thermal expansion. When the silicon chip is mounted to the copper a bimetallic strip is created which bends as the temperature changes. This causes stresses that tend to peel the silicon chip from its mount at the chip's edges.

The purpose of this research is to examine the stresses in a microchip due to the curing process of the epoxy by which it is attached to its lead frame. This was accomplished by creating a large scale model of a microchip and analyzing the stress field of a cross-section of the chip by moire interferometry. Moire interferometry is a strain measurement technique by which a strain field on a flat surface is determined by examining the interference pattern between a virtual grating and an actual grating on the surface after strain. The virtual grating is the

interference pattern of two coherent beams of laser light at right angles. The resulting interference pattern is at the same frequency as the actual grating before strain. Thus fringes or nodes are produced as the strain of the actual grating causes its frequency to change. Sensitivity of measurement is highest with gratings of high frequency. The frequency of the gratings used was 1200 per inch.

The results of this analysis were compared to a finite element analysis of the chip model. The finite element program used was MSC Nastran.

## RESEARCH

To begin research, existing microchips were sliced to examine the cross section of a typical microchip on its mounting. After slicing three integrated circuits, it was determined that the chips being examined were too small to show appreciable thermal strain, even with moire interferometry. Furthermore, the chip's aspect ratio, approximately four to one, was too low for bending to occur. To measure the thermal effects on a microchip, larger dimensions were needed to use moire interferometry, and a higher aspect ratio, corresponding to a larger chip, was also needed. Therefore, materials were obtained to make a model of the largest dimensions possible for the most accurate measurements of strain.

A model was made by attaching with epoxy a piece of silicon from a 6 inch diameter silicon wafer to a plate of copper. The dimensions of the model were 2.8 inches by 3 inches with thicknesses of silicon, epoxy and copper being .033 in, .003 in and .1255 in respectively. The thickness of the epoxy was maintained by inserting between the silicon and copper mylar sheets as shims. The curing temperature was 150 Celsius so that upon cooling the resulting model showed appreciable thermal strain, for the model curved as a bimetallic strip does. Next, a thin cross section was cut from the middle of the chip model so that a strain field could be measured by moire interferometry.

Two methods of thermal stress analysis were investigated. The first method was to apply a grating that is on zerodur, a material that has a coefficient of thermal expansion of zero, at high temperature and then examine the fringe pattern upon cooling. The second method was to apply a grating after cooling and relieve the stresses mechanically after which a fringe pattern was observed.

A method was sought to apply a grating at 150 Celsius, the curing temperature of the microchip adhesive. The grating molds available were composed of silicon rubber, phenolic resin and photoresist. Photoresist does not hold

its integrity at high temperature, therefore it was not investigated as a mold at high temperature. Silicon definitely holds its integrity at high temperature. Phenolic resin needed to be investigated. Phenolic resin gratings were examined at various temperatures up to 227 Celsius. Up to 163 Celsius the phenolic resin grating appeared adequate for moire interferometry with the only adverse effects from temperature being a darkening of color and a lessoning of diffraction. Therefore, phenolic resin and silicon were used in attempts to apply a grating at 150 Celsius.

Phenolic resin gratings can be made from a silicon mold with ease at room temperature since silicon and phenolic resin do not adhere. Silicon gratings should be able to be made from phenolic resin gratings. However, this was not the case in our lab. Phenolic resin inhibited the curing of silicon. Many attempts were made at replicating silicon gratings at various temperatures but none worked satisfactorily. The best results were obtained at low temperatures. Apparently phenolic resin gives off a substance that inhibits the curing of silicon.

This lead to attempts to isolate the curing silicon from the phenolic resin. A coating (SS4177) from G.E. Silicones to inhibit the substance given off by phenolic resin was used and found to be inadequate. Photoflo was used in a similar way, and the same results were obtained.

The next step was to determine if aluminum layers could be used to isolate the curing substance, silicon, from the grating mold substance, phenolic resin. Aluminum foil could not be used since it is too thick, so the aluminum had to be vacuum deposited. An experiment was performed to determine if silicon adhesive would cure on a grating of phenolic resin with one layer of vacuum deposited aluminum. The silicon cured, but it stuck to the aluminum too strongly and the two layers could not be separated.

A possibility for relieving the problem of adhesion is to apply two layers of aluminum separated by a layer of aluminum oxide. This is the method used when the grating is made from photoresist. Many attempts were made at creating a phenolic resin grating with two layers of aluminum. However, it was discovered that the vacuum depositing machine at our facilities was defective. So a piece of zerodur with a phenolic resin grating was sent to Virginia Tech to obtain suitable aluminum layers. This piece was used in applying a layer of aluminum grating to one of the models at 150 Celsius. The results were poor since the phenolic resin degraded and the silicon did not adhere evenly. The possibility remains that a similar experiment with phenolic resin being replaced by silicon would be successful since silicon does not degrade at 150 Celsius.

Without any real success from high temperature application of a grating, attention was turned to a more conventional method of residual strain analysis. This was the technique of mechanical stress removal. Experiments were performed to determine the effectiveness of various different slicing techniques for relieving residual stresses.

The first attempt to determine residual stresses involved removing the silicon from the copper by machining it away with a diamond cutter. The results were totally inconclusive. A different attempt was made at removing the copper from the silicon and a photo was taken of the result. See Figure 1 for the U field fringe pattern and Figure 2 for the V field fringe pattern.

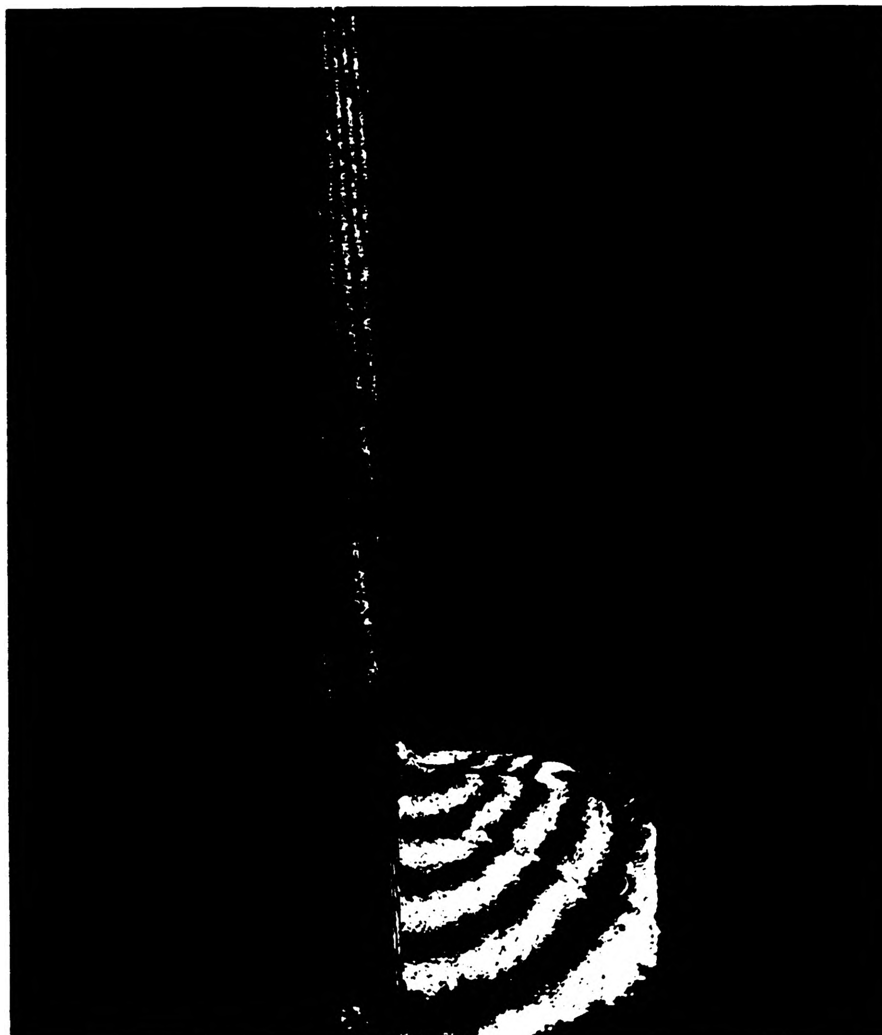

Figure 1. U Field Fringe Pattern

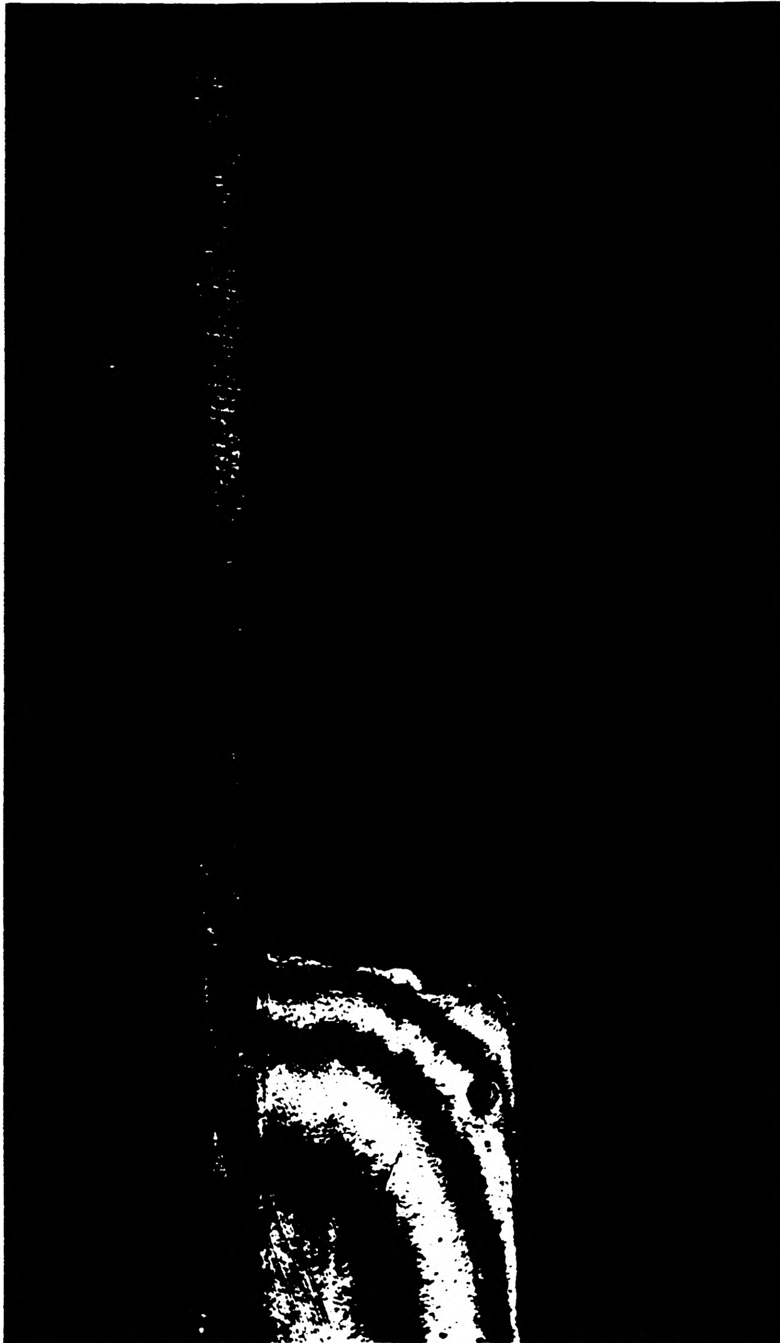

Figure 2. V Field Fringe Pattern

Although the photograph of the U field shows high shear stress near the edge of the copper, the results are poor since a null field was not obtained and a great deal of rotation occurred.

The second and final attempt at strain measurement was to examine the residual stresses at the midpoint of the microchip model. The first step was to photograph the

microchip model cross-section to obtain a null field. See Figures 3 and 4.

Figure 3. U Field (Null)

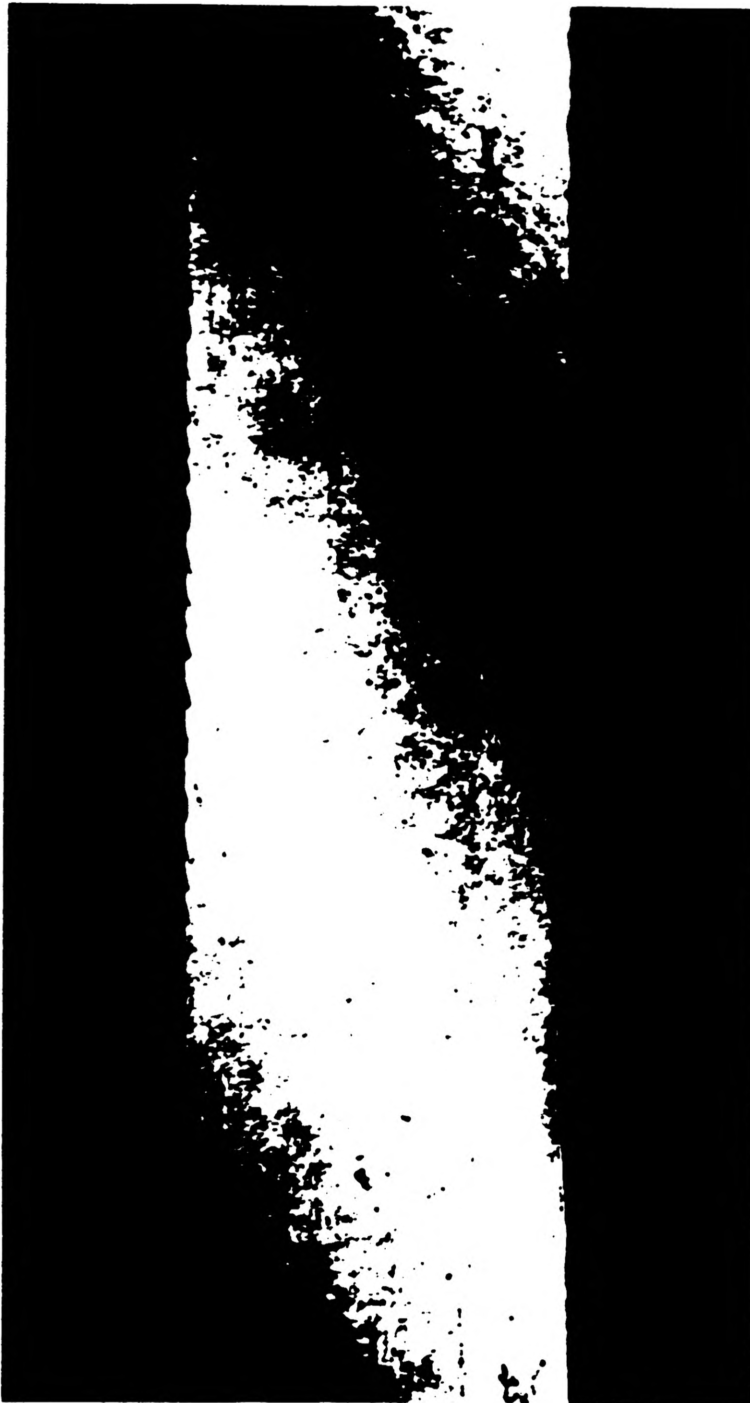

Figure 4. V Field (Null)

The notch on the right side of each photograph indicates where the cut was to be made. Next a cut was made along the centerline of the model perpendicular to the layers. This cut relieved the stresses at the centerline at the edge of

the cut. As would be expected, Figure 5, the U field photo, shows very little stress in the U direction.

Figure 5. U Field of Cut Model

The only change is a small amount of shear stress at the epoxy and some rotation. The V field, however, shows a definite pattern of stress. See Figure 6 on the following page. The silicon is in a state of compression, and it shows three fringe orders of strain. Quantitatively this amount of strain is small since the stress is not completely relieved, but qualitatively it agrees with theory. The next layer is a layer of epoxy. This layer shows a very large amount of shear strain, near 1.67 inches per inch. But this does not indicate an extremely high stress since the elastic modulus of the epoxy is on the order of 6.5^5 psi. The

Figure 6. V Field of Cut Model

copper is in both tension and compression. Adjacent to the epoxy the copper is in tension, and the fringe pattern shows this tension relieved. Between the epoxy and the right edge the stress changes to compression which is a maximum at the right edge.

This compression at the right edge of the copper is a limiting factor for the bending of the specimen. This part of the copper is resisting the moment created by the part of the copper in tension and the silicon which is in

compression.

A finite element analysis was done for comparison of the stresses in the model. See Figure 7 for the graphic side view. This graph shows the elements before and after thermal loading.

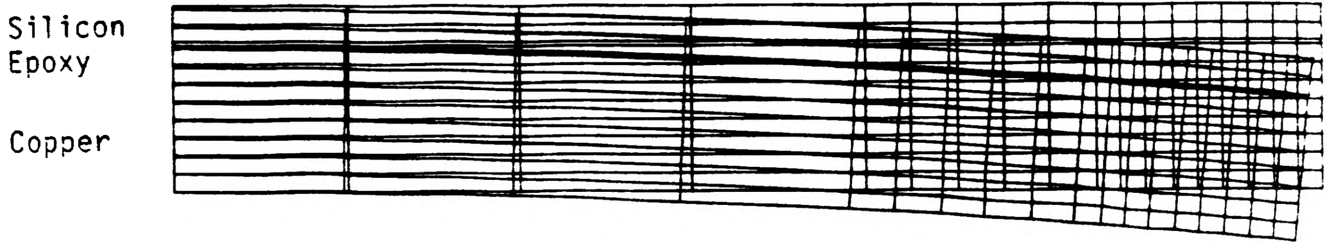


Figure 7. Finite Element Side View

This analysis agrees with the results of the stress release due to the centerline cut of the actual model. Both the model and the analysis show appreciable bending. See Figure 8 for the stress profile.

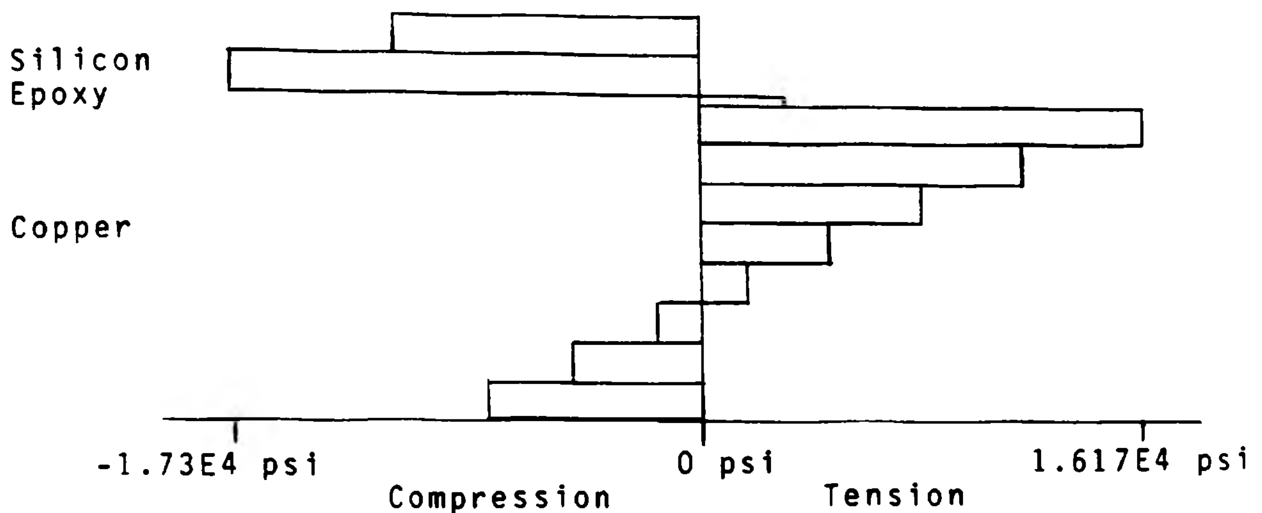


Figure 8. Stress Profile of the Finite Element Model at the Centerline

This profile shows a linear variation of stress in the copper, and this linearity is in agreement with an analytical model.

## CONCLUSIONS

In conclusion, the results of the centerline cut experiment show that it is possible to reduce the stresses that a microchip would undergo at very low temperatures. If another chip of silicon were to be attached to the opposite side of the copper lead frame, a symmetric situation would arise, and the bending would be eliminated. This would eliminate the possibility of peeling and reduce the amount of normal stress in the silicon and reduce the amount of shear stress that the adhesive would experience. Unfortunately, time did not allow for the production of a modified model with an extra layer of silicon for symmetry, nor did it allow for an attempt to apply an aluminum layer from a silicon grating at high temperature.

## ACKNOWLEDGMENTS

I thank Dr. Duksung Joh for his assistance and guidance in basic research especially in experimental techniques and for the use of his lab. I also thank Kook Yun Byun for his cooperation and help with moire interferometry and the use of Nastran. I also thank Patrick O'Mahony for his help with Nastran.