A 5-W GaN Doherty Amplifier for Ka-Band Satellite Downlink With 4-GHz Bandwidth and 17-dB NPR

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***Abstract*—This paper presents the design and experimental characterization of a GaN-Si monolithic Doherty power amplifier for Ka-band satellite downlink. The fabricated amplifier favorably compares with the current state of the art, achieving, on a record 16.3 GHz to 20.3 GHz band (4 GHz, 22% relative bandwidth), 36.6–37.7 dBm output power, 23–31% power-added efficiency, and 18–22 dB gain at saturation, and around 20% power-added efficiency at 6 dB output back-off. At 18.8 GHz, the amplifier shows a Noise to Power Ratio higher than 17 dB at all power levels, making it suitable for satellite applications where additional linearization is usually unfeasible.**

***Index Terms*—Doherty, Gallium Nitride, MMIC, NPR, Power Amplifier, Satellite, Wideband.**

I. Introduction

THE Power Amplifier (PA) plays a key role in meeting the stringent requirements on power consumption, and thus on the efficiency, of both terrestrial and space transmitters. For the satellite transmitters, integration is driven by the availability of Solid State PAs (SSPAs) based on Gallium Nitride High Electron Mobility Transistors (GaN HEMTs), which can provide the power density and efficiency performance to make them a viable solution for space-borne antennas [1], [2].

The recent adoption of large Peak-to-Average Power Ratio (PAPR) signals also in satellite applications leads to challenging requirements to the SSPA in terms of efficiency and linearity. As a consequence, PA architectures enhancing the back-off efficiency are being explored, most notably the Doherty Power Amplifier (DPA), which successfully addressed this issue in ground base-stations. Furthermore, due to limited availability of digital predistorters on board of satellites, the intrinsic linearity of the DPA will need to be sufficient to meet a fairly stringent Noise-to-Power Ratio (NPR) target [3], [4], typically of 15 dB [5], posing a further design challenge.

The Ka-band satellite downlink (17.3 GHz–20.3 GHz) active antenna applications require power levels in the range of 1–10 W, which are hardly achievable by a single chip adopting Silicon or Gallium Arsenide technologies, especially for a load modulated architecture such as the Doherty, thus requiring the adoption of GaN technology.

This work explores the feasibility of a single-chip GaN DPA with the following performance targets: 30 dB small-signal gain, 36 dBm output power, 35% power-added efficiency (PAE) and 15 dB NPR, with 25% derating of the drain supply voltage and limiting the maximum junction temperature to 160°C for reliability purposes. The state of the art (SOA) at similar frequencies [6]–[9] shows that such performance has never been achieved simultaneously, not even for terrestrial applications where technology can be exploited at its full potential. The DPA presented in this paper achieves the output power and NPR targets, while maintaining high gain and PAE over the whole band and complying with the derating rules, demonstrating the innovative nature of the work.

II. Design

The selected technology is the commercial 100 nm GaN-Si HEMT process (D01GH) provided by OMMIC [10]. Based on the gain and output power requirements, and on the maximum available device periphery, the selected architecture is a three-stage DPA, with four transistors in the final stage.

In [11], we introduced two possible strategies to design the DPA, discussing advantages and disadvantages of on-chip power combination at device level and at DPA level. This paper focuses on the combination at DPA level, presenting the design approach and experimental results, both in continuous wave (CW) and with modulated signal in terms of NPR.

The individual DPA cells are matched on 100 Ω at the output, to allow for direct combination using a 50 Ω output load. This allows to avoid additional loss and area consumption from power combiners, thus maximising PAE. On the other hand, this choice doubles the output impedance transformation ratio compared to a conventional 50 Ω design, making the achievement of wideband operation increasingly challenging.

The output combiner of the DPA cell is therefore designed based on a wideband approach, embedding the output capacitance [12], [13]. Fig. 1(a) illustrates the selected approach, with a scheme of principle highlighting all the functional blocks, including the Main impedance inverter, two $\lambda/4$ sections on the Auxiliary and a two-section real-to-real post-matching. Fig. 1(b) shows the final implementation, where capacitors connected to the same nodes have been merged for compactness, and the series inductors are realized

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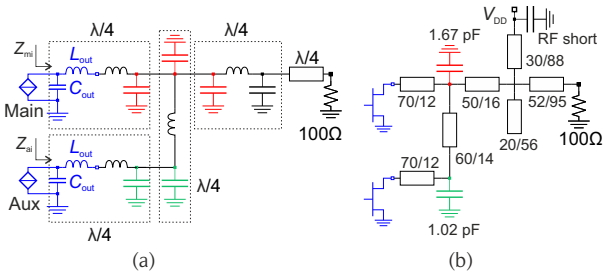

Fig. 1. Scheme of principle (a) and final implementation (b) of the output section of the DPA cell. TL parameters are given as: characteristic impedance (Ω)/electrical length (°).

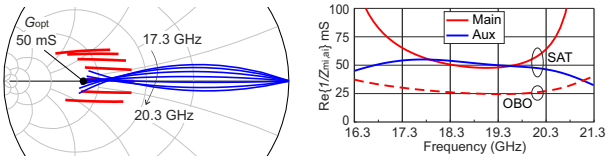

Fig. 2. Synthesized intrinsic loads of Main (red) and Auxiliary (blue) devices versus frequency, (a) on a 50 Ω Smith chart versus input drive, and (b) at fixed input drive.

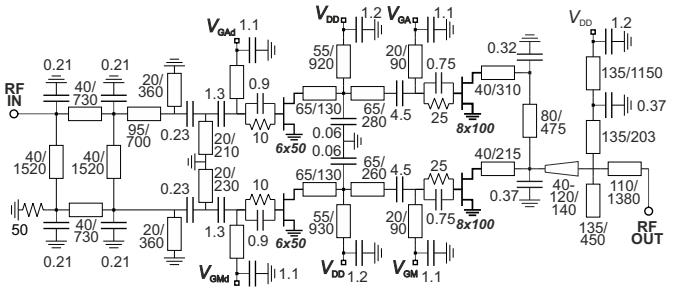

Fig. 3. Schematic of the DPA cell. Resistors and capacitors values are in Ω and pF, respectively, and dimensions of the microstrip lines are given as width/length in μm.

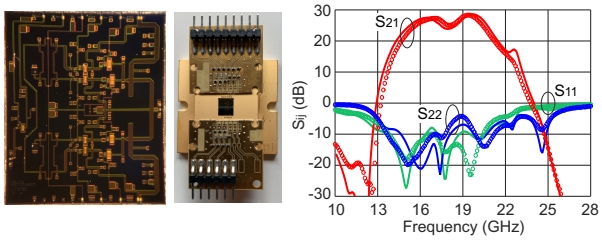

Fig. 4. Photographs of the MMIC (chip area $5\times6\,\mathrm{mm}^2$) (left) and of the test fixture (center). Comparison of simulated (solid) and measured (symbols) scattering parameters of the fixtured DPA (right).

by transmission line (TL) sections. The combiner has been carefully optimized to trade off between output power, gain compression, and efficiency both at saturation and in back-off, estimated adopting the method in [12]. According to this linear analysis, the combiner allows to achieve the desired power and linearity target over a 4-GHz bandwidth centered around 18.8 GHz. Therefore, it allows to fully cover the frequency band targeted by the application with some margin, thus providing robustness in case of process variations. Fig. 2 reports the loads synthesized at the current generator plane of the two devices by the combiner of Fig. 1(b), according to the linear device model. The reflection coefficients on the Smith Chart, that refer to Z_{mi}, Z_{ai} (indicated in Fig. 1) normalized to 50 Ω, prove that the load modulation trajectories are maintained reasonably close to the real axis over the whole band. While Fig. 2(b) shows that the desired admittance values are also maintained over the bandwidth, the main intrinsic load retains a non-negligible imaginary part, which is sub-optimal in terms of matching but minimizes complexity and losses. In fact, when implemented adopting microstrips and integrated capacitors, a better control of the main loading conditions requires complex networks with higher losses, negatively impacting both on output power and on PAE.

The complete DPA architecture consists of two parallel combined DPA cells (schematic in Fig. 3) based on individual $8\times100\,\mu$m devices for the main and auxiliary final stages and $6\times50\,\mu$m drivers in each branch, and a $4\times50\,\mu$m pre-driver. To preserve the correct signal phase alignment over a wide band, inter-stage (ISMN) and input (IMN) matching networks adopt the same topology on both branches. Both ISMN and IMN are second order filters, to trade off between performance (ohmic and mismatch losses), complexity, area occupation, and sensitivity to process variations. At the input of the DPA cell, an uneven branchline power splitter (power ratio Auxiliary/Main of 1.3) feeds the two branches.

III. Fabrication and Characterization

The manufactured chip shown in Fig. 4 has an area of $5\times6\,\mathrm{mm}^2$. The preliminary on-wafer screening (DC+scattering) has reported a yield of around 68% (15 working chips out of 22). The chips have been selected, diced and silver glued on a copper carrier, with three levels of DC decoupling capacitors/resistors. The photograph of the test fixture is shown in Fig. **??**.

A. Small and large signal characterization

The characterization has been performed under the following bias conditions: 50 mA/mm class AB for pre-driver and Main branch, class C for the Auxiliary branch ($V_{\mathrm{G,Adr}} = -2.4$ V, $V_{\mathrm{G,A}} = -2.2$ V), $V_{\mathrm{DD}} = 11$ V for all devices.

Fig. 4 reports the simulated and measured scattering parameters of the DPA. A very good agreement is found between simulations and measurements, with measured input return loss better than 10 dB and associated gain higher than 20 dB from 14 GHz to 20.4 GHz.

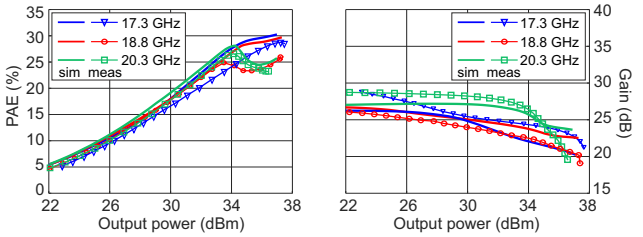

Fig. 5. Comparison of simulated (solid) and measured (symbols) CW power sweeps at 17.3 GHz, 18.8 GHz, and 20.3 GHz: PAE (left) and gain (right).

TABLE I
COMPARISON WITH SOA KA-BAND SSPAS.

Technology	Architecture	Frequency (GHz)	Bandwidth (GHz)	Bandwidth %	$P_{out,sat}$ (dBm)	PAE_{sat} (%)	$PAE_{6dB\ OBO}$ (%)	$Gain_{sat}$ (dB)	Ref.
GaN-SiC	Class AB	17.2–20.2	3	16	41	35	15	15	[5]
GaN-Si	Class AB	17–20.2	3.2	17	41	36	–	20	[14]
CMOS-SOI	Doherty	25 – 31	6	21	19.8–22.4	30–42	19–28	10	[15]
GaAs	Doherty	28	-	-	26	40	29	12	[16]
GaAs	Doherty	21 – 25	4	17	29.5–30.2	30–37	19–24	10	[13]
GaN-SiC	Doherty	20–21	1	5	35	35	15	22	[6]
GaN-SiC	Doherty	27–29.5	2.5	9	39	24	20	-	[17]
GaN-SiC	Doherty	27.5–29.5	2	7	35.6	23	18	12	[18]
GaN-SiC	Doherty	24–28	4	15	32	15	10	≈ 6	[19]
GaN-SiC	Doherty	24–28	4	15	34–36	23–41	14–32	11–13	[20]
GaN-Si	**Doherty**	**16.3 – 20.3**	**4**	**22**	**36.6–37.7**	**23–31**	**19–21**	**18–22**	**T.W.**

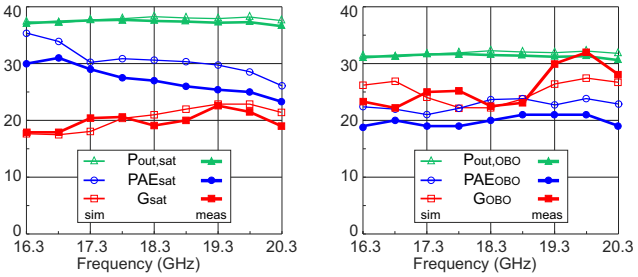

Fig. 6. Comparison of simulated and measured CW performance over the 16.3–20.3 GHz band, at saturation (left) and at 6 dB OBO (right).

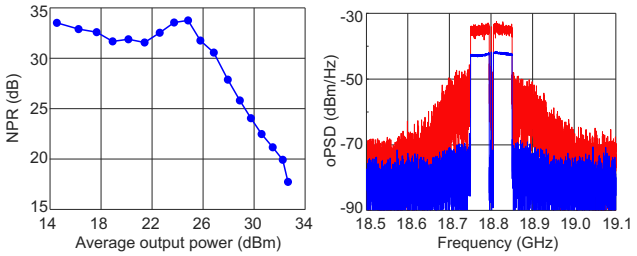

Fig. 7. NPR versus average output power at 18.8 GHz (left) and measured output power spectra (right) at low power (blue, average output power 24.8 dBm, NPR 33.7 dB, average efficiency 6%) and at high power (red, average output power 32.6 dBm, NPR 17.7 dB, average efficiency 23%).

The large signal CW characterization has been performed adopting a real-time vector system, on-wafer calibrated using a 2-port Short-Open-Load-Thru (SOLT) procedure, plus a SOL calibration at an extended port connected to a power meter for the absolute power calibration. Fig. 5 reports the simulated and measured power gain and PAE at the center and edges of the targeted band. The characterization results from 16.3 GHz to 20.3 GHz are summarized in Fig. 6, where they are compared to the simulated results. A fairly good agreement is found even in the large signal performance, except for the absolute values of the measured PAE, which is at most 5% lower than the simulated one, as it has been already observed during the load-pull measurements on the bare die devices [21]. The trends, however, are well captured for all quantities. At saturation, the DPA achieves output power, gain and PAE in excess of 36.6 dBm, 18 dB and 23%, respectively, in the 16.3–20.3 GHz band. The PAE at 6 dB output back-off (OBO) is around 20% on the same band. The performance is summarized and compared to the SOA in Table I. The presented DPA favourably compares with the SOA, achieving a 4-GHz (22%) bandwidth with high power and good efficiency.

B. System level characterization

To evaluate the DPA linearity under modulated signals, system level characterization based on NPR has been performed. It consists in evaluating the ratio between nonlinear distortion noise and signal power spectral density (PSD) at the output of the DPA when Additive White Gaussian Noise (AWGN) with a central notch is applied at the input.

A multi-sine approach is used, with 1001 tones, occupying a bandwidth of 100 MHz, designed to resemble AWGN; 5% of the tones are turned off to form a 5 MHz notch. The PAPR is controlled during signal design, to guarantee that the AWGN statistical characteristics are preserved. Note that for the classical NPR characterization, the AWGN distribution imposes a PAPR of 8 dB, which is higher than the one of the modulated signals foreseen for the targeted application. Nevertheless, this classical approach ensures that different NPR measurements are comparable, without the need of specifying the IQ data of the adopted signal, i.e., it prevents the linearity analysis from being application dependent.

Fig. 7 shows the measured NPR curve as a function of the average output power at 18.8 GHz and the output power spectral densities (oPSDs) in two cases, namely the most linear point, in deep back-off (left, average output power 24.8 dBm, NPR 33.7 dB, average efficiency 6%) and the highest power point (right, average output power 32.6 dBm, NPR 17.7 dB, average efficiency 23%). The DPA achieves NPR above 17 dB over the whole operating range, considering that 32.6 dBm is the highest achievable average power while maintaining reasonable clipping, given the statistics of the adopted stimulus (8 dB PAPR). According to the obtained results, the DPA complies with the specification for this work (15 dB NPR at 36 dBm saturated output power).

IV. CONCLUSION

This work has presented a GaN-Si 5 W Doherty power amplifier, with a 4-GHz bandwidth completely covering the Ka-band satellite downlink. The fabricated chip showed a measured NPR in excess of 17 dB in all operating conditions, suggesting that its intrinsic linearity is sufficient to make it a

good candidate for satellite communications, without the need of additional linearization circuitry.

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