Experimental investigations on the tuning of active gate drivers under load current variations

Experimental Investigations on the Tuning of Active Gate Drivers under Load Current Variations

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***Abstract*—Active Gate Drivers have gained of interest as they allow one to shape the switching waveforms finely, thus reducing overshoots and oscillations. However, when fast power switches are exploited, the tuning of such drivers is still challenging. This paper investigates the adjustment of gate current profile under load variations, which is a crucial issue when targeting practical applications. Indeed, a technique, based on the stretching of time intervals, is proposed and its effectiveness, in terms of undershoot reduction, is experimentally assessed.**

***Keywords*—Active Gate Driver (AGD), switching waveforms, AGD tuning, power transistors.**

I. Introduction

In recent years, the design of power modules featuring higher efficiency has been achieved by the exploitation of faster power switches, amongst which SiC and GaN transistors. Indeed, the former outperforms traditional Si transistors in terms of on-resistance and thermal reliability, the latter in terms of lower parasitic capacitances [1]. As the use of such devices is spreading among practitioners, some drawbacks should be carefully taken into account. Faster devices imply higher dV/dt and dI/dt, which worsen the Electro-Magnetic Interference (EMI) performance of power modules [2]. Over-voltages and over-currents are also more prone to occur, thus affecting the reliability of the system [3]. Finally, resonant circuits comprising the inductive and capacitive parasitics of layout, packaging and of active devices themselves may be triggered, resulting in unwanted oscillations superimposed onto the switching waveforms.

Active Gate Drivers (AGDs) are currently being investigated to address the aforementioned issues, as they allow to shape the switching waveforms by modulating the driver strength during transients [4]. Indeed, the modulation can be achieved by modifying the current/voltage/resistance value, and the profile can be fixed, modified during the transient or adapted cycle-by-cycle to account for operating condition variations [5]. With respect to traditional solutions, e.g., snubbers and ferrite beads, AGDs allow a better trade-off between switching power losses and overshoot reduction as the power transistor is slowed down only for a part of the overall transient [6]. As far as fast power switches are concerned, e.g., GaN transistors, research has focused on open-loop AGDs, as they do not require high-bandwidth sensing circuit to measure peaks and slopes, nor fast digital circuits to evaluate the new profile on the basis of some algorithm. However, they may result in oscillating waveforms when the operating conditions are not constant, as reported in [7]. More precisely, variations of the load current should be careful considered, as they are rather common in practical scenarios. Reference [8] suggests to reduce the clock frequency of the proposed AGD when the load current increases. In [7], both current and temperature variations were investigated, and, a look-up table is proposed to store the AGD profiles for different currents in [9]. However, none of these works provides a method to adapt the AGD modulation profile to load current variations. Indeed, this issue deserves further investigations as it is crucial for the practical use of open-loop AGDs. The aim of this paper is to provide an experimental relation between the AGD parameters and the actual load current, in such a way, the nominal profile can be adapted to different loads without the need of a large memory to store the driving patterns or of devoting several steps to find the optimal profile, as discussed in [5].

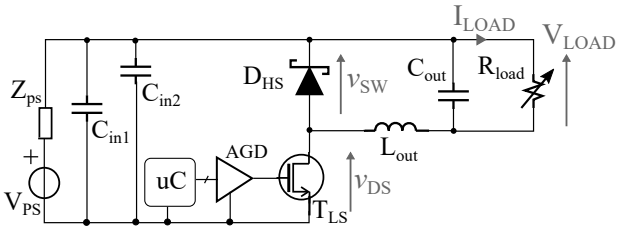

Fig. 1. Circuit schematic of the Buck converter exploited as case study.

The remainder of the paper is organized as follows. In Section II, the prototyped Buck converter featuring an AGD, which is later exploited as case study, is presented, then, the experimental setup and the effects of different load currents on switching waveforms are discussed in Section III. An effective tuning technique is presented in Section IV, and it is compared against the use of a fixed profile. Concluding remarks are drawn in Section V.

II. The case study

A low-side asynchronous Buck converter, like the one shown in Fig. 1, was exploited as case study in what

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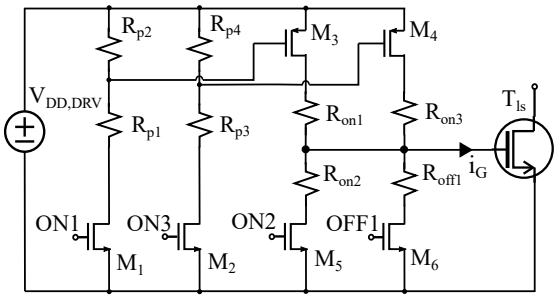

Fig. 2. The schematic of the prototyped AGD.

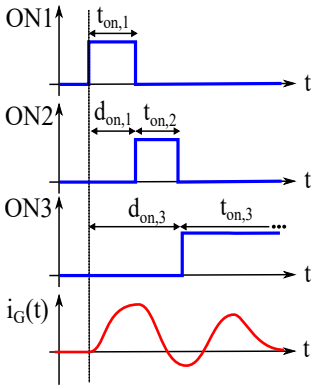

Fig. 3. The timing of the AGD control signals provided by the microcontroller.

follows. The power switch $T_{\rm ls}$ turns-on and turns-off with a fixed 0.25 duty cycle by means of the prototyped AGD shown in Fig. 2. The free-wheeling diode $D_{\rm hs}$ let the current flowing in $L_{\rm out}$ to discharge when $T_{\rm ls}$ is off. Input ($C_{\rm in,1-2}$) and output ($C_{\rm out}$) capacitors have been included to reduce the ripple affecting input and output voltages. Under nominal conditions, the converter steps down a 24 V input voltage ($V_{\rm PS}$) to a 6 V output voltage ($V_{\rm LOAD}$), while providing the load with a 0.5 A output current ($I_{\rm LOAD}$). The nominal values of active and passive components exploited are listed in Table I.

The $T_{\rm ls}$ turn-on and the turn-off is achieved by means of the AGD shown in Fig. 2, which consists of discrete level components entirely. Such a driver is able either to turn-on the power transistor sharply or by modulating the gate current $i_{\rm G}$, depending on the control signals $ON1, ON2, ON3$. Referring to Fig. 3, $ON1, ON2, ON3$ are Pulse-Width-Modulated (PWM) outputs of the on-board microcontroller, whose duty cycles and phases can be interdependently adjusted by the firmware. The M_{1-2}, M_{5-6} transistors were chosen to be in deep triode when the PWM signals are high. As far as the $T_{\rm ls}$ turn-on is concerned, when $ON1$ is activated, M_1 and M_3 turn-on, thus the gate terminal of $T_{\rm ls}$ is connected to $V_{DD,DRV}$ through $R_{\rm on1}$. When $T_{\rm ls}$ reaches the Miller's plateau, $ON1$ is deactivated, meaning that M_1 and M_3 turn-off and $ON2$ is activated. As a consequence, some current is sunk by the $T_{\rm ls}$ gate and the power transistor is slowed down, resulting in an increase of the $T_{\rm ls}$ drain-source voltage ($v_{\rm DS}$). Finally, M_5 is turned-off and $ON3$ is activated, so $T_{\rm ls}$ can entirely turns-on, eventually. As depicted in Fig. 3, the duty cycles of $ON1, ON2, ON3$ are named $t_{\rm on,1-3}$, and the $ON2, ON3$ delays with respect to $ON1$ are called

TABLE I
PARAMETER VALUES OF THE DESIGNED CONVERTER.

Parameter	Value	Parameter	Value	Parameter	Value
$C_{\rm in,1}$	100 μF	$V_{\rm LOAD}$	6 V	$V_{\rm PS}$	24 V
$C_{\rm in,2}$	2.2 μF	$R_{\rm load}$	12 Ω	$L_{\rm out}$	220 μH
$T_{\rm ls}$	[11]	$R_{\rm p1}$	20 Ω	$R_{\rm p2}$	28 Ω
$R_{\rm p3}$	39 Ω	$R_{\rm p4}$	56 Ω	$R_{\rm on1}, R_{\rm on3}$	4.7 Ω
$R_{\rm on2}, R_{\rm off1}$	0 Ω	$V_{\rm DD,DRV}$	10 V	$I_{\rm LOAD,max}$	5 A

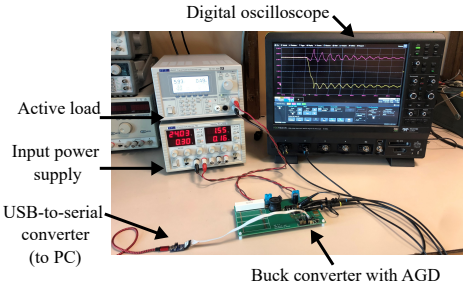

Fig. 4. Photograph of the experimental setup.

$d_{\rm on,2-3}$, respectively. By exploiting the proposed circuit, it is possible to generate an $i_{\rm G}(t)$ current profile similar to that discussed in [10], which was found to damp the turn-on oscillations. The $T_{\rm ls}$ turn-off is always achieved by a single level, i.e., only $OFF1$ is exploited, as the oscillations affecting such transient are negligible.

III. EXPERIMENTAL SETUP

Aiming to modify the AGD parameters, i.e., $t_{\rm on,1-3}$ and $d_{\rm on,2-3}$, automatically and to assess their impacts on switching waveforms, the experimental setup shown in Fig. 4 was exploited. The prototyped converter is supplied by a 24 V DC input voltage, and the resistor $R_{\rm load}$ is emulated by an active load, which allows one to modify the output current $I_{\rm LOAD}$. The converter is provided with a serial interface, thereby the AGD parameters can be modified on-the-fly by a proper software running on the PC. In such a way, the corresponding switching waveforms acquired by the digital oscilloscope can be saved synchronously with the actual values of AGD parameters. As previously mentioned, the developed AGD can also operate as a Conventional Gate Driver (CGD) if $ON1$ only is activated for the entire on-time of $T_{\rm ls}$. In such a case, and with the converter providing 0.5 A to the load, the corresponding $v_{\rm DS}$ voltage is shown in Fig. 5(a) by dashed line. It is affected by oscillations at 30 MHz due to the parasitic resonant circuit excited during the transient, which result in the peak affecting the amplitude of the $v_{\rm DS}$ frequency spectrum, as shown in 5(b). Such oscillation does not only impact on the EMI of the converter, but also causes over-current and over-voltage on $i_{\rm SW}$ and $v_{\rm SW}$, eventually.

Then, the AGD parameters were manually tuned to account for the AGD propagation delays also, resulting in the $v_{\rm DS}$ shown in Fig. 5(a) by solid line. The unwanted oscillations were entirely damped, thanks to a local increase of $v_{\rm DS}$ caused by the $ON2$ activation. Indeed, the frequency spectrum of $v_{\rm DS}$ is no longer affected by the peak at 30 MHz, as shown in Fig. 5(b), meaning that a tuned AGD is effective in reducing the delivered EMI. The AGD benefits come at the cost of a slightly decrease

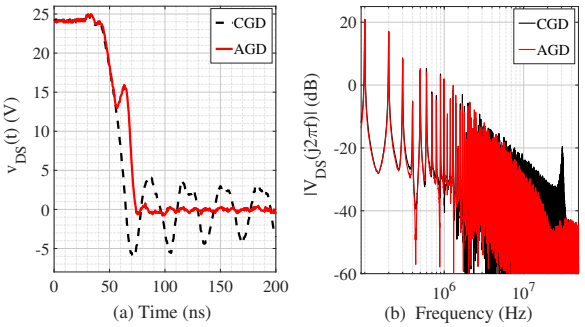

Fig. 5. The drain-source voltage $v_{\rm DS}$ (a) with the power transistor driven sharply (dashed line) and by the tuned AGD (solid line) for a 0.5 load current acquired by the oscilloscope, (b) the corresponding frequency spectra.

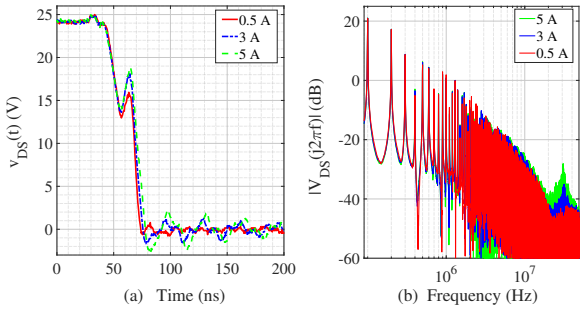

Fig. 6. The drain-source voltage $v_{\rm DS}$ with (a) the AGD parameters are fixed and the current is increased to 3 A (dotted) and to 5 A (dashed line). In (b), the corresponding frequency spectra.

in the converter efficiency, as it reduces from 83.3% (CGD) to 82.7% (AGD). However, it should be noticed that AGDs outperform traditional solutions in terms of switching power losses [6]. It was set $t_{\rm on1,nom}$=16 ns, $d_{\rm on2,nom}$=12.5 ns, $t_{\rm on2,nom}$=15.25 ns and $d_{\rm on3,nom}$=17 ns. On the contrary, the actual value of $t_{\rm on3,nom}$ is only related to the $T_{\rm ls}$ on-time, thus it does not impact on switching performance.

With the load current increased whilst keeping constant the AGD parameters to their nominal values, the resulting $v_{\rm DS}$ are shown in Fig. 6(a) in the case of $I_{\rm LOAD}$=3 A (dotted line), $I_{\rm LOAD}$=5 A (dashed line), as well as $I_{\rm LOAD}$=0.5 A (solid line) as a reference. The amplitude of oscillations increases, as well as the 30 MHz peak in the frequency spectra, as shown in Fig. 6(b), which at 5 A output current is 10 dB higher than in nominal condition.

IV. Tuning of AGD Parameters

In order to address such an issue, the proposed setup was used to modify the AGD parameters under different load currents to adapt the original profile, i.e., the one with the nominal parameters, to $I_{\rm LOAD}$ variations. The results of such investigations are reported in the remainder of the paper.

A. Stretch of ON1

As far as the $T_{\rm ls}$ turn-on is concerned, it results that oscillations are triggered by the $v_{\rm SW}$ rising edge, which takes place after the current in the power transistor ($i_{\rm SW}$) has reached $I_{\rm LOAD}$ [12]. Indeed, the $i_{\rm SW}$ slope is limited by the parasitic inductance of the power loop and by the input voltage, meaning that the higher $I_{\rm LOAD}$, the longer

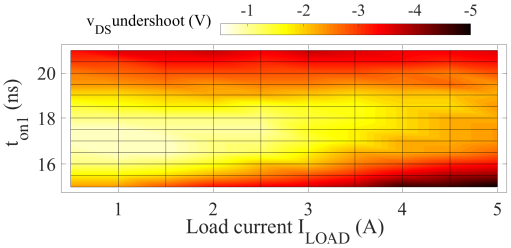

Fig. 7. Color-map representing the $v_{\rm DS}$ undershoot for [0.5,5] A load current and with the AGD parameters modified in according to (1).

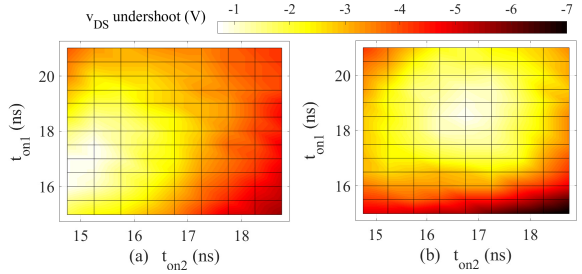

Fig. 8. Color-map representing the $v_{\rm DS}$ undershoot for (a) 0.5 A and (b) 5 A load current when both $t_{\rm on,1}$ and $t_{\rm on,2}$ are modified.

$T_{\rm ls}$ will take to reach $I_{\rm LOAD}$. Thus, it seems reasonable to increase $t_{\rm on,1}$ as the output current increases and to delay $ON2, ON3$ in the meanwhile. The AGD parameters were modified as

$$\begin{aligned} t_{\rm on1} &= t_{\rm on1,nom} + \Delta_1 \quad & d_{\rm on2} &= d_{\rm on2,nom} + \Delta_1 \\ t_{\rm on2} &= t_{\rm on2,nom} & d_{\rm on3} &= d_{\rm on3,nom} + \Delta_1 \end{aligned} \tag{1}$$

where Δ_1=[-1, 5] ns with a 0.5 ns step and the load current was varied in the [0.5, 5] A range. The color-map shown in Fig. 7 reports the $v_{\rm DS}$ undershoot for each configuration, more precisely, a darker color represents a higher undershoot. By increasing $t_{\rm on,1}$ to 19 ns for a 5 A load current, the undershoot is equal to 2.2 V, which is lower than the one with $t_{\rm on,1,nom}$ (3.2 V). However, by stretching $t_{\rm on,1}$ only, oscillations are not entirely damped.

B. Stretch of ON1 and ON2

Besides the $t_{\rm on,1}$ increase, which resulted in few advantages, also $t_{\rm on,2}$ was modified. As the load current increases, then also the energy stored in the parasitic inductance of the power loop increases, thus the power transistor has to dissipate more power to damp the oscillations. As previously discussed in Sect. II, $ON2$ controls the amount of gate charge sunk when $T_{\rm ls}$ is in Miller region, meaning that the longer $ON2$ lasts, the more $v_{\rm DS}$ increases. With these considerations, both $t_{\rm on,1}$ and $t_{\rm on,2}$ were modified as

$$\begin{aligned} t_{\rm on1} &= t_{\rm on1,nom} + \Delta_1 \quad & d_{\rm on2} &= d_{\rm on2,nom} + \Delta_1 \\ t_{\rm on2} &= t_{\rm on2,nom} + \Delta_2 & d_{\rm on3} &= d_{\rm on3,nom} + \Delta_1 + \Delta_2, \end{aligned} \tag{2}$$

with Δ_1, Δ_2 in the [-1,5] ns and [-0.5,3.5] ns ranges, respectively. Figure 8(a) shows a color-map of the $v_{\rm DS}$ undershoot for $I_{\rm LOAD}$=0.5 A, Fig. 8(b) for $I_{\rm LOAD}$=5 A. As it can be noticed, the lightest region, i.e., the one with minimum undershoot, has moved to higher $t_{\rm on,1}$ and $t_{\rm on,2}$, thus assessing the theoretical motivations reported. Indeed, by modifying both parameters, the undershoot can be effectively reduced.

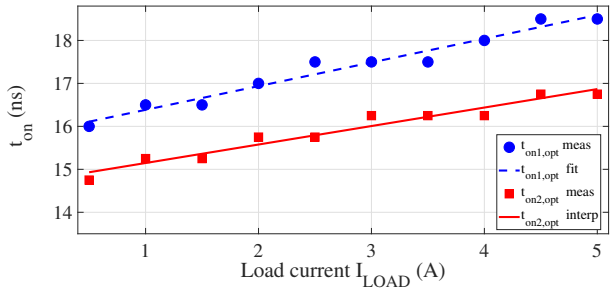

Fig. 9. Optimal values of $t_{\mathrm{on},1}$ (circle markers) and $t_{\mathrm{on},2}$ (square markers) obtained from experimental data, and the corresponding linear fit in dashed and solid line, respectively.

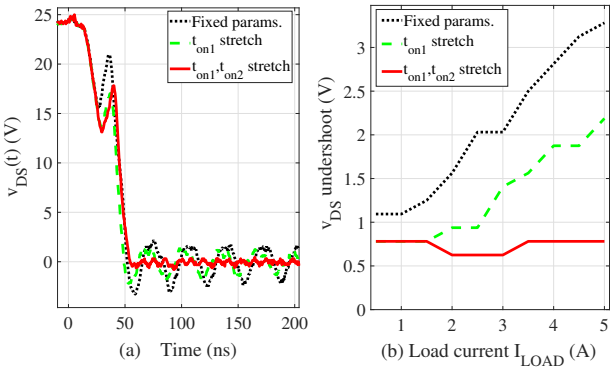

Fig. 10. In (a) the drain-source voltage with 5 A load current, in (b) the v_{DS} undershoot. Dotted lines refer to fixed AGD parameters, dashed lines to $t_{\mathrm{on},1}$ stretch, and solid lines to $t_{\mathrm{on},1}$ and $t_{\mathrm{on},2}$ stretch.

In order to find a relation between the AGD parameters and the load current, the optimal $t_{\mathrm{on},1}$,$t_{\mathrm{on},2}$ values related to the minimum undershoot were extrapolated for each current, and plotted in Fig. 9 by circle and square markers, respectively. Then, a linear fit was performed resulting in the dashed and solid curves shown in the same plot, which well fit the experimental data. The resulting expressions were found to be equal to

$$t_{\mathrm{on},1} = p_1 I_{\mathrm{LOAD}} + p_0 \quad t_{\mathrm{on},2} = p_3 I_{\mathrm{LOAD}} + p_2 \qquad (3)$$

where p_0=15.8 ns, p_1=0.55 ns/A, p_2 = 14.7 ns and p_3=0.43 ns/A. This point is crucial, as it states that the gate current profile, obtained under a given load current, can be adapted to different load currents without affecting the undershoot. Indeed, only four coefficients are needed to be stored, while the computation of the new parameters required sums and products only.

C. Comparison of the analyzed techniques

Finally, a comparison between the analyzed techniques, i.e., fixed profile, $ON1$ only and $ON1, ON2$ stretch, is presented. For a load current of 5 A, the configuration that minimize the undershoot was selected for each technique, and the corresponding v_{DS} shown in Fig. 10(a). With the AGD parameters kept fixed, oscillations are superimposed onto v_{DS}, as shown by the dotted line. If $t_{\mathrm{on},1}$ is increased, they are mitigated but they are still not negligible (dashed line), on the contrary, when both $t_{\mathrm{on},1}$ and $t_{\mathrm{on}21}$ increase proportionally to I_{LOAD}, then v_{DS} is not affected by oscillations (solid line). Finally, the undershoot was measured for each technique and plotted in Fig. 10(b). For the [0.5,5] A current range, only the third technique allows the AGD to keep the undershoot to its minimum value (solid line), whether in case of fixed profile (dotted line) or by changing $t_{\mathrm{on},1}$ only (dashed line) the undershoot increases.

V. Conclusion

As far as fast power switches are concerned, open-loop AGDs are a viable solution, however, they suffer from suboptimal tuning when the load current changes. This paper investigates such an issue on a prototyped Buck converter, in which the power transistor is driven by an AGD, capable of modulating the gate current profile. Experimental results assessed the AGD under nominal conditions, and they pointed out its lack of effect when the operating conditions are modified. It was found that the undershoot affecting the drain-source voltage is effectively controlled if the timing parameters of the AGD varies proportionally with the load current.

VI. Acknowledgment

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