Parallel Computation in the Racetrack Memory

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Fabrizio Riente, *Member, IEEE,* Giovanna Turvani, Marco Vacca, Mariagrazia Graziano

Abstract—Racetrack memories are promising candidates for next-generation solid-state storage devices. Various racetrack memories have been proposed in the literature, skyrmion based or domain wall based. However, none of them show integrated computing capabilities. Here, we introduce a new domain wall based racetrack concept that can operate both as a memory and as a computing device. The computation is defined by changing locally the anisotropy of the film. Stray fields from nearby cells are exploited to implement reconfigurable logic gates. We demonstrate that the racetrack array can operate in parallel in every cell. This is achieved by an external out-of-plane Zeeman field applied to the array. As proof-of-principle, we verified the single computing cell and multiple connected cells operating in parallel by micromagnetic simulations. Logic NAND/NOR is implemented independently in every computing cell. This study provides the guidelines for the development and optimization of this family of logic gates.

Index Terms—Spintronics, computing-in-memory, magnetic devices, racetrack memory

1 Introduction

The demand for faster, ultra-dense massive storage devices is pushing the research community to explore novel memories. Different alternatives have been proposed in recent years. The development of extraordinarily sensitive sensors has made possible the greatest evolution of spintronic devices. Magnetic Random Access Memory (MRAM) is just one example. Racetrack memory is a solid-state device with no moving parts, firstly proposed by S.Parkin and S.H.Yang [1]. Many improvements to the first concept have been made, thanks to important findings from the fabrication process. The digital information in these devices can be encoded in a sequence of domain walls [2]. The working principle was firstly demonstrated on permalloy nanowires [3]. However, better performance can be achieved by using materials that exhibit perpendicular magnetic anisotropy (PMA) , such as Co/Ni [4] [5]. A shift register implementation on a racetrack has been presented by J.H. Franken *et al*. [6]. They engineered the energy profile of the nanowires in a saw tooth shape, giving a unidirectional propagation by using local or global field pulses. The main drawback is that the information stored in the magnetic track can only be moved in one direction, reducing device flexibility. An improved solution has been proposed for the purely magnetic-field-driven racetrack, where the combination of in-plane field and out-of-plane field is exploited, combined with a tuning of the energy landscape [7]. Recent works show skyrmion based racetracks as a promising carrier of digital information in future solid-state devices [8], [9], [10]. Moreover, a recent finding from Deger [11] presents a hybrid usage of domain wall and skyrmion based racetracks without the need of geometrical restrictions for the conversion between the two domains.

However, none of the proposed devices show a functionally complete set of reconfigurable logic gates. Here, we propose a solution that enriches the storage property of the domain wall based racetrack enabling highly parallel computation. The elaboration is achieved by superposition of fringing fields, leading to a purely magnetic-field-computing racetrack array. We focus on a conceptual racetrack memory, where storage and computing capabilities are integrated into the same device. We performed micromagnetic simulations to study the conceptual computing cell, exploiting thin film with perpendicular magnetic anisotropy. We tested the stability of the device at room temperature to ensure that the computing cells operate in parallel. To model the device, we used a framework based on the Landau-Lifshitz-Gilbert equation [12]. The simulation parameters are reported in section 3. The results show that the computing cell provides a functionally complete set of reconfigurable logic gates. The device supports bi-directional data movement, controlled using a spin-polarized current [13], [14], to provide maximum flexibility.

2 Conceptual Device

In the following, we simulate and analyze a device with three computing cells operating in parallel. First, we show the memory array organization and the structure of a single computing device, and how elaboration is achieved by superposition of stray fields from nearby memory elements. Thereafter, we present the micromagnetic simulations of a three gates racetrack. We performed the magnetostatic analysis of an array with three computing cells and we studied the dynamic behavior of the devices at room temperature, considering variations in the racetrack distances. The system organization is schematically represented in Fig. 1, by an array of racetracks. The computing array consists of groups of four parallel racetracks. All the tracks are formed by material that show perpendicular magnetic anisotropy such as Co/Pt or Co/Ni superlattices. Three of them represent the inputs and one the outputs. Three lie in the same plane, while the fourth is placed above or below the central nanowire. The binary information is encoded

F. Riente, G. Turvani, M. Vacca, M. Graziano are with the Department of Electronics and Telecommunication Engineering, Politecnico di Torino, Torino, To, 10129 email: fabrizio.riente@polito.it.

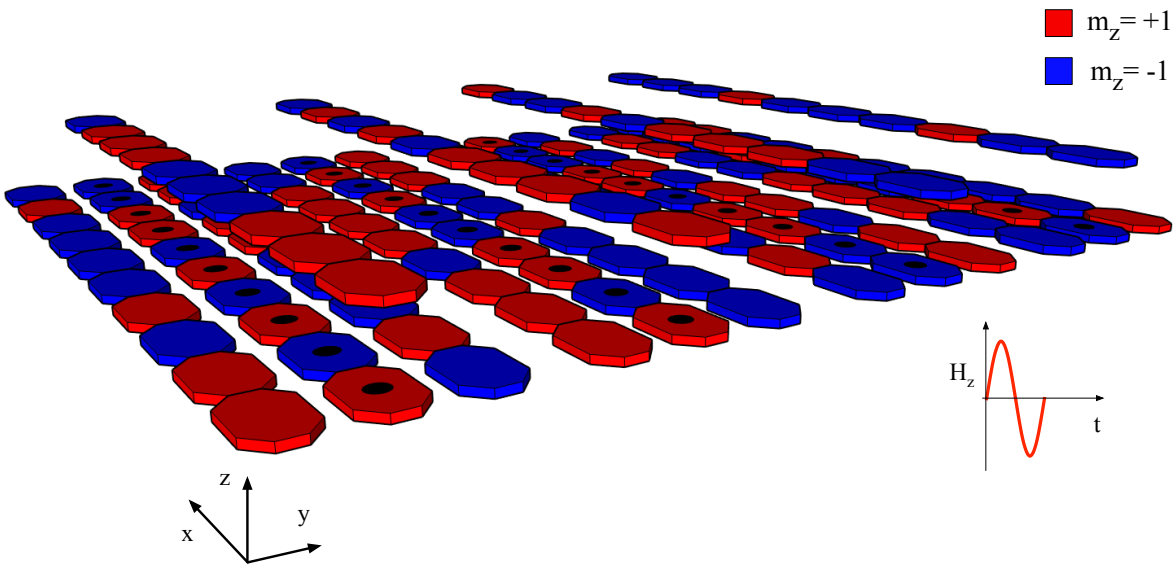

Fig. 1. Concept of the racetrack array with computing capabilities. The racetrack is a ferromagnetic nanowire where the binary information is encoded by sequences of domain walls. Data movement is achieved by spin-polarized current that coherently shifts the domain walls along the x-axis. Parallel bit-wise operation takes place when series of positive and negative out-of-plane field pulses are applied to the device.

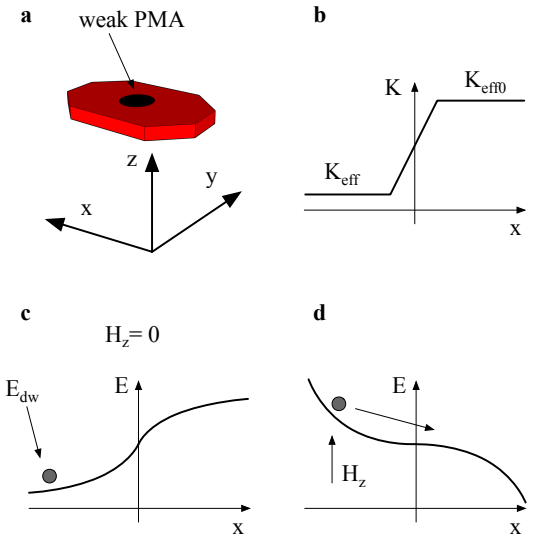

Fig. 2. **a**, Evaluation element with a weak PMA region. **b**, Schematic representation of the step in the magnetic anisotropy. **c**, The step in the magnetic anisotropy leads to an energy barrier for the nucleated domain wall. **d**, The Zeeman field H_z tilts the energy barrier and the nucleated domain wall can reverse the magnetization of the output element.

in small domains separated by domain walls [1], [2]. The digital information is confined between two notches. The notch defines a pinning site for the domain wall. When the domain wall nucleates in the output element, it expands its area and pins at the notches. The side-tracks store the inputs, while the racetrack above the central nanowire stores reconfigurable inputs and defines the logic function implemented. These programmable inputs are used to individually configure the function implemented by each computing cell. The feasibility of 3D stacked Co/Pt or Co/Ni PMA patterned layers has been experimentally demonstrated in the literature for perpedicular Nano Magnet Logic devices [15]. In this approach, every patterned layer is planarized with a spin-on glass called hydrogen silsesquioxane (HSQ). HSQ has good planarization properties and proved to be an adequate seed for the growth of additional magnetic layers and build monolithic 3D devices [16]. In addition, thanks to its transparency, it is suitable for Kerr microscopy measurements. The computing cell can implement the three-input-majority function, or, by configuring the input on the programmable layer to m_z=+1 or m_z=-1, each cell can operate as a NAND or a NOR respectively. Here, we combine the well known characteristics of perpendicular Nano Magnetic Logic (pNML) [15] and the racetrack properties, this leads to an extremely parallel and ultra-dense logic array. The computing cell provides a functionally complete set of gates to implement any Boolean function and therefore increases the design flexibility as well. The central nanowire, surrounded by the other three racetracks, evaluates and stores the output of the logic gates.

To control the region where the computation takes place, we engineered the energy landscape of the output element. The evaluation element shows a weak PMA spot at its center, (Fig. 2.a). The locally reduced anisotropy is tuned by the focused ion beam (FIB) irradiation [17], leading to lower domain wall energy [18]. The lower coercivity (H_c) gives the possibility to control where the domain wall nucleates. However, the nucleated domain wall experiences the energy barrier introduced by the step in the magnetic anisotropy, (Fig. 2.c). The energy barrier can be overcome by appliying an external Zeeman field that tilts the energy landscape, (Fig. 2.d). The single computing cell is schematically represented in Fig. 3.a. The lateral elements storing the inputs are located at *d2* and *d3* from the output element. On top of them, the programmable input is positioned at *d1*, centered on top of the output element. In this cell, the stray fields from the input elements superpose with the trigger Zeeman field (H_z) and can contribute to the switching of the output. Therefore, when the external field is applied, two scenario

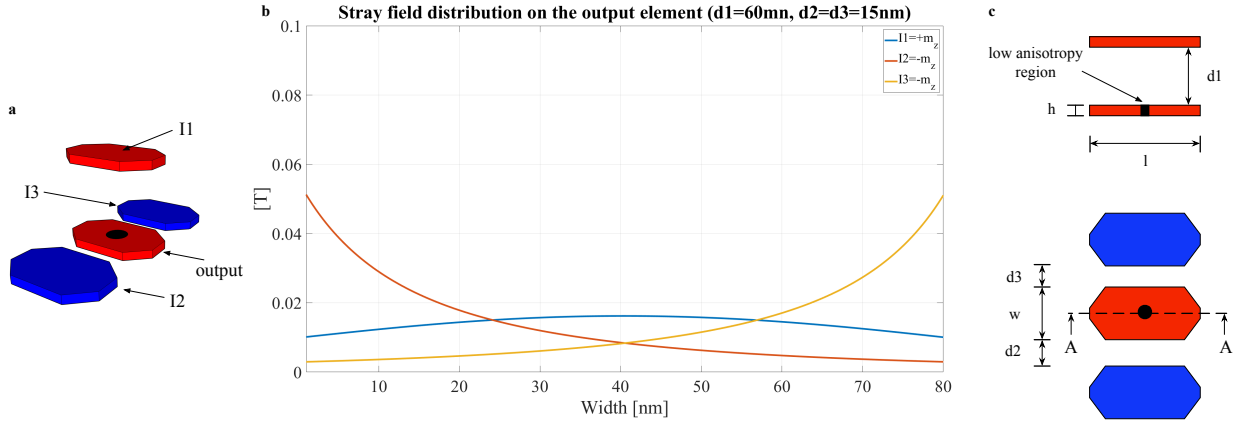

Fig. 3. Schematic representation of the elementary computing cell. **a**, 3D view where inputs are surrounding the evaluation element. Here inputs *I2* and *I3* were saturated to -m_z and *I1* to +m_z. **b**, Stray field distribution at the cross-section of the $80\,\mathrm{nm}$ width output element with *I2* and *I3* placed at *d2*=*d3*=$15\,\mathrm{nm}$, *I1* placed at *d1*=$60\,\mathrm{nm}$ and magnetized according to **a**. **c**, Top view and cross-section of the cell showing the input *I1* aligned over the output cell.

can be identified. The overall fringing field contributions are added to the Zeeman field, supporting the switching of the output element. This situation, where $H_{tot} > H_c$, determines the computation. On the contrary, if the stray fields show opposite contribution to the Zeeman field, they prevent the switching of the output ($H_{tot} < H_c$). Longitudinal domain wall motion is achieved by spin-polarized currents along the x-axis. This 3D structure has several interesting properties. First, the logic operation of each cell of the array can be dynamically reconfigured. Second, the array can perform logic operations in parallel only if a Zeeman field is applied. In steady state condition, it behaves as a large memory array. Third, the dynamic reconfigurability makes it possible to increase the data density by a factor of four at the expense of loosing the computing capabilities.

3 Simulation Method

We performed finite-difference simulations using the GPU-accelerated package MuMax3 [19]. We considered a $8\,\mathrm{nm}$ thick Co/Pt superlattice with perpendicular magnetic anisotropy. The saturation magnetization was M_s=$723 \times 10^3\,\mathrm{A\,m^{-1}}$ and the exchange constant A=$1.3 \times 10^{-11}\,\mathrm{J\,m^{-1}}$. The Co/Pt film uniaxial anisotropy constant was K_u=$3.63 \times 10^5\,\mathrm{J\,m^{-3}}$ and on the FIB irradiated region $K_u = 1.45 \times 10^5\,\mathrm{J\,m^{-3}}$. The discretization of the three-dimensional sample was 1x1x2 $\mathrm{nm^3}$. The soft magnetic spots were 50x50 $\mathrm{nm^2}$ and 40x60 $\mathrm{nm^2}$ wide. A variation of 5% of the anisotropy constant was applied over the whole film. The damping constant was α=0.3 according to the measurements in Co/Pt films [20], [21]. The *d2* and *d3* parameters were varied from $10\,\mathrm{nm}$ to $20\,\mathrm{nm}$ with a $5\,\mathrm{nm}$ step size. The *d1* distance varied from $60\,\mathrm{nm}$ to $80\,\mathrm{nm}$ with a $4\,\mathrm{nm}$ step size. According to Brown [22], the temperature effect was included by means of a fluctuating thermal field $\vec{B}_T$:

$$\vec{B}_T = \eta \sqrt{\frac{2\mu_0 \alpha k_B T}{B_{sat}\gamma_{LL}\Delta V \Delta t}} \qquad (1)$$

where, k_B is the Boltzmann constant, T the temperature, B_{sat} the saturation magnetization, γ_{LL} is the gyromagnetic ratio, ΔV the cell volume and Δt the time step. This quantity is multiplied by a random vector η from a standard normal distribution, which is changed at every time step, from a standard normal distribution. The time step Δt was $1 \times 10^{-15}\,\mathrm{s}$ and the temperature T =293 K. Exhaustive simulations were performed for every set of *d1*, *d2*, *d3* with an external field B_z of $55\,\mathrm{mT}$ and $35\,\mathrm{mT}$, respectively for the 50x50 $\mathrm{nm^2}$ and 40x60 $\mathrm{nm^2}$ weak spot. The Zeeman field was a sine wave with a frequency of $25\,\mathrm{MHz}$, applied for a single period. To shift the processed information an homogeneous current density J=$7.4 \times 10^8\,\mathrm{A\,cm^{-2}}$ was applied on the output racetrack. The polarization was $p = 0.56$ according to the measurements in Co/Pt films [23].

4 In-Racetrack Computing

4.1 Static analysis of the computing cell

We propose a way to add computing capabilities to the racetrack memory array by domain wall nucleation on the output element. Firstly, the single computing cell showed in Fig. 3.a was studied. We analyzed the magnetostatic field produced by every input element on different device geometry. We also investigated the effect of the size of the weak PMA region. Fig. 3.c specifies the dimensions involved in the computing cell. In this analysis, we maintained constant the size of each element in the computing cell and varied the distances *d1*, *d2*, *d3* and the size of the weak PMA spot. An example of our results is reported in Fig. 3.b. Here, the field distribution due to every input surrounding the output element is reported. The plot indicates the fringing field distribution across the $80\,\mathrm{nm}$ wide output element. Having the inputs *I2* and *I3* equal to -1, their contributions are positive. Similarly, the contribution of the ferromagnetically coupled input *I1* is also positive. In this example from our results, we consider *d2*=*d3*=$15\,\mathrm{nm}$, while *d1*=$60\,\mathrm{nm}$. The average fringing fields on a 40x60 $\mathrm{nm^2}$ region from *I1*, *I2*, *I3* are respectively $11.3\,\mathrm{mT}$, $11.3\,\mathrm{mT}$ and $15.1\,\mathrm{mT}$. The characterization of the input stray fields is reported in Fig. 4.a-b. We analyzed different aspect ratio of the weak PMA region as function of the input distances. Both coplanar inputs show very similar fields as expected. To match the

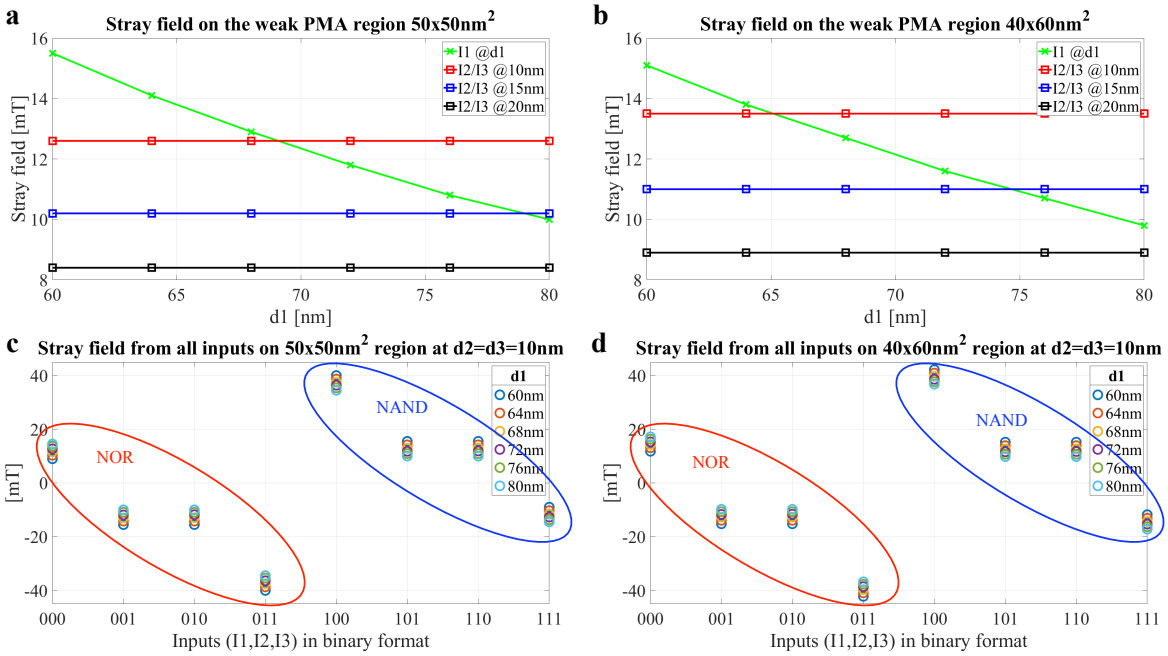

Fig. 4. Stray field on the irradiated region on the evaluation element. Average field distribution as function of the vertical (*d1*) and horizontal distances (*d2*=*d3*). **a**, Input contributions on a 50x50 nm^2 region. **b**, Input contributions on a 40x60 nm^2 region. Here the lateral coupling is higher due to the aspect ratio of the irradiated area. **c**, Stray field from every input (*I1*,*I2*,*I3*) on the FIB irradiated area when *d2*=*d3*=10 nm. The cell can operate as NAND or NOR gate depending on the value of input *I1*. **d**, Contribution of every input when *d2*=*d3*=10 nm on a 40x60 nm^2 region.

contribution from the input (*I1*), we consider the intersection between *I1* and the side inputs. It can be observed that to obtain a similar coupling when *I2* and *I3* are at 20 nm, input *I1* should be further. This is not necessarily a drawback, as long as the contribution of two inputs magnetized in the same direction is higher than the third input with opposite magnetization. From Fig. 4.b, it can be observed that by tuning the aspect ratio of the irradiated spot, the vertical distance *d1* can be reduced or increased to match the lateral contributions. The superposition of the fringing fields due to every permutation of the inputs is showed in Fig. 4.c-d. The inputs are reported in binary format, where the logic 1 is encoded by $+m_z$ and the logic 0 by $-m_z$. Fig. 4.d shows that the size of the weak PMA region with dimensions 40x60 nm exhibit better coupling even if its area is smaller compared to Fig. 4.c. The soft magnetic spot with higher aspect ratio is subjected to higher stray fields from the coplanar inputs. This can be observed by looking at the inputs 000 and 111, where both *I2* and *I3* are pointing in the same direction, opposed to *I1*. It can be noted from Fig. 4.c-d that the computing cell shows NAND or NOR logic behavior when the input *I1* is 1 or 0 respectively. However, to start the computation, the out-of-plane Zeeman field is applied to overcome the H_c of the output element. We also investigated the contributions of neighboring computing cells. For this analysis we considered two additional computing cells, with all the elements saturated first to $+m_z$ and later to $-m_z$. Saturate the neighboring coplanar elements in one direction and to the opposite value the one in the layer above puts the device in the worst case scenario, where all the stray fields are superposing with the same sign. However, this contribution is very similar varying the distances. For example, on a weak PMA region 40x60 nm the their contribution is 3.3 mT.

4.2 Dynamic analysis of parallel operating cells

To investigate the stability of the device, we performed dynamic micromagnetic simulations at room temperature on a memory array made of three computing cells operating in parallel. The inputs and the reconfigurable track can be loaded using single or multiple write heads positioned along the tracks [1]. The same approach can be used for read-out operations. Both these operations can be performed by every track in parallel and independently. In this way, new data can be stored simultaneously into the memory or the reconfigurable track. Similarly, computed values can be extracted from the output track. The superposition of the input stray fields and the external field determine the switching of the output of the computing cell. The whole system can perform bit-wise computations in parallel by sequences of positive and negative pulses. Fig. 5.a shows three computing cells in the relaxed micromagnetic state, where no external field is applied. From a functional point of view, the inputs are stored on the three racetracks that surround the central nanowire. The inputs on the side tracks are antiferromagnetically coupled to the evaluation elements, whereas the programmable inputs are ferromagnetically coupled. Here, the three cells are configured as NAND, NOR, NAND gates respectively. The nanowires have *d2* and *d3* separations on the same plane and *d1* in the vertical direction. In Fig. 5, *d2*=*d3* =10 nm, while *d1*=60 nm. In this dynamic analysis, the information is represented by a 200x80x8 nm^3 element. Fig. 5.c reports the magnetization over time (z-component) of every output element. The external field was a sine wave with a frequency of 25 MHz applied for one period and amplitude 55 mT (Fig. 5.c).

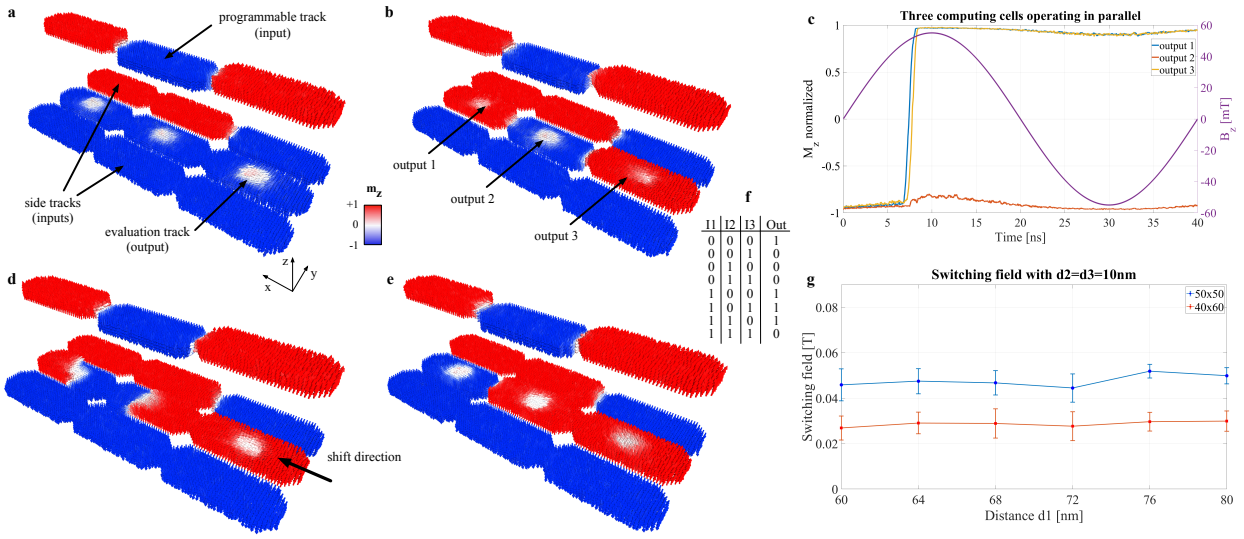

Fig. 5. **a**, Three computing cells with inputs (1, -1, 1), (-1, -1, 1), (1, -1, -1), where the first value represents the ferromagnetic coupled input laying above the central track (*I1*). The programmable track is $60\,\mathrm{nm}$ above the evaluation track and the *d2*=*d3*=$10\,\mathrm{nm}$. The evaluation elements are initialized to -m_z. **b**, The output elements switched after the external Zeeman field ($55\,\mathrm{mT}$) was applied for one period. **c**, The normalized magnetization (z-component) of the three output elements and the B_z field over time. **d**, The spin-polarized current (J = $740 \times 10^{12}\,\mathrm{A\,m^{-2}}$) shifting the computed values after $0.5\,\mathrm{ns}$. **c**, Shifted binary information in the output racetrack after a $1\,\mathrm{ns}$ pulse. **f**, Truth table of the single computing cell. **g**, Switching field at different *d1* distances and *d2*=*d3*=$10\,\mathrm{nm}$ considering a 50x$50\,\mathrm{nm}$ and 40x$60\,\mathrm{nm}$ weak PMA spot. The B_z is extracted in correspondence of the normalized magnetization equal to 0.9 on the output element.

The soft PMA region was 50x$50\,\mathrm{nm}$. The output of every computing cell is the result of the superposition of the three inputs and the out-of-plane field. The micromagnetic simulations, at 293K, show a correct switching behavior and confirm that the cell behaves as a NAND gate when the programmable input is set to logic 1, whereas it operates as a NOR gate in the opposite condition, see Fig. 5b and Fig. 5.f. In particular, when the distance among the coplanar racetracks ranges from $10\,\mathrm{nm}$ to $15\,\mathrm{nm}$, the computing cell switches correctly, even if the fringing fields from all inputs are not balanced. However, when the distance increases to $20\,\mathrm{nm}$, the cells with input 000 and 111 show switching errors and does not operate as NAND/NOR. This behavior is explained by the large difference between the coupling of *I2* and *I3* compared to *I1*, see Fig. 4.a. In this case, the sum of the coplanar inputs is lower than the fringing field from *I1*, resulting in switching errors.

Fig. 5.g shows that for a 40x$60\,\mathrm{nm}$ weak PMA region the external field required to properly switch the output is much lower compared to the 50x$50\,\mathrm{nm}$ weak spot. Here, the external field amplitude was $35\,\mathrm{mT}$. Even if the switching volume is smaller in the 40x$60\,\mathrm{nm}$ region, a lower Zeeman field is required. This reduction is explained by the higher aspect ratio of the soft region being subjected by strong stray fields. The switching variation derive from fact that the nucleation is a stochastic, thermally activated process influenced by the coupling field of the neighboring input elements [24]. The effective field acting on the weak PMA spot is given by the external field H_z and the coupling field (C_i) from the surrounding inputs (I_i), $H_{eff} = H_z + (C_1 I_1 - C_2 I_2 - C_3 I_3)$. Therefore, the energy barrier on the weak PMA spot is increased or decreased according to the magnetization of the inputs. The C value plays an important role on the logic behavior of the computing cell. We observed a correct NAND/NOR switching of the output in all other input configurations in every computing cell. We validated the shift operation by spin-polarized current on the output racetrack being more critical due to the weak PMA spot and the notches (Fig. 5.d-e). The critical current density to uniformly shift the single bit over the weak PMA was $7.4 \times 10^8\,\mathrm{A\,cm^{-2}}$. This large current is mainly related to the depth of the introduced pinning sites.

5 Conclusion and Perspectives

The objective of this work was to provide a proof-of-concept racetrack memory device enriched with computing capabilities. This device is based on domain wall motion for data movement, and stray field superpositions from nearby elements for computing. We performed dynamic micromagnetic simulations at room temperature to demonstrate the stability of the device. The input contributions can be tuned by properly designing the weak PMA region. The large damping we used, typical of Co/Pt films (α=0.3), show a switching time in the range of $\sim$6.85 ns. Faster devices can be obtained with low damping materials like CoFeB/MgO, where α=0.015 was recently measured [25]. We showed that tuning the size of the irradiated spot can lead to properly matched input weights and increase the strength of the lateral stray fields leading to a lower Zeeman field. Parallel logic computation is achievable in domain wall based racetrack memories via the superposition of stray fields. The NAND/NOR logic behavior provides a functionally complete logic sets to implement any logic function. In order to reduce the shift current, further engineering of the pinning site is required, as an example exploiting the Voltage Controlled Magnetic Anisotropy effect to increase the energy barrier. We hope that this preliminary proof-of-principle device, combined with the hybrid usage of domain wall and skyrmion based racetracks recently proposed

in [11], will expedite the development of ultra-dense in-racetrack computing arrays.

ACKNOWLEDGMENT

We gratefully acknowledge the support of NVIDIA Corporation with the donation of the Titan Xp GPU used for this research.

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APPENDIX

Supplemental Material

The following files are available.

- computing_cell.mov: movie of three computing cells operating in parallel and independently when the Zeeman field is applied for a single period. The three cells in the array implement respectively the NAND, NOR, NAND gates.
- shift_operation.mov: movie of the domain wall motion on the central track storing the computed values.